



STN1NF20

N-channel 200 V, 1.1 Ω , 1 A SOT-223
STripFET™ II Power MOSFET

Features

Order code	V _{DSS}	R _{DS(on)} max	I _D
STN1NF20	200 V	< 1.5 Ω	1 A

- 100% avalanche tested
- Low gate charge
- Exceptional dv/dt capability

Applications

- Switching applications

Description

This Power MOSFET has been developed using STMicroelectronics' unique STripFET™ process, which is specifically designed to minimize input capacitance and gate charge. This renders the device suitable for use as primary switch in advanced high-efficiency isolated DC-DC converters for telecom and computer applications, and applications with low gate charge driving requirements.

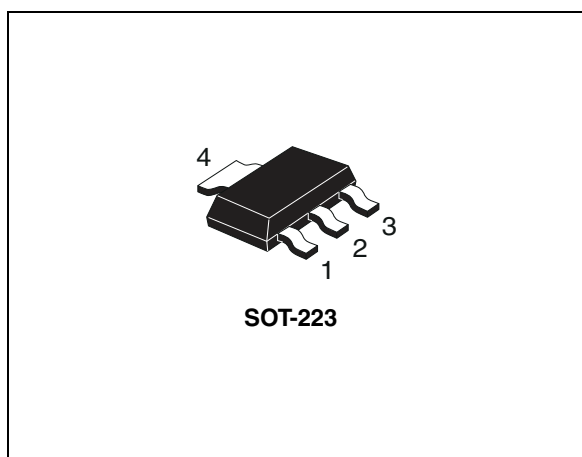


Figure 1. Internal schematic diagram

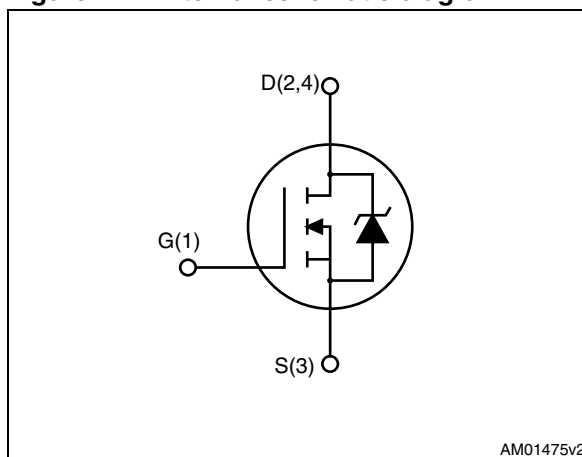


Table 1. Device summary

Order code	Marking	Package	Packaging
STN1NF20	1NF20	SOT-223	Tape and reel

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1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{GS}	Gate-source voltage	± 20	V
I_D	Drain current continuous $T_{amb} = 25\text{ °C}$	1	A
I_D	Drain current continuous $T_{amb} = 100\text{ °C}$	1	A
$I_{DM}^{(1)}$	Drain current pulsed	4	A
P_{TOT}	Total dissipation at $T_{amb} = 25\text{ °C}$	2	W
$dv/dt^{(2)}$	Peak diode recovery voltage slope	10	V/ns
T_j T_{stg}	Operating junction temperature Storage temperature	-55 to 150	°C

1. Pulse width limited by safe operating area.
2. $I_{sd} \leq 1\text{ A}$, $di/dt \leq 200\text{ A}/\mu\text{s}$, $V_{DD} \leq 80\% V_{(BR)DSS}$.

Table 3. Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-amb}$	Thermal resistance junction to ambient	62.50	°C/W

Table 4. Thermal data

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or not repetitive ⁽¹⁾	1	A
E_{AS}	Single pulse avalanche energy ⁽²⁾	70	mJ

1. Pulse width limited by T_{JMAX} .
2. Starting $T_j = 25\text{ °C}$, $I_D = I_{AR}$, $V_{DD} = 50\text{ V}$.

2 Electrical characteristics

(T_{case} = 25 °C unless otherwise specified)

Table 5. On /off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V _{(BR)DSS}	Drain-source breakdown voltage	I _D = 1 mA, V _{GS} = 0	200			V
I _{DSS}	Zero gate voltage drain current (V _{GS} = 0)	V _{DS} = 200 V V _{DS} = 200 V, T _C =125 °C			1 50	μA μA
I _{GSS}	Gate-body leakage current	V _{GS} = ± 20 V, V _{DS} =0			±100	nA
V _{GS(th)}	Gate threshold voltage	V _{GS} = V _{DS} , I _D = 250 μA	2	3	4	V
R _{DS(on)}	Static drain-source on resistance	V _{GS} = 10 V, I _D = 0.5 A		1.1	1.5	Ω

Table 6. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C _{iss}	Input capacitance	V _{DS} = 25 V, f = 1 MHz, V _{GS} = 0	-	90	-	pF
C _{oss}	Output capacitance			30		pF
C _{rss}	Reverse transfer capacitance			4		pF
R _g	Intrinsic gate resistance	f=1 MHz open drain	-	4.8	-	Ω
Q _g	Total gate charge	V _{DD} = 160 V, I _D = 1 A,	-	5.7	-	nC
Q _{gs}	Gate-source charge	V _{GS} = 10 V		1.1		nC
Q _{gd}	Gate-drain charge	(see Figure 14)		3.0		nC

Table 7. Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max	Unit
$t_{d(v)}$	Voltage delay time	$V_{DD} = 100\text{ V}$, $I_D = 0.5\text{ A}$, $R_G = 4.7\ \Omega$, $V_{GS} = 10\text{ V}$ (see Figure 13)	-	4	-	ns
t_r	Voltage rise time			5.6		ns
t_f	Current fall time			12.4		ns
$t_{c(off)}$	Crossing time			15.8		ns

Table 8. Source drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		1	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)				4	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 1\text{ A}$, $V_{GS} = 0$	-		1.6	V
t_{rr}	Reverse recovery time	$I_{SD} = 1\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$	-	51.8		ns
Q_{rr}	Reverse recovery charge	$V_{DD} = 20\text{ V}$		90.7		nC
I_{RRM}	Reverse recovery current	(see Figure 15)		3.5		A
t_{rr}	Reverse recovery time	$I_{SD} = 1\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$	-	58.0		ns
Q_{rr}	Reverse recovery charge	$V_{DD} = 20\text{ V}$, $T_j = 150\text{ }^\circ\text{C}$		106.7		nC
I_{RRM}	Reverse recovery current	(see Figure 15)		3.7		A

1. Pulse width limited by safe operating area

2. Pulsed: pulse duration = 300 μs , duty cycle 1.5%

2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

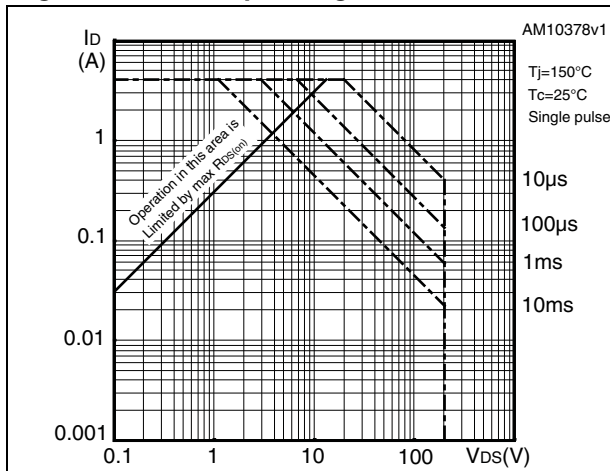


Figure 3. Thermal impedance

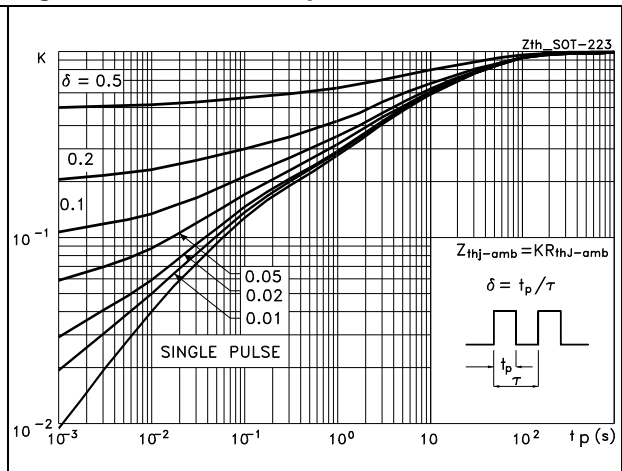


Figure 4. Output characteristics

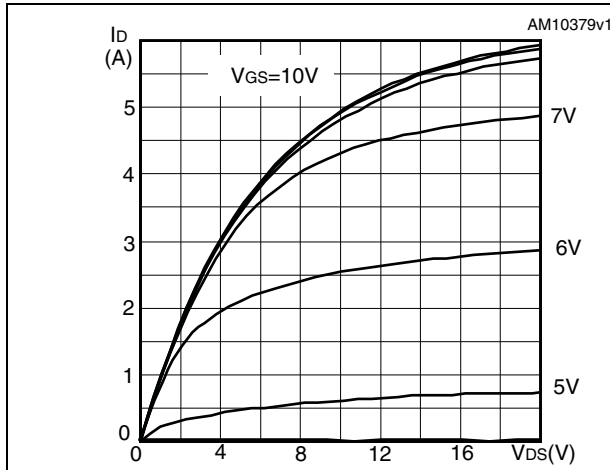


Figure 5. Transfer characteristics

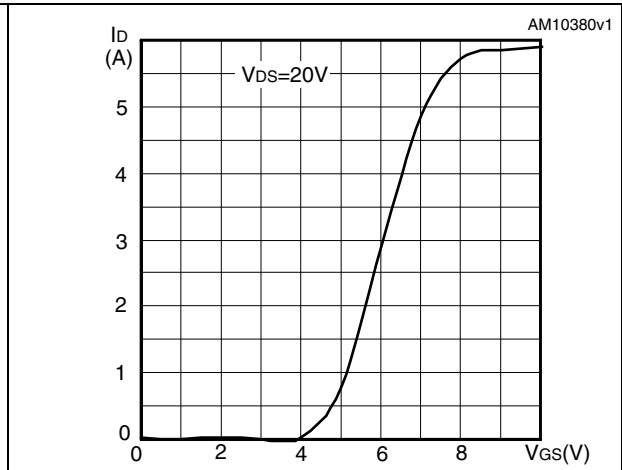


Figure 6. Normalized $B_{V_{DSS}}$ vs temperature

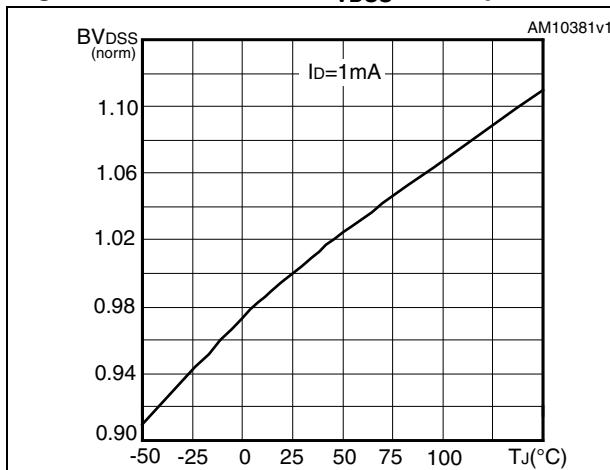


Figure 7. Static drain-source on resistance

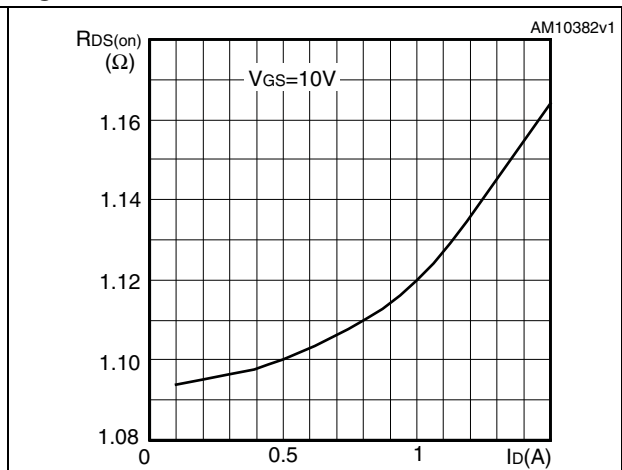


Figure 8. Gate charge vs gate-source voltage Figure 9. Capacitance variations

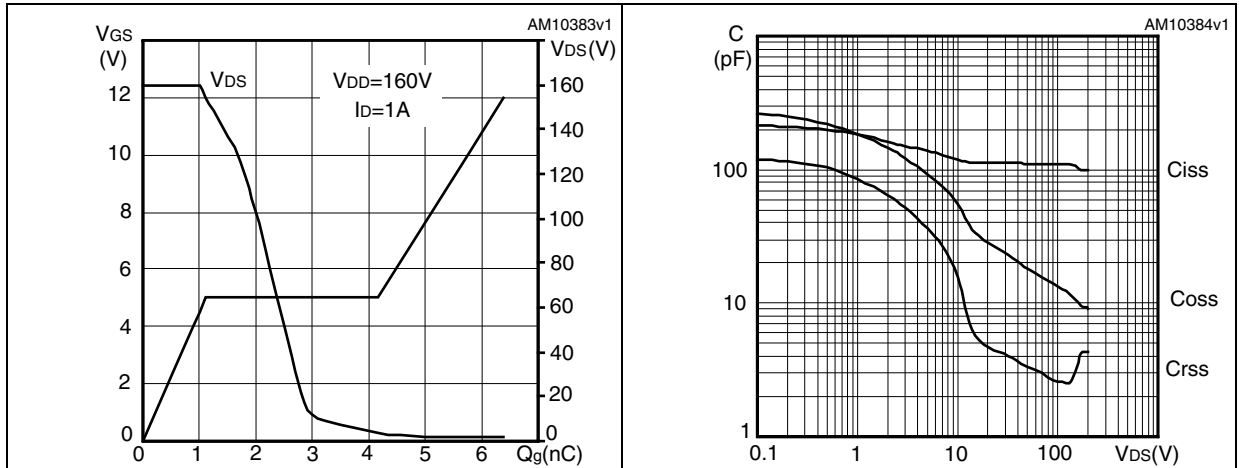


Figure 10. Normalized gate threshold voltage vs temperature Figure 11. Normalized on resistance vs temperature

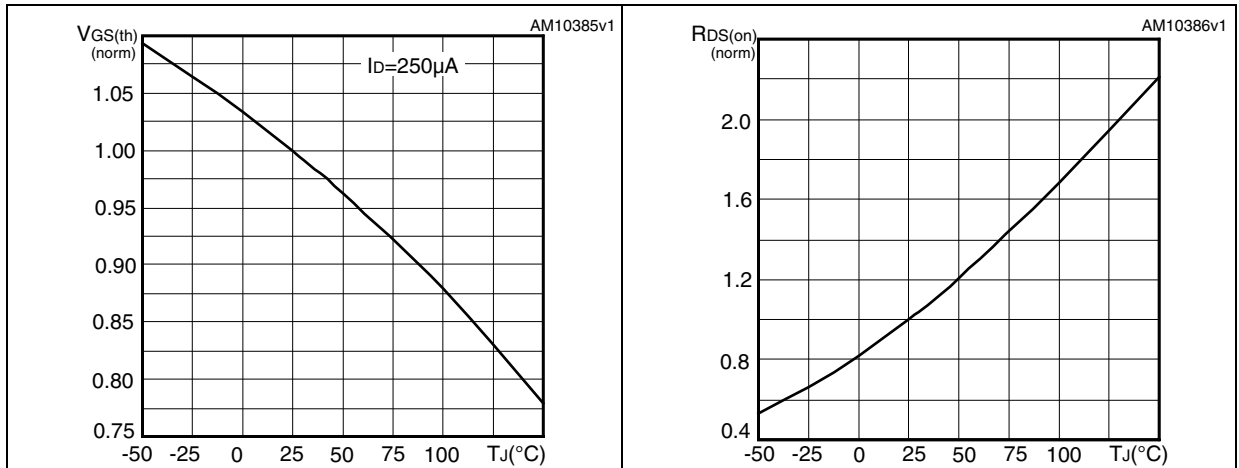
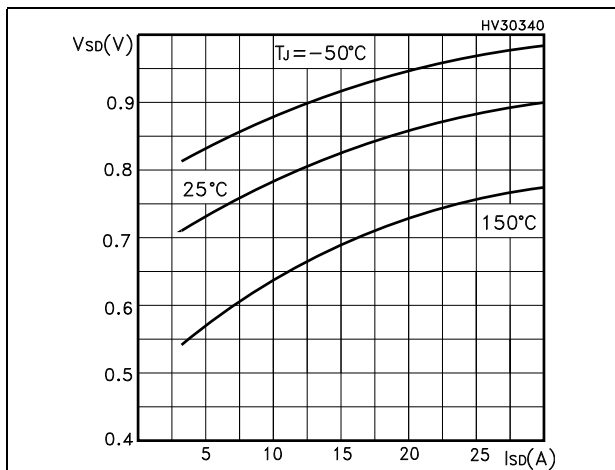
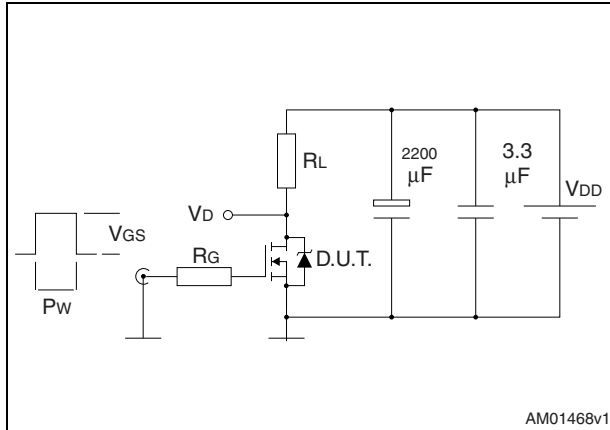


Figure 12. Source-drain diode forward characteristics



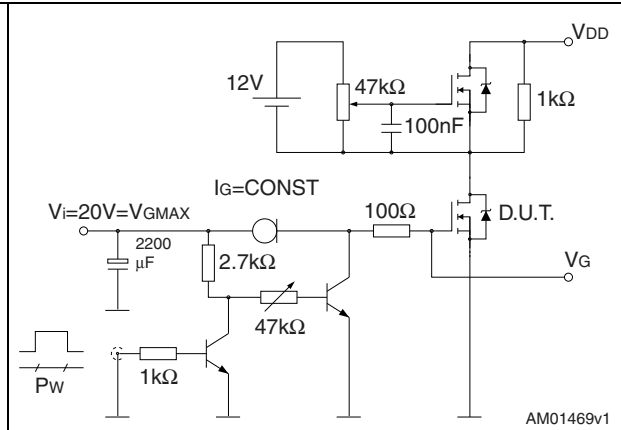
3 Test circuits

Figure 13. Switching times test circuit for resistive load



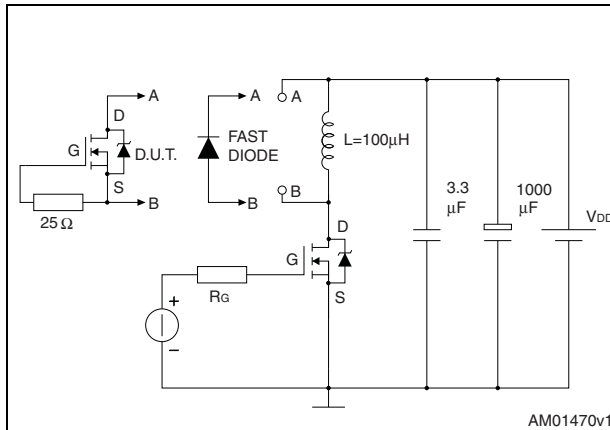
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Figure 14. Gate charge test circuit



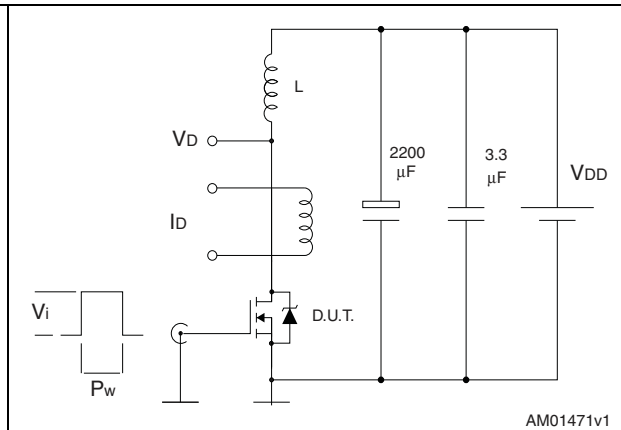
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Figure 15. Test circuit for inductive load switching and diode recovery times



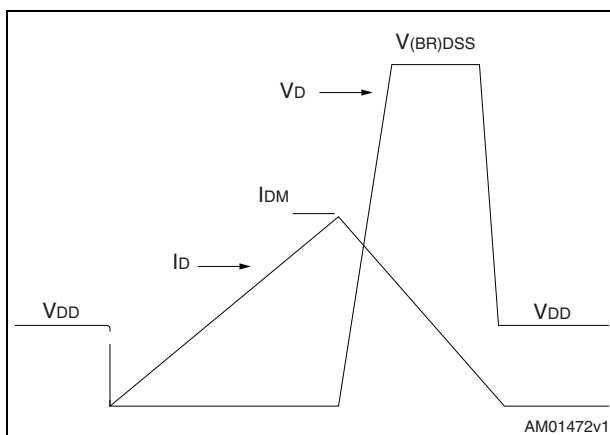
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Figure 16. Unclamped inductive load test circuit



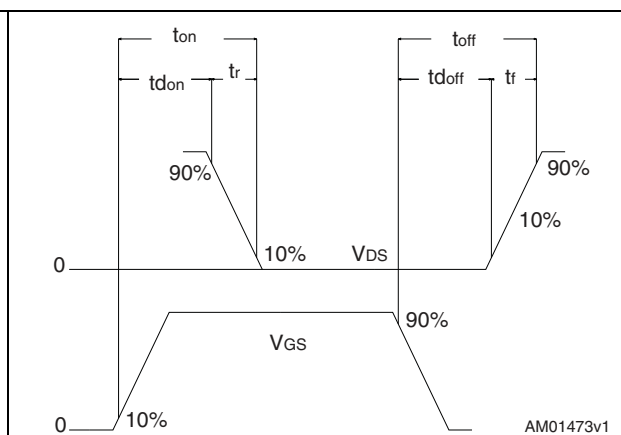
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Figure 17. Unclamped inductive waveform



AM01472v1

Figure 18. Switching time waveform



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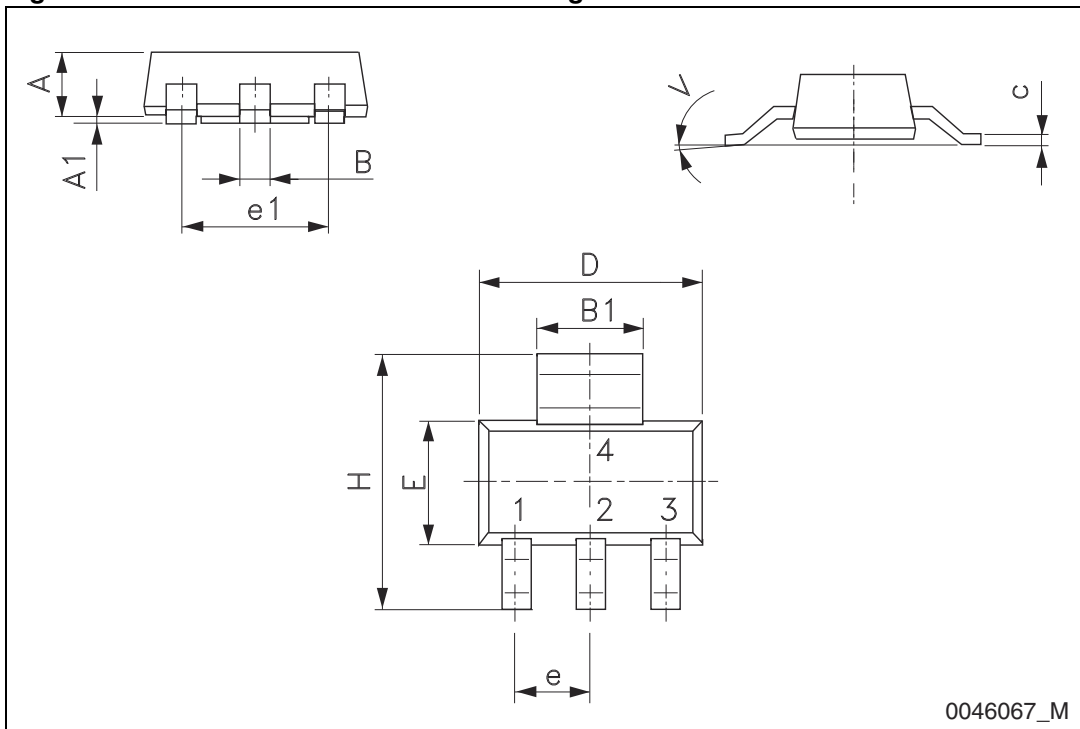
4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK[®] packages, depending on their level of environmental compliance. ECOPACK[®] specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

Table 9. SOT-223 mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A			1.80
A1	0.02		0.1
B	0.60	0.70	0.85
B1	2.90	3.00	3.15
c	0.24	0.26	0.35
D	6.30	6.50	6.70
e		2.30	
e1		4.60	
E	3.30	3.50	3.70
H	6.70	7.00	7.30
V			10°

Figure 19. SOT-223 mechanical data drawing



5 Revision history

Table 10. Document revision history

Date	Revision	Changes
04-Nov-2011	1	First release.

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