

# A5G35S004N

## Airfast RF Power GaN Transistor

Rev. 4 — November 2022

Data Sheet: Technical Data

This RF power GaN transistor is designed for cellular base station applications covering the frequency range of 3300 to 4300 MHz.

### 3500 MHz

- Typical Single-Carrier W-CDMA Reference Circuit Performance:  
 $V_{DD} = 48$  Vdc,  $I_{DQ} = 12$  mA,  $P_{out} = 24.5$  dBm Avg., Input Signal PAR = 9.9 dB @ 0.01% Probability on CCDF.<sup>(1)</sup>

Frequency	$G_{ps}$ (dB)	$\eta_D$ (%)	Output PAR (dB)	ACPR (dBc)
3400 MHz	19.3	19.5	9.9	-38.7
3500 MHz	19.4	20.0	9.7	-40.3
3600 MHz	18.8	20.4	9.4	-42.1

1. All data measured in reference circuit with device soldered to printed circuit board.

### 3700–4000 MHz

- Typical Single-Carrier W-CDMA Reference Circuit Performance:  
 $V_{DD} = 48$  Vdc,  $I_{DQ} = 10$  mA,  $P_{out} = 28$  dBm Avg., Input Signal PAR = 9.9 dB @ 0.01% Probability on CCDF.<sup>(1)</sup>

Frequency	$G_{ps}$ (dB)	$\eta_D$ (%)	Output PAR (dB)	ACPR (dBc)
3700 MHz	18.3	22.5	8.4	-35.2
3800 MHz	18.8	25.2	8.5	-38.6
3900 MHz	18.1	23.8	8.5	-41.2
4000 MHz	17.2	21.6	8.6	-42.4

1. All data measured in reference circuit with device soldered to printed circuit board.

### 4100–4300 MHz

- Typical Single-Carrier W-CDMA Reference Circuit Performance:  
 $V_{DD} = 48$  Vdc,  $I_{DQ} = 10$  mA,  $P_{out} = 28$  dBm Avg., Input Signal PAR = 9.9 dB @ 0.01% Probability on CCDF.<sup>(1)</sup>

Frequency	$G_{ps}$ (dB)	$\eta_D$ (%)	Output PAR (dB)	ACPR (dBc)
4100 MHz	17.6	26.5	7.6	-33.2
4200 MHz	17.2	26.5	7.8	-36.2
4300 MHz	16.5	26.5	7.9	-38.3

1. All data measured in reference circuit with device soldered to printed circuit board.

### Features

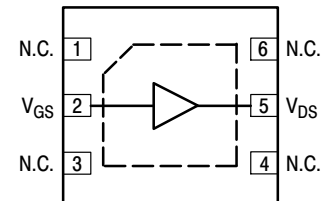
- High terminal impedances for optimal broadband performance
- Designed for low complexity linearization systems
- Universal broadband driver
- Optimized for massive MIMO active antenna systems for 5G base stations

## A5G35S004N

3300–4300 MHz, 24.5 dBm Avg., 48 V  
AIRFAST RF POWER GaN  
TRANSISTOR



DFN 4.5 × 4  
PLASTIC



(Top View)

Note: Exposed backside of the package is the source terminal for the transistor.

Figure 1. Pin Connections

**Table 1. Maximum Ratings**

Rating	Symbol	Value	Unit
Drain–Source Voltage	$V_{DSS}$	125	Vdc
Gate–Source Voltage	$V_{GS}$	–16, 0	Vdc
Operating Voltage	$V_{DD}$	55	Vdc
Maximum Forward Gate Current @ $T_C = 25^\circ\text{C}$	$I_{GMAX}$	0.74	mA
Storage Temperature Range	$T_{stg}$	–65 to +150	$^\circ\text{C}$
Case Operating Temperature Range	$T_C$	–55 to +150	$^\circ\text{C}$
Maximum Channel Temperature	$T_{CH}$	225	$^\circ\text{C}$

**Table 2. Recommended Operating Conditions**

Characteristic	Symbol	Value	Unit
Operating Voltage	$V_{DD}$	48	Vdc

**Table 3. Thermal Characteristics**

Characteristic	Symbol	Value	Unit
Thermal Resistance by Infrared Measurement, Active Die Surface–to–Case Case Temperature $113^\circ\text{C}$ , $P_D = 1.3\text{ W}$	$R_{\theta JC}$ (IR)	8.9 (1)	$^\circ\text{C/W}$
Thermal Resistance by Finite Element Analysis, Channel–to–Case Case Temperature $113^\circ\text{C}$ , $P_D = 1.3\text{ W}$	$R_{\theta CHC}$ (FEA)	32 (2)	$^\circ\text{C/W}$

**Table 4. ESD Protection Characteristics**

Test Methodology	Class
Human Body Model (per JS–001–2017)	1A
Charge Device Model (per JS–002–2014)	C2A

**Table 5. Moisture Sensitivity Level**

Test Methodology	Rating	Package Peak Temperature	Unit
Per JESD22–A113, IPC/JEDEC J–STD–020	3	260	$^\circ\text{C}$

**Table 6. Electrical Characteristics** ( $T_A = 25^\circ\text{C}$  unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
----------------	--------	-----	-----	-----	------

**Off Characteristics**

Off–State Drain Leakage ( $V_{DS} = 150\text{ Vdc}$ , $V_{GS} = -8\text{ Vdc}$ )	$I_{D(BR)}$	—	—	0.74	mAdc
---	-------------	---	---	------	------

**On Characteristics**

Gate Threshold Voltage ( $V_{DS} = 10\text{ Vdc}$ , $I_D = 0.74\text{ mAdc}$ )	$V_{GS(th)}$	–4.9	–2.5	–1.9	Vdc
Gate Quiescent Voltage ( $V_{DD} = 48\text{ Vdc}$ , $I_D = 12\text{ mAdc}$ , Measured in Functional Test)	$V_{GS(Q)}$	–2.78	–2.53	–2.30	Vdc
Gate–Source Leakage Current ( $V_{DS} = 150\text{ Vdc}$ , $V_{GS} = -12\text{ Vdc}$ )	$I_{GSS}$	–0.74	—	—	mAdc

1. Refer to AN1955, *Thermal Measurement Methodology of RF Power Amplifiers*. Go to <http://www.nxp.com/RF> and search for AN1955.
2.  $R_{\theta CHC}$  (FEA) must be used for purposes related to reliability and limitations on maximum channel temperature. MTTF may be estimated by the expression  $MTTF$  (hours) =  $10^{[A + B/(T + 273)]}$ , where  $T$  is the channel temperature in degrees Celsius,  $A = -11.1$  and  $B = 8366$ .

(continued)

**Table 6. Electrical Characteristics** ( $T_A = 25^\circ\text{C}$  unless otherwise noted) (continued)

Characteristic	Symbol	Min	Typ	Max	Unit
<b>Functional Tests</b> <sup>(1)</sup> (In NXP Production Test Fixture, 50 ohm system) $V_{DD} = 48\text{ Vdc}$ , $I_{DQ} = 12\text{ mA}$ , $P_{out} = 24.5\text{ dBm Avg.}$ , $f = 3500\text{ MHz}$ , 1-tone CW.					
Power Gain	$G_{ps}$	15.5	16.9	19.5	dB
Drain Efficiency	$\eta_D$	16.0	19.0	—	%
$P_{out}$ @ 6 dB Compression Point	P6dB	35.0	37.0	—	dBm
<b>Wideband Ruggedness</b> <sup>(2)</sup> (In NXP Reference Circuit, 50 ohm system) $I_{DQ} = 12\text{ mA}$ , $f = 3500\text{ MHz}$ , Additive White Gaussian Noise (AWGN) with 10 dB PAR					
ISBW of 400 MHz at 55 Vdc, 0.58 W Avg. Modulated Output Power (3 dB Input Overdrive from 0.28 W Avg. Modulated Output Power)	No Device Degradation				
<b>Typical Performance</b> <sup>(2)</sup> (In NXP Reference Circuit, 50 ohm system) $V_{DD} = 48\text{ Vdc}$ , $I_{DQ} = 12\text{ mA}$ , 3400–3600 MHz Bandwidth					
VBW Resonance Point (IMD Third Order Intermodulation Inflection Point)	$VBW_{res}$	—	300	—	MHz
Gain Flatness in 200 MHz Bandwidth @ $P_{out} = 24.5\text{ dBm Avg.}$	$G_F$	—	0.74	—	dB
<b>Fast CW, 27 ms Sweep</b>					
$P_{out}$ @ 6 dB Compression Point	P6dB	—	4.6	—	W
AM/PM (Maximum value measured at the P6dB compression point across the 3400–3600 MHz bandwidth)	$\Phi$	—	-16	—	°
Gain Variation over Temperature (-40°C to +85°C)	$\Delta G$	—	0.032	—	dB/°C
Output Power Variation over Temperature (-40°C to +85°C)	$\Delta P_{6dB}$	—	0.007	—	dB/°C

**Table 7. Ordering Information**

Device	Tape and Reel Information	Package
A5G35S004NT6	T6 Suffix = 5,000 Units, 12 mm Tape Width, 13-inch Reel	DFN 4.5 × 4

1. Part internally input matched.
2. All data measured in reference circuit with device soldered to printed circuit board.

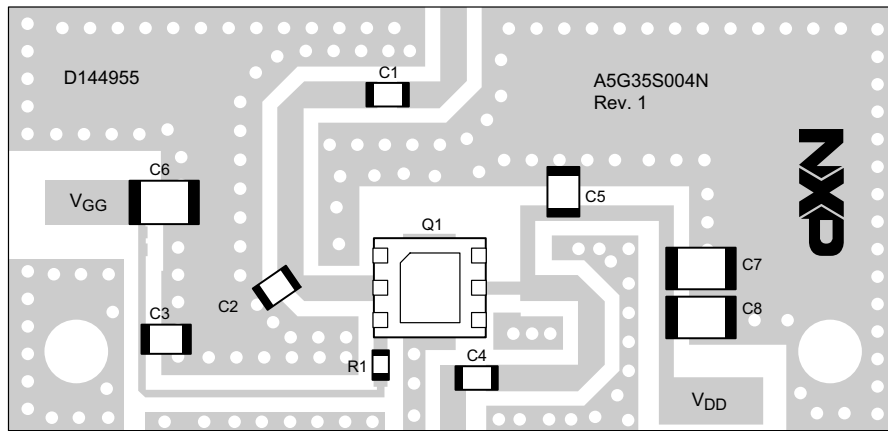
## Correct Biasing Sequence for GaN Depletion Mode Transistors

### Turning the device ON

1. Set  $V_{GS}$  to the pinch-off voltage, typically -5 V.
2. Turn on  $V_{DS}$  to nominal supply voltage (+48 V).
3. Increase  $V_{GS}$  until  $I_{DS}$  current is attained.
4. Apply RF input power to desired level.

### Turning the device OFF

1. Turn RF power off.
2. Reduce  $V_{GS}$  down to the pinch-off voltage, typically -5 V.
3. Adjust drain voltage  $V_{DS}$  to 0 V. Allow adequate time for drain voltage to reduce to 0 V from external drain capacitors.
4. Turn off  $V_{GS}$ .



Note: All data measured in reference circuit with device soldered to printed circuit board. *aaa-039743*

**Figure 2. A5G35S004N Reference Circuit Component Layout**

**Table 8. A5G35S004N Reference Circuit Component Designations and Values**

Part	Description	Part Number	Manufacturer
C1, C3, C4, C5	10 pF Chip Capacitor	600S100JT250XT	ATC
C2	1.6 pF Chip Capacitor	600S1R6BT250XT	ATC
C6, C7, C8	4.7 μF Chip Capacitor	GRM55ER72A475KA01B	Murata
Q1	RF Power GaN Transistor	A5G35S004N	NXP
R1	10 Ω, 1/10 W Chip Resistor	CRCW060310R0FKEA	Vishay
PCB	Rogers RO4350B , 0.020", ε <sub>r</sub> = 3.66	D144955	MTL

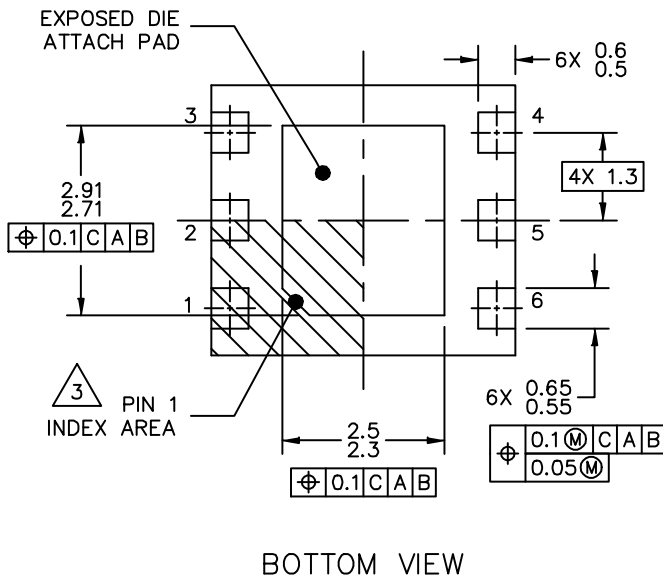
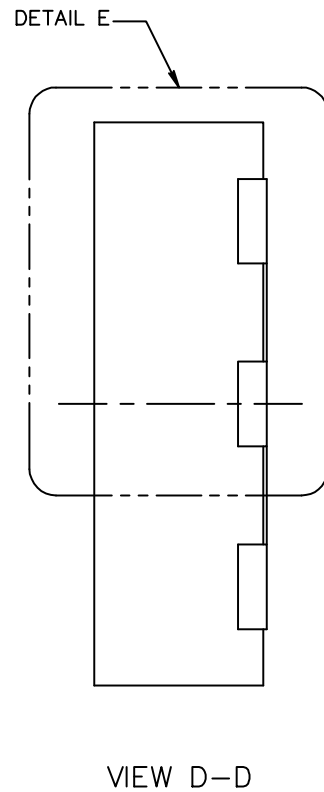
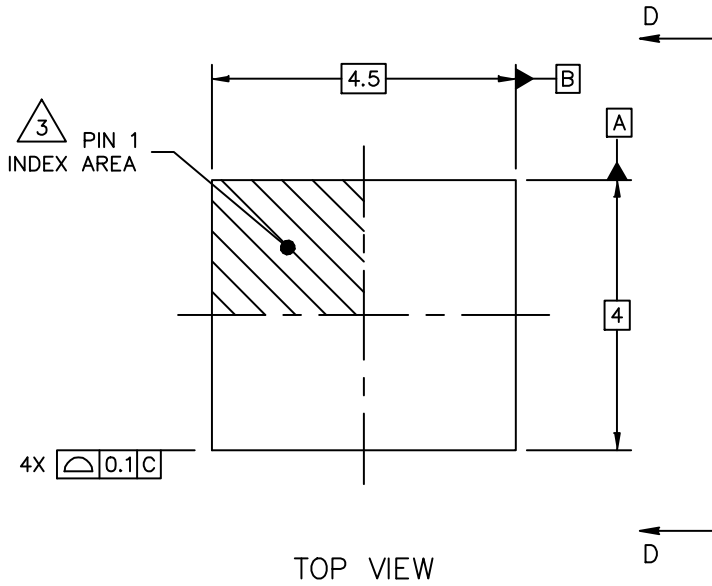


**Figure 3. Product Marking**

# Package Information

H-PDFN-6 I/O  
4.5 X 4.0 X 1.2 PKG, 1.3 PITCH

SOT2040-1



RELEASED FOR EXTERNAL ASSEMBLY ONLY. THIS DESIGN ONLY MEETS EXTERNAL DESIGN AND ASSEMBLY RULES. MUST BE REVIEWED AND UPDATED BEFORE BEING ASSEMBLED INTERNALLY.

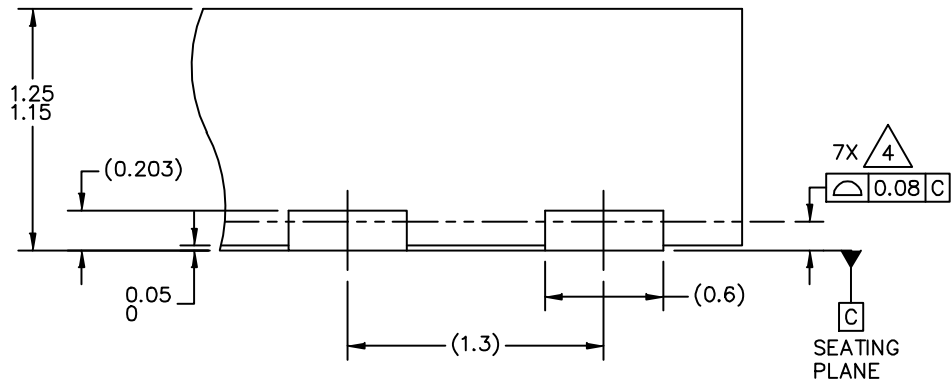
© NXP B.V. ALL RIGHTS RESERVED

DATE: 01 AUG 2019

MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON JEDEC	DRAWING NUMBER: 98ASA01496D	REVISION: 0	PAGE: 1 OF 6
--	------------------------	--------------------------------	----------------	-----------------

H-PDFN-6 I/O  
4.5 X 4.0 X 1.2 PKG, 1.3 PITCH

SOT2040-1



DETAIL E  
VIEW ROTATED 90°CW

RELEASED FOR EXTERNAL ASSEMBLY ONLY. THIS DESIGN ONLY MEETS EXTERNAL DESIGN AND ASSEMBLY RULES. MUST BE REVIEWED AND UPDATED BEFORE BEING ASSEMBLED INTERNALLY.

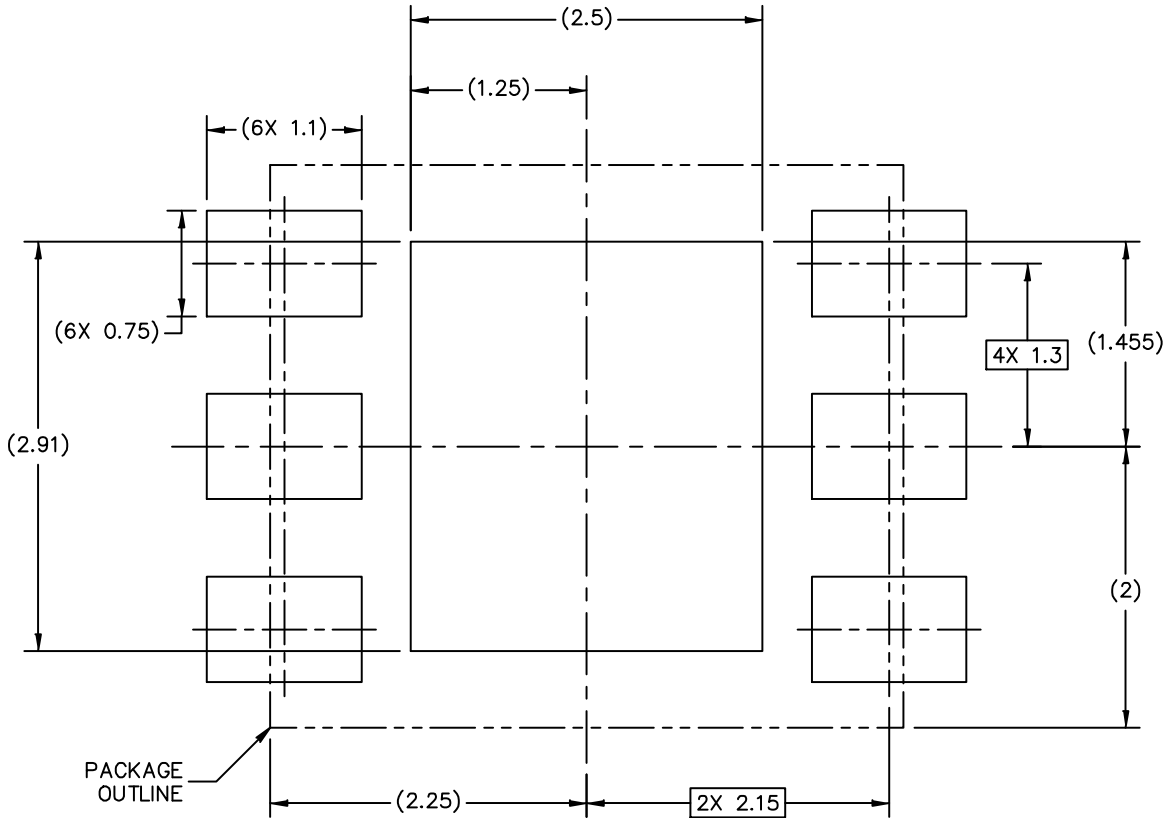
© NXP B.V. ALL RIGHTS RESERVED

DATE: 01 AUG 2019

MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON JEDEC	DRAWING NUMBER: 98ASA01496D	REVISION: 0	PAGE: 2
--	------------------------	--------------------------------	----------------	------------

H-PDFN-6 I/O  
4.5 X 4.0 X 1.2 PKG, 1.3 PITCH

SOT2040-1



PCB DESIGN GUIDELINES – SOLDER MASK OPENING PATTERN

THIS SHEET SERVES ONLY AS A GUIDELINE TO HELP DEVELOP A USER SPECIFIC SOLUTION. DEVELOPMENT EFFORT WILL STILL BE REQUIRED BY END USERS TO OPTIMIZE PCB MOUNTING PROCESSES AND BOARD DESIGN IN ORDER TO MEET INDIVIDUAL/SPECIFIC REQUIREMENTS.

© NXP B.V. ALL RIGHTS RESERVED

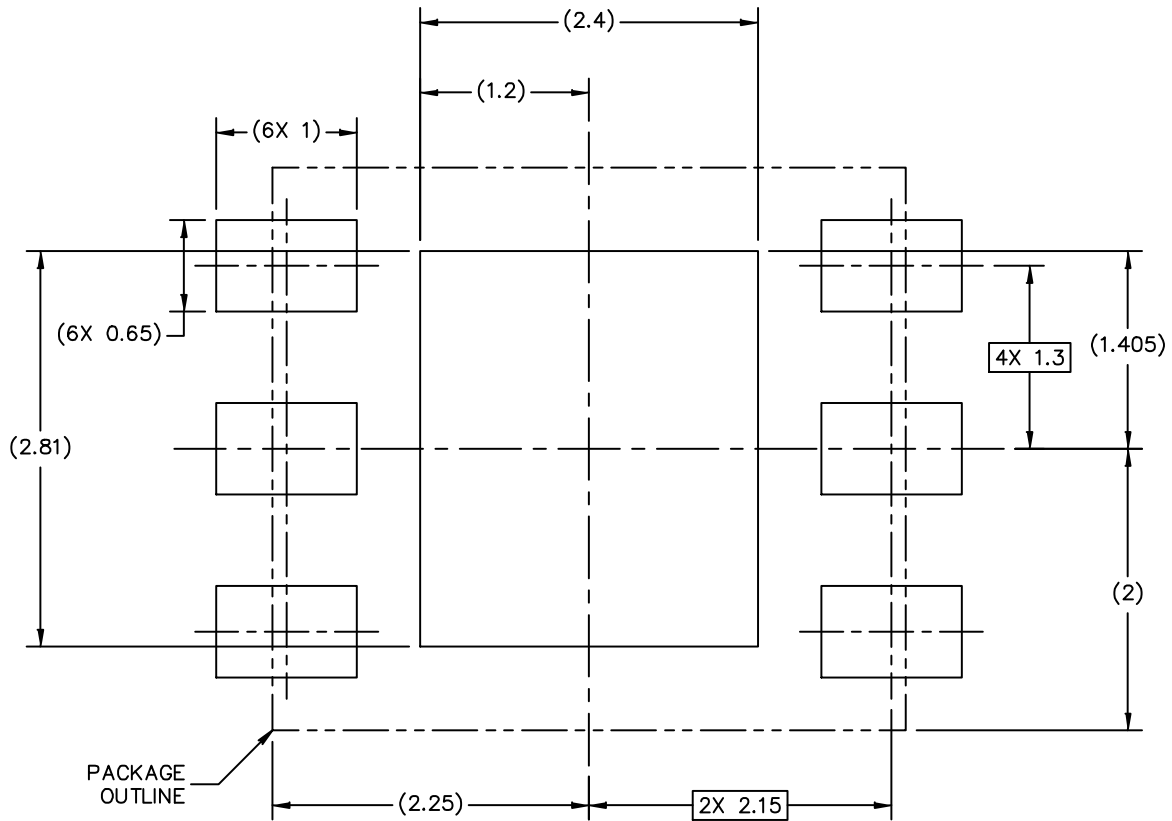
DATE: 01 AUG 2019

MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON JEDEC	DRAWING NUMBER: 98ASA01496D	REVISION: 0	PAGE: 3
--	------------------------	--------------------------------	----------------	------------



H-PDFN-6 I/O  
4.5 X 4.0 X 1.2 PKG, 1.3 PITCH

SOT2040-1



PCB DESIGN GUIDELINES – I/O PADS AND SOLDERABLE AREA

THIS SHEET SERVES ONLY AS A GUIDELINE TO HELP DEVELOP A USER SPECIFIC SOLUTION. DEVELOPMENT EFFORT WILL STILL BE REQUIRED BY END USERS TO OPTIMIZE PCB MOUNTING PROCESSES AND BOARD DESIGN IN ORDER TO MEET INDIVIDUAL/SPECIFIC REQUIREMENTS.

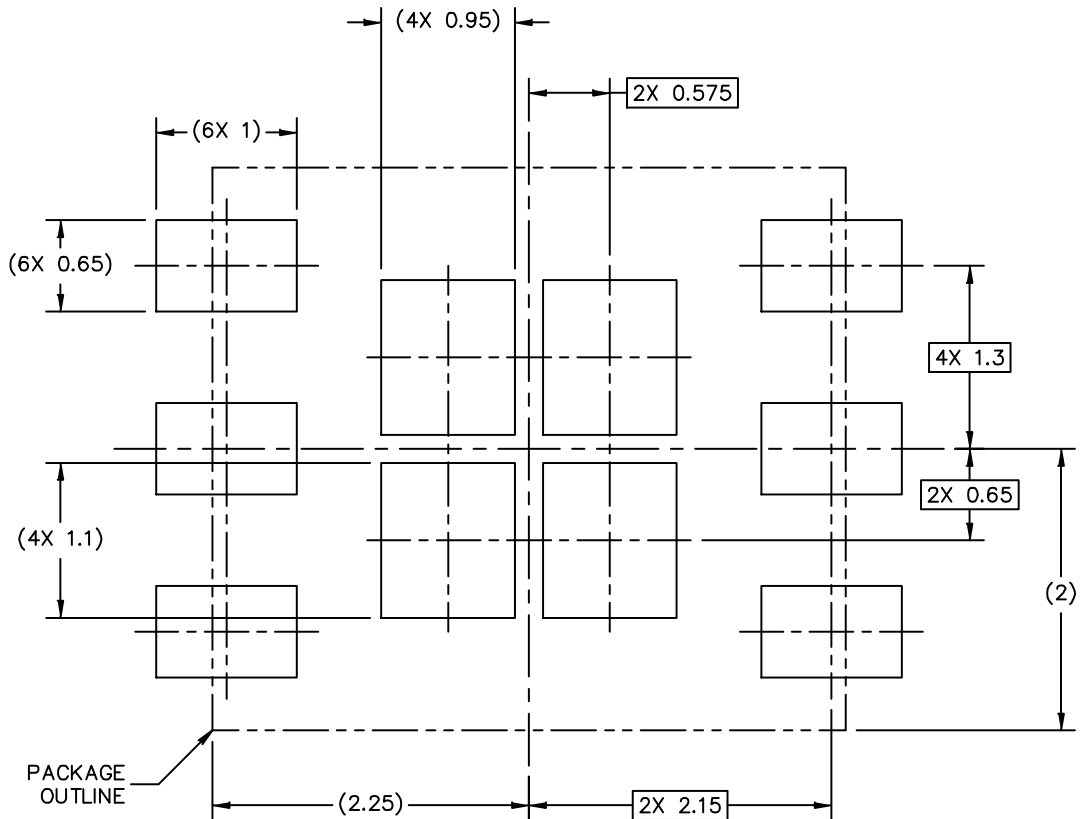
© NXP B.V. ALL RIGHTS RESERVED

DATE: 01 AUG 2019

MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON JEDEC	DRAWING NUMBER: 98ASA01496D	REVISION: 0	PAGE: 4
--	------------------------	--------------------------------	----------------	------------

H-PDFN-6 I/O  
4.5 X 4.0 X 1.2 PKG, 1.3 PITCH

SOT2040-1



RECOMMENDED STENCIL THICKNESS 0.125 OR 0.15

PCB DESIGN GUIDELINES – SOLDER PASTE STENCIL

THIS SHEET SERVES ONLY AS A GUIDELINE TO HELP DEVELOP A USER SPECIFIC SOLUTION. DEVELOPMENT EFFORT WILL STILL BE REQUIRED BY END USERS TO OPTIMIZE PCB MOUNTING PROCESSES AND BOARD DESIGN IN ORDER TO MEET INDIVIDUAL/SPECIFIC REQUIREMENTS.

© NXP B.V. ALL RIGHTS RESERVED

DATE: 01 AUG 2019

MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON JEDEC	DRAWING NUMBER: 98ASA01496D	REVISION: 0	PAGE: 5
--	------------------------	--------------------------------	----------------	------------

H-PDFN-6 I/O  
4.5 X 4.0 X 1.2 PKG, 1.3 PITCH

SOT2040-1

## NOTES:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
3. PIN 1 FEATURE SHAPE, SIZE AND LOCATION MAY VARY.
4. COPLANARITY APPLIES TO LEADS AND DIE ATTACH FLAG.

© NXP B.V. ALL RIGHTS RESERVED

DATE: 01 AUG 2019

MECHANICAL OUTLINE PRINT VERSION NOT TO SCALE	STANDARD: NON JEDEC	DRAWING NUMBER: 98ASA01496D	REVISION: 0	PAGE: 6
--	------------------------	--------------------------------	----------------	------------

## Product Documentation, Software and Tools

Refer to the following resources to aid your design process.

### Application Notes

- AN1907: Solder Reflow Attach Method for High Power RF Devices in Plastic Packages
- AN1955: Thermal Measurement Methodology of RF Power Amplifiers

### Software

- .s2p File

### Development Tools

- Printed Circuit Boards

## Revision History

The following table summarizes revisions to this document.

Revision	Date	Description
0	Dec. 2020	<ul style="list-style-type: none"> <li>• Initial release of data sheet</li> </ul>
1	Jan. 2021	<ul style="list-style-type: none"> <li>• Table 1, Maximum Ratings: updated operating voltage for complete data sheet standardization, p. 2</li> <li>• Table 2, Recommended Operating Conditions: added to data sheet, p. 2</li> </ul>
2	Jan. 2022	<ul style="list-style-type: none"> <li>• Table 6, DC On Characteristics, <math>V_{GS(th)}</math>: Min, Typ and Max values updated to match production test values, p. 2</li> </ul>
3	July 2022	<ul style="list-style-type: none"> <li>• Table 6, DC On Characteristics, <math>V_{GS(Q)}</math>: Min, Typ and Max values updated to match production test values, p. 2</li> </ul>
4	Nov. 2022	<ul style="list-style-type: none"> <li>• Table 1, Maximum Ratings: Gate–Source Voltage: updated –8, 0 to –16, 0 Vdc, p. 2</li> <li>• Table 4, ESD Protection Characteristics, Human Body Model: updated to reflect test data, p. 2</li> <li>• General updates made to align data sheet to current standard</li> </ul>

## ***How to Reach Us***

**Home Page:**  
[nxp.com](http://nxp.com)

**Web Support:**  
[nxp.com/support](http://nxp.com/support)

Information in this document is provided solely to enable system and software implementers to use NXP products. There are no express or implied copyright licenses granted hereunder to design or fabricate any integrated circuits based on the information in this document. NXP reserves the right to make changes without further notice to any products herein.

NXP makes no warranty, representation, or guarantee regarding the suitability of its products for any particular purpose, nor does NXP assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation consequential or incidental damages. "Typical" parameters that may be provided in NXP data sheets and/or specifications can and do vary in different applications, and actual performance may vary over time. All operating parameters, including "typicals," must be validated for each customer application by customer's technical experts. NXP does not convey any license under its patent rights nor the rights of others. NXP sells products pursuant to standard terms and conditions of sale, which can be found at the following address: [nxp.com/SalesTermsandConditions](http://nxp.com/SalesTermsandConditions).

NXP, the NXP logo, Freescale, the Freescale logo and Airfast are trademarks of NXP B.V. All other product or service names are the property of their respective owners.

© NXP B.V. 2020–2022

**All rights reserved.**

For more information, please visit: <http://www.nxp.com>

For sales office addresses, please send an email to: [salesaddresses@nxp.com](mailto:salesaddresses@nxp.com)

Date of release: November 2022  
Document identifier: A5G35S004N