## Features

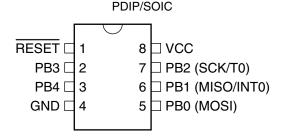
- Utilizes the AVR<sup>®</sup> RISC Architecture
- AVR High-performance and Low-power RISC Architecture
  - 118 Powerful Instructions Most Single Clock Cycle Execution
  - 32 x 8 General Purpose Working Registers
  - Up to 1MIPS Throughput at 1MHz
- Data and Nonvolatile Program Memory
  - 2K Bytes of In-System Programmable Flash Endurance 1,000 Write/Erase Cycles
    - 128 Bytes of internal SRAM
    - 128 Bytes of In-System Programmable EEPROM
      - Endurance: 100,000 Write/Erase Cycles
- Programming Lock for Flash Program and EEPROM Data Security
- Peripheral Features
  - One 8-bit Timer/Counter with Separate Prescaler
  - Programmable Watchdog Timer with On-chip Oscillator
  - SPI Serial Interface for In-System Programming
- Special Microcontroller Features
  - Low-power Idle and Power Down Modes
  - External and Internal Interrupt Sources
  - Power-on Reset Circuit
  - On-chip RC Oscillator
- Specifications
  - Low-power, High-speed CMOS Process Technology
- Fully Static Operation
- Power Consumption at 3V, 25°C
  - Active: 1.5 mA
  - Idle Mode: 100 μA
  - Power Down Mode: <1 µA</p>
- I/O and Packages
  - 5 Programmable I/O Lines
  - 8-pin PDIP and SOIC
- Operating Voltages
- 2.7 6.0V
- Speed Grade
  - Internal Oscillator ~1MHz @ 5.0V

## Description

The ATtiny22L is a low-power CMOS 8-bit microcontroller based on the AVR RISC architecture. By executing powerful instructions in a single clock cycle, the ATtiny22L achieves throughputs approaching 1 MIPS per MHz allowing the system designer to optimize power consumption versus processing speed.

The AVR core combines a rich instruction set with 32 general purpose working registers. All the 32 registers are directly connected to the Arithmetic Logic Unit (ALU),

## **Pin Configuration**





8-bit **AVR**<sup>®</sup> Microcontroller with 2K Bytes of In-System Programmable Flash

# ATtiny22L

# Preliminary

Rev. 1273BS-02/00

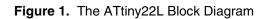
Note: This is a summary document. For the complete 56-page document, please visit our web site at *www.atmel.com* or e-mail at *literature@atmel.com* and request literature #1273B.

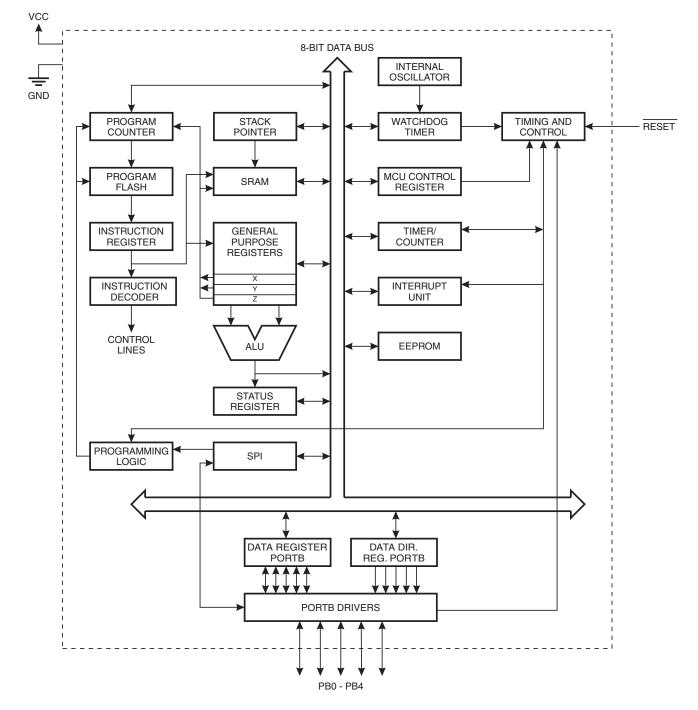




allowing two independent registers to be accessed in one single instruction executed in one clock cycle. The resulting architecture is more code efficient while achieving throughputs up to ten times faster than conventional CISC microcontrollers.

### **Block Diagram**





ATtiny22L

ATtiny22L

The ATtiny22L provides the following features: 2K bytes of In-System Programmable Flash, 128 bytes EEPROM, 128 bytes SRAM, five general purpose I/O lines, 32 general purpose working registers, an 8-bit timer/counter, internal and external interrupts, programmable Watchdog Timer with internal oscillator, an SPI serial port for Flash Memory downloading and two software selectable power saving modes. The Idle Mode stops the CPU while allowing the SRAM, timer/counters, SPI port and interrupt system to continue functioning. The power down mode saves the register contents but freezes the oscillator, disabling all other chip functions until the next interrupt or hardware reset.

The device is manufactured using Atmel's high density nonvolatile memory technology. The on-chip Flash allows the program memory to be reprogrammed in-system through an SPI serial interface. By combining an 8-bit RISC CPU with ISP Flash on a monolithic chip, the Atmel ATtiny22L is a powerful microcontroller that provides a highly flexible and cost effective solution to many embedded control applications.

The ATtiny22L AVR is supported with a full suite of program and system development tools including: C compilers, macro assemblers, program debugger/simulators, in-circuit emulators, and evaluation kits.

## **Pin Descriptions ATtiny22L**

#### vcc

Supply voltage pin.

### GND

Ground pin.

### Port B (PB4..PB0)

Port B is a 5-bit bi-directional I/O port with internal pull-up resistors. The Port B output buffers can sink 20 mA. As inputs, Port B pins that are externally pulled low, will source current if the pull-up resistors are activated.

Port B also serves the functions of various special features.

Port pins can provide internal pull-up resistors (selected for each bit). The port B pins are tri-stated when a reset condition becomes active.

### RESET

Reset input. An external reset is generated by a low level on the RESET pin. Reset pulses longer than 50 ns will generate a reset, even if the clock is not running. Shorter pulses are not guaranteed to generate a reset.

## **Clock Source**

The ATtiny22L is clocked by an on-chip RC oscillator. This RC oscillator runs at a nominal frequency of 1 MHz (VCC = 5V).

## **Architectural Overview**

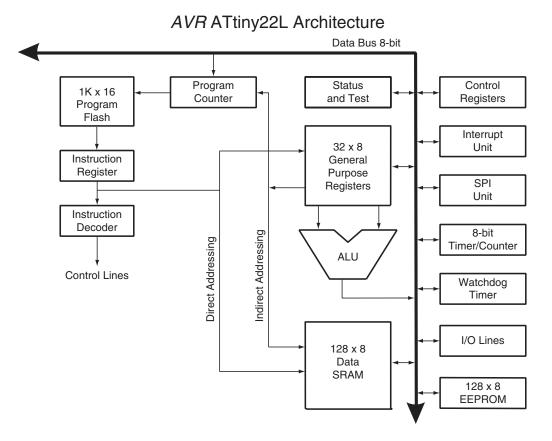
The fast-access register file concept contains 32 x 8-bit general purpose working registers with a single clock cycle access time. This means that during one single clock cycle, one arithmetic logic unit (ALU) operation is executed. Two operands are output from the register file, the operation is executed, and the result is stored back in the register file in one clock cycle.

Six of the 32 registers can be used as three 16-bit indirect address register pointers for Data Space addressing enabling efficient address calculations. One of the three address pointers is also used as the address pointer for the constant table look up function. These added function registers are the 16-bit X-register, Y-register and Z-register.





#### Figure 2. The ATtiny22L AVR RISC Architecture



The ALU supports arithmetic and logic functions between registers or between a constant and a register. Single register operations are also executed in the ALU. Figure 2 shows the ATtiny22L AVR RISC microcontroller architecture.

In addition to the register operation, the conventional memory addressing modes can be used on the register file as well. This is enabled by the fact that the register file is assigned the 32 lowermost Data Space addresses (\$00 - \$1F), allowing them to be accessed as though they were ordinary memory locations.

The I/O memory space contains 64 addresses for CPU peripheral functions as Control Registers, Timer/Counters, A/D-converters, and other I/O functions. The I/O memory can be accessed directly, or as the Data Space locations following those of the register file, \$20 - \$5F.

The AVR has Harvard architecture - with separate memories and buses for program and data. The program memory is accessed with a two stage pipeline. While one instruction is being executed, the next instruction is pre-fetched from the program memory. This concept enables instructions to be executed in every clock cycle. The program memory is in-system downloadable Flash memory.

With the relative jump and call instructions, the whole 1K address space is directly accessed. Most AVR instructions have a single 16-bit word format. Every program memory address contains a 16- or 32-bit instruction.

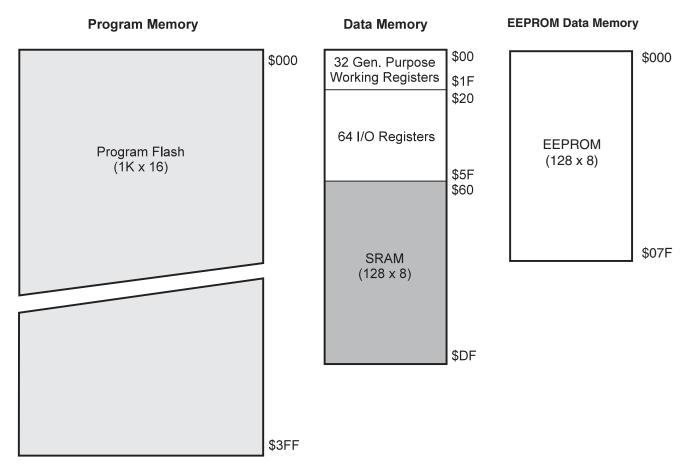
During interrupts and subroutine calls, the return address program counter (PC) is stored on the stack. The stack is effectively allocated in the general data SRAM, and consequently the stack size is only limited by the total SRAM size and the usage of the SRAM. All user programs must initialize the SP in the reset routine (before subroutines or interrupts are executed). The 8-bit stack pointer SP is read/write accessible in the I/O space.

The 128 bytes data SRAM + register file and I/O registers can be easily accessed through the five different addressing modes supported in the AVR architecture.

The memory spaces in the AVR architecture are all linear and regular memory maps.

# ATtiny22L

Figure 3. Memory Maps



A flexible interrupt module has its control registers in the I/O space with an additional global interrupt enable bit in the status register. All the different interrupts have a separate interrupt vector in the interrupt vector table at the beginning of the program memory. The different interrupts have priority in accordance with their interrupt vector position. The lower the interrupt vector address, the higher the priority.





## **Register Summary**

Address	Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Page
\$3F (\$5F)	SREG	I	Т	Н	S	V	N	Z	С	page 16
\$3E (\$5E)	Reserved				•			•		
\$3D (\$5D)	SPL	SP7	SP6	SP5	SP4	SP3	SP2	SP1	SP0	page 17
\$3C (\$5C)	Reserved				•			•	•	
\$3B (\$5B)	GIMSK	-	INT0	-	-	-	-	-	-	page 23
\$3A (\$5A)	GIFR	-	INTF0							page 23
\$39 (\$59)	TIMSK	-	-	-	-	-	-	TOIE0	-	page 23
\$38 (\$58)	TIFR	-	-	-	-	-	-	TOV0	-	page 24
\$37 (\$57)	Reserved							•		
\$36 (\$56)	Reserved									
\$35 (\$55)	MCUCR	-	-	SE	SM	-	-	ISC01	ISC00	page 24
\$34 (\$54)	MCUSR	-	-	-	-	-	-	EXTRF	PORF	page 22
\$33 (\$53)	TCCR0	-	-	-	-	-	CS02	CS01	CS00	page 27
\$32 (\$52)	TCNT0	Timer/Co	ounter0 (8 Bit	)					İ	page 28
\$31 (\$51)	Reserved		•							
\$30 (\$50)	Reserved									
\$2F (\$4F)	Reserved									
\$2E (\$4E)	Reserved									
\$2D (\$4D)	Reserved									
\$2C (\$4C)	Reserved									
\$2B (\$4B)	Reserved									
\$2A (\$4A)	Reserved									
\$29 (\$49)	Reserved									
\$28 (\$48)	Reserved									
\$27 (\$47)	Reserved									
\$26 (\$46)	Reserved									
\$25 (\$45)	Reserved									
\$24 (\$44)	Reserved									
\$23 (\$43)	Reserved									
\$22 (\$42)	Reserved									
\$21 (\$41)	WDTCR	-	-	-	WDTOE	WDE	WDP2	WDP1	WDP0	page 28
\$20 (\$40)	Reserved				•					1 3 4
\$1F (\$3F)	Reserved									
\$1E (\$3E)	EEAR	-	EEPROM	Address Re	gister					page 30
\$1D (\$3D)	EEDR		I Data registe		U - · ·				1	page 30
\$1C (\$3C)	EECR	-	-	-	-	-	EEMW	EEWE	EERE	page 30
\$1B (\$3B)	Reserved									- 30 00
\$1A (\$3A)	Reserved									
\$19 (\$39)	Reserved									
	PORTB	_	-	-	PORTB	PORTB	PORTB	PORTB	PORTB	page 32
	DDRB	_	-	-	DDB4	DDB3	DDB2	DDB1	DDB0	page 32
\$18 (\$38)				-	PINB4	PINB3	PINB2	PINB1	PINB0	page 32
\$18 (\$38) \$17 (\$37)		-	-							
\$18 (\$38) \$17 (\$37) \$16 (\$36)	PINB	-	-							page or
\$18 (\$38) \$17 (\$37)		-	-					•		pago oz

Notes: 1. For compatibility with future devices, reserved bits should be written to zero if accessed. Reserved I/O memory addresses should never be written.

 Some of the status flags are cleared by writing a logical one to them. Note that the CBI and SBI instructions will operate on all bits in the I/O register, writing a one back into any flag read as set, thus clearing the flag. The CBI and SBI instructions work with registers \$00 to \$1F only.

# ATtiny22L

# Instruction Set Summary

Mnemonics	Operands	Description	Operation	Flags	#Clock
ARITHMETIC AN	ID LOGIC INSTRU			•	
ADD	Rd, Rr	Add two Registers	$Rd \leftarrow Rd + Rr$	Z,C,N,V,H	1
ADC	Rd, Rr	Add with Carry two Registers	$Rd \leftarrow Rd + Rr + C$	Z,C,N,V,H	1
ADIW	Rdl,K	Add Immediate to Word	$Rdh:RdI \leftarrow Rdh:RdI + K$	Z,C,N,V,S	2
SUB	Rd, Rr	Subtract two Registers	$Rd \leftarrow Rd - Rr$	Z,C,N,V,H	1
SUBI	Rd, K	Subtract Constant from Register	$Rd \leftarrow Rd - K$	Z,C,N,V,H	1
SBIW	Rdl,K	Subtract Immediate from Word	$Rdh:RdI \leftarrow Rdh:RdI - K$	Z,C,N,V,S	2
SBC	Rd, Rr	Subtract with Carry two Registers	$Rd \leftarrow Rd - Rr - C$	Z,C,N,V,H	1
SBCI	Rd, K	Subtract with Carry Constant from Reg.	$Rd \leftarrow Rd - K - C$	Z,C,N,V,H	1
AND	Rd, Rr	Logical AND Registers	$Rd \leftarrow Rd \bullet Rr$	Z,N,V	1
ANDI	Rd, K	Logical AND Register and Constant	$Rd \leftarrow Rd \bullet K$	Z,N,V	1
OR	Rd, Rr	Logical OR Registers	$Rd \leftarrow Rd v Rr$	Z,N,V	1
ORI	Rd, K	Logical OR Register and Constant	$Rd \leftarrow Rd \ v \ K$	Z,N,V	1
EOR	Rd, Rr	Exclusive OR Registers	$Rd \leftarrow Rd \oplus Rr$	Z,N,V	1
COM	Rd	One's Complement	Rd ← \$FF – Rd	Z,C,N,V	1
NEG	Rd	Two's Complement	Rd ← \$00 - Rd	Z,C,N,V,H	1
SBR	Rd,K	Set Bit(s) in Register	$Rd \leftarrow Rd v K$	Z,N,V	1
CBR	Rd,K	Clear Bit(s) in Register	$Rd \leftarrow Rd \bullet (\$FF - K)$	Z,N,V	1
INC	Rd	Increment	$Rd \leftarrow Rd + 1$	Z,N,V	1
DEC	Rd	Decrement	$Rd \leftarrow Rd - 1$	Z,N,V	1
TST	Rd	Test for Zero or Minus	$Rd \leftarrow Rd \bullet Rd$	Z,N,V	1
CLR	Rd	Clear Register	$Rd \leftarrow Rd \oplus Rd$	Z,N,V	1
SER	Rd	Set Register	Rd ← \$FF	None	1
BRANCH INSTR					
RJMP	k	Relative Jump	$PC \leftarrow PC + k + 1$	None	2
IJMP	K	Indirect Jump to (Z)	PC ← Z	None	2
RCALL	k	Relative Subroutine Call	$PC \leftarrow PC + k + 1$	None	3
ICALL		Indirect Call to (Z)	PC ← Z	None	3
RET		Subroutine Return	PC ← STACK	None	4
RETI		Interrupt Return	PC ← STACK		4
CPSE	Rd,Rr	Compare, Skip if Equal	if (Rd = Rr) PC $\leftarrow$ PC + 2 or 3	None	1/2/3
CP	Rd,Rr	Compare	Rd – Rr	Z, N,V,C,H	1
CPC	Rd,Rr	Compare with Carry	Rd – Rr – C	Z, N,V,C,H	1
CPI	Rd,K	Compare Register with Immediate	Rd – K	Z, N,V,C,H	1
SBRC	Rr, b	Skip if Bit in Register Cleared	if (Rr(b)=0) PC $\leftarrow$ PC + 2 or 3	None	1/2/3
SBRS	Rr, b	Skip if Bit in Register is Set	if (Rr(b)=1) PC $\leftarrow$ PC + 2 or 3	None	1/2/3
SBIC	P, b	Skip if Bit in I/O Register Cleared	if $(P(b)=0) PC \leftarrow PC + 2 or 3$	None	1/2/3
SBIS	P, b	Skip if Bit in I/O Register is Set	if $(R(b)=1) PC \leftarrow PC + 2 or 3$	None	1/2/3
BRBS	s, k	Branch if Status Flag Set	if (SREG(s) = 1) then $PC \leftarrow PC + k + 1$	None	1/2
BRBC	s, k	Branch if Status Flag Cleared	if (SREG(s) = 0) then $PC \leftarrow PC + k + 1$	None	1/2
BREQ	k	Branch if Equal	if (Z = 1) then PC $\leftarrow$ PC + k + 1	None	1/2
BRNE	k	Branch if Not Equal	if (Z = 0) then PC $\leftarrow$ PC + k + 1	None	1/2
BRCS	k	Branch if Carry Set	if (C = 1) then PC $\leftarrow$ PC + k + 1	None	1/2
BRCC	k k	Branch if Carry Cleared	if (C = 0) then PC $\leftarrow$ PC + k + 1 if (C = 0) then PC $\leftarrow$ PC + k + 1	None	1/2
BRSH	k	Branch if Same or Higher	if (C = 0) then PC $\leftarrow$ PC + k + 1	None	1/2
BRLO	k	Branch if Lower	if (C = 1) then PC $\leftarrow$ PC + k + 1	None	1/2
BRMI	k k	Branch if Minus	if (N = 1) then PC $\leftarrow$ PC + k + 1	None	1/2
BRPL					
BRGE	k	Branch if Plus	if (N = 0) then PC $\leftarrow$ PC + k + 1 if (N $\oplus$ V= 0) then PC $\leftarrow$ PC + k + 1	None	1/2
	k	Branch if Greater or Equal, Signed	if $(N \oplus V = 0)$ then PC $\leftarrow$ PC + k + 1 if $(N \oplus V = 1)$ then PC $\leftarrow$ PC + k + 1	None	1/2
BRLT	k	Branch if Less Than Zero, Signed Branch if Half Carry Flag Set	if $(N \oplus V = 1)$ then PC $\leftarrow$ PC + k + 1 if $(H = 1)$ then PC $\leftarrow$ PC + k + 1	None	1/2
BRHS	k	, ,		None	
BRHC	k	Branch if Half Carry Flag Cleared	if $(H = 0)$ then $PC \leftarrow PC + k + 1$	None	1/2
BRTS	k	Branch if T Flag Set	if $(T = 1)$ then PC $\leftarrow$ PC + k + 1	None	1/2
BRTC	k	Branch if T Flag Cleared	if (T = 0) then PC $\leftarrow$ PC + k + 1	None	1/2
BRVS	k	Branch if Overflow Flag is Set	if (V = 1) then PC $\leftarrow$ PC + k + 1	None	1/2
BRVC	k	Branch if Overflow Flag is Cleared	if (V = 0) then PC $\leftarrow$ PC + k + 1	None	1/2
BRIE	k	Branch if Interrupt Enabled	if (I = 1) then PC $\leftarrow$ PC + k + 1	None	1/2
BRID	k	Branch if Interrupt Disabled	if (I = 0) then PC $\leftarrow$ PC + k + 1	None	1/2





# Instruction Set Summary (Continued)

Mnemonics	Operands	Description	Operation	Flags	#Clock
DATA TRANSFER	INSTRUCTIONS	•			
MOV	Rd, Rr	Move Between Registers	Rd ← Rr	None	1
LDI	Rd, K	Load Immediate	$Rd \leftarrow K$	None	1
LD	Rd, X	Load Indirect	$Rd \leftarrow (X)$	None	2
LD	Rd, X+	Load Indirect and Post-Inc.	$Rd \leftarrow (X),  X \leftarrow X + 1$	None	2
LD	Rd, - X	Load Indirect and Pre-Dec.	$X \leftarrow X - 1, Rd \leftarrow (X)$	None	2
LD	Rd, Y	Load Indirect	$Rd \leftarrow (Y)$	None	2
LD	Rd, Y+	Load Indirect and Post-Inc.	$Rd \leftarrow (Y), Y \leftarrow Y + 1$	None	2
LD	Rd, - Y	Load Indirect and Pre-Dec.	$Y \leftarrow Y - 1$ , Rd $\leftarrow$ (Y)	None	2
LDD	Rd,Y+q	Load Indirect with Displacement	$Rd \leftarrow (Y + q)$	None	2
LD	Rd, Z	Load Indirect	$Rd \leftarrow (Z)$	None	2
LD	Rd, Z+	Load Indirect and Post-Inc.	$Rd \leftarrow (Z), Z \leftarrow Z+1$	None	2
LD	Rd, -Z	Load Indirect and Pre-Dec.	$Z \leftarrow Z - 1$ , Rd $\leftarrow (Z)$	None	2
LDD	Rd, Z+q	Load Indirect with Displacement	$Rd \leftarrow (Z + q)$	None	2
LDS	Rd. k	Load Direct from SRAM	$Rd \leftarrow (k)$	None	2
ST	X, Rr	Store Indirect	$(X) \leftarrow Rr$	None	2
ST	X+, Rr	Store Indirect and Post-Inc.	$(X) \leftarrow \text{Rr}, X \leftarrow X + 1$	None	2
ST	- X, Rr	Store Indirect and Pre-Dec.	$X \leftarrow X - 1, (X) \leftarrow Rr$	None	2
ST	Y, Rr	Store Indirect	$(Y) \leftarrow Rr$	None	2
ST	Y+, Rr	Store Indirect and Post-Inc.	$(Y) \leftarrow Rr, Y \leftarrow Y + 1$	None	2
ST	- Y, Rr	Store Indirect and Pre-Dec.	$Y \leftarrow Y - 1, (Y) \leftarrow Rr$	None	2
STD	Y+q,Rr	Store Indirect with Displacement	$(Y+q) \leftarrow Rr$	None	2
ST	Z, Rr	Store Indirect	$(Z) \leftarrow Rr$	None	2
ST	Z+, Rr	Store Indirect and Post-Inc.	$(Z) \leftarrow \operatorname{Rr}, Z \leftarrow Z + 1$	None	2
ST	-Z, Rr	Store Indirect and Pre-Dec.	$Z \leftarrow Z - 1, (Z) \leftarrow Rr$	None	2
STD	Z+q,Rr	Store Indirect with Displacement	$(Z + q) \leftarrow Rr$	None	2
STS	k, Rr	Store Direct to SRAM	$(k) \leftarrow Rr$	None	2
LPM	к, пі	Load Program Memory	$(R) \leftarrow DI$ $R0 \leftarrow (Z)$	None	3
	Rd, P	In Port	$Rd \leftarrow P$	None	1
		Out Port			-
PUSH	P, Rr		P ← Rr	None	1
	Rr	Push Register on Stack	STACK ← Rr	None	2
POP BIT AND BIT-TES		Pop Register from Stack	Rd ← STACK	None	2
SBI	P,b	Set Bit in I/O Register	1/O(Bb) 1	None	2
CBI	P,b		$I/O(P,b) \leftarrow 1$	None	2
		Clear Bit in I/O Register	$I/O(P,b) \leftarrow 0$		
LSL	Rd	Logical Shift Left	$Rd(n+1) \leftarrow Rd(n), Rd(0) \leftarrow 0$	Z,C,N,V	1
LSR	Rd	Logical Shift Right	$Rd(n) \leftarrow Rd(n+1), Rd(7) \leftarrow 0$	Z,C,N,V	
ROL	Rd	Rotate Left Through Carry	$Rd(0) \leftarrow C, Rd(n+1) \leftarrow Rd(n), C \leftarrow Rd(7)$	Z,C,N,V	1
ROR	Rd	Rotate Right Through Carry	$Rd(7) \leftarrow C, Rd(n) \leftarrow Rd(n+1), C \leftarrow Rd(0)$	Z,C,N,V	1
ASR	Rd	Arithmetic Shift Right	$Rd(n) \leftarrow Rd(n+1), n=06$	Z,C,N,V	1
SWAP	Rd	Swap Nibbles	Rd(30)←Rd(74),Rd(74)←Rd(30)	None	1
BSET	S	Flag Set	SREG(s) ← 1	SREG(s)	1
BCLR	S	Flag Clear	SREG(s) ← 0	SREG(s)	1
BST	Rr, b	Bit Store from Register to T	T ← Rr(b)		1
BLD	Rd, b	Bit load from T to Register	Rd(b) ← T	None	1
SEC		Set Carry	C ← 1	С	1
CLC		Clear Carry	$C \leftarrow 0$	С	1
SEN		Set Negative Flag	N ← 1	N	1
CLN		Clear Negative Flag	N ← 0	N	1
SEZ		Set Zero Flag	Z ← 1	Z	1
CLZ		Clear Zero Flag	$Z \leftarrow 0$	Z	1
SEI		Global Interrupt Enable	I ← 1	1	1
CLI		Global Interrupt Disable	l ← 0		1
SES		Set Signed Test Flag	S ← 1	S	1
		Clear Signed Test Flag	S ← 0	S	1
CLS		Set Twos Complement Overflow	V ← 1	V	1
SEV			$V \leftarrow 0$	V	1
SEV CLV		Clear Twos Complement Overflow			
SEV		Set T in SREG	T ← 1	Т	1
SEV CLV			T ← 1	T T	1
SEV CLV SET		Set T in SREG Clear T in SREG		-	
SEV CLV SET CLT SEH		Set T in SREG Clear T in SREG Set Half Carry Flag in SREG	$\begin{array}{c} T \leftarrow 1 \\ T \leftarrow 0 \\ H \leftarrow 1 \end{array}$	Т	1
SEV CLV SET CLT SEH CLH		Set T in SREG Clear T in SREG Set Half Carry Flag in SREG Clear Half Carry Flag in SREG	$\begin{array}{c} T \leftarrow 1 \\ T \leftarrow 0 \end{array}$	T H H	1
SEV CLV SET CLT SEH		Set T in SREG Clear T in SREG Set Half Carry Flag in SREG	$\begin{array}{c} T \leftarrow 1 \\ T \leftarrow 0 \\ H \leftarrow 1 \end{array}$	T H	1 1 1

# ATtiny22L



# **Ordering Information**

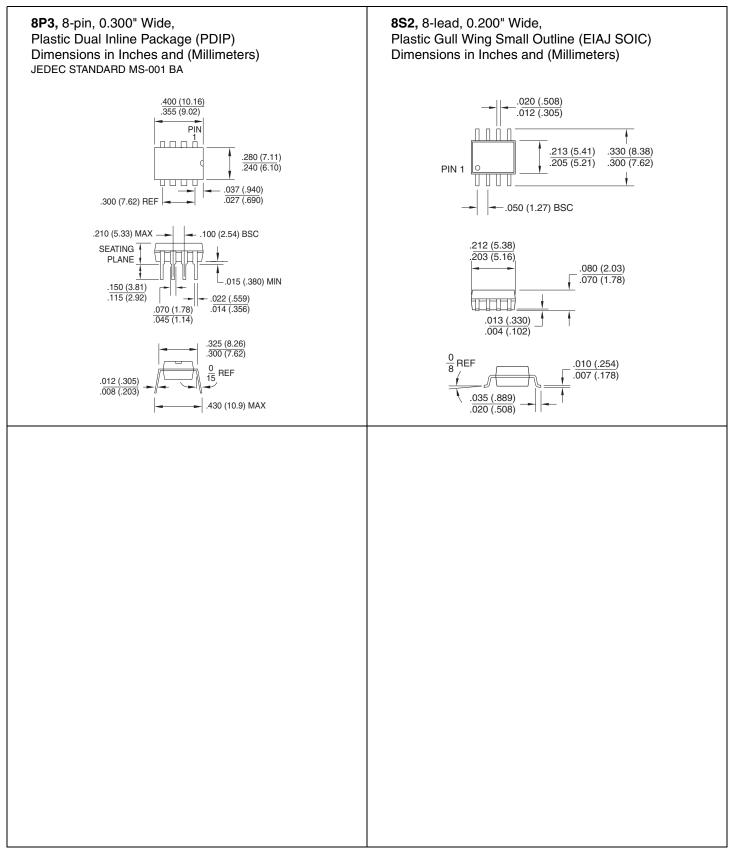
Power Supply	Speed (MHz)	Ordering Code	Package	<b>Operation Range</b>
2.7 - 6.0V	Internal Osc ~1MHz@5.0V	ATtiny22L-1PC ATtiny22L-1SC	8P3 8S2	Commercial (0°C to 70°C)
		ATtiny22L-1PI ATtiny22L-1SI	8P3 8S2	Industrial (-40°C to 85°C)

Package Type					
8P3	8-pin, 0.300" Wide, Plastic Dual Inline Package (PDIP)				
8S2	8-lead, 0.200" Wide, Plastic Gull-Wing Small Outline (EIAJ SOIC)				
032	o-lead, 0.200 Wide, Flastic Guil-Wing Small Outline (EIAJ SOIC)				





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