

High-voltage evaluation board for the PWD13F60 full-bridge high density power driver

Data brief



Features

- Power system-in-package integrating gate drivers and high-voltage power MOSFETs:
 - Low $R_{DS(on)}$ = 320 m Ω
 - BV_{DSS} = 600 V
- Suitable for operating as:
 - Full-bridge
 - Dual independent half-bridges
- Wide input supply voltage down to 6.5 V
- UVLO protection on supply voltage
- 3.3 V to 15 V compatible inputs with hysteresis and pull-down
- Interlocking function to prevent cross conduction
- Internal bootstrap diodes
- QFN (10x13 mm) package
- Very compact layout
- RoHS compliant

Applications

- Motor drivers for industrial and home appliances
- Factory automation
- Fans and pumps
- HID, ballasts
- Power supply units
- DC-DC and DC-AC converters

Description

The PWD13F60 is a high density power driver integrating gate drivers and four N-channel power MOSFETs in dual half-bridge configuration.

The integrated power MOSFETs have a low $R_{DS(on)}$ of 320 m Ω and 600 V drain-source breakdown voltage, while the embedded gate drivers high-side can be easily supplied by the integrated bootstrap diode. The high integration of the device allows loads in a tiny space to be driven efficiently.

The PWD13F60 accepts a supply voltage (V_{CC}) extending over a wide range and is protected by a low voltage UVLO detection on the supply voltage.

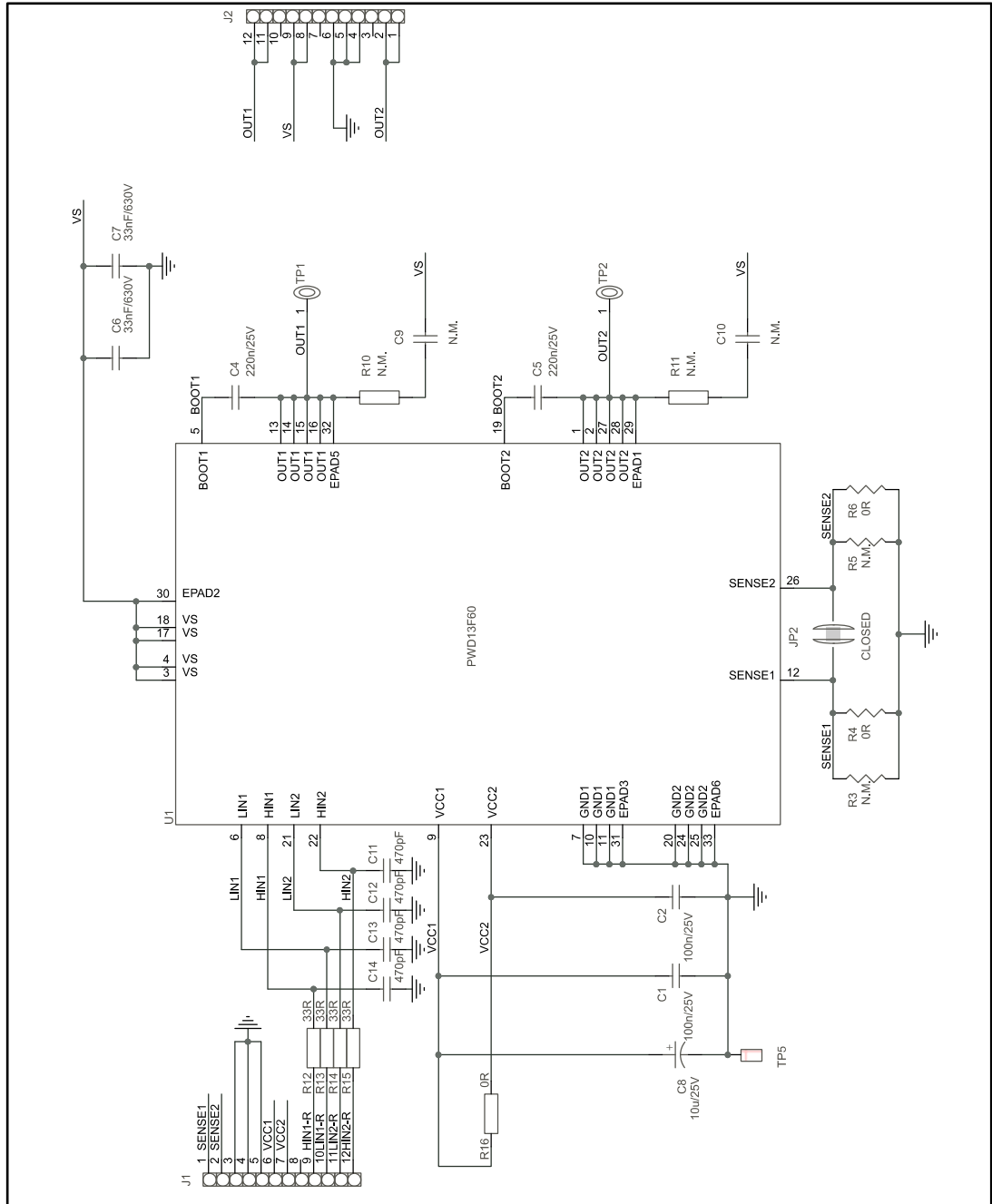
The input pin extended range allows easy interfacing with microcontrollers, DSP units or Hall effect sensors.

The EVALPWD13F60 is 48 x 53 mm wide, FR-4 PCB resulting in an $R_{th(J-A)}$ of 18 °C/W, capable to drive loads up to 2 A_{RMS} , without forced airflow cooling.

Both controlling and power signals are available on pin strip for easy connection to customer's board.

1 Schematic diagram

Figure 1: EVALPWD13F60 circuit schematic



2 Bill of material

Table 1: EVALPWD13F60 bill of materials

Reference	Part/value	Description
C1, C2	100 nF / 25 V	Ceramic capacitor, SMT 0603
C4, C5	220 nF / 25 V	Ceramic capacitor, SMT 0805
C6, C7	33 nF / 630 V	Ceramic capacitor, SMT 1206
C8	10 μ F / 25 V	Ceramic capacitor, SMT 1206
C9, C10	N.M.	Ceramic capacitor, SMT 1206
C11, C12, C13, C14	470 pF	Ceramic capacitor, SMT 0603
JP2	Closed	SMT jumper
J1, J2	Pin strip	Conn. header 12 POS 2.54 mm
R3, R5	N.M.	Chip resistor, SMT 2512
R4, R6	0 Ω	Chip resistor, SMT 2512
R10, R11	N.M.	Chip resistor, SMT 0805
R12, R13, R14, R15	33 Ω	Chip resistor, SMT 0603
R16	0 Ω	Chip resistor, SMT 0603
TP1, TP2	Test point	Loop test point, THT
TP5	Test point	Pin test point, THT
U1	PWD13F60	Full-bridge with integrated gate driver, QFN 10x13 mm

3 PCB layout

Figure 2: EVALPWD13F60 – layout (component placement view)

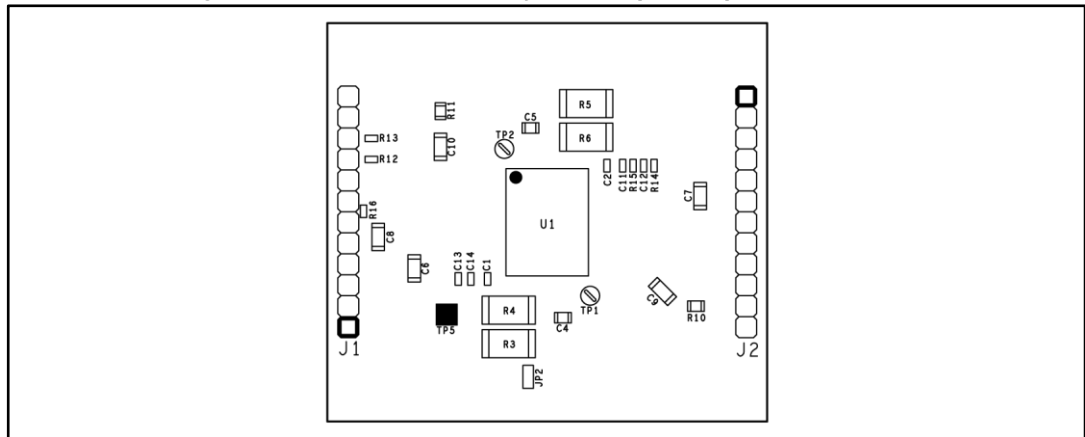


Figure 3: EVALPWD13F60 – layout (top layer 1)

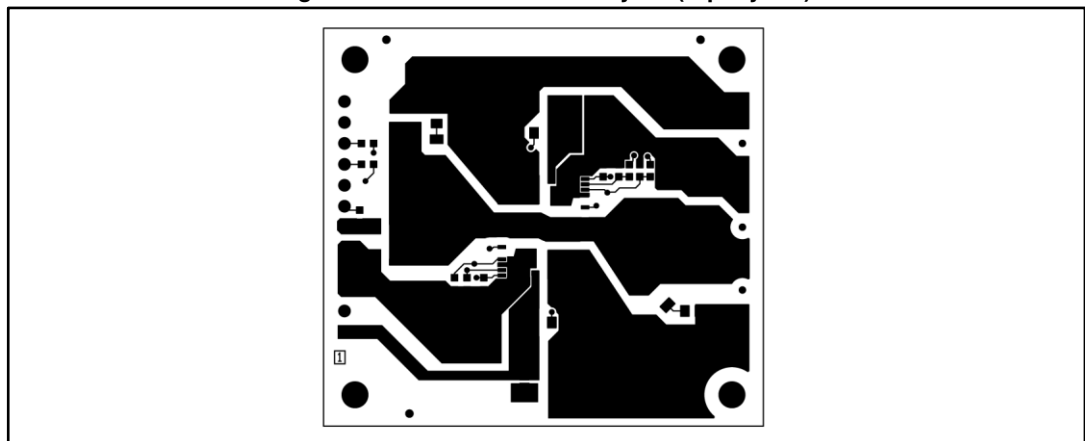


Figure 4: EVALPWD13F60 – layout (inner layer 2)

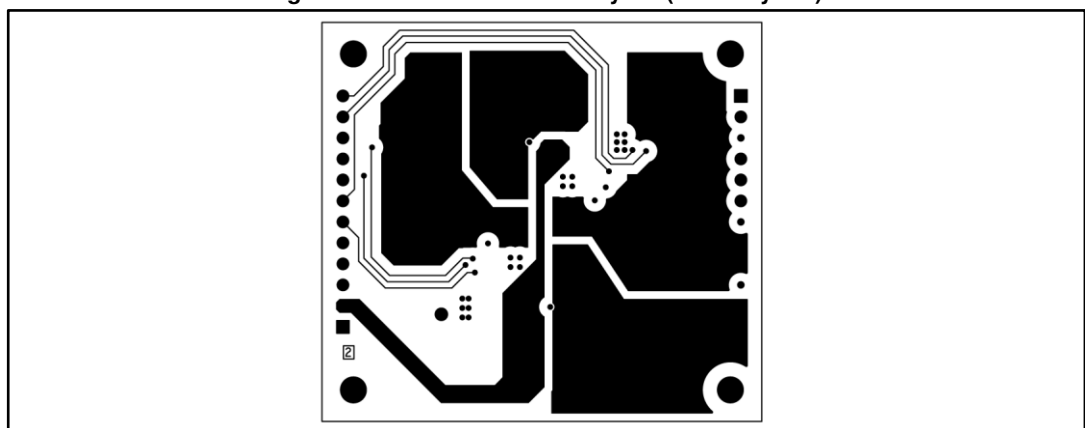


Figure 5: EVALPWD13F60 – layout (inner layer 3)

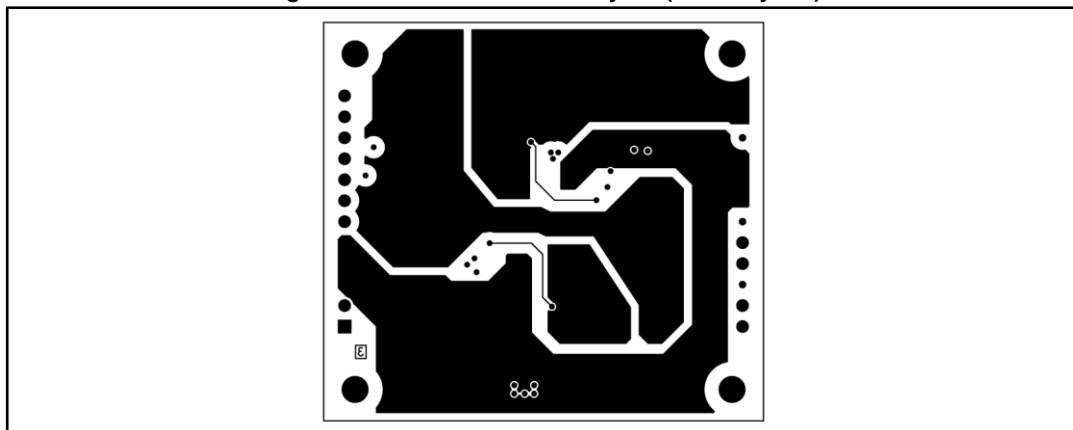
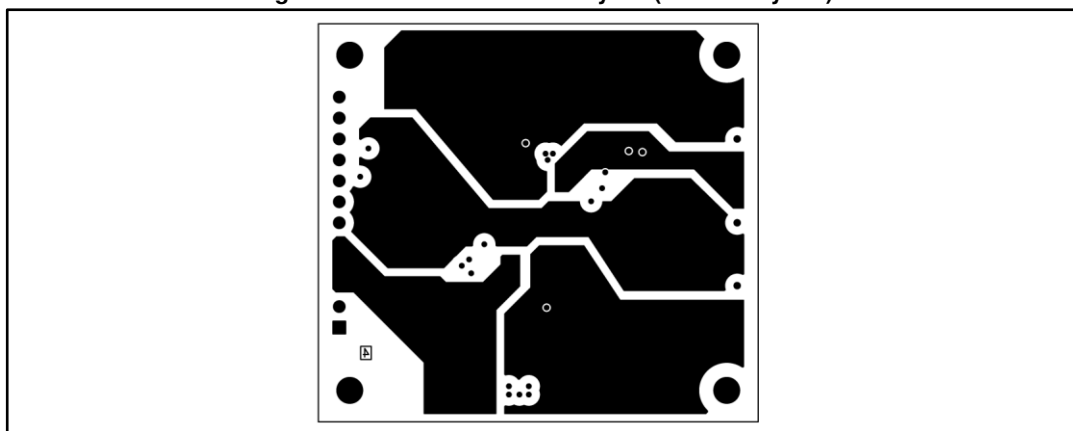


Figure 6: EVALPWD13F60 – layout (bottom layer 4)



4 Revision history

Table 2: Document revision history

Date	Version	Changes
23-Aug-2017	1	Initial release.
13-Nov-2017	2	Updated the title, features and description in cover page. Updated <i>Figure 1: "EVALPWD13F60 circuit schematic"</i> . Added <i>Table 1: "EVALPWD13F60 bill of materials"</i> .

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