Development Board EPC9005 Quick Start Guide

40 V Half-Bridge with Gate Drive, Using EPC2014

DESCRIPTION

The EPC9005 development board is a 40 V maximum device voltage, 7 A maximum output current, half bridge with onboard gate drives, featuring the EPC2014 enhancement mode (*eGaN*®) field effect transistor (FET). The purpose of this development board is to simplify the evaluation process of the EPC2014 eGaN FET by including all the critical components on a single board that can be easily connected into any existing converter.

The EPC9005 development board is 2" x 1.5" and contains two EPC2014 *eGaN* FET in a half bridge configuration using Texas Instruments LM5113 gate driver, supply and bypass capacitors. The board contains all critical components and layout for optimal switching performance. There are also various probe points to facilitate simple waveform measurement and efficiency calculation. A complete block diagram of the circuit is given in Figure 1.

For more information on the EPC2014s *eGaN* FET please refer to the datasheet available from EPC at www.epc-co.com. The datasheet should be read in conjunction with this quick start guide.

Table 1: Performance Summary (TA = 25°C)

SYMBOL	PARAMETER	CONDITIONS	MIN	MAX	UNITS
V_{DD}	Gate Drive Input Supply Range		7	12	V
V_{IN}	Bus Input Voltage Range			24*	V
V_{OUT}	Switch Node Output Voltage			40	V
I_{OUT}	Switch Node Output Current			7*	A
V_{PWM}	PWM Logic Input Voltage Threshold	Input 'High'	3.5	6	V
		Input 'Low'	0	1.5	V
	Minimum 'High' State Input Pulse Width	VPWM rise and fall time < 10ns	30		ns
	Minimum 'Low' State Input Pulse Width	VPWM rise and fall time < 10ns	100#		ns

* Assumes inductive load, maximum current depends on die temperature – actual maximum current with be subject to switching frequency, bus voltage and thermals.
\# Limited by time needed to 'refresh' high side bootstrap supply voltage.

Quick Start Procedure

Development board EPC9005 is easy to set up to evaluate the performance of the EPC2014 *eGaN* FET. Refer to Figure 2 for proper connect and measurement setup and follow the procedure below:

1. With power off, connect the input power supply bus to $+V_{IN}$ (J5, J6) and ground / return to $-V_{IN}$ (J7, J8).
2. With power off, connect the switch node of the half bridge OUT (J3, J4) to your circuit as required.
3. With power off, connect the gate drive input to $+V_{DD}$ (J1, Pin-1) and ground return to $-V_{DD}$ (J1, Pin-2).
4. With power off, connect the input PWM control signal to PWM (J2, Pin-1) and ground return to any of the remaining J2 pins.
5. Turn on the gate drive supply – make sure the supply is between 7 V and 12 V range.
6. Turn on the bus voltage to the required value (do not exceed the absolute maximum voltage of 40 V on V_{OUT}).
7. Turn on the controller / PWM input source and probe switching node to see switching operation.
8. Once operational, adjust the bus voltage and load PWM control within the operating range and observe the output switching behavior, efficiency and other parameters.
9. For shutdown, please follow steps in reverse.

NOTE. When measuring the high frequency content switch node (OUT), care must be taken to avoid long ground leads. Measure the switch node (OUT) by placing the oscilloscope probe tip through the large via on the switch node (designed for this purpose) and grounding the probe directly across the GND terminals provided. See Figure 3 for proper scope probe technique.

THERMAL CONSIDERATIONS

The EPC9005 development board showcases the EPC2014 *eGaN* FET. Although the electrical performance surpasses that for traditional silicon devices, their relatively smaller size does magnify the thermal management requirements. The EPC9005 is intended for bench evaluation with low ambient temperature and convection cooling. The addition of heat-sinking and forced air cooling can significantly increase the current rating of these devices, but care must be taken to not exceed the absolute maximum die temperature of 125°C.

NOTE. The EPC9005 development board does not have any current or thermal protection on board.

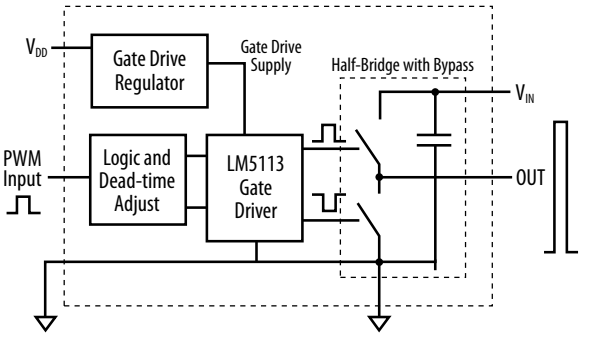


Figure 1: Block Diagram of EPC9005 Development Board

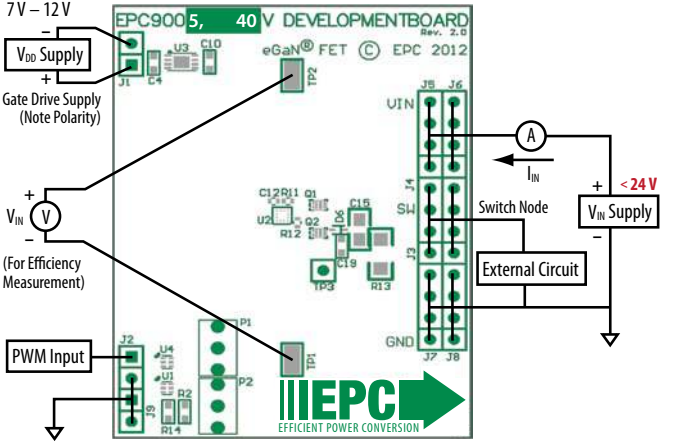


Figure 2: Proper Connection and Measurement Setup

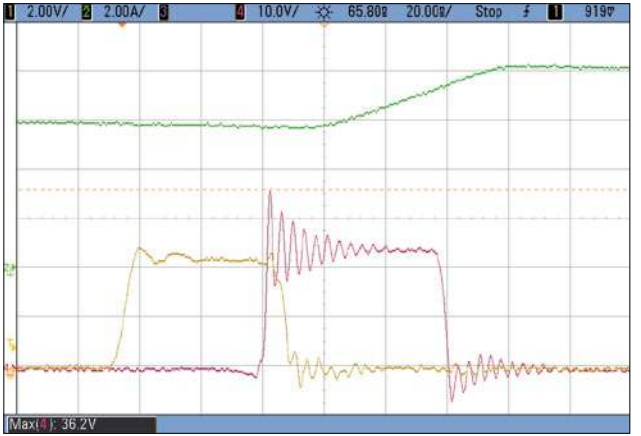


Figure 4: Typical Waveforms for V_{IN} = 24 V to 1.2 V/7 A (1000kHz) Buck converter
CH1: V_{PWM} Input voltage – CH2: (I_{OUT}) Switch node current – CH4: (V_{OUT}) Switch node voltage

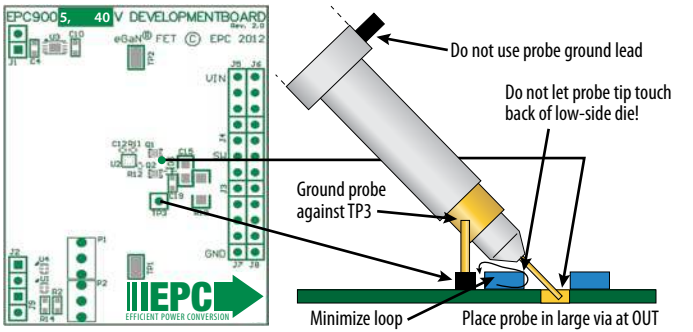
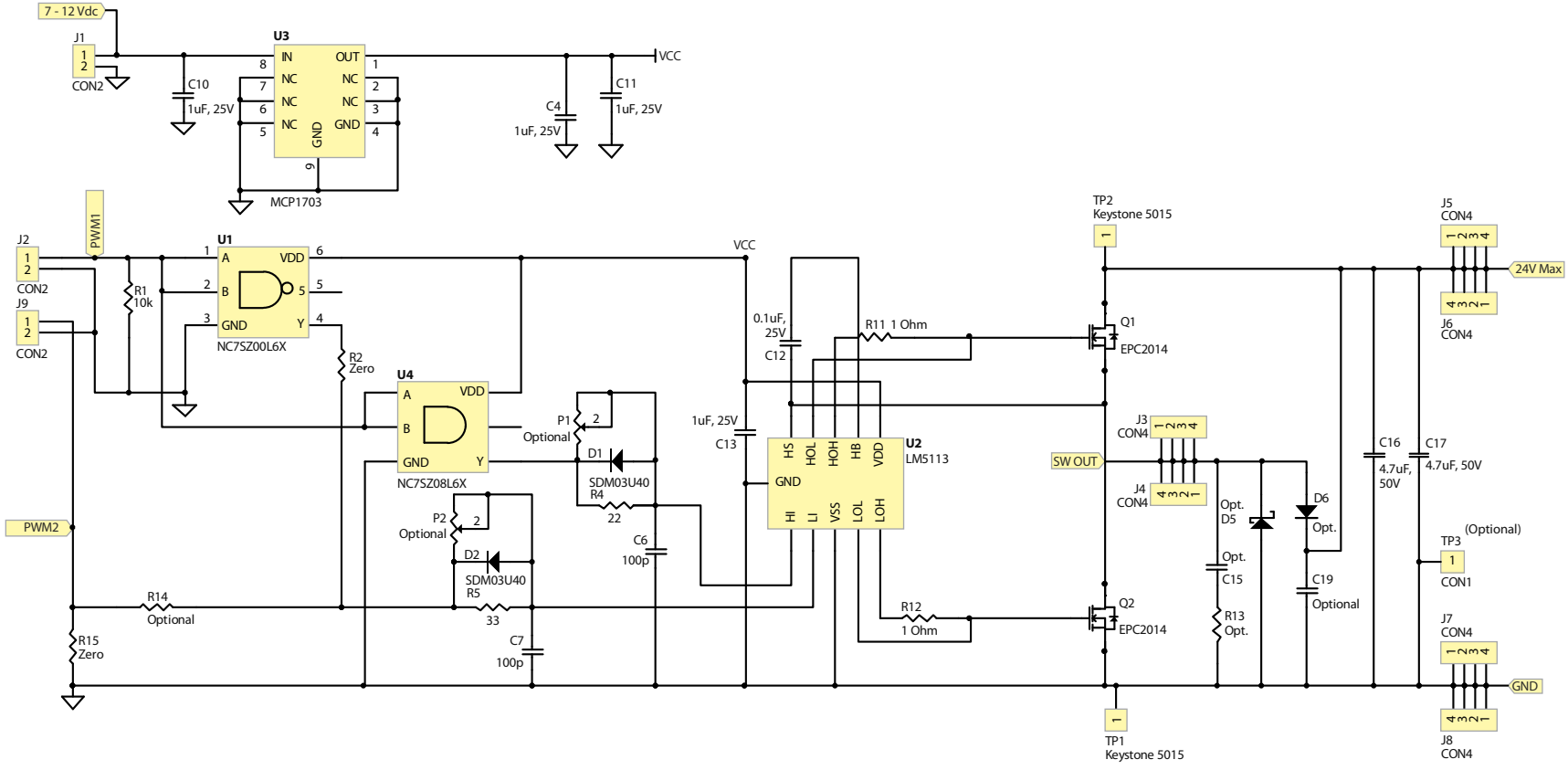


Figure 3: Proper Measurement of Switch Node – OUT

Table 2 : Bill of Material

Item	Qty	Reference	Part Description	Manufacturer / Part #
1	4	C4, C10, C11, C13	Capacitor, 1uF, 10%, 25V, X5R	Murata, GRM188R61E105KA12D
2	2	C6, C7	Capacitor, 100pF, 5%, 50V, NP0	TDK, C1608C0G1H101J
3	1	C12	Capacitor, 0.1uF, 10%, 25V, X5R	TDK, C1608X5R1E104K
4	2	C16, C17	Capacitor, 4.7uF, 20%, 50V, X5R	Taiyo Yuden, UMK325BJ475M
5	2	D1, D2	Schottky Diode, 30V	Diodes Inc., SDM03U40-7
6	3	J1, J2, J9,TP3 (See Note 1)	Connector	FCI, 68001-236HLF
7	1	J3, J4, J5, J6, J7, J8	Connector	FCI, 68602-224HLF
8	2	Q1, Q2	eGaN® FET	EPC, EPC2014
9	1	R1	Resistor, 10.0K, 5%, 1/8W	Stackpole, RMCF0603FT10K0
10	2	R2, R15	Resistor, 0 Ohm, 1/8W	Stackpole, RMCF0603ZT0R00
11	1	R4	Resistor, 22 Ohm, 1%, 1/8W	Stackpole, RMCF0603FT22R0
12	1	R5	Resistor, 33 Ohm, 1%, 1/8W	Stackpole, RMCF0603FT33R0
13	2	R11, R12	Resistor, 0 Ohm, 1/8W	Stackpole, RMCF0603ZT0R00
14	2	TP1, TP2	Test Point	Keystone Elect, 5015
16	1	U1	I.C., Logic	Fairchild, NC7SZ00L6X
17	1	U2	I.C., Gate driver	Texas Instruments, LM5113
18	1	U3	I.C., Regulator	Microchip, MCP1703T-5002E/MC
19	1	U4	I.C., Logic	Fairchild, NC7SZ08L6X
20	0	R13, R14	Optional Resistor Optional	
21	0	C15, C19	Capacitor Optional Diode	
22	0	D5, D6	Optional Potentiometer	
23	0	P1, P2		

Note 1: 36 pin Header to be cut as follows: J1: cut 2 pins used, J2 & J9: cut 4 pins used, TP3: cut 1 pin used



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Rev 2.0

Contact us:

www.epc-co.com

Renee Yawger
WW Marketing
Office: +1.908.475.5702
Mobile: +1.908.619.9678
renee.yawger@epc-co.com

Bhasy Nair
Global FAE Support
Office: +1.972.805.8585
Mobile: +1.469.879.2424
bhasy.nair@epc-co.com

Stephen Tsang
Sales, Asia
Mobile: +852.9408.8351
stephen.tsang@epc-co.com

Peter Cheng
FAE Support, Asia
Mobile: +886.938.009.706
peter.cheng@epc-co.com

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