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Old Company Name in Catalogs and Other Documents

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Renesas Electronics website: <http://www.renesas.com>

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (<http://www.renesas.com>)

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SWITCHING
N-CHANNEL POWER MOS FET

DESCRIPTION

The μ PA2752GR is Dual N-Channel MOS Field Effect Transistor designed for DC/DC converters and power management applications of notebook computers.

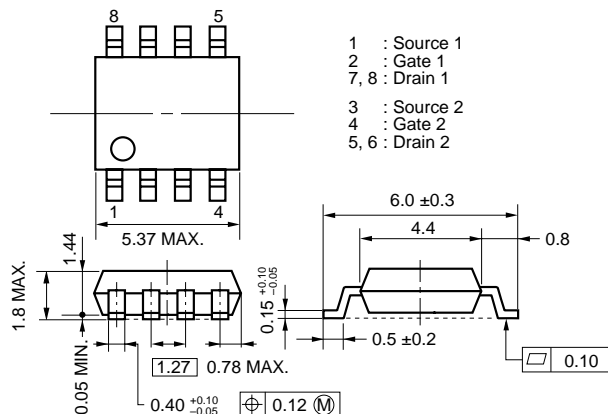
FEATURES

- Dual chip type
- Low on-state resistance
 $R_{DS(on)1} = 23.0 \text{ m}\Omega \text{ MAX. (} V_{GS} = 10 \text{ V, } I_D = 4.0 \text{ A)}$
 $R_{DS(on)2} = 35.0 \text{ m}\Omega \text{ MAX. (} V_{GS} = 4.5 \text{ V, } I_D = 4.0 \text{ A)}$
 $R_{DS(on)3} = 41.0 \text{ m}\Omega \text{ MAX. (} V_{GS} = 4.0 \text{ V, } I_D = 4.0 \text{ A)}$
- Low C_{iss} : $C_{iss} = 480 \text{ pF TYP.}$
- Built-in G-S protection diode
- Small and surface mount package (Power SOP8)

ORDERING INFORMATION

PART NUMBER	PACKAGE
μ PA2752GR	Power SOP8

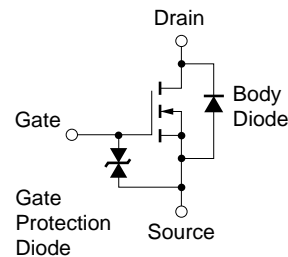
PACKAGE DRAWING (Unit: mm)



ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$, All terminals are connected.)

Drain to Source Voltage ($V_{GS} = 0 \text{ V}$)	V_{DSS}	30	V
Gate to Source Voltage ($V_{DS} = 0 \text{ V}$)	V_{GSS}	± 20	V
Drain Current (DC) ($T_C = 25^\circ\text{C}$)	$I_{D(DC)}$	± 8.0	A
Drain Current (pulse) ^{Note1}	$I_{D(pulse)}$	± 32	A
Total Power Dissipation (1 unit) ^{Note2}	P_T	1.7	W
Total Power Dissipation (2 unit) ^{Note2}	P_T	2.0	W
Channel Temperature	T_{ch}	150	$^\circ\text{C}$
Storage Temperature	T_{stg}	-55 to +150	$^\circ\text{C}$
Single Avalanche Current ^{Note3}	I_{AS}	8	A
Single Avalanche Energy ^{Note3}	E_{AS}	6.4	mJ

EQUIVALENT CIRCUIT
(1/2 Circuit)



- Notes
1. $PW \leq 10 \mu\text{s}$, Duty cycle $\leq 1\%$
 2. $T_A = 25^\circ\text{C}$, Mounted on ceramic substrate of $2000 \text{ mm}^2 \times 2.2 \text{ mm}$
 3. Starting $T_{ch} = 25^\circ\text{C}$, $V_{DD} = 15 \text{ V}$, $R_G = 25 \Omega$, $V_{GS} = 20 \rightarrow 0 \text{ V}$

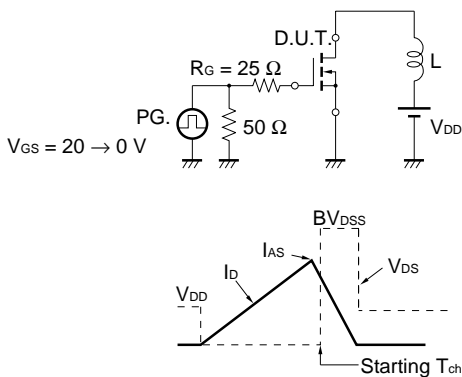
Remark The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

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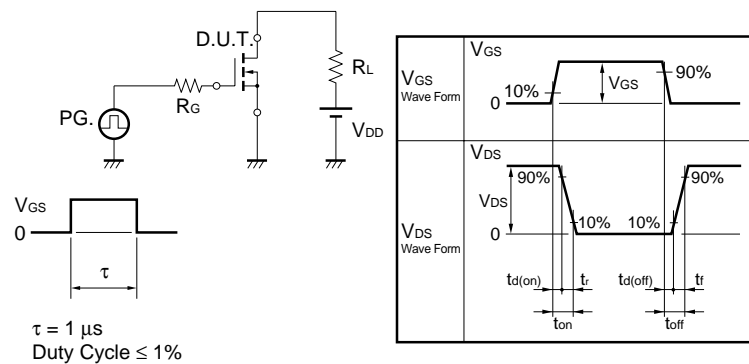
ELECTRICAL CHARACTERISTICS (T_A = 25°C, All terminals are connected.)

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 30 V, V _{GS} = 0 V			10	μA
Gate Leakage Current	I _{GSS}	V _{GS} = ±18 V, V _{DS} = 0 V			±10	μA
Gate Cut-off Voltage	V _{GS(off)}	V _{DS} = 10 V, I _D = 1 mA	1.5	2.0	2.5	V
Forward Transfer Admittance	y _{fs}	V _{DS} = 10 V, I _D = 4.0 A	3.5	7.0		S
Drain to Source On-state Resistance	R _{DS(on)1}	V _{GS} = 10 V, I _D = 4.0 A		18.0	23.0	mΩ
	R _{DS(on)2}	V _{GS} = 4.5 V, I _D = 4.0 A		25.0	35.0	mΩ
	R _{DS(on)3}	V _{GS} = 4.0 V, I _D = 4.0 A		28.5	41.0	mΩ
Input Capacitance	C _{iss}	V _{DS} = 10 V		480		pF
Output Capacitance	C _{oss}	V _{GS} = 0 V		190		pF
Reverse Transfer Capacitance	C _{rss}	f = 1 MHz		70		pF
Turn-on Delay Time	t _{d(on)}	V _{DD} = 15 V, I _D = 4.0 A		9.9		ns
Rise Time	t _r	V _{GS} = 10 V		6.2		ns
Turn-off Delay Time	t _{d(off)}	R _G = 10 Ω		25		ns
Fall Time	t _f			5.8		ns
Total Gate Charge	Q _G	V _{DD} = 24 V		10		nC
Gate to Source Charge	Q _{GS}	V _{GS} = 10 V		1.9		nC
Gate to Drain Charge	Q _{GD}	I _D = 8.0 A		2.6		nC
Body Diode Forward Voltage	V _{F(S-D)}	I _F = 8.0 A, V _{GS} = 0 V		0.81		V
Reverse Recovery Time	t _{rr}	I _F = 8.0 A, V _{GS} = 0 V		28		ns
Reverse Recovery Charge	Q _{rr}	di/dt = 100 A/μs		23		nC

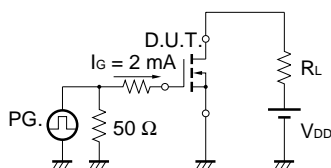
TEST CIRCUIT 1 AVALANCHE CAPABILITY



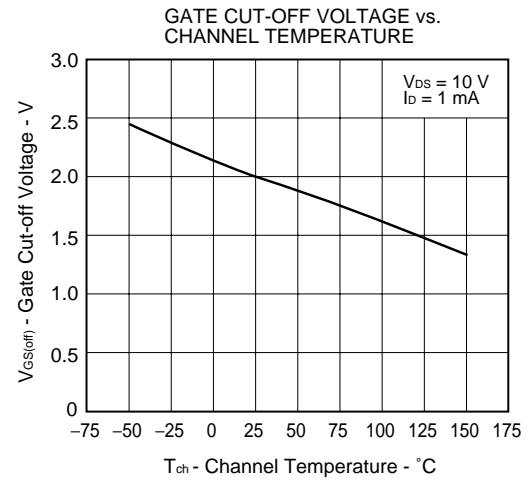
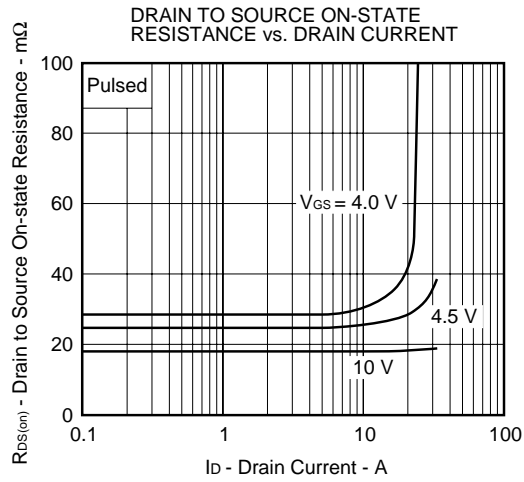
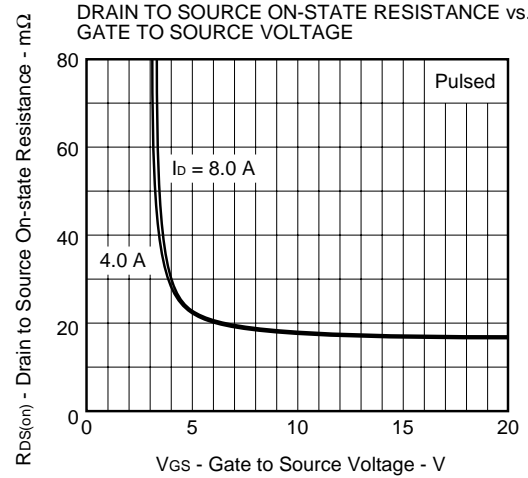
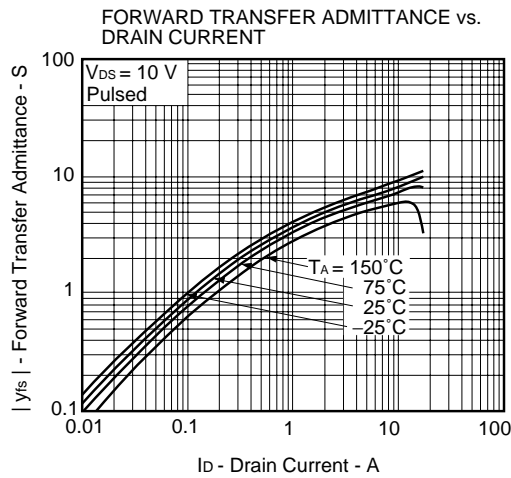
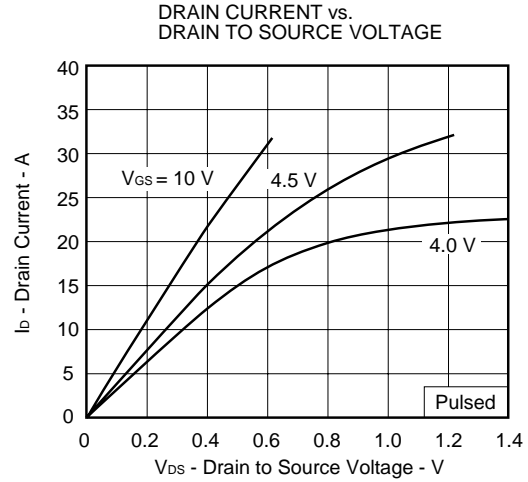
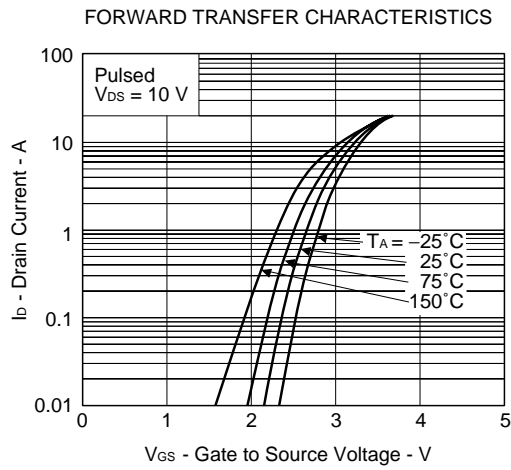
TEST CIRCUIT 2 SWITCHING TIME

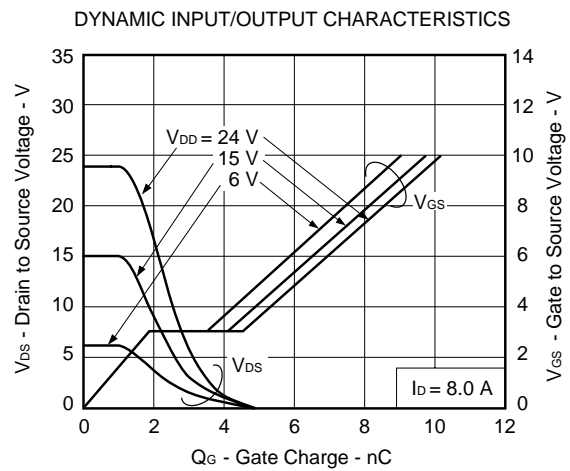
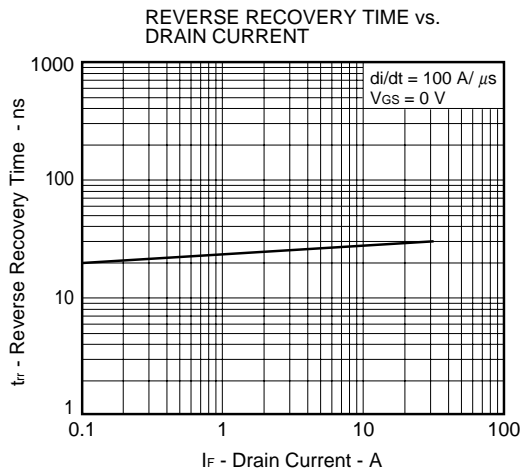
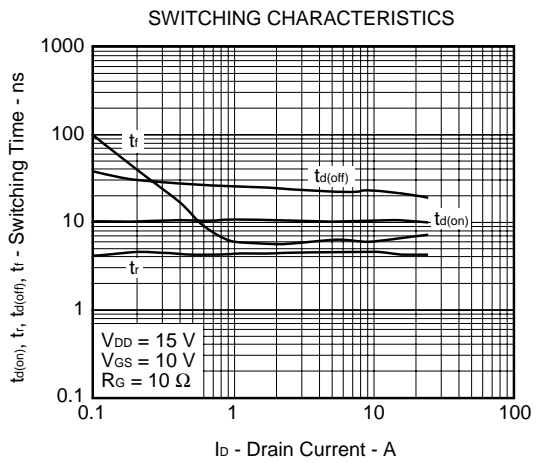
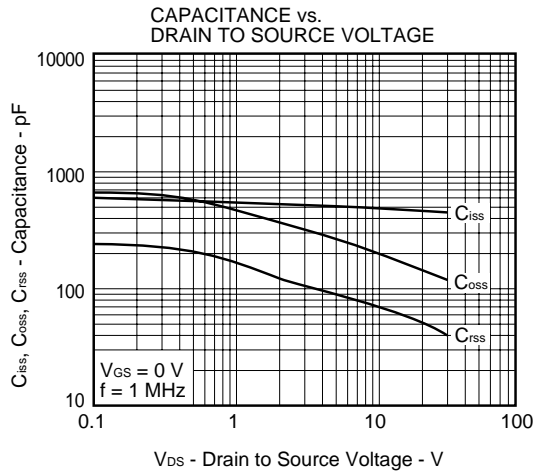
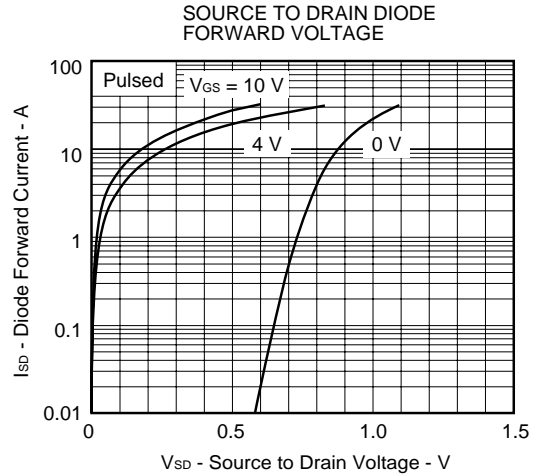
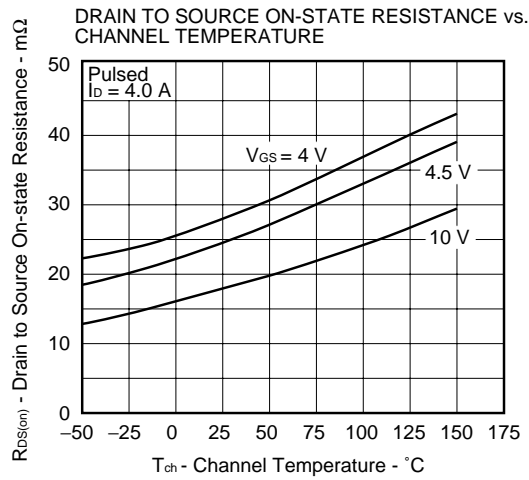


TEST CIRCUIT 3 GATE CHARGE

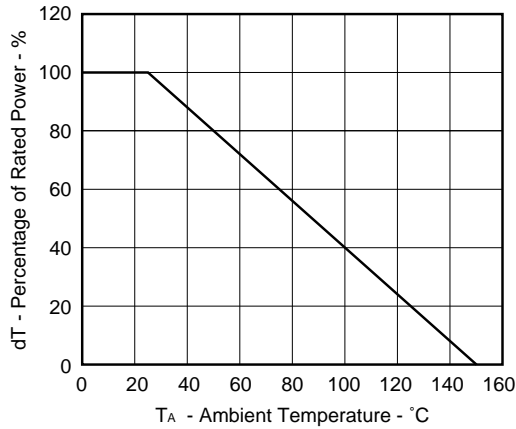


TYPICAL CHARACTERISTICS (TA = 25°C)

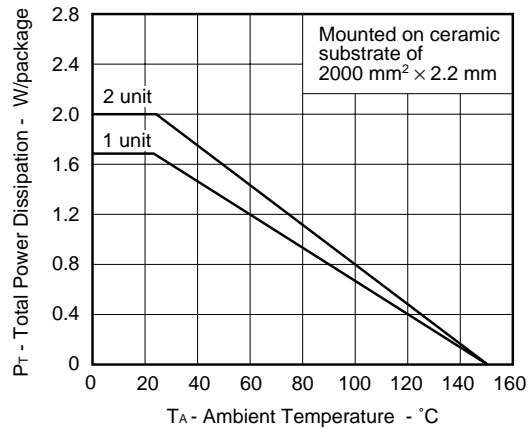




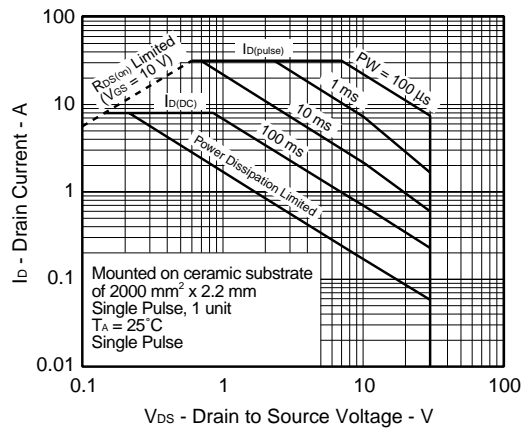
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



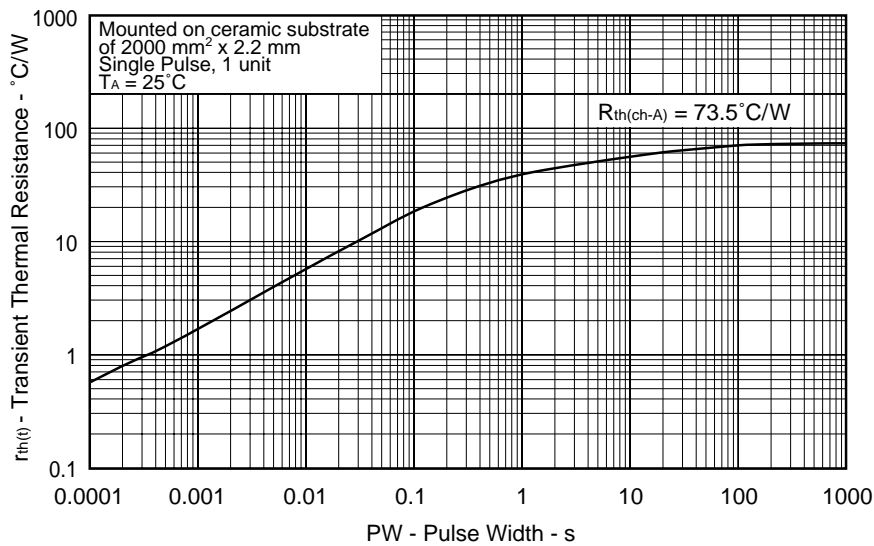
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE

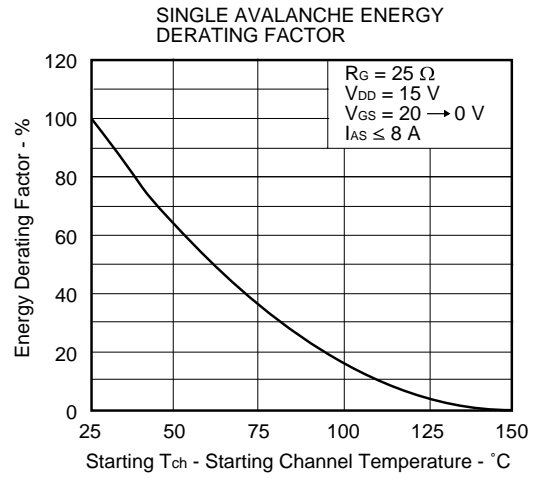
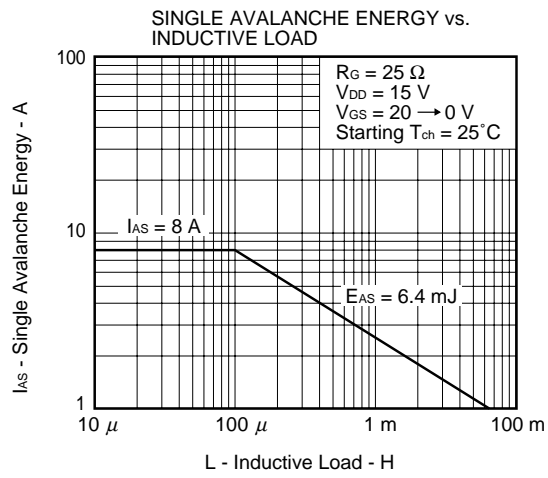


FORWARD BIAS SAFE OPERATING AREA



TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH





[MEMO]

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