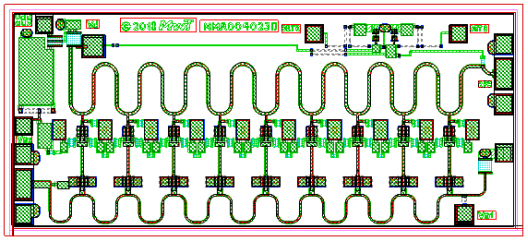
MicroWave Technology
An IXYS Company

MMA-004023D

30KHz-50GHz Traveling Wave Amplifier With Output Power Detector Preliminary Data Sheet

Features:

- **Frequency Range: 30KHz – 50 GHz**
- **P1dB: +23 dBm**
- **Vout: 7V p-p @50Ω**
- **Gain: 15.5 dB**
- **Vdd =7 V**
- **Ids = 240 mA**
- **Input and Output Fully Matched to 50 Ω**
- **On-Chip Output Power Voltage Detector**



Die Size 2.35mm x 1.05mm x 0.05 mm

Applications:

- **Fiber optics communication systems**
- **Microwave and wireless communication systems**
- **Microwave and optical instrumentations**
- **Military and EW equipments**

Description:

The MMA-004023D is a broadband GaAs MMIC Traveling Wave Amplifier (TWA) with medium output power and high gain over full 30KHz to 50GHz frequency range. This amplifier is optimally designed for broadband applications requiring flat gain and group delay with excellent input and output matches over a 30KHz to 50GHz frequency range.

Absolute Maximum Ratings: *(Ta= 25 ºC)**

SYMBOL	PARAMETERS	UNITS	Min.	Max.
Vds	Drain-Source Voltage	V		10
Vg1	First Gate-Source Voltage	V	-8	0
Ig1	First Gate Current	mA	-38	1
Vg2	Second Gate-Source Voltage	V	-3.5	4
Ig2	Second Gate-Source Current	mA	-20	
Ids	Drain Current	mA		340
Pin max	RF Input Power	dBm		17
Tch	Channel Temperature	ºC		+150
Tstg	Storage Temperature	ºC		-55 to +165
Tmax	Max. Assembly Temp (60 sec max)	ºC		+300

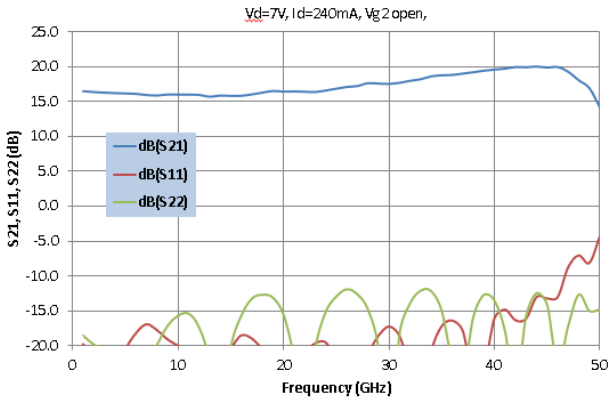
*Operation of this device above any one of these parameters may cause permanent damage.

Electrical Specifications: *Vds=7V, Vg1=-2.7V, Vg2=open, Ids=240mA, Ta=25°C Z0=50 ohm*

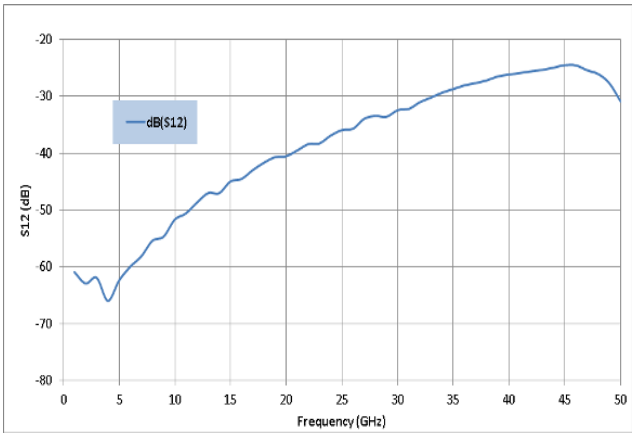
Parameter	Units	Min.	Typ.	Max.
Frequency Range	MHz	0.03		50,000
Gain (Typ/Min)	dB	13.5	15.5	
Gain Flatness (Typ/Max)	+/- dB		1	1.2
Input RL (Typ/Max)	dB	12	15	
Output RL (Typ/Max)	dB	12	15	
Output P1dB (Typ/Min) 20GHz 30GHz 40GHz	 dBm dBm dBm	 21 19.5 17.2	 22 20.5 18.5	
Output IP3 (1)	dBm		30	
Output Psat (Typ)	dBm		25.5	
Vdet (VdeR – VdeO) @Po = +20dBm 1GHz 10GHz 20GHz 40GHz	 V V V V		 0.53 0.53 0.54 0.55	
Noise Figure 20GHz 40GHz 50GHz	 dB dB dB		 2.8 5.5 9.0	 3.5 6.2
Operating Current at P1dB (Typ/Max)	mA		240	
Thermal Resistance	°C/W		16	
Operating Temperature Range		-40°C	+25°C	+85°C

(1) Output IP3 is measured with two tones at output power of 10 dBm/tone separated by 20 MHz.

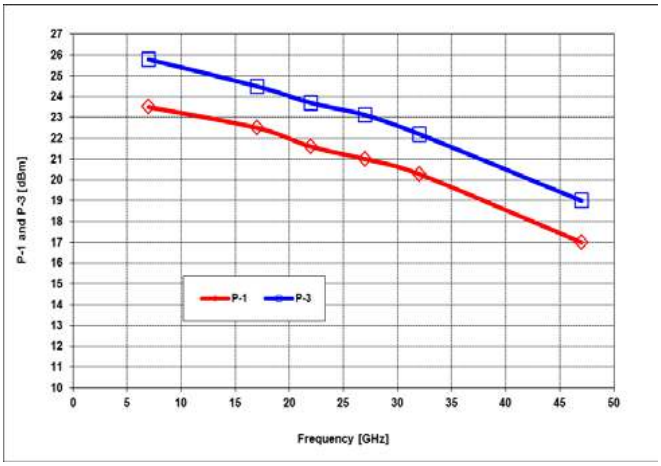
Typical RF Performance: *Vds=7V, Vg1=-2.7V, Vg2=open, Ids=240mA, Z0=50 ohm, Ta=25 ºC*



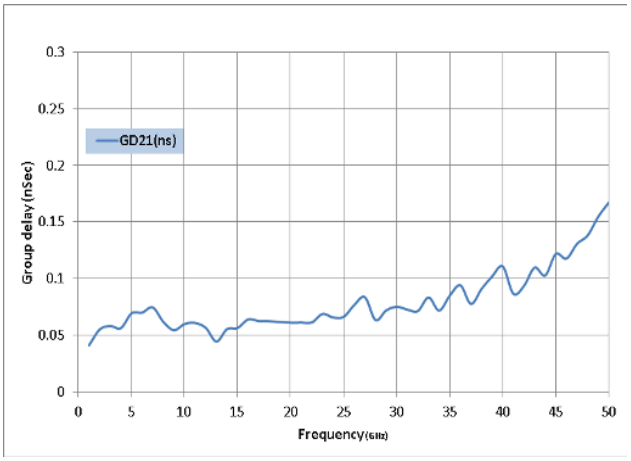
Typical Room Temperature RF Performance



S12(dB) vs. Frequency

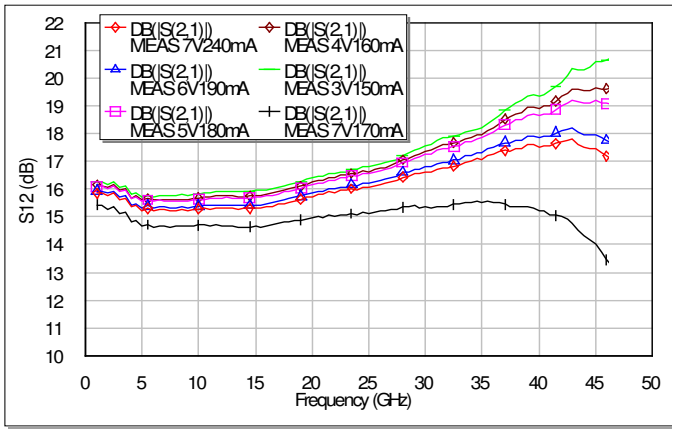


P-1 and P-3 vs. Frequency

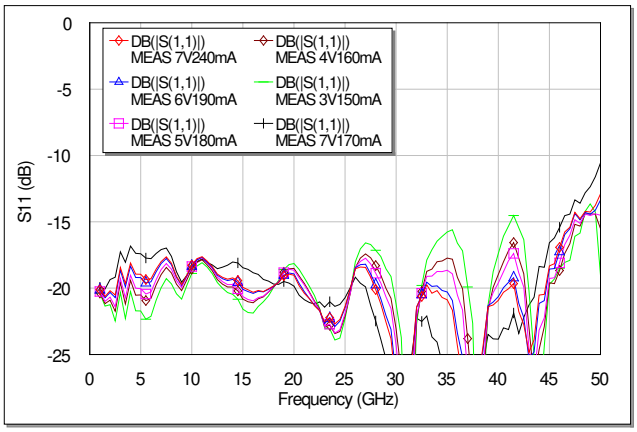


Group Delay vs. Frequency

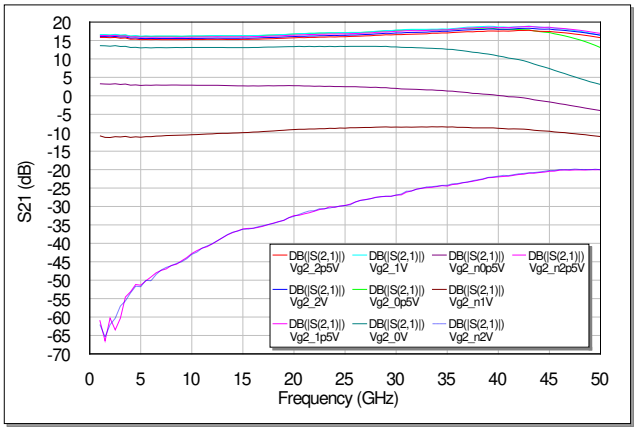
Typical RF Performance: *(Over voltage)*



S21 (dB) over biasing

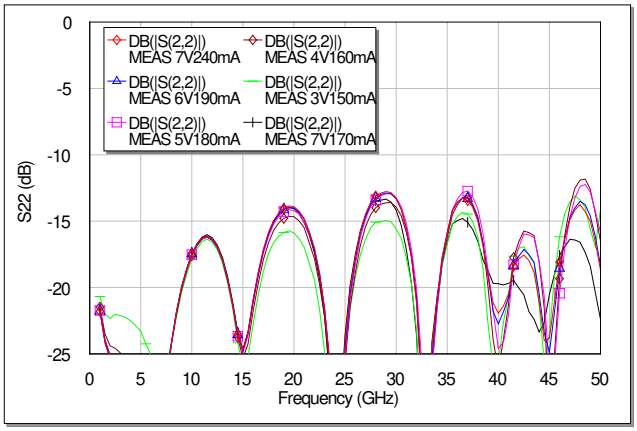


S11 (dB) over biasing

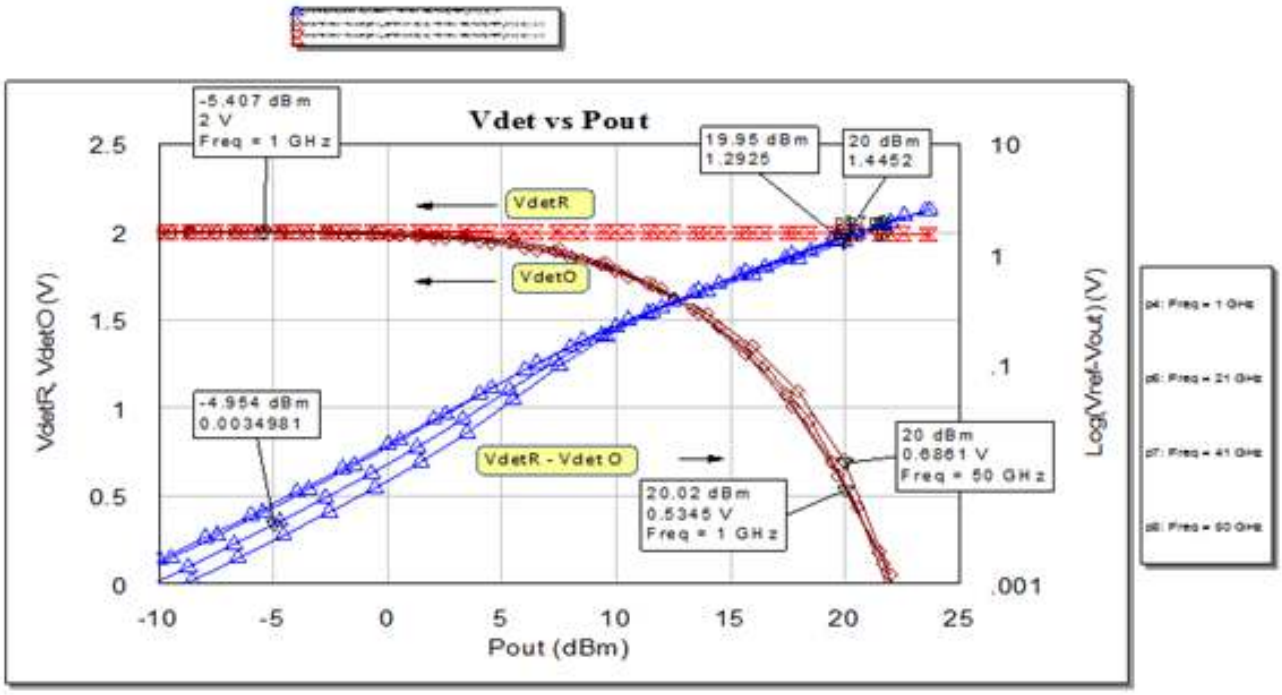


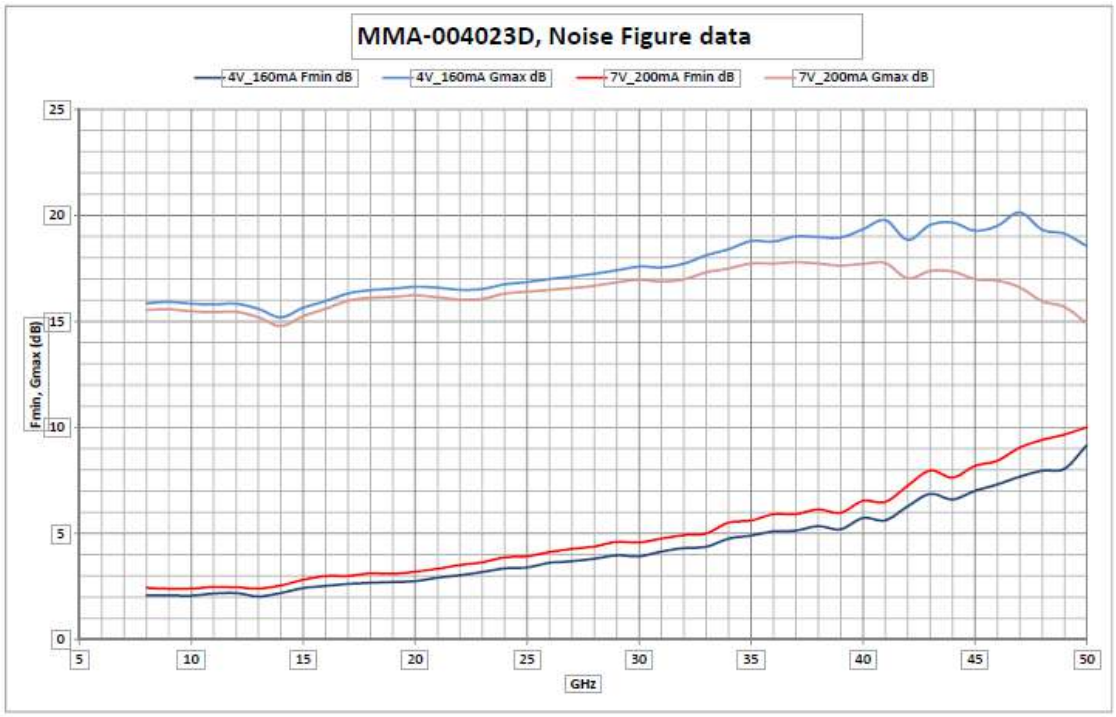
Gain control over Vg2 (-2.5V to +2.5V, 0.5V step)

Vds=7V, Ids=240mA @Vg2=open

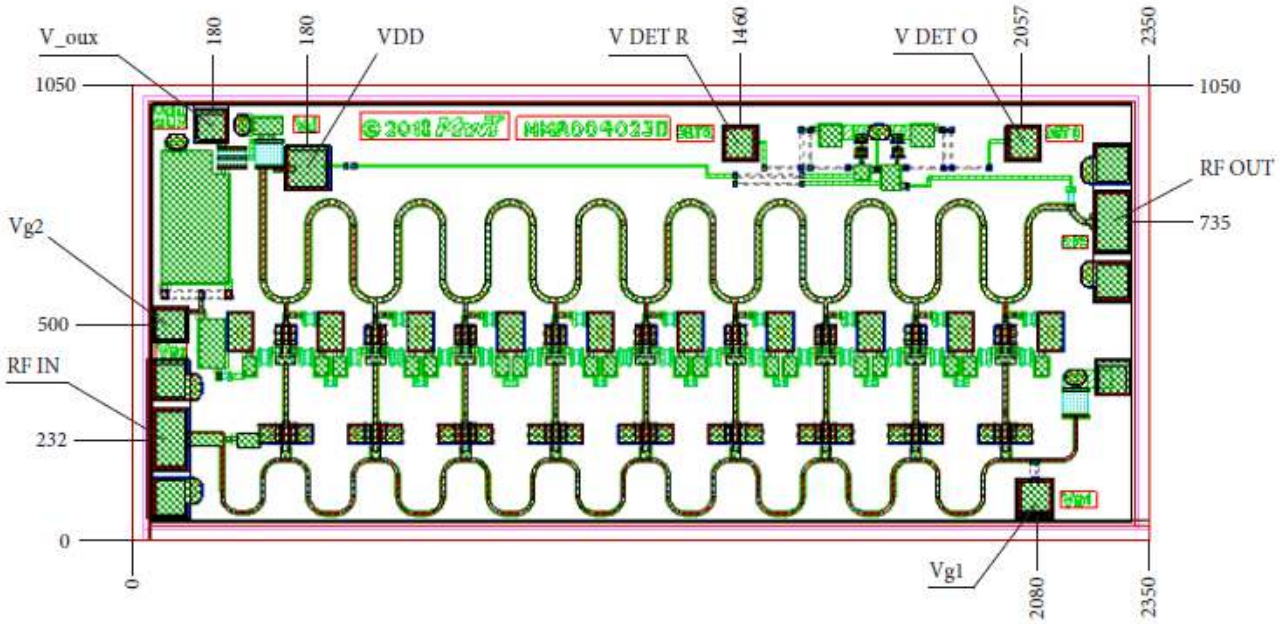


S22 (dB) over biasing





Mechanical Information: *Top view*



Applications

The **MMA-004023D** traveling wave amplifier is designed for use as a general purpose wideband power stage in microwave and optical communication systems, and test fiber optic/microwave test equipments. It is ideally suited for broadband applications requiring a flat gain response and excellent port matches over a 2 to 50 GHz frequency range. Dynamic gain control and low-frequency extension capabilities are designed into these devices.

Biasing and Operation

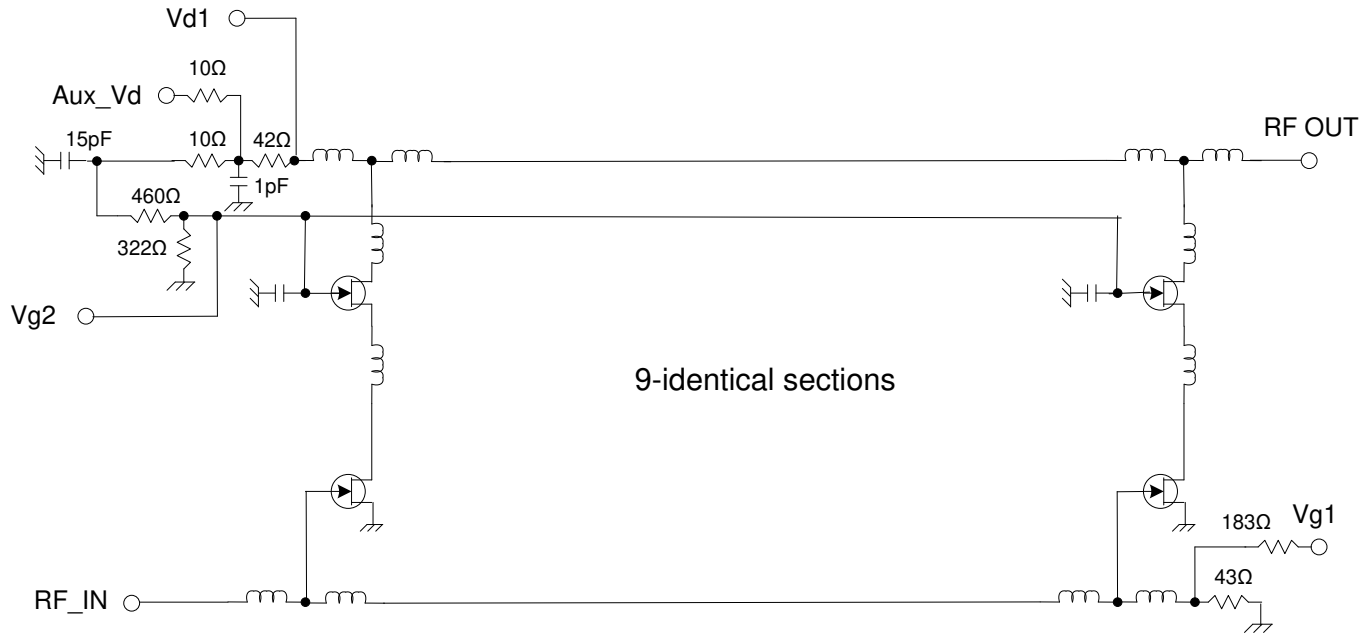
The recommended bias conditions for best performance for the **MMA-004023D** are V_{DD} = 7.0V, I_{DD} = 240mA. To achieve these drain current levels, V_{g1} is typically biased -2.7V with approximately 10mA. No other bias supplies or connections to the device are required for 2 to 50 GHz operation. The gate voltage (V_{g1}) should be applied prior to the drain voltage (V_{d1}) during power up and removed after the drain voltage during power down. The **MMA-004023D** is a DC coupled amplifier. External coupling capacitors are needed on RF_{IN} and RF_{OUT} ports. The drain bias pad is connected to RF and must be decoupled to the lowest operating frequency. An auxiliary drain contacts is provided when performance below 1 GHz in required. Connect external capacitors to ground to maintain input and output VSWR at low frequencies (see additional application note). Do not apply bias to these pads. The second gate (V_{g2}) can be used to obtain 30 dB (typical) dynamic gain control. For normal operation, no external bias is required on this contact.

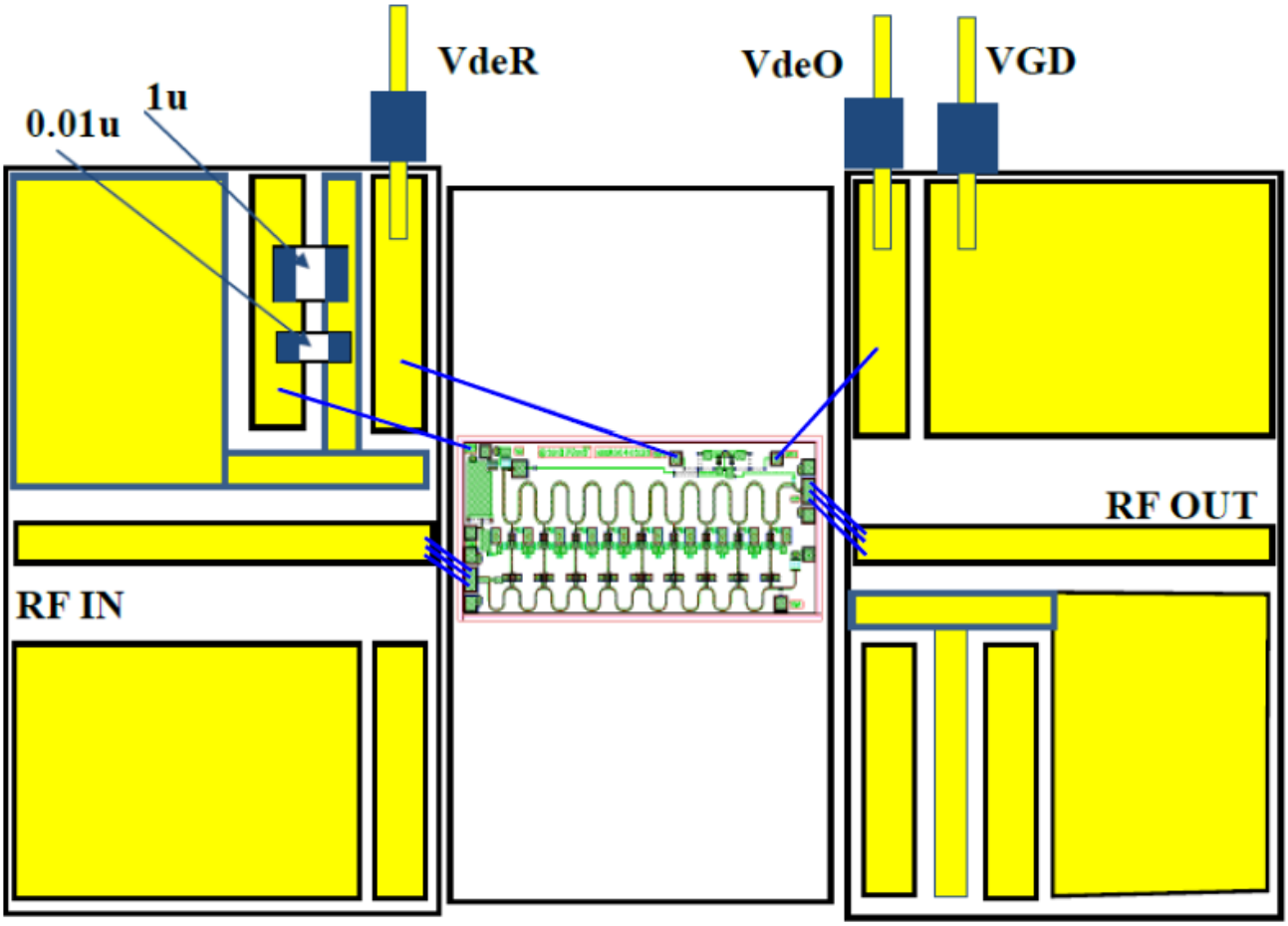
Assembly Techniques

GaAs MMICs are ESD sensitive. ESD preventive measures must be employed in all aspects of storage, handling, and assembly. MMIC ESD precautions, handling considerations, die attach and bonding methods are critical factors in successful GaAs MMIC performance and reliability. MMA-004023D can be attached using AuSn(Gold/Tin) preform or conductive epoxy.

Additional References:

MMA-004023D Application note v.1.0





Assembly Diagram for 0.1- 50GHz Applications
Using External Bias-Tees at Input and Output
with VDD = +7V, 240mA, Vg = -0.5V, 10mA

Broad-band application

This section is an operational guide for broad-band applications for MwT's MMA-004023D Traveling Wave Amplifier (TWA). For operation below 2 GHz, additional passive components are required to extend the low frequency end of the band down to 30 kHz. With low frequency bias components, the MMA-004023D may be used in a variety of time-domain applications through 40 GB/s.

Device Operation

The MMA-004023D is biased with a single positive drain supply (Vdd) and a negative gate supply (Vg1). For best overall performance, the recommended bias is Vdd = 7 V and Idd = 240 mA. To achieve this drain current level, Vg1 is typically -2.7 V. Typical DC current flow for Vg1 is -10 mA. The MMA-004023D has a second gate bias (Vg2) that may be used for gain control. When not being utilized, Vg2 should be left open circuited. The cascode bias structure of the TWA results in an RF "hot" drain bias that must be isolated from the drain DC supply. This topology creates the need for a decoupling bias network on the drain bias line. Decoupling is the isolation of RF and DC circuits on a common line. The decoupling network is usually a low-pass filter, as shown in Figure 1.

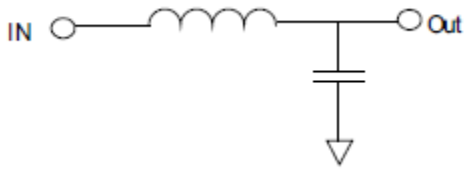


Figure 1. Decoupling Network

The decoupling bias circuit will pass DC to the drain line of the TWA and prevent the RF signal, present on the drain line, from appearing on the DC bias line. This bias network configuration is also referred to as an RF choke. The corner frequency (low frequency roll-off) of the drain bias RF choke is determined by the parallel combination of the drain inductance and the on-chip 50 Ω resistor shown below in Figure 2.

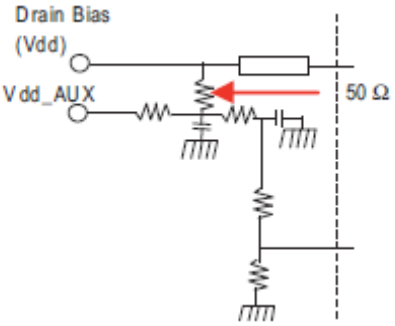


Figure 2. On-chip 50 Ω resistor

The lower frequency limit (f_{LD}) due to this inductance can be calculated using the following equation.

$$f_{LD} = \frac{Ro}{(2\pi L_D)} \text{ (Hz)}$$

Where, R_O is the RF input/output 50 Ω terminating resistance, and L_D is the inductance associated with the off-chip drain bias circuit shown in Figure 1. For 2-40GHz operation, the minimum drain inductance is 4.5 nH. A 0.007 in. diameter gold wire with a length of approximately 0.200" will achieve this value. Spiral chip inductors are also available with typical dimensions of

0.030 x 0.030 x 0.007 in. It is important to note that capacitive parasitics, in the drain bias network will result in resonances in the frequency response of the TWA. Therefore, it is strongly recommended to reduce parasitic capacitance as much as possible. To minimize resonances, an inductor with a high self-resonate frequency is recommended. If a spiral chip inductor is used, a 50 to 200 Ω, parallel de-queuing resistor will also be necessary. A thin film alumina resistor is recommended for minimal associated parasitics. The schematic in Figure 3 illustrates the external bias recommended for basic operation. Input and output RF ports are DC coupled and will require DC blocking capacitors, C1 and C2, if DC is present on these paths. Selection of DC blocks will be dependent on operating frequency bandwidth. See Table 1 for recommended passive components.

The schematic in Figure 4 illustrates external bias for utilizing the Vg2 gain control.

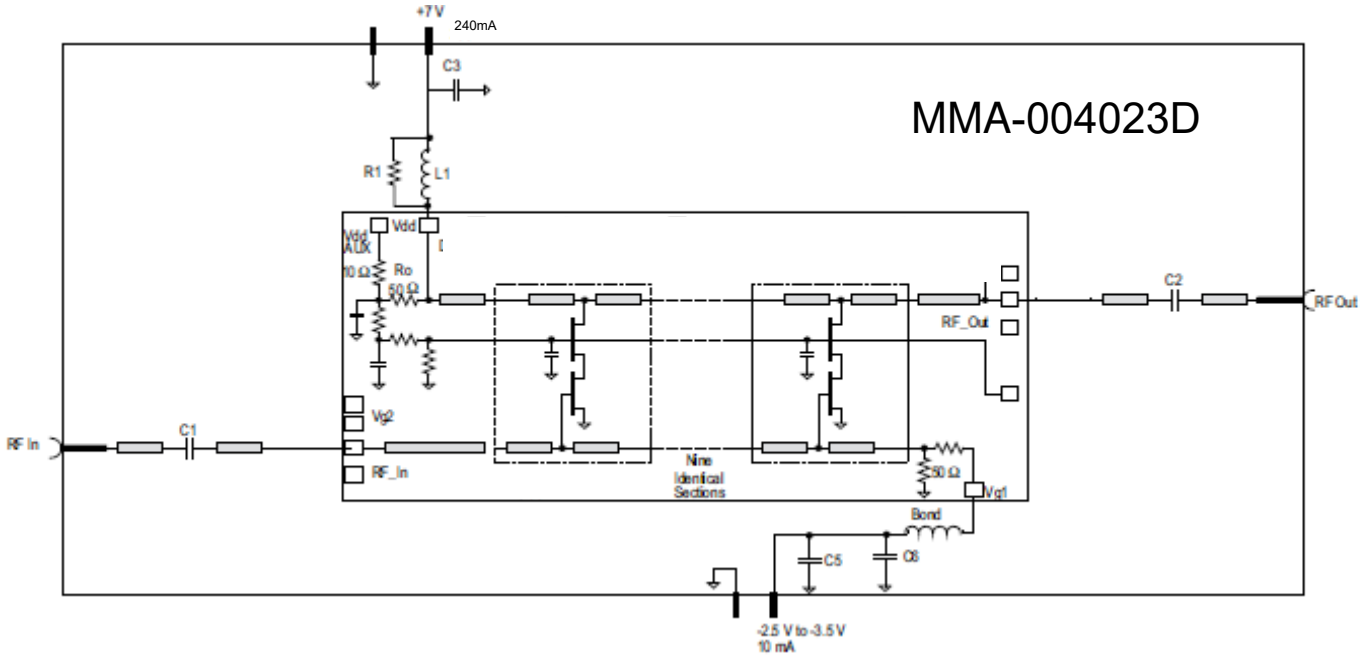


Figure 3. Basic 2 GHz to 50 GHz Schematic

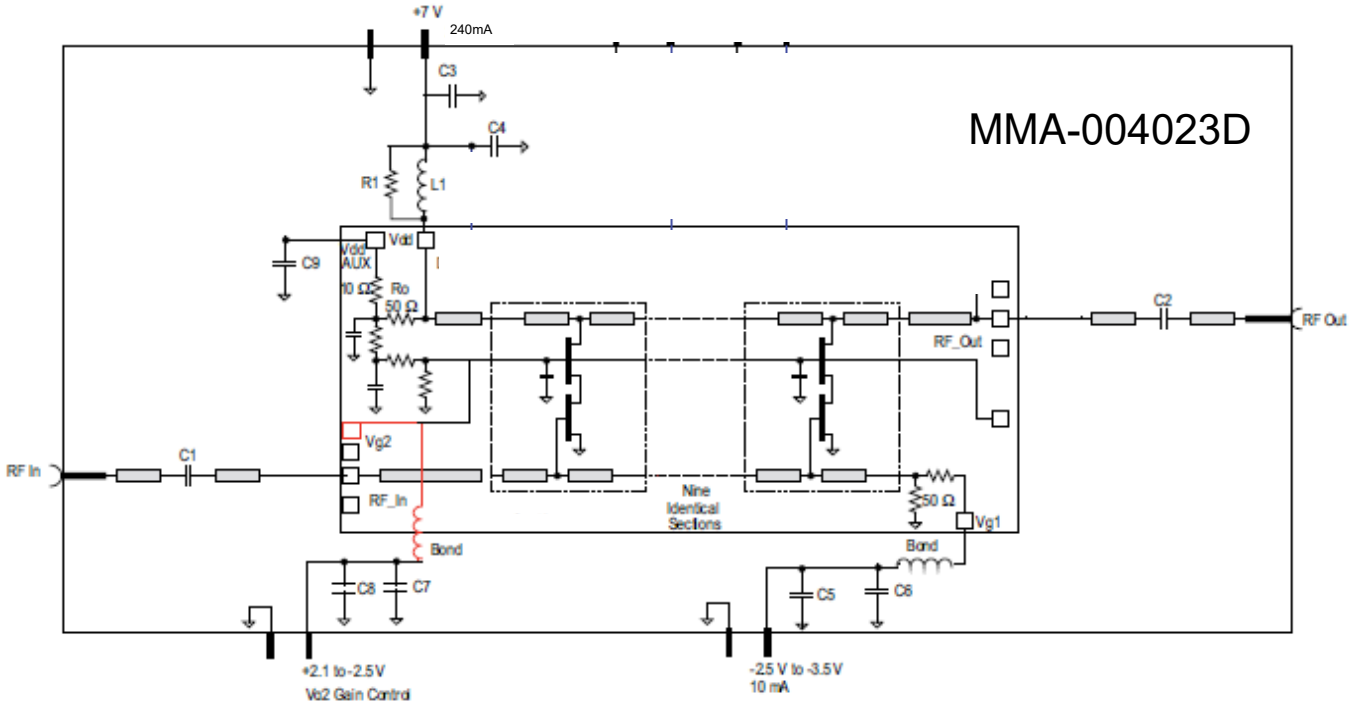


Figure 4. Low Frequency Bypass with a Gain control (Vg2)

Low Frequency Extension

As the area required for capacitive bypass lower than 2 GHz would be quite large, the MMA-004023 provides the Vdd Auxilary (support) bypass pad, shown in Figure 5, to add the additional large capacitance as required.

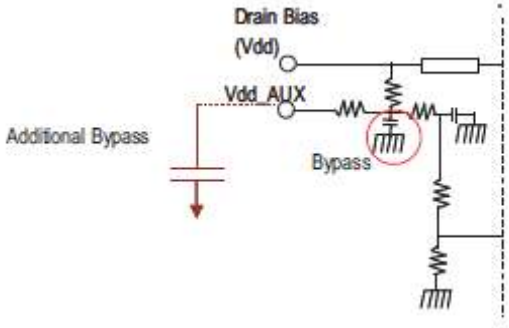


Figure 5. Vdd Auxiliary (support) Bypass Pad

The MMA-004023D can operate down to frequencies as low as a few hundred kilohertz by:
1) Adding external capacitors to the auxiliary drain pad.
2) Increasing the capacitance of the DC blocking capacitors at the RF input and output.
3) Increasing the inductance of the drain inductor (L1, Figure 6) to provide high impedance bias feed at the lower frequencies.

All three factors are equally important since any one of these can limit the low frequency performance. Input and output return loss degrades as the drain and gate line loads deviate from 50 Ω. The load can be restored close to 50 Ω and RF performance improved by adding large external capacitors in parallel with the on-chip capacitors, as shown in Figure 6. When the additional bypass capacitors are connected, the low frequency limit is extended down to the corner frequency determined by the bypass capacitors, the combination of the on-chip 50Ω load, and the small de-queing resistor. At this low-end band edge, the small signal gain will increase in magnitude and stay at this elevated level down to the point where the CAUX bypass capacitor acts as an open circuit, effectively rolling off the gain completely. The low frequency capacitive extension limit can be approximated from the following equation:

$$f_{CAUX} = \frac{1}{2\pi\,(R_O + R_{DE\text{-}Q})\,C_{AUX}} \text{ (Hz)}$$

Where, RO is the 50 Ω gate or drain line terminating resistor. RDE is the small series (<15 Ω de-queing resistor). CAUX is the capacitance of the bypass capacitor connected to the Aux Drain or gate pad, in farads.

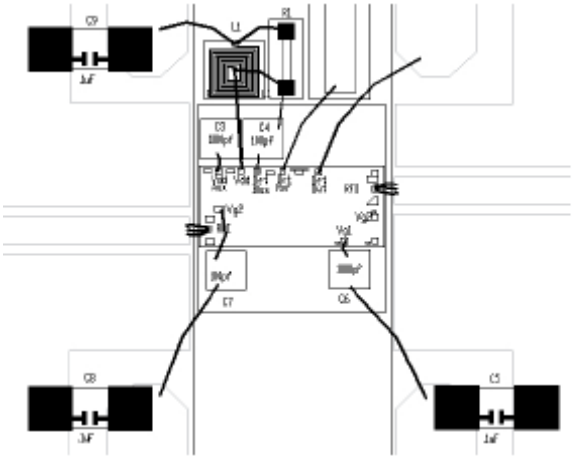


Figure 6

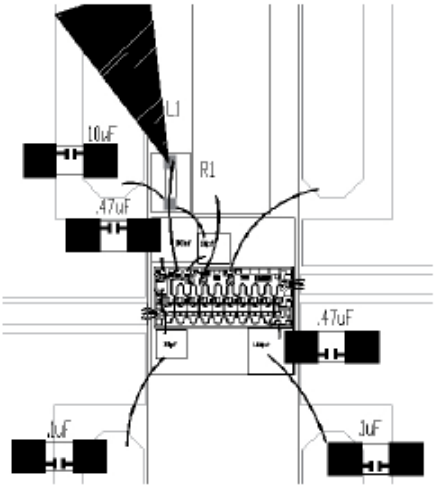


Figure 7

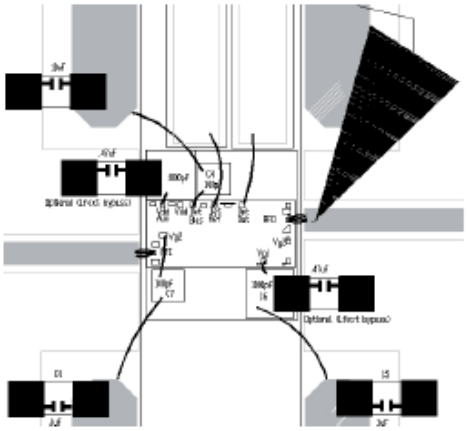


Figure 8

Using this equation, C_{DC} can be calculated for different desired corner frequencies. The equation is an approximation because it does not take into account other factors, such as transmission line impedances and TWA termination networks. In a typical assembly, the bypass capacitors are usually mono-block capacitors on the order of 0.01 or 0.47 µF, depending on the desired low frequency operating point. Keep in mind that these mono-blocks have series parasitic inductance. Since the RF DC blocking capacitors are the most sensitive, in this respect, we show a few recommended broadband DC blocks in Table 1. Figure 6, illustrates a 2 GHz to 50 GHz laminate PCB assembly. L1 is a chip inductor, and R1 is the de-queing alumina chip resistor. Figure 7, illustrates a 10 MHz to 50 GHz laminate PCB assembly. L1 is a Piconics broadband inductor. This inductor has an iron filling that negates the parallel resistor for de-queing. R1 is used simply as a means of launching the inductor. As discussed previously, as the DC bias is on the same electrical path as the RF path, it is possible to bias the TWA through the RF transmission line. Figure 7 illustrates this alternative method.

The 0.01 GHz to 40 GHz RF performance, using a 7 turn Micrometrics chip inductor shown in Figure 7, are illustrated in Figure 9. This module is for 2 to 40GHz applications. All module losses are included in this data.

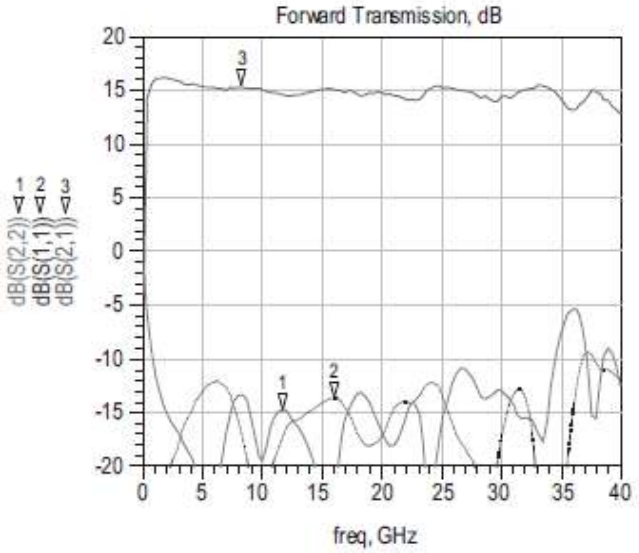


Figure 9. 0.01 to 40 GHz S-parameters using a seven-turn micrometrics chip inductor

The 0.01 GHz to 40 GHz RF performance, using a conical ferrite core inductor shown in Figure 7, is illustrated in Figure 9. This module is for 0.01 to 40GHz applications. All module losses are included in this data. To extend low-end frequency range to 30 KHz, an additional RFC is required in series to the conical ferrite core inductor.

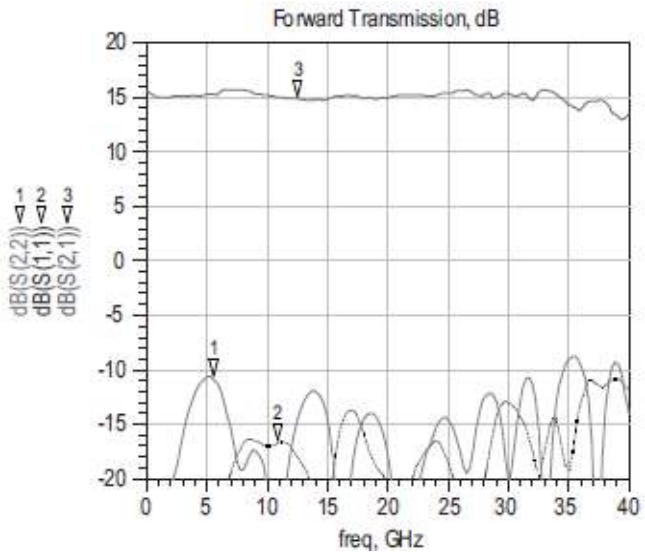


Figure 10. 0.01 to 40 GHz S-parameters using a conical ferrite core inductor

Table 1. Recommended Passives for the MMA-004023D, 30 kHz - 50 GHz TWA

Passive Type	Description	Vendor	Part#	Qty
100 pf Capacitor	**Bypass Cap**	**Presidio**	SA1515BX101M2HX5#00XF	**4**
0.1 µF Capacitor	**Bypass Cap**	AVX	AVX0402YG104ZAT2A	**3**
1000 pf Capacitor	Vdd Aux/Vg1 Bypass	Tecdia	SK04B102M11A6	**2**
0.47 µF Capacitor	Vdd Aux Bypass Cap	Murata	GRP155F51A474ZDO2B	**1**
*BB DC block capacitors	DC Block Cap	Presidio	BB0302X7R123M16VP8205	**2**
*BB DC block capacitors	DC Block Cap	ATC	545L Series	**2**
10 MHz-40 GHz Inductor	0.26uH Inductor	Gowanda	C100FL3944G6	**1**
*Spiral chip Inductor	Selective RF Choke	MicroFab	www.microfabnh.com	**1**
*Spiral chip Inductor	Selective RF Choke	Micrometrics	www.micrometrics.com	**1**
**Alumina Chip Resistor	De-queing Resistor	ATP	www.thinfilm.com	**1**