1 Ω Typical On Resistance, ±5 V, +12 V, +5 V, and +3.3 V Dual SPDT Switches

Data Sheet **ADG1636**

FEATURES

- 1 Ω typical on resistance
- 0.2 Ω on resistance flatness
- ±3.3 V to ±8 V dual supply operation
- 3.3 V to 16 V single supply operation
- No V_L supply required
- 3 V logic-compatible inputs
- Rail-to-rail operation
- Continuous current per channel
  - LFCSP: 385 mA
  - TSSOP: 238 mA
- 16-lead TSSOP and 16-lead, 4 mm × 4 mm LFCSP

APPLICATIONS

- Communication systems
- Medical systems
- Audio signal routing
- Video signal routing
- Automatic test equipment
- Data acquisition systems
- Battery-powered systems
- Sample-and-hold systems
- Relay replacements

FUNCTIONAL BLOCK DIAGRAMS

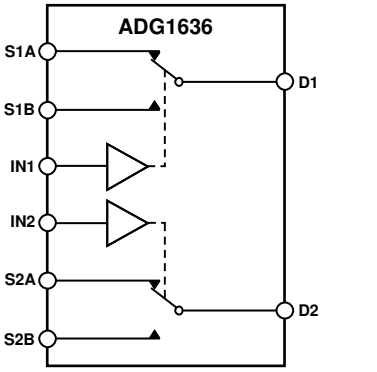


Figure 1. 16-Lead TSSOP

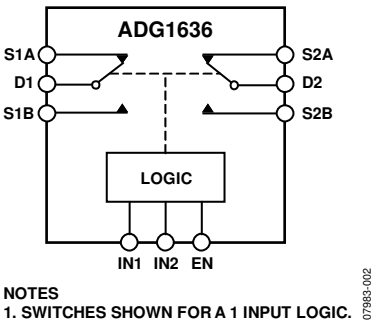


Figure 2. 16-Lead LFCSP

GENERAL DESCRIPTION

The ADG1636 is a monolithic CMOS device containing two independently selectable single-pole/double-throw (SPDT) switches. An EN input is used to enable or disable the device. When disabled, all channels are switched off. Each switch conducts equally well in both directions when on and has an input signal range that extends to the supplies. In the off condition, signal levels up to the supplies are blocked. Both switches exhibit break-before-make switching action for use in multiplexer applications.

The ultralow on resistance of these switches make them ideal solutions for data acquisition and gain switching applications where low on resistance and distortion is critical. The on resistance profile is very flat over the full analog input range, ensuring excellent linearity and low distortion when switching audio signals.

The CMOS construction ensures ultralow power dissipation, making the devices ideally suited for portable and battery-powered instruments.

PRODUCT HIGHLIGHTS

1. 1.6 Ω maximum on resistance over temperature.
2. Minimum distortion: THD + N = 0.007%.
3. 3 V logic-compatible digital inputs: V_{INH} = 2.0 V, V_{INL} = 0.8 V.
4. No V_L logic power supply required.
5. Ultralow power dissipation: <16 nW.
6. 16-lead TSSOP and 16-lead 4 mm × 4 mm LFCSP.

Rev. B
Document Feedback
Information furnished by Analog Devices is believed to be accurate and reliable. However, no responsibility is assumed by Analog Devices for its use, nor for any infringements of patents or other rights of third parties that may result from its use. Specifications subject to change without notice. No license is granted by implication or otherwise under any patent or patent rights of Analog Devices. Trademarks and registered trademarks are the property of their respective owners.

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 ©2009–2016 Analog Devices, Inc. All rights reserved.
Technical Support www.analog.com

TABLE OF CONTENTS

Features ... 1
Applications ... 1
General Description ... 1
Functional Block Diagrams ... 1
Product Highlights ... 1
Revision History ... 2
Specifications ... 3
±5 V Dual Supply ... 3
12 V Single Supply ... 4
5 V Single Supply ... 5
3.3 V Single Supply ... 6
Continuous Current per Channel, S or D ... 7
Absolute Maximum Ratings ... 8
ESD Caution ... 8
Pin Configurations and Function Descriptions ... 9
Typical Performance Characteristics ... 10
Test Circuits ... 13
Terminology ... 15
Outline Dimensions ... 16
Ordering Guide ... 16

REVISION HISTORY

3/16—Rev. A to Rev. B

Changed CP-16-13 to CP-16-26 ... Throughout
Changes to Figure 3, Figure 4, and Table 7 ... 9
Updated Outline Dimensions ... 16
Changes to Ordering Guide ... 16

9/09—Rev. 0 to Rev. A

Changes to Table 4 ... 6

1/09—Revision 0: Initial Version

SPECIFICATIONS

±5 V DUAL SUPPLY

V_{DD} = +5 V ± 10%, V_{SS} = −5 V ± 10%, GND = 0 V, unless otherwise noted.

Table 1.

Parameter	25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					
Analog Signal Range			V_{DD} to V_{SS}	V	
On Resistance (R_{ON})	1			Ω typ	V_S = ±4.5 V, I_S = −10 mA; see Figure 23
	1.2	1.4	1.6	Ω max	V_{DD} = ±4.5 V, V_{SS} = ±4.5 V
On Resistance Match Between Channels (ΔR_{ON})	0.04			Ω typ	V_S = ±4.5 V, I_S = −10 mA
	0.08	0.09	0.1	Ω max	
On Resistance Flatness ($R_{FLAT(ON)}$)	0.2			Ω typ	V_S = ±4.5 V, I_S = −10 mA
	0.25	0.29	0.34	Ω max	
LEAKAGE CURRENTS					V_{DD} = +5.5 V, V_{SS} = −5.5 V
Source Off Leakage, I_S (Off)	±0.1			nA typ	V_S = ±4.5 V, V_D = ∓4.5 V; see Figure 24
	±0.25	±1	±4	nA max	
Drain Off Leakage, I_D (Off)	±0.1			nA typ	V_S = ±4.5V, V_D = ∓4.5 V; see Figure 24
	±0.25	±2	±10	nA max	
Channel On Leakage, I_D, I_S (On)	±0.3			nA typ	V_S = V_D = ±4.5 V; see Figure 25
	±0.6	±2	±12	nA max	
DIGITAL INPUTS					
Input High Voltage, V_{INH}			2.0	V min	
Input Low Voltage, V_{INL}			0.8	V max	
Input Current, I_{INL} or I_{INH}	0.005			μA typ	V_{IN} = V_{GND} or V_{DD}
			±0.1	μA max	
Digital Input Capacitance, C_{IN}	5			pF typ	
DYNAMIC CHARACTERISTICS[1]					
Transition Time, $t_{TRANSITION}$	130			ns typ	R_L = 300 Ω, C_L = 35 pF
	209	245	273	ns max	V_S = 2.5 V; see Figure 30
t_{ON} (EN)	119			ns typ	R_L = 300 Ω, C_L = 35 pF
	148	166	176	ns max	V_S = 2.5 V; see Figure 30
t_{OFF} (EN)	182			ns typ	R_L = 300 Ω, C_L = 35 pF
	228	259	281	ns max	V_S = 2.5 V; see Figure 30
Break-Before-Make Time Delay, t_D	30			ns typ	R_L = 300 Ω, C_L = 35 pF
			17	ns min	V_{S1} = V_{S2} = 2.5 V; see Figure 31
Charge Injection	130			pC typ	V_S = 0 V, R_S = 0 Ω, C_L = 1 nF; see Figure 32
Off Isolation	70			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; see Figure 26
Channel-to-Channel Crosstalk	90			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; see Figure 28
Total Harmonic Distortion + Noise (THD + N)	0.007			% typ	R_L = 110 Ω, 5 V p-p, f = 20 Hz to 20 kHz; see Figure 29
−3 dB Bandwidth	25			MHz typ	R_L = 50 Ω, C_L = 5 pF; see Figure 27
C_S (Off)	68			pF typ	V_S = 0 V, f = 1 MHz
C_D (Off)	127			pF typ	V_S = 0 V, f = 1 MHz
C_D, C_S (On)	220			pF typ	V_S = 0 V, f = 1 MHz
POWER REQUIREMENTS					V_{DD} = +5.5 V, V_{SS} = −5.5 V
I_{DD}	0.001			μA typ	Digital inputs = 0 V or V_{DD}
			1.0	μA max	
V_{DD}/V_{SS}			±3.3/±8	V min/max	

[1] Guaranteed by design, not subject to production test.

12 V SINGLE SUPPLY

V_{DD} = 12 V ± 10%, V_{SS} = 0 V, GND = 0 V, unless otherwise noted.

Table 2.

Parameter	25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					
Analog Signal Range			0 V to V_{DD}	V	
On Resistance (R_{ON})	0.95			Ω typ	V_S = 0 V to 10 V, I_S = −10 mA; see Figure 23
	1.1	1.25	1.45	Ω max	V_{DD} = 10.8 V, V_{SS} = 0 V
On Resistance Match Between Channels (ΔR_{ON})	0.03			Ω typ	V_S = 10 V, I_S = −10 mA
	0.06	0.07	0.08	Ω max	
On Resistance Flatness ($R_{FLAT(ON)}$)	0.2			Ω typ	V_S = 0 V to 10 V, I_S = −10 mA
	0.23	0.27	0.32	Ω max	
LEAKAGE CURRENTS					V_{DD} = 13.2 V, V_{SS} = 0 V
Source Off Leakage, I_S (Off)	±0.1			nA typ	V_S = 1 V/10 V, V_S = 10 V/1 V; see Figure 24
	±0.25	±1	±4	nA max	
Drain Off Leakage, I_D (Off)	±0.1			nA typ	V_S = 1 V/10 V, V_S = 10 V/1 V; see Figure 24
	±0.25	±2	±10	nA max	
Channel On Leakage, I_D, I_S (On)	±0.3			nA typ	V_S = V_D = 1 V or 10 V; see Figure 25
	±0.6	±2	±12	nA max	
DIGITAL INPUTS					
Input High Voltage, V_{INH}			2.0	V min	
Input Low Voltage, V_{INL}			0.8	V max	
Input Current, I_{INL} or I_{INH}	0.001			μA typ	V_{IN} = V_{GND} or V_{DD}
			±0.1	μA max	
Digital Input Capacitance, C_{IN}	5			pF typ	
DYNAMIC CHARACTERISTICS[1]					
Transition Time, $t_{TRANSITION}$	100			ns typ	R_L = 300 Ω, C_L = 35 pF
	153	183	206	ns max	V_S = 8 V; see Figure 30
t_{ON} (EN)	80			ns typ	R_L = 300 Ω, C_L = 35 pF
	95	103	110	ns max	V_S = 8 V; see Figure 30
t_{OFF} (EN)	133			ns typ	R_L = 300 Ω, C_L = 35 pF
	161	187	210	ns max	V_S = 8 V; see Figure 30
Break-Before-Make Time Delay, t_D	25			ns typ	R_L = 300 Ω, C_L = 35 pF
			17	ns min	V_{S1} = V_{S2} = 8 V; see Figure 31
Charge Injection	150			pC typ	V_S = 6 V, R_S = 0 Ω, C_L = 1 nF; see Figure 32
Off Isolation	70			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; see Figure 26
Channel-to-Channel Crosstalk	90			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 1 MHz; see Figure 28
Total Harmonic Distortion + Noise (THD + N)	0.013			% typ	R_L = 110 Ω, 5 V p-p, f = 20 Hz to 20 kHz; see Figure 29
−3 dB Bandwidth	27			MHz typ	R_L = 50 Ω, C_L = 5 pF; see Figure 27
C_S (Off)	65			pF typ	V_S = 6 V, f = 1 MHz
C_D (Off)	120			pF typ	V_S = 6 V, f = 1 MHz
C_D, C_S (On)	216			pF typ	V_S = 6 V, f = 1 MHz
POWER REQUIREMENTS					V_{DD} = 12 V
I_{DD}	0.001			μA typ	Digital inputs = 0 V or V_{DD}
			1	μA max	
I_{DD}	230			μA typ	Digital inputs = 5 V
			360	μA max	
V_{DD}			3.3/16	V min/max	

[1] Guaranteed by design, not subject to production test.

5 V SINGLE SUPPLY

V_{DD} = 5 V ± 10%, V_{SS} = 0 V, GND = 0 V, unless otherwise noted.

Table 3.

Parameter	25°C	−40°C to +85°C	−40°C to 125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					
Analog Signal Range			0 V to V_{DD}	V	
On Resistance (R_{ON})	1.7			Ω typ	V_S = 0 V to 4.5 V, I_S = −10 mA; see Figure 23
	2.15	2.4	2.7	Ω max	V_{DD} = 4.5 V, V_{SS} = 0 V
On Resistance Match Between Channels (ΔR_{ON})	0.05			Ω typ	V_S = 0 V to 4.5 V, I_S = −10 mA
	0.09	0.12	0.15	Ω max	
On Resistance Flatness ($R_{FLAT(ON)}$)	0.4			Ω typ	V_S = 0 V to 4.5 V, I_S = −10 mA
	0.53	0.55	0.6	Ω max	
LEAKAGE CURRENTS					V_{DD} = 5.5 V, V_{SS} = 0 V
Source Off Leakage, I_S (Off)	±0.05			nA typ	V_S = 1 V/4.5 V, V_D = 4.5 V/1 V; see Figure 24
	±0.25	±1	±4	nA max	
Drain Off Leakage, I_D (Off)	±0.05			nA typ	V_S = 1 V/4.5 V, V_D = 4.5 V/1 V; see Figure 24
	±0.25	±2	±10	nA max	
Channel On Leakage, I_D, I_S (On)	±0.1			nA typ	V_S = V_D = 1 V or 4.5 V; see Figure 25
	±0.6	±2	±12	nA max	
DIGITAL INPUTS					
Input High Voltage, V_{INH}			2.0	V min	
Input Low Voltage, V_{INL}			0.8	V max	
Input Current, I_{INL} or I_{INH}	0.001			μA typ	V_{IN} = V_{GND} or V_{DD}
			±0.1	μA max	
Digital Input Capacitance, C_{IN}	5			pF typ	
DYNAMIC CHARACTERISTICS[1]					
Transition Time, $t_{TRANSITION}$	160			ns typ	R_L = 300 Ω, C_L = 35 pF
	271	319	355	ns max	V_S = 2.5 V; see Figure 30
t_{ON} (EN)	132			ns typ	R_L = 300 Ω, C_L = 35 pF
	172	185	201	ns max	V_S = 2.5 V; see Figure 30
t_{OFF} (EN)	210			ns typ	R_L = 300 Ω, C_L = 35 pF
	268	313	345	ns max	V_S = 2.5 V; see Figure 30
Break-Before-Make Time Delay, t_D	30			ns typ	R_L = 300 Ω, C_L = 35 pF
			17	ns min	V_{S1} = V_{S2} = 2.5 V; see Figure 31
Charge Injection	70			pC typ	V_S = 2.5 V, R_S = 0 Ω, C_L = 1 nF; see Figure 32
Off Isolation	70			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 100 kHz; see Figure 26
Channel-to-Channel Crosstalk	90			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 100 kHz; see Figure 28
Total Harmonic Distortion + Noise (THD + N)	0.09			% typ	R_L = 110 Ω, f = 20 Hz to 20 kHz, V_S = 3.5 V p-p; see Figure 29
−3 dB Bandwidth	26			MHz typ	R_L = 50 Ω, C_L = 5 pF; see Figure 27
C_S (Off)	76			pF typ	V_S = 2.5 V, f = 1 MHz
C_D (Off)	145			pF typ	V_S = 2.5 V, f = 1 MHz
C_D, C_S (On)	237			pF typ	V_S = 2.5 V, f = 1 MHz
POWER REQUIREMENTS					V_{DD} = 5.5 V
I_{DD}	0.001			μA typ	Digital inputs = 0 V or V_{DD}
		1.0	1.0	μA max	
V_{DD}			3.3/16	V min/max	

[1] Guaranteed by design, not subject to production test.

3.3 V SINGLE SUPPLY

V_{DD} = 3.3 V, V_{SS} = 0 V, GND = 0 V, unless otherwise noted.

Table 4.

Parameter	25°C	−40°C to +85°C	−40°C to +125°C	Unit	Test Conditions/Comments
ANALOG SWITCH					
Analog Signal Range			0 V to V_{DD}	V	
On Resistance (R_{ON})	3.2	3.4	3.6	Ω typ	V_S = 0 V to V_{DD}, I_S = −10 mA; see Figure 23
					V_{DD} = 3.3 V, V_{SS} = 0 V
On Resistance Match Between Channels (ΔR_{ON})	0.06	0.07	0.08	Ω typ	V_S = 0 V to V_{DD}, I_S = −10 mA
On Resistance Flatness ($R_{FLAT(ON)}$)	1.2	1.3	1.4	Ω typ	V_S = 0 V to V_{DD}, I_S = −10 mA
LEAKAGE CURRENTS					V_{DD} = 3.6 V, V_{SS} = 0 V
Source Off Leakage, I_S (Off)	±0.02			nA typ	V_S = 0.6 V/3 V, V_D = 3 V/0.6 V; see Figure 24
	±0.25	±1	±4	nA max	
Drain Off Leakage, I_D (Off)	±0.02			nA typ	V_S = 0.6 V/3 V, V_D = 3 V/0.6 V; see Figure 24
	±0.25	±2	±10	nA max	
Channel On Leakage, I_D, I_S (On)	±0.05			nA typ	V_S = V_D = 0.6 V or 3 V; see Figure 25
	±0.6	±2	±12	nA max	
DIGITAL INPUTS					
Input High Voltage, V_{INH}			2.0	V min	
Input Low Voltage, V_{INL}			0.8	V max	
Input Current, I_{INL} or I_{INH}	0.001			μA typ	V_{IN} = V_{GND} or V_{DD}
			±0.1	μA max	
Digital Input Capacitance, C_{IN}	5			pF typ	
DYNAMIC CHARACTERISTICS[1]					
Transition Time, $t_{TRANSITION}$	275			ns typ	R_L = 300 Ω, C_L = 35 pF
	449	506	550	ns max	V_S = 1.5 V; see Figure 30
t_{ON} (EN)	225			ns typ	R_L = 300 Ω, C_L = 35 pF
	306	327	338	ns max	V_S = 1.5 V; see Figure 30
t_{OFF} (EN)	340			ns typ	R_L = 300 Ω, C_L = 35 pF
	454	512	553	ns max	V_S = 1.5 V; see Figure 30
Break-Before-Make Time Delay, t_D	50			ns typ	R_L = 300 Ω, C_L = 35 pF
			28	ns min	V_{S1} = V_{S2} = 1.5 V; see Figure 31
Charge Injection	50			pC typ	V_S = 1.5 V, R_S = 0 Ω, C_L = 1 nF; see Figure 32
Off Isolation	70			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 100 kHz; see Figure 26
Channel-to-Channel Crosstalk	90			dB typ	R_L = 50 Ω, C_L = 5 pF, f = 100 kHz; see Figure 28
Total Harmonic Distortion + Noise (THD + N)	0.19			% typ	R_L = 33 Ω, f = 20 Hz to 20 kHz, V_S = 2 V p-p; see Figure 29
−3 dB Bandwidth	26			MHz typ	R_L = 50 Ω, C_L = 5 pF; see Figure 27
C_S (Off)	80			pF typ	V_S = 1.5 V, f = 1 MHz
C_D (Off)	153			pF typ	V_S = 1.5 V, f = 1 MHz
C_D, C_S (On)	243			pF typ	V_S = 1.5 V, f = 1 MHz
POWER REQUIREMENTS					V_{DD} = 3.6 V
I_{DD}	0.001			μA typ	Digital inputs = 0 V or V_{DD}
		1.0	1.0	μA max	
V_{DD}			3.3/16	V min/max	

[1] Guaranteed by design, not subject to production test.

CONTINUOUS CURRENT PER CHANNEL, S OR D

Table 5.

Parameter	25°C	85°C	125°C	Unit
CONTINUOUS CURRENT, S OR D				
V_{DD} = +5 V, V_{SS} = −5 V				
TSSOP (θ_{JA} = 150.4°C/W)	238	151	88	mA maximum
LFCSP (θ_{JA} = 48.7°C/W)	385	220	105	mA maximum
V_{DD} = 12 V, V_{SS} = 0 V				
TSSOP (θ_{JA} = 150.4°C/W)	280	175	98	mA maximum
LFCSP (θ_{JA} = 48.7°C/W)	469	259	119	mA maximum
V_{DD} = 5 V, V_{SS} = 0 V				
TSSOP (θ_{JA} = 150.4°C/W)	189	126	77	mA maximum
LFCSP (θ_{JA} = 48.7°C/W)	301	182	98	mA maximum
V_{DD} = 3.3 V, V_{SS} = 0 V				
TSSOP (θ_{JA} = 150.4°C/W)	189	130	84	mA maximum
LFCSP (θ_{JA} = 48.7°C/W)	305	189	105	mA maximum

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 6.

Parameter	Rating
V_{DD} to V_{SS}	18 V
V_{DD} to GND	−0.3 V to +18 V
V_{SS} to GND	+0.3 V to −18 V
Analog Inputs[1]	V_{SS} − 0.3 V to V_{DD} + 0.3 V or 30 mA, whichever occurs first
Digital Inputs[1]	GND − 0.3 V to V_{DD} + 0.3 V or 30 mA, whichever occurs first
Peak Current, S or D	850 mA (pulsed at 1 ms, 10% duty cycle maximum)
Continuous Current, S or D[2]	Data + 15%
Operating Temperature Range	
Industrial (Y Version)	−40°C to +125°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
θ_{JA} Thermal Impedance	
16-Lead TSSOP (2-Layer Board)	150.4°C/W
16-Lead LFCSP (4-Layer Board)	48.7°C/W
Reflow Soldering Peak Temperature, Pb free	260°C

[1] Overvoltages at IN, S, or D are clamped by internal diodes. Current should be limited to the maximum ratings given.
[2] See Table 5.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATIONS AND FUNCTION DESCRIPTIONS

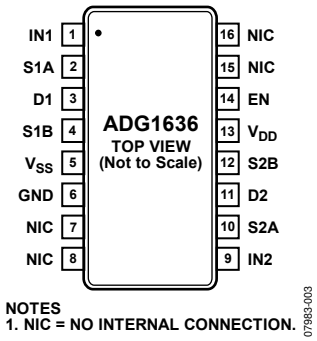


Figure 3. 16-Lead TSSOP Pin Configuration

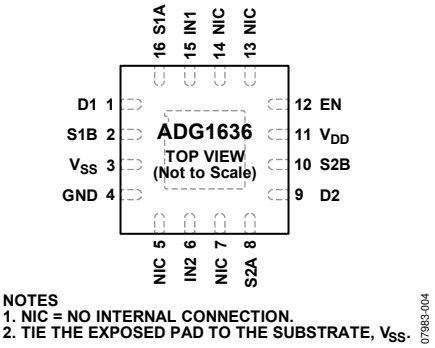


Figure 4. 16-Lead LFCSP Pin Configuration

Table 7. Pin Function Descriptions

Pin No.			
TSSOP	**LFCSP**	**Mnemonic**	**Description**
1	15	IN1	Logic Control Input.
2	16	S1A	Source Terminal. This pin can be an input or output.
3	1	D1	Drain Terminal. This pin can be an input or output.
4	2	S1B	Source Terminal. This pin can be an input or output.
5	3	V_{SS}	Most Negative Power Supply Potential.
6	4	GND	Ground (0 V) Reference.
7, 8, 15, 16	5, 7, 13, 14	NIC	No Internal Connection.
9	6	IN2	Logic Control Input.
10	8	S2A	Source Terminal. This pin can be an input or output.
11	9	D2	Drain Terminal. This pin can be an input or output.
12	10	S2B	Source Terminal. This pin can be an input or output.
13	11	V_{DD}	Most Positive Power Supply Potential.
14	12	EN	Active High Digital Input. When this pin is low, the device is disabled and all switches are off. When this pin is high, the Ax logic inputs determine the on switches.
N/A[1]	0	EPAD	Exposed Pad. Tie the exposed pad to the substrate, V_{SS}.

[1] N/A means not applicable.

Table 8. ADG1636 TSSOP Truth Table

EN	INx	SxA	SxB
0	X	Off	Off
1	0	Off	On
1	1	On	Off

Table 9. ADG1636 LFCSP Truth Table

EN	INx	SxA	SxB
0	X	Off	Off
1	0	Off	On
1	1	On	Off

TYPICAL PERFORMANCE CHARACTERISTICS

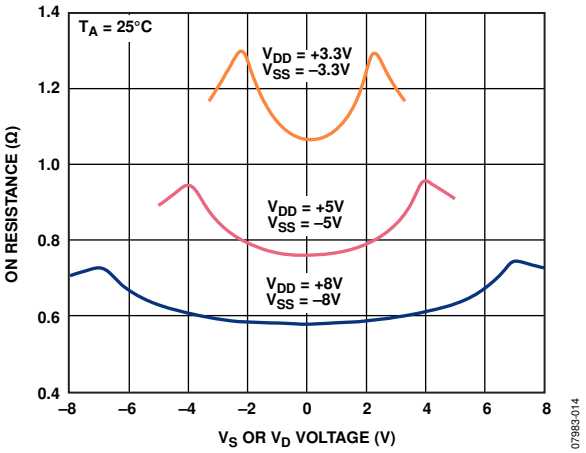


Figure 5. On Resistance as a Function of V_D (V_S) for Dual Supply

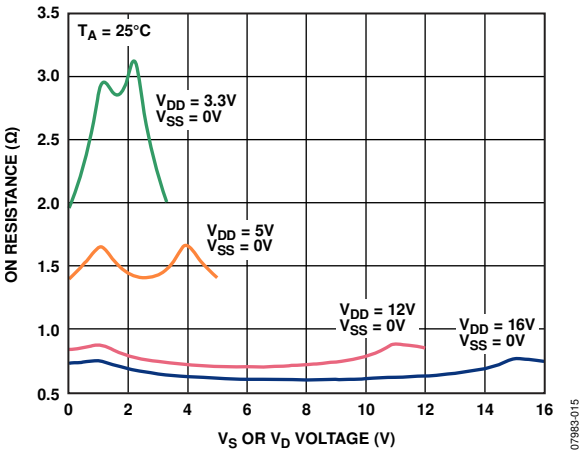


Figure 6. On Resistance as a Function of V_D (V_S) for Single Supply

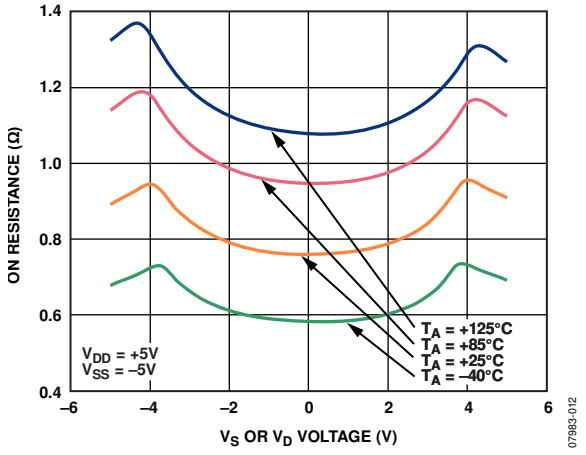


Figure 7. On Resistance as a Function of V_D (V_S) for Different Temperatures, ±5 V Dual Supply

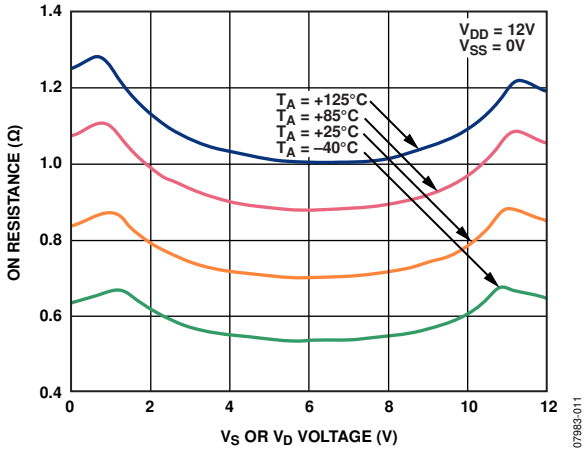


Figure 8. On Resistance as a Function of V_D (V_S) for Different Temperatures, 12 V Single Supply

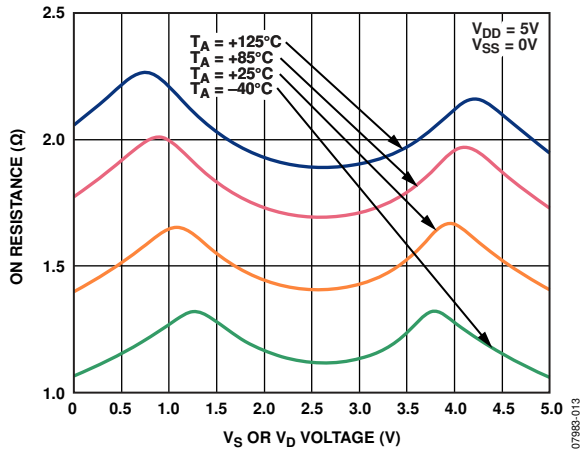


Figure 9. On Resistance as a Function of V_D (V_S) for Different Temperatures, 5 V Single Supply

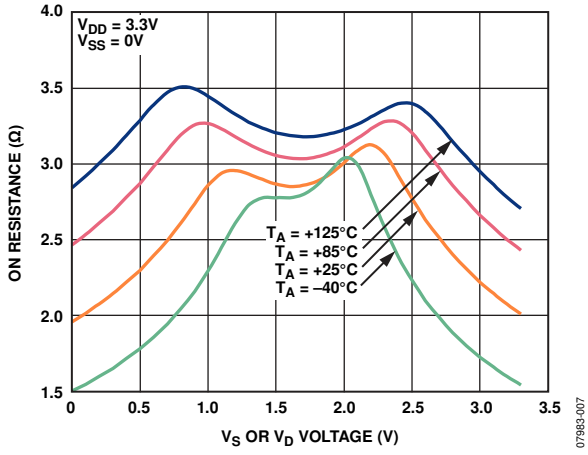


Figure 10. On Resistance as a Function of V_D (V_S) for Different Temperatures, 3.3 V Single Supply

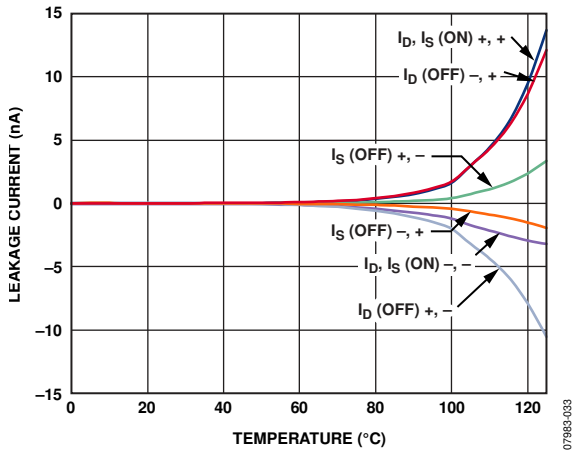


Figure 11. Leakage Currents as a Function of Temperature, ±5 V Dual Supply

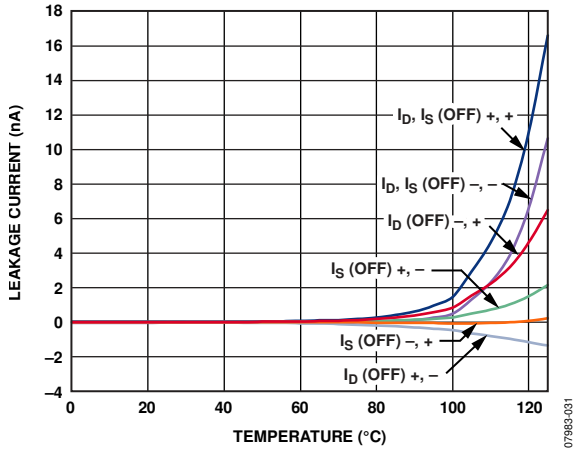


Figure 14. Leakage Currents as a Function of Temperature, 3.3 V Single Supply

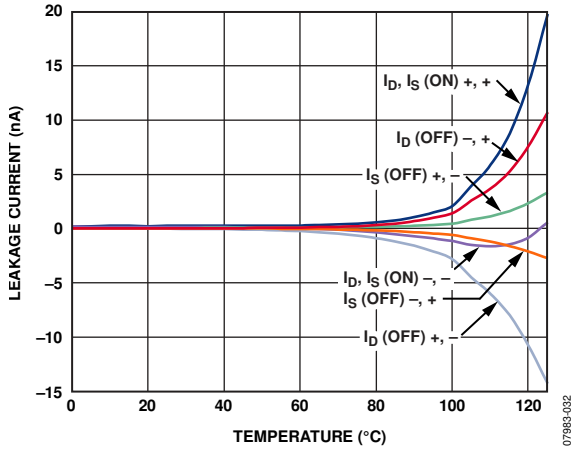


Figure 12. Leakage Currents as a Function of Temperature, 12 V Single Supply

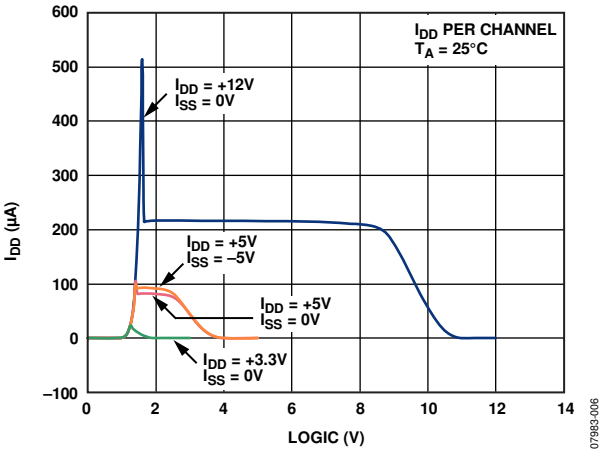


Figure 15. I_{DD} vs. Logic Level

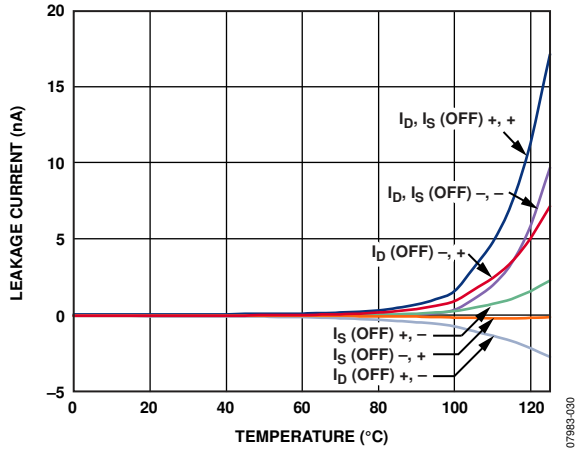


Figure 13. Leakage Currents as a Function of Temperature, 5 V Single Supply

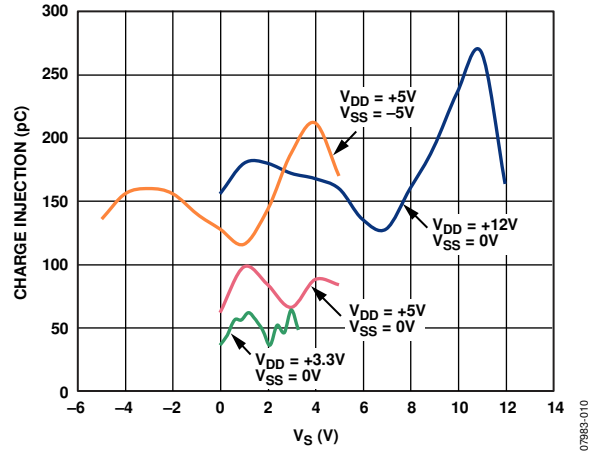


Figure 16. Charge Injection vs. Source Voltage

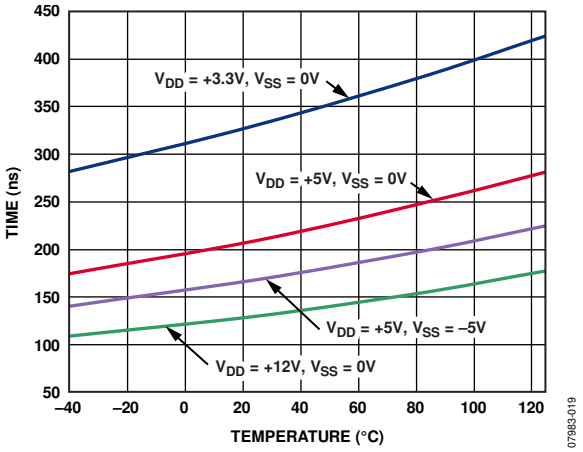


Figure 17. t_{ON}/t_{OFF} Times vs. Temperature

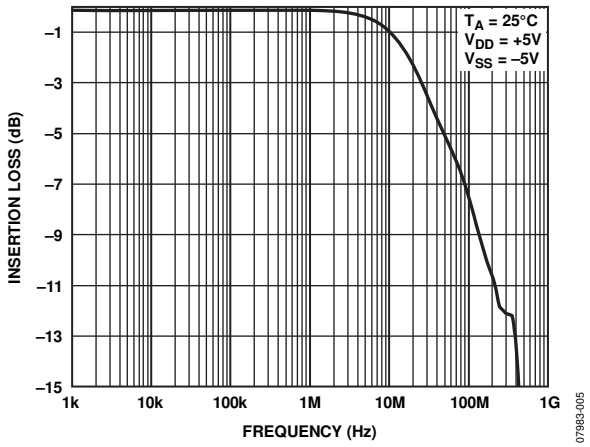


Figure 20. On Response vs. Frequency

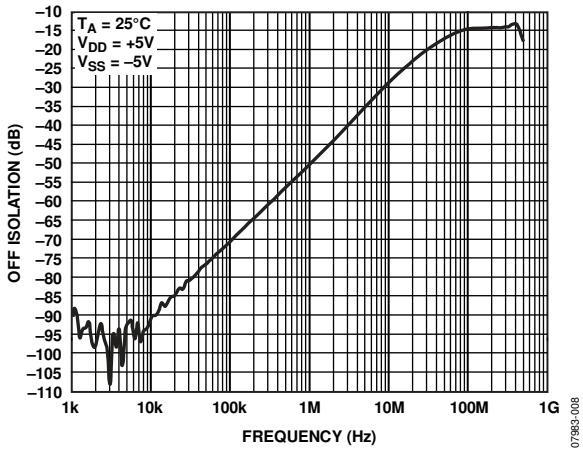


Figure 18. Off Isolation vs. Frequency

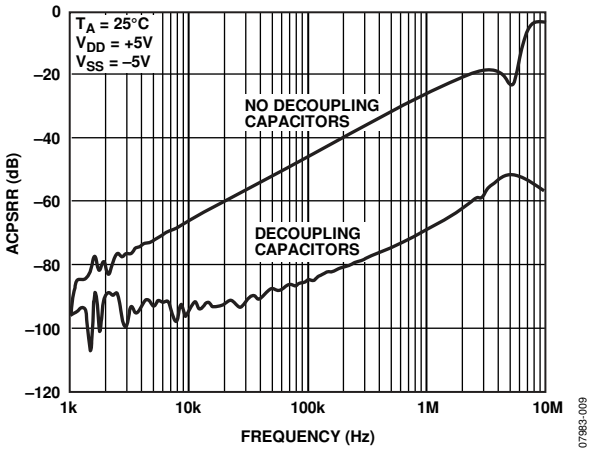


Figure 21. ACPSRR vs. Frequency

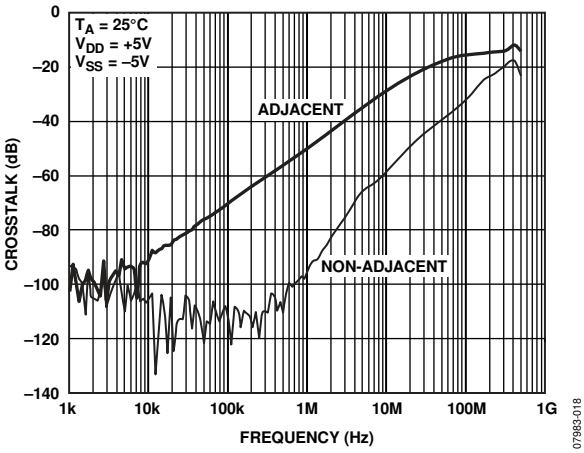


Figure 19. Crosstalk vs. Frequency

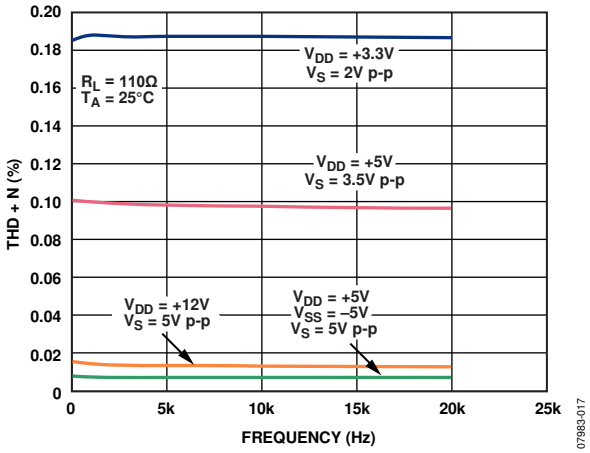


Figure 22. THD + N vs. Frequency

TEST CIRCUITS

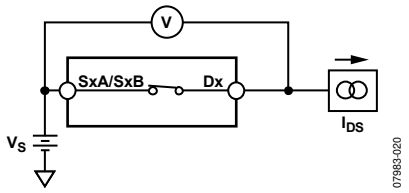


Figure 23. On Resistance

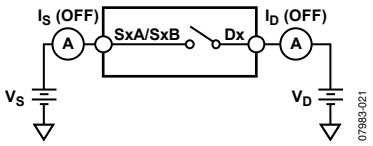


Figure 24. Off Leakage

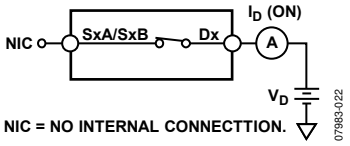


Figure 25. On Leakage

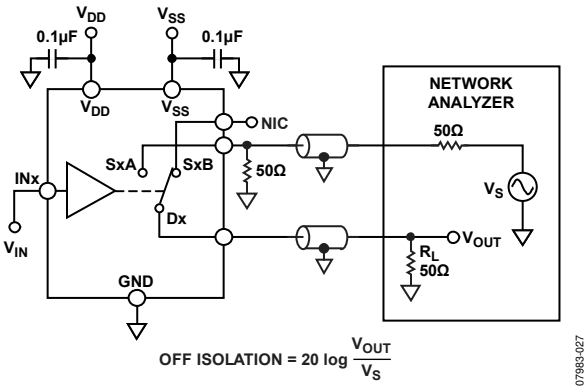


Figure 26. Off Isolation

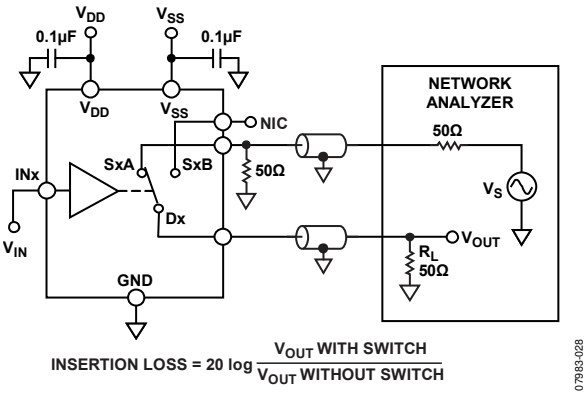


Figure 27. Bandwidth

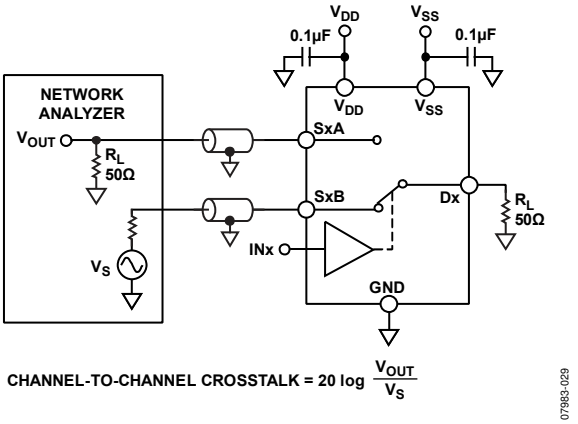


Figure 28. Channel-to-Channel Crosstalk

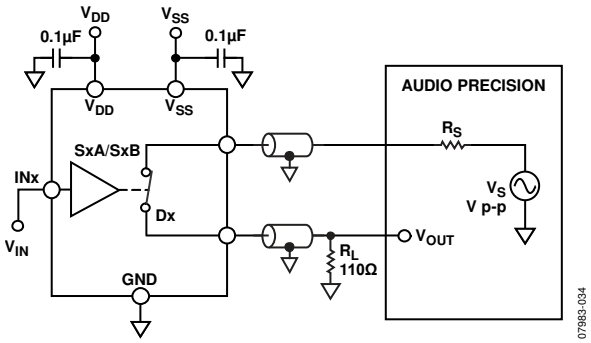


Figure 29. THD + Noise

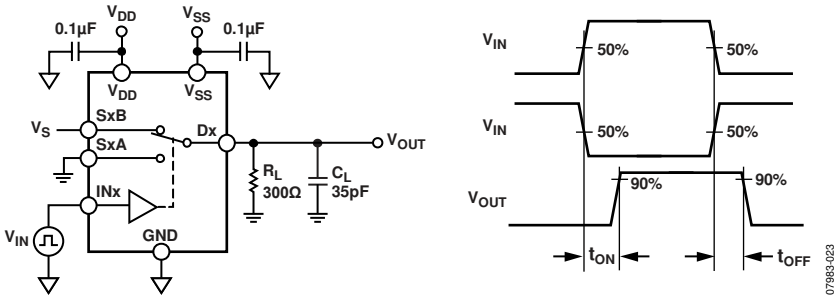


Figure 30. Switching Times

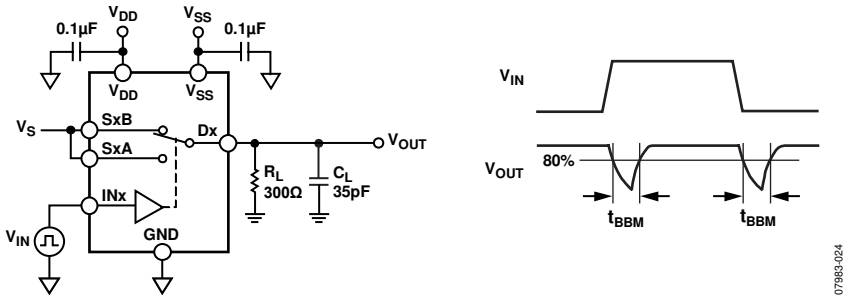


Figure 31. Break-Before-Make Time Delay

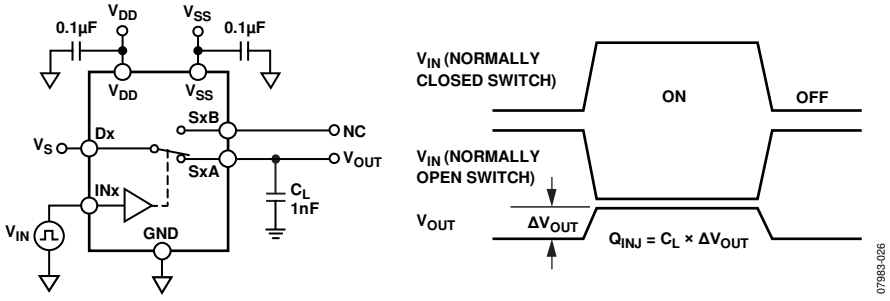


Figure 32. Charge Injection

TERMINOLOGY

I_{DD}
The positive supply current.

I_{SS}
The negative supply current.

V_D (V_S)
The analog voltage on Terminal D and Terminal S.

R_{ON}
The ohmic resistance between Terminal D and Terminal S.

$R_{FLAT(ON)}$
Flatness that is defined as the difference between the maximum and minimum value of on resistance measured over the specified analog signal range.

I_S (Off)
The source leakage current with the switch off.

I_D (Off)
The drain leakage current with the switch off.

I_D, I_S (On)
The channel leakage current with the switch on.

V_{INL}
The maximum input voltage for Logic 0.

V_{INH}
The minimum input voltage for Logic 1.

I_{INL} (I_{INH})
The input current of the digital input.

C_S (Off)
The off switch source capacitance, which is measured with reference to ground.

C_D (Off)
The off switch drain capacitance, which is measured with reference to ground.

C_D, C_S (On)
The on switch capacitance, which is measured with reference to ground.

C_{IN}
The digital input capacitance.

$t_{TRANSITION}$
The delay time between the 50% and 90% points of the digital input and switch on condition when switching from one address state to another.

t_{ON} (EN)
The delay between applying the digital control input and the output switching on. See Figure 30.

t_{OFF} (EN)
The delay between applying the digital control input and the output switching off. See Figure 30.

Charge Injection
A measure of the glitch impulse transferred from the digital input to the analog output during switching.

Off Isolation
A measure of unwanted signal coupling through an off switch.

Crosstalk
A measure of unwanted signal that is coupled through from one channel to another as a result of parasitic capacitance.

Bandwidth
The frequency at which the output is attenuated by 3 dB.

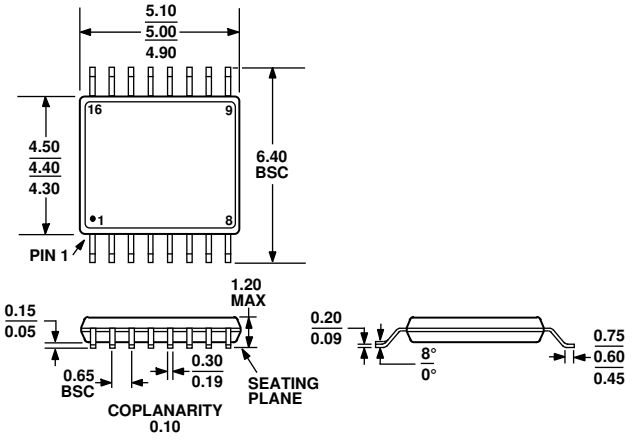
On Response
The frequency response of the on switch.

Insertion Loss
The loss due to the on resistance of the switch.

Total Harmonic Distortion + Noise (THD + N)
The ratio of the harmonic amplitude plus noise of the signal to the fundamental.

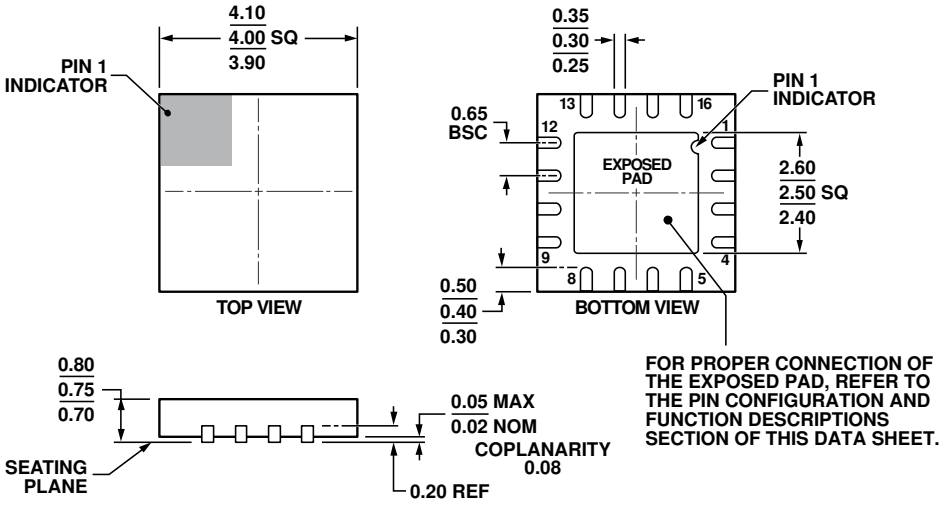
AC Power Supply Rejection Ratio (ACPSRR)
The ratio of the amplitude of signal on the output to the amplitude of the modulation. This is a measure of the ability of the device to avoid coupling noise and spurious signals that appear on the supply voltage pin to the output of the switch. The dc voltage on the device is modulated by a sine wave of 0.62 V p-p.

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-153-AB

Figure 33. 16-Lead Thin Shrink Small Outline Package [TSSOP]
(RU-16)
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-220-WGGC.

Figure 34. 16-Lead Lead Frame Chip Scale Package [LFCSP]
4 mm × 4 mm Body and 0.75 mm Package Height
(CP-16-26)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
ADG1636BRUZ	−40°C to +125°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16
ADG1636BRUZ-REEL	−40°C to +125°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16
ADG1636BRUZ-REEL7	−40°C to +125°C	16-Lead Thin Shrink Small Outline Package [TSSOP]	RU-16
ADG1636BCPZ-REEL	−40°C to +125°C	16-Lead Lead Frame Chip Scale Package [LFCSP]	CP-16-26
ADG1636BCPZ-REEL7	−40°C to +125°C	16-Lead Lead Frame Chip Scale Package [LFCSP]	CP-16-26

[1] Z = RoHS Compliant Part.

©2009–2016 Analog Devices, Inc. All rights reserved. Trademarks and registered trademarks are the property of their respective owners.
D07983-0-3/16(B)