

TOSHIBA Field Effect Transistor Silicon P Channel MOS Type

SSM3J36FS

○ Power Management Switches

- 1.5-V drive
- Low ON-resistance: $R_{ON} = 3.60 \Omega$ (max) (@ $V_{GS} = -1.5$ V)
 $R_{ON} = 2.70 \Omega$ (max) (@ $V_{GS} = -1.8$ V)
 $R_{ON} = 1.60 \Omega$ (max) (@ $V_{GS} = -2.8$ V)
 $R_{ON} = 1.31 \Omega$ (max) (@ $V_{GS} = -4.5$ V)

Absolute Maximum Ratings ($T_a = 25^\circ\text{C}$)

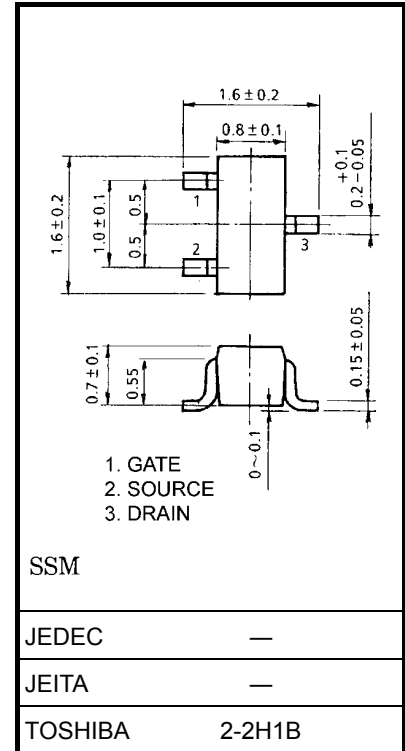
Characteristics	Symbol	Rating	Unit
Drain-source voltage	V_{DSS}	-20	V
Gate-source voltage	V_{GSS}	± 8	V
Drain current	DC	I_D	mA
	Pulse	I_{DP}	
Drain power dissipation	P_D (Note1)	150	mW
Channel temperature	T_{ch}	150	$^\circ\text{C}$
Storage temperature range	T_{stg}	-55 to 150	$^\circ\text{C}$

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/ "Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc.).

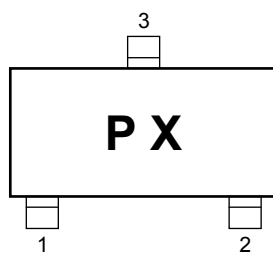
Note1: Mounted on an FR4 board
(25.4 mm \times 25.4 mm \times 1.6mm, Cu Pad: 0.36 mm² \times 3)

Unit: mm

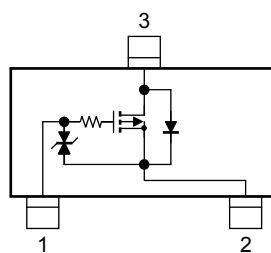


Weight: 2.4 mg (typ.)

Marking



Equivalent Circuit (top view)



Handling Precaution

When handling individual devices (which are not yet mounted on a circuit board), ensure that the environment is protected against static electricity. Operators should wear anti-static clothing, and containers and other objects that come into direct contact with devices should be made of anti-static materials.

Usage Considerations

Let V_{th} be the voltage applied between gate and source that causes the drain current (I_D) to below -1 mA for the SSM3J36FS). Then, for normal switching operation, $V_{GS(on)}$ must be higher than V_{th} , and $V_{GS(off)}$ must be lower than V_{th} . This relationship can be expressed as: $V_{GS(off)} < V_{th} < V_{GS(on)}$.

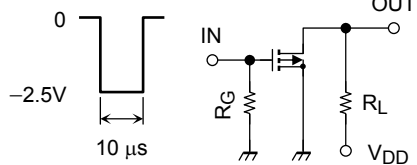
Take this into consideration when using the device.

Start of commercial production
2008-06

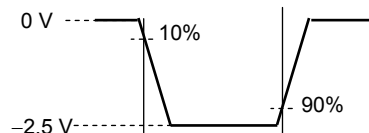
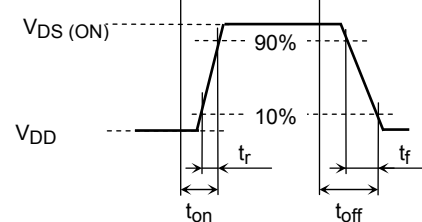
Electrical Characteristics (Ta = 25°C)

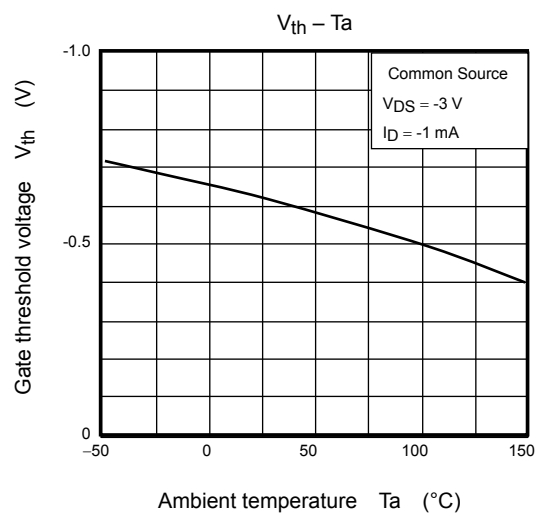
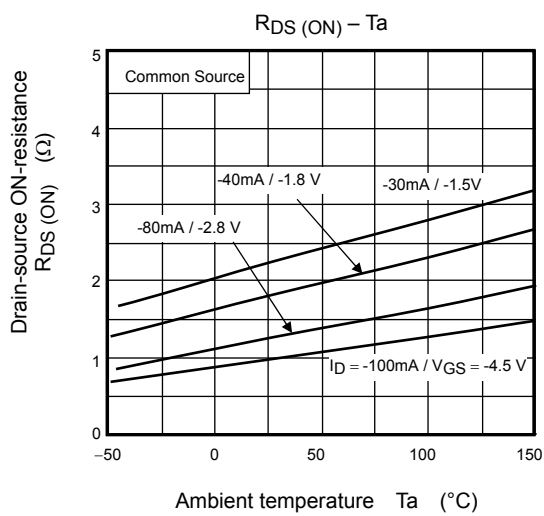
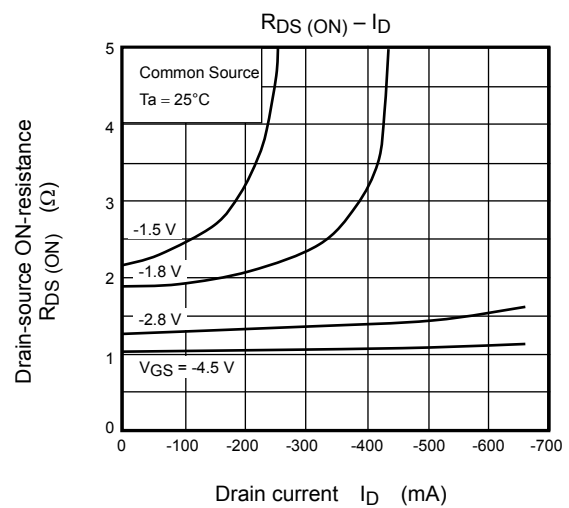
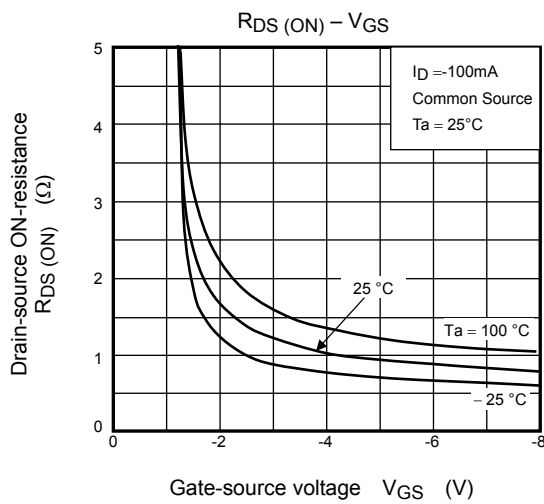
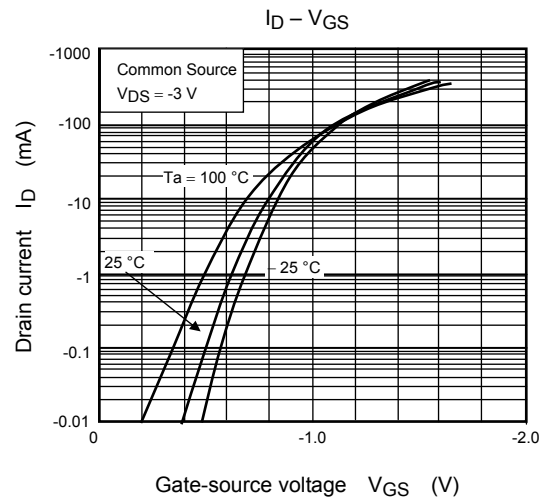
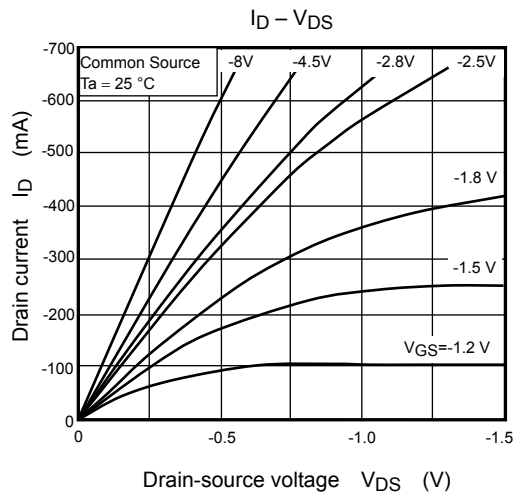
Characteristics	Symbol	Test Conditions	Min	Typ.	Max	Unit
Drain-source breakdown voltage	$V_{(BR)DSS}$	$I_D = -1 \text{ mA}$, $V_{GS} = 0 \text{ V}$	-20	—	—	V
	$V_{(BR)DSX}$	$I_D = -1 \text{ mA}$, $V_{GS} = 8 \text{ V}$	-12	—	—	
Drain cutoff current	I_{DSS}	$V_{DS} = -16 \text{ V}$, $V_{GS} = 0 \text{ V}$	—	—	-10	μA
Gate leakage current	I_{GSS}	$V_{GS} = \pm 8 \text{ V}$, $V_{DS} = 0 \text{ V}$	—	—	± 1	μA
Gate threshold voltage	V_{th}	$V_{DS} = -3 \text{ V}$, $I_D = -1 \text{ mA}$	-0.3	—	-1.0	V
Forward transfer admittance	$ Y_{fs} $	$V_{DS} = -3 \text{ V}$, $I_D = -100 \text{ mA}$ (Note2)	190	—	—	mS
Drain-source ON-resistance	$R_{DS(ON)}$	$I_D = -100 \text{ mA}$, $V_{GS} = -4.5 \text{ V}$ (Note2)	—	0.95	1.31	Ω
		$I_D = -80 \text{ mA}$, $V_{GS} = -2.8 \text{ V}$ (Note2)	—	1.22	1.60	
		$I_D = -40 \text{ mA}$, $V_{GS} = -1.8 \text{ V}$ (Note2)	—	1.80	2.70	
		$I_D = -30 \text{ mA}$, $V_{GS} = -1.5 \text{ V}$ (Note2)	—	2.23	3.60	
Input capacitance	C_{iss}	$V_{DS} = -10 \text{ V}$, $V_{GS} = 0 \text{ V}$, $f = 1 \text{ MHz}$	—	43	—	pF
Output capacitance	C_{oss}		—	10.3	—	
Reverse transfer capacitance	C_{rss}		—	6.1	—	
Total Gate Charge	Q_g	$V_{DS} = -10 \text{ V}$, $I_{DS} = -330 \text{ mA}$, $V_{GS} = -4 \text{ V}$	—	1.2	—	nC
Gate-Source Charge	Q_{gs}		—	0.85	—	
Gate-Drain Charge	Q_{gd}		—	0.35	—	
Switching time	Turn-on time	$V_{DD} = -10 \text{ V}$, $I_D = -100 \text{ mA}$ $V_{GS} = 0 \text{ to } -2.5 \text{ V}$, $R_G = 50 \Omega$	—	90	—	ns
	Turn-off time		—	200	—	
Drain-source forward voltage	V_{DSF}	$I_D = 330 \text{ mA}$, $V_{GS} = 0 \text{ V}$ (Note2)	—	0.88	1.2	V

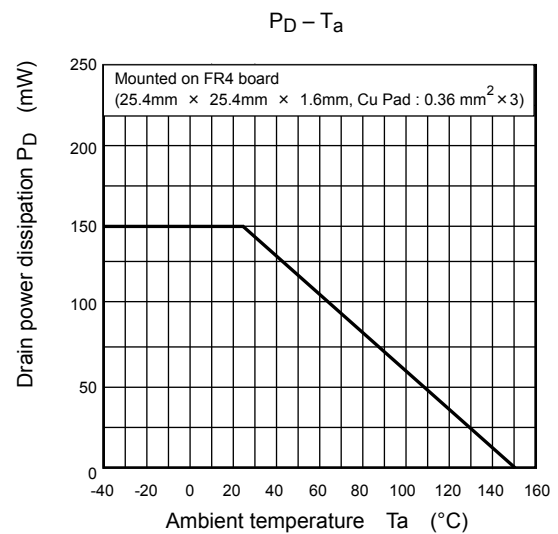
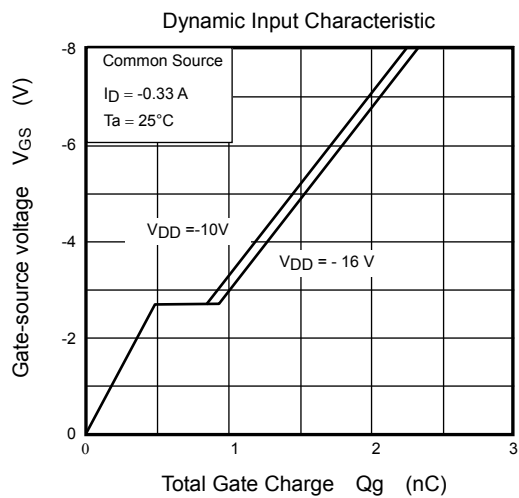
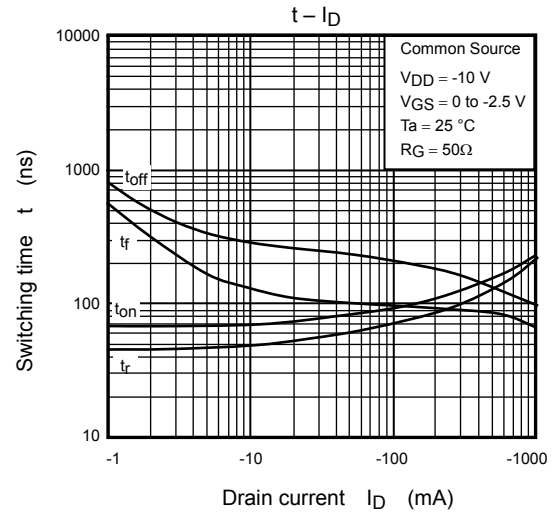
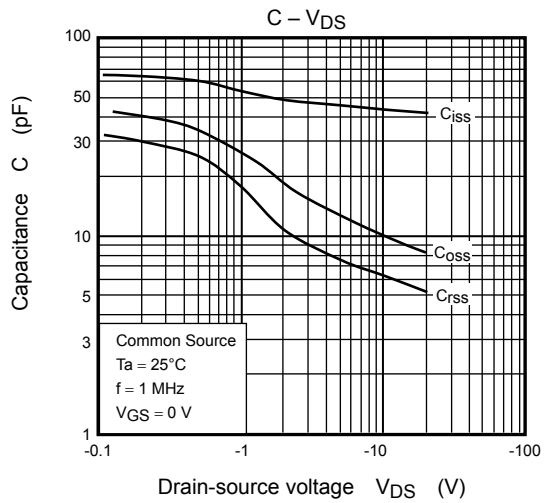
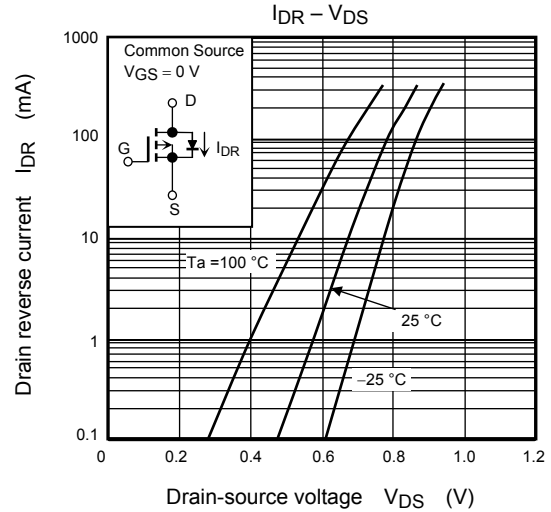
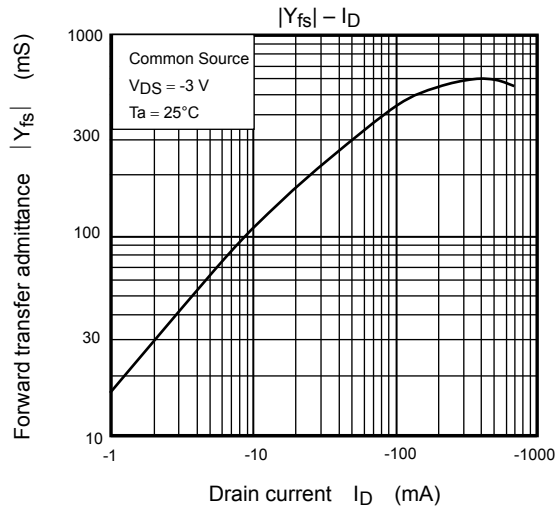
Note2: Pulse test

Switching Time Test Circuit
(a) Test circuit


$V_{DD} = -10 \text{ V}$
 Duty $\leq 1\%$
 V_{IN} : t_r , $t_f < 5 \text{ ns}$
 $(Z_{out} = 50 \Omega)$
 Common Source
 $T_a = 25^\circ\text{C}$

(b) V_{IN}

(c) V_{OUT}






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