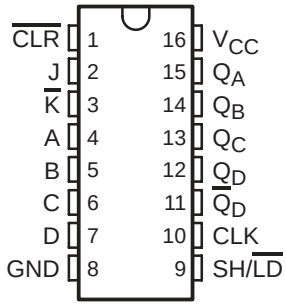
SDAS138B − DECEMBER 1983 − REVISED JANUARY 1995

- **Parallel-to-Serial, Serial-to-Parallel Conversions**
- **Parallel Synchronous Loading**
- **J and $\overline{K}$ Inputs to First Stage**
- **Right Shift Only With Complementary Outputs on Last Stage**
- **Direct Overriding Clear**
- **Package Options Include Plastic Small-Outline (D) Packages and Standard Plastic (N) 300-mil DIPs**

D OR N PACKAGE
(TOP VIEW)



description

This 4-bit bidirectional universal shift register features parallel (A, B, C, D) inputs, parallel (Q_A, Q_B, Q_C, Q_D, $\overline{Q}_D$) outputs, J-$\overline{K}$ serial (J, $\overline{K}$) inputs, shift/load control (SH/$\overline{LD}$) input, and a direct overriding clear ($\overline{CLR}$). The registers have two modes of operation:

- Parallel (broadside) load
- Shift (in the direction Q_A toward Q_D)

Parallel loading is accomplished by applying the four bits of data and taking SH/$\overline{LD}$ low. The data is loaded into the associated flip-flops and appears at the outputs after the positive transition of the clock (CLK) input. During loading, serial data flow is inhibited.

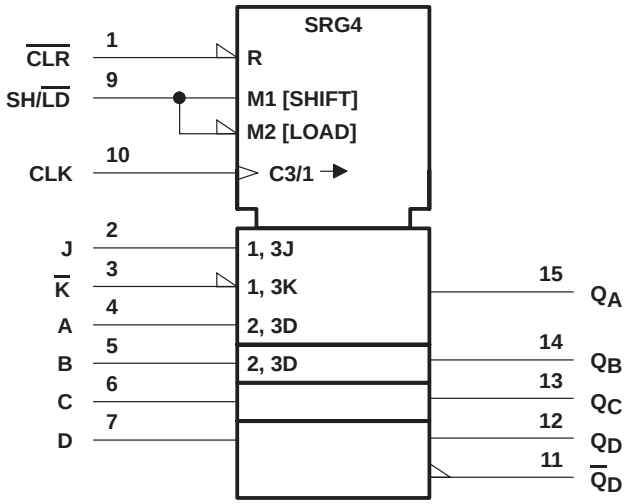
Shifting is accomplished synchronously when SH/$\overline{LD}$ is high. Serial data for this mode is entered at the J-$\overline{K}$ inputs. These inputs permit the first stage to perform as a J-$\overline{K}$, D-, or T-type flip-flop as shown in the function table.

The SN74AS195 is characterized for operation from 0°C to 70°C.

FUNCTION TABLE

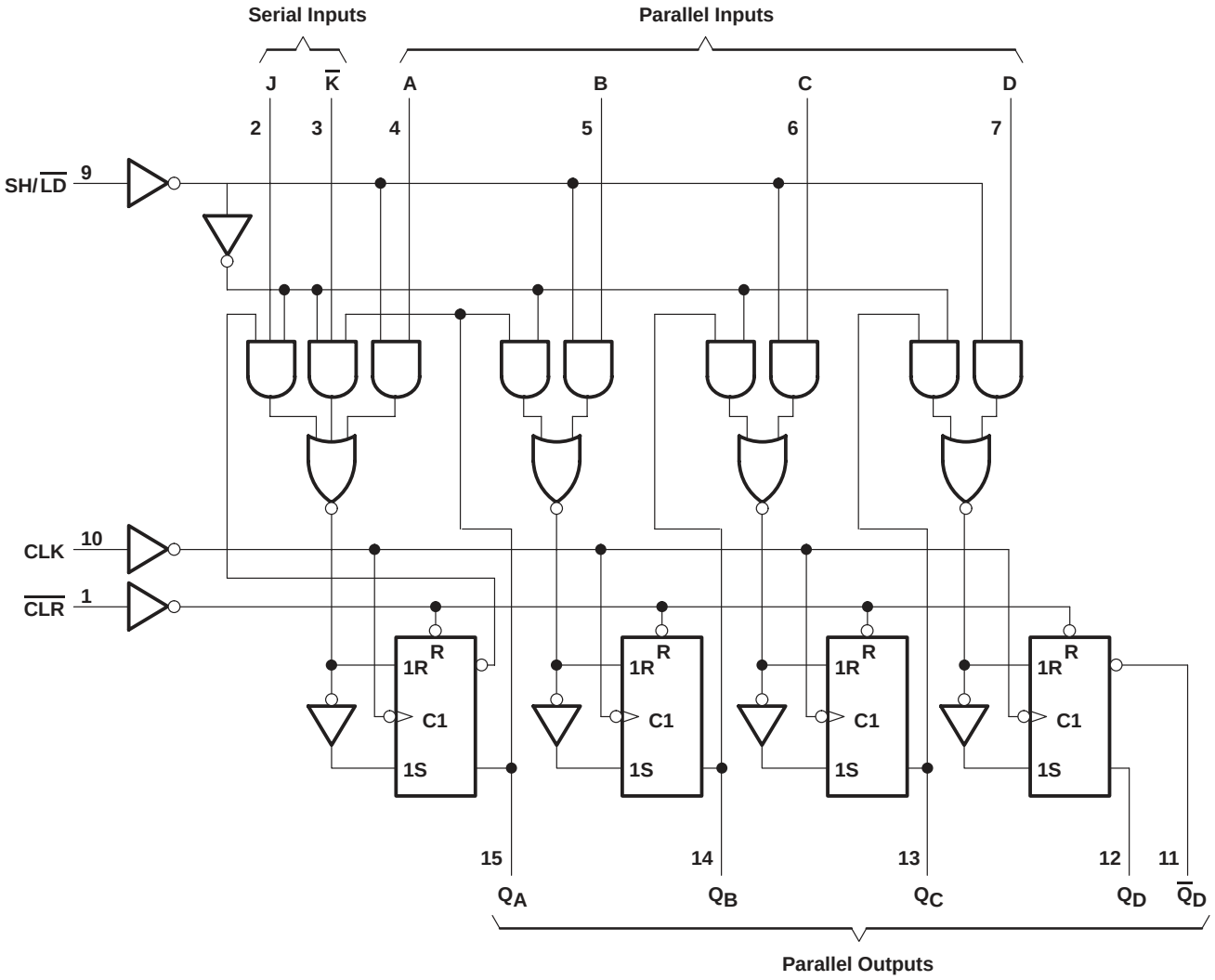
INPUTS									OUTPUTS				
			SERIAL		PARALLEL								
$\overline{CLR}$	SH/$\overline{LD}$	CLK	J	$\overline{K}$	A	B	C	D	Q_A	Q_B	Q_C	Q_D	$\overline{Q}_D$
L	X	X	X	X	X	X	X	X	L	L	L	L	H
H	L	↑	X	X	a	b	c	d	a	b	c	d	$\overline{d}$
H	H	L	X	X	X	X	X	X	Q_{A0}	Q_{B0}	Q_{C0}	Q_{D0}	$\overline{Q}_{D0}$
H	H	↑	L	H	X	X	X	X	Q_{A0}	Q_{A0}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$
H	H	↑	L	L	X	X	X	X	L	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$
H	H	↑	H	H	X	X	X	X	H	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$
H	H	↑	H	L	X	X	X	X	$\overline{Q}_{AN}$	Q_{An}	Q_{Bn}	Q_{Cn}	$\overline{Q}_{Cn}$

logic symbol†



† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

logic diagram (positive logic)



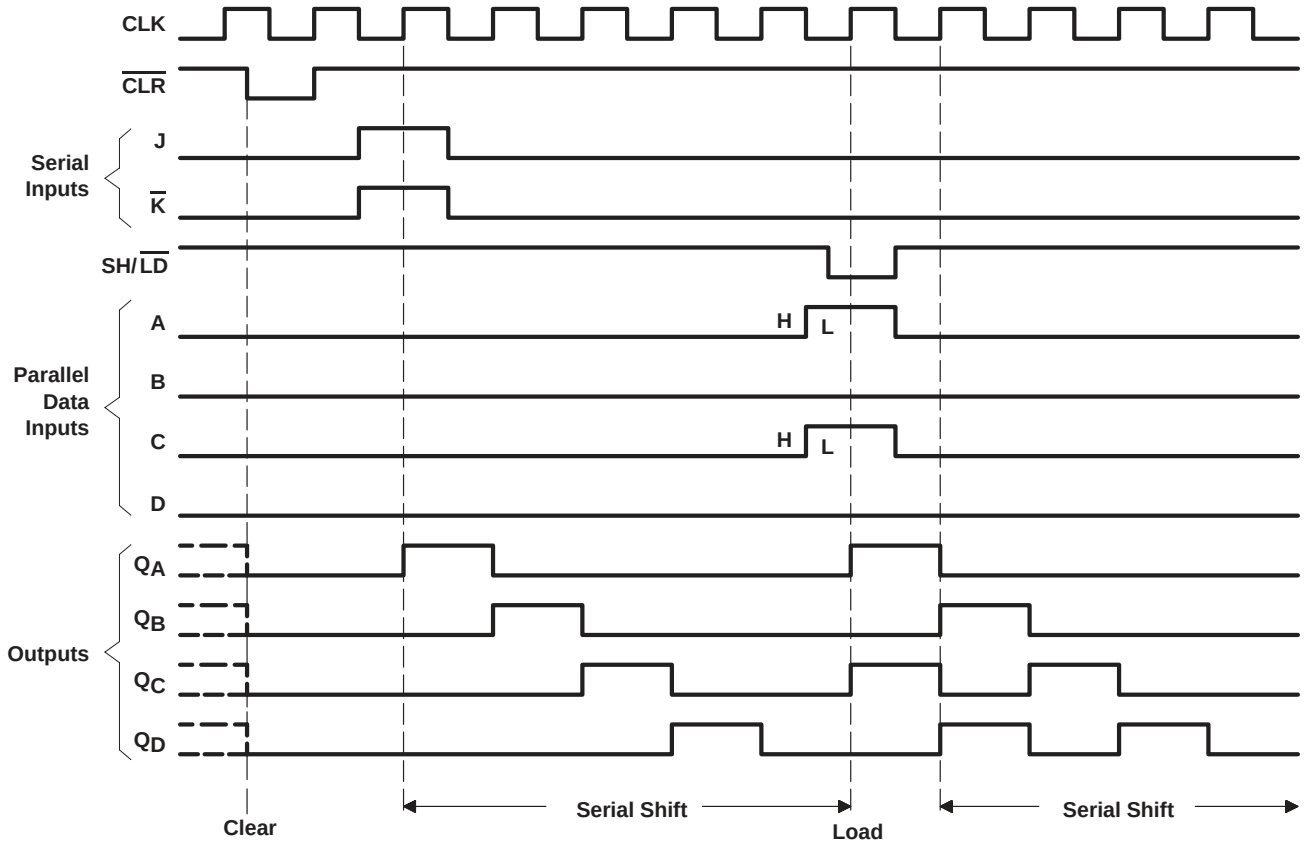


Figure 1. Typical Clear, Shift, and Load Sequences

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage, V_{CC} . . . . . 7 V
Input voltage, V_I . . . . . 7 V
Operating free-air temperature range, T_A . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

recommended operating conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	V
V_{IH}	High-level input voltage		2			V
V_{IL}	Low-level input voltage				0.8	V
I_{OH}	High-level output current				−2	mA
I_{OL}	Low-level output current				20	mA
f_{clock}	Clock frequency		0		70	MHz
t_w	Pulse duration	CLK high	4			ns
		$\overline{CLR}$ low	7.2			
t_{su}	Setup time	Data before CLK↑	3.5			ns
		SH/$\overline{LD}$ before CLK↑	8			
		$\overline{CLR}$ high before CLK↑	6			
t_h	Hold time	Data after CLK↑	1			ns
		SH/$\overline{LD}$ after CLK↑	0			
T_A	Operating free-air temperature		0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP†	MAX	UNIT
V_{IK}		V_{CC} = 4.5 V,	I_I = −18 mA			−1.2	V
V_{OH}		V_{CC} = 4.5 V to 5.5 V,	I_{OH} = −2 mA	V_{CC}−2			V
V_{OL}		V_{CC} = 4.5 V,	I_{OL} = 20 mA		0.35	0.5	V
I_I	SH/$\overline{LD}$	V_{CC} = 5.5 V,	V_I = 7 V			0.2	mA
	All others					0.1	
I_{IH}	SH/$\overline{LD}$	V_{CC} = 5.5 V,	V_I = 2.7 V			40	µA
	All others					20	
I_{IL}	SH/$\overline{LD}$	V_{CC} = 5.5 V,	V_I = 0.4 V			−1	mA
	All others					−0.5	
I_O‡		V_{CC} = 5.5 V,	V_O = 2.25 V	−30		−112	mA
I_{CCH}		V_{CC} = 5.5 V			32	51	mA
I_{CCL}		V_{CC} = 5.5 V			36	57	mA

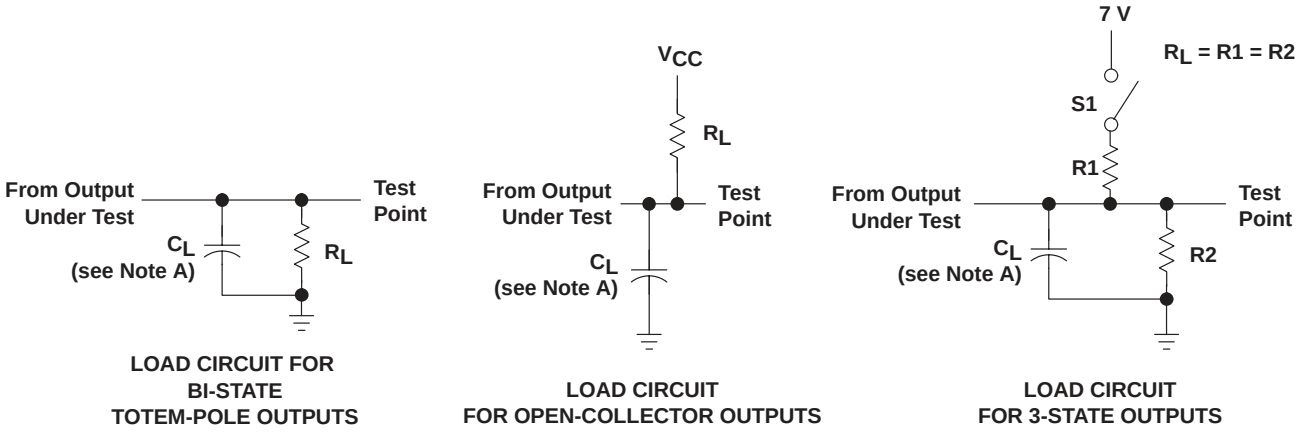
† All typical values are at V_{CC} = 5 V, T_A = 25°C.
‡ The output conditions have been chosen to produce a current that closely approximates one half of the true short-circuit output current, I_{OS}.

switching characteristics (see Figure 2)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 4.5 V to 5.5 V, C_L = 50 pF, R_L = 500 Ω, T_A = MIN to MAX†		UNIT
			MIN	MAX	
f_{max}			70		MHz
t_{PLH}	CLK	Any Q	3	8.5	ns
t_{PHL}			2.5	10.5	
t_{PLH}	$\overline{CLR}$	$\overline{Q}_D$	4	8	ns
t_{PHL}		Q_A thru Q_D	5	11.5	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

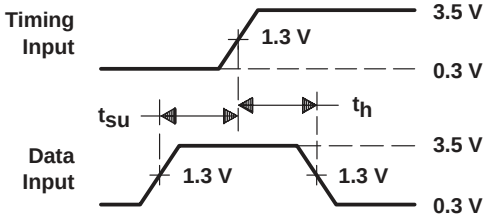
PARAMETER MEASUREMENT INFORMATION
SERIES 54ALS/74ALS AND 54AS/74AS DEVICES



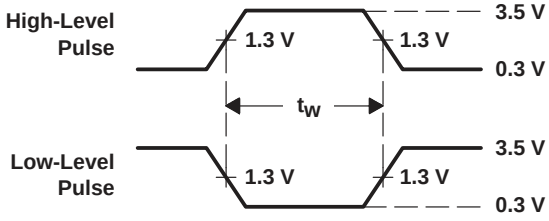
LOAD CIRCUIT FOR BI-STATE TOTEM-POLE OUTPUTS

LOAD CIRCUIT FOR OPEN-COLLECTOR OUTPUTS

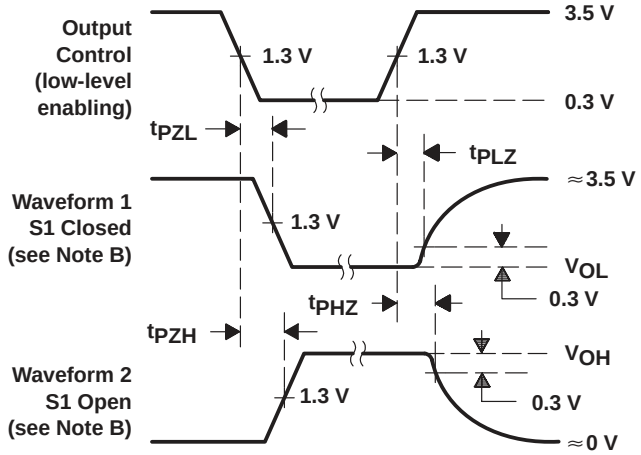
LOAD CIRCUIT FOR 3-STATE OUTPUTS



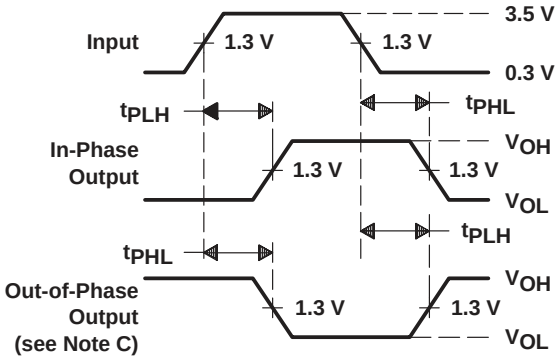
VOLTAGE WAVEFORMS SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS PULSE DURATIONS



VOLTAGE WAVEFORMS ENABLE AND DISABLE TIMES, 3-STATE OUTPUTS



VOLTAGE WAVEFORMS PROPAGATION DELAY TIMES

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. When measuring propagation delay items of 3-state outputs, switch S1 is open.
D. All input pulses have the following characteristics: PRR ≤ 1 MHz, $t_r = t_f$ = 2 ns, duty cycle = 50%.
E. The outputs are measured one at a time with one transition per measurement.

Figure 2. Load Circuits and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
SN74AS195N	OBSOLETE	PDIP	N	16		TBD	Call TI	Call TI

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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