

NTE3087 Optoisolator High Speed, Open Collector, NAND Gate Output

Description:

The NTE3087 is an optoisolator which combines a GaAsP LED as the emitter and an integrated high gain multi-stage high speed photodetector. The output of the detector circuit is an open collector, Schottky clamped transistor capable of sinking 50mA. The open collector output provides capability for bussing, ORing and strobing. The NTE3087 is packaged in a plastic 8-pin mini-DIP.

Features:

- LSTTL/TTL Compatible: 5V Supply
- Ultra High Speed
- Guaranteed Performance Over Temperature
- High Isolation Voltage: 2500V_{rms}

Absolute Maximum Ratings: (T_A = 0°C to +70°C unless otherwise specified)

Input Forward Current (Note 2), I _F	20mA
Pulse Forward Current (Note 3), I _{FP}	40mA
Reverse Voltage, V _R	5V
Output Current, I _O	50mA
Output Voltage, V _O	7V
Supply Voltage (1 minute max), V _{CC}	7V
Enable Input Voltage (Not to Exceed V _{CC} by More than 500mV) , V _{EH}	5.5V
Output Collector Power Dissipation, P _O	85mW
Operating Temperature Range, T _{opr}	0° to +70°C
Storage Temperature Range, T _{stg}	-55° to +125°C
Isolation Voltage (Note 3), BV _s	2500V _{rms}

Note 1. Device considered a two-terminal device: Pin1, 2, 3, and 4 are shorted together, and Pin5, 6, 7, and 8 are shorted together.

Note 2. 50% Duty Cycle, 1ms Pulse Width.

Note 3. R.H. = 40 to 60%, AC/1min.

Recommended Operating Conditions:

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Input Current, Low Level (Each Channel)	I _{FL}		0	–	250	μA
Input Current, High Level (Each Channel)	I _{FH}		6.3	–	15.0	mA
Enable Voltage, Low Level (Output High)	V _{EL}		0	–	0.8	V
Enable Voltage, High Level	V _{EH}		2.0	–	V _{CC}	V
Operating Temperature	T _A		0	–	70	°C
Fan Out (TTL Load)	N		–	–	8	

Electrical Characteristics: ($T_A = 0^\circ\text{C}$ to $+70^\circ\text{C}$, Note 4 unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
High Level Output Current	I_{OH}	$V_{CC} = 5.5\text{V}$, $V_O = 5.5\text{V}$, $I_F = 250\mu\text{A}$, $V_E = 2\text{V}$	–	1	250	μA
Low Level Output Voltage	V_{OL}	$V_{CC} = 5.5\text{V}$, $I_F = 5\text{mA}$, $V_{EH} = 2\text{V}$, $I_{OL} = 13\text{mA}$	–	0.4	0.6	V
High Level Enable Current	I_{EH}	$V_{CC} = 5.5\text{V}$, $V_E = 2.0\text{V}$	–	–1.0	–	mA
Low Level Enable Current	I_{EL}	$V_{CC} = 5.5\text{V}$, $V_E = 0.5\text{V}$	–	–1.6	–2.0	mA
High Level Supply Current	I_{CCH}	$V_{CC} = 5.5\text{V}$, $I_F = 0$, $V_E = 0.5\text{V}$	–	7	14	mA
Low Level Supply Current	I_{CCL}	$V_{CC} = 5.5\text{V}$, $I_F = 10\text{mA}$, $V_E = 0.5\text{V}$	–	12	18	mA
Resistance (Input-to-Output)	R_{I-O}	$V_{I-O} = 500\text{V}$, $T_A = +25^\circ\text{C}$	–	10^{12}	–	Ω
Capacitance (Input-to-Output)	C_{I-O}	$f = 1\text{MHz}$, $T_A = +25^\circ\text{C}$	–	0.6	–	pF
Input Forward Voltage	V_F	$I_F = 10\text{mA}$, $T_A = +25^\circ\text{C}$	–	1.65	1.9	V
Input Reverse Breakdown Voltage	$V_{(BR)R}$	$I_R = 10\mu\text{A}$, $T_A = +25^\circ\text{C}$	5.0	–	–	V
Input Capacitance	C_{IN}	$V_F = 0$, $f = 1\text{MHz}$	–	30	–	pF
Current Transfer Ratio	CTR	$I_F = 5\text{mA}$, $R_L = 10\Omega$	–	1000	–	%

Note 4. All typical values at $V_{CC} = 5\text{V}$, $T_A = +25^\circ\text{C}$.

Switching Characteristics: ($T_A = +25^\circ\text{C}$, $V_{CC} = 5\text{V}$ unless otherwise specified)

Parameter	Symbol	Test Conditions	Min	Typ	Max	Unit
Propagation Delay Time to High level Output	t_{PLH}	$R_L = 350\Omega$, $C_L = 15\text{pF}$, $I_F = 7.5\text{mA}$	–	60	120	ns
Propagation Delay Time to Low level Output	t_{PLH}		–	60	120	ns
Output Rise-Fall Time (10% to 90%)	t_r, t_f	$R_L = 350\Omega$, $C_L = 15\text{pF}$, $I_F = 7.5\text{mA}$	–	30	–	ns
Propagation Delay Time of Enable from V_{EH} to V_{EL}	t_{ELH}	$R_L = 350\Omega$, $C_L = 15\text{pF}$, $I_F = 7.5\text{mA}$, $V_{EH} = 3\text{V}$, $V_{EL} = 0.5\text{V}$	–	25	–	ns
Propagation Delay Time of Enable from V_{EL} to V_{EH}	t_{EHL}		–	25	–	ns
Common Mode Transient Immunity at Logic High Output Level	CM_H	$V_{CM} = 10\text{V}$, $R_L = 350\Omega$, $V_{O(\min)} = 2\text{V}$, $I_F = 0\text{mA}$	–	150	–	$\text{V}/\mu\text{s}$
Common Mode Transient Immunity at Logic Low Output Level	CM_L	$V_{CM} = 10\text{V}$, $R_L = 350\Omega$, $V_{O(\max)} = 0.8\text{V}$, $I_F = 5\text{mA}$	–	–150	–	$\text{V}/\mu\text{s}$

Truth Table: (0.1 μF bypass capacitor must be connected between Pin8 and Pin5)

Input	Enable	Output
H	H	L
L	H	H
H	L	H
L	L	H

Pin Connection Diagram

