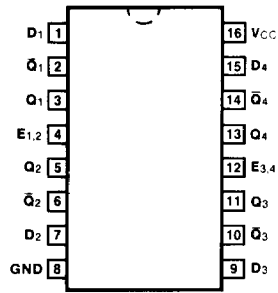


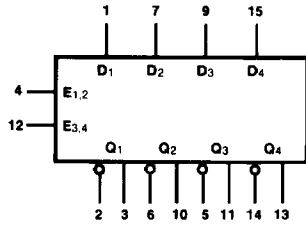
✓ **54LS/74LS375** 011139  
**4-BIT LATCH**

**CONNECTION DIAGRAM**  
**PINOUT A**



**DESCRIPTION** — The '375 is a 4-bit D-type latch for use as temporary storage for binary information between processing units and input/output or indicator units. When its Enable (E) input is HIGH, a latch is transparent, i.e., the Q output will follow the D input each time it changes. When E is LOW a latch stores the last valid data present on the D input preceding the HIGH-to-LOW transition of E. The '375 is functionally identical to the '75 except for the corner power pins.

**LOGIC SYMBOL**



VCC = Pin 16  
 GND = Pin 8

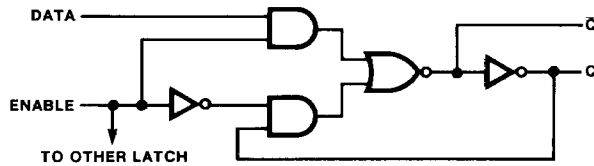
**ORDERING CODE:** See Section 9

PKGS	PIN OUT	COMMERCIAL GRADE	MILITARY GRADE	PKG TYPE
		VCC = +5.0 V ±5%, TA = 0°C to +70°C	VCC = +5.0 V ±10%, TA = -55°C to +125°C	
Plastic DIP (P)	A	74LS375PC		9B
Ceramic DIP (D)	A	74LS375DC	54LS375DM	6B
Flatpak (F)	A	74LS375FC	54LS375FM	4L

**INPUT LOADING/FAN-OUT:** See Section 3 for U.L. definitions

PIN NAMES	DESCRIPTION	54/74LS (U.L.) HIGH/LOW
D1 — D4	Data Inputs	0.5/0.25
E1,2	Latches 1, 2 Enable Input	2.0/1.0
E3,4	Latches 3, 4 Enable Input	2.0/1.0
Q1 — Q4	Latch Outputs	10/5.0 (2.5)
Q̄1 — Q̄4	Complementary Latch Outputs	10/5.0 (2.5)

**LOGIC DIAGRAM**  
(1/4 of diagram shown)



**TRUTH TABLE**  
(Each Latch)

$t_n$	$t_{n+1}$
D	Q
H	H
L	L

$t_n$  = Bit time before Enable negative going transition.  
 $t_{n+1}$  = Bit time after Enable negative going transition.  
 H = HIGH Voltage Level  
 L = LOW Voltage Level

**DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE** (unless otherwise specified)

SYMBOL	PARAMETER	54/74LS		UNITS	CONDITIONS
		Min	Max		
$I_{CC}$	Power Supply Current		12	mA	$V_{CC} = \text{Max}$

**AC CHARACTERISTICS:**  $V_{CC} = +5.0 \text{ V}$ ,  $T_A = +25^\circ \text{C}$  (See Section 3 for waveforms and load configurations)

SYMBOL	PARAMETER	54/74LS		UNITS	CONDITIONS
		$C_L = 15 \text{ pF}$			
		Min	Max		
$t_{PLH}$ $t_{PHL}$	Propagation Delay $D_n$ to $Q_n$		27 17	ns	Figs. 3-1, 3-5
$t_{PLH}$ $t_{PHL}$	Propagation Delay $D_n$ to $\bar{Q}_n$		20 15	ns	Figs. 3-1, 3-4
$t_{PLH}$ $t_{PHL}$	Propagation Delay $E_n$ to $Q_n$		27 25	ns	Figs. 3-1, 3-8
$t_{PLH}$ $t_{PHL}$	Propagation Delay $E_n$ to $\bar{Q}_n$		30 15	ns	

**AC OPERATING REQUIREMENTS:**  $V_{CC} = +5.0 \text{ V}$ ,  $T_A = +25^\circ \text{C}$

SYMBOL	PARAMETER	54/74LS		UNITS	CONDITIONS
		Min	Max		
$t_s$ (H) $t_s$ (L)	Setup Time HIGH or LOW $D_n$ to $E_n$	20		ns	Fig. 3-14
$t_h$ (H) $t_h$ (L)	Hold Time HIGH or LOW $D_n$ to $E_n$	0		ns	
$t_w$ (H)	$E_n$ Pulse Width HIGH	20		ns	Fig. 3-8