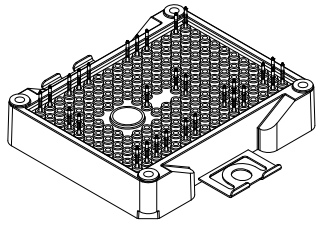
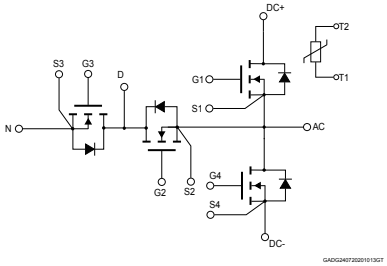
A2U12M12W2-F2

Datasheet

ACEPACK 2 power module, 3-level topology, 1200 V, 13 mΩ typ. SiC Power MOSFET gen.2 with NTC



ACEPACK 2



Features

- 3-level topology
- ACEPACK 2 power module
  - 13 mΩ of typical $R_{DS(on)}$ each switch
  - Insulation voltage UL certified of 2.5 kVrms
  - Integrated NTC temperature sensor
  - DBC Cu-Al_2O_3-Cu based
  - Press fit contact pins

Applications

- DC/DC converter

Description

This ACEPACK 2 power module represents a leg of a T-type 3-level inverter topology that integrates the advanced silicon carbide Power MOSFET technology from STMicroelectronics. This module leverages the innovative properties of the wide-bandgap SiC material and a high-thermal-performance substrate. The result is exceptionally low on-resistance per unit area and excellent switching performance that is virtually independent of temperature. An NTC sensor completes the design.

Product status link
A2U12M12W2-F2

Product summary	
Order code	A2U12M12W2-F2
Marking	A2U12M12W2-F2
Package	ACEPACK 2
Packing	Tray
Leads type	Press fit

1 Electrical rating

T_J = 25 °C unless otherwise specified.

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	1200	V
V_{GS}	Gate-source voltage	-10 to 22	V
	Gate-source voltage, recommended operating values	-5 to 18	
I_D	Drain current (continuous) at T_H = 25 °C	75	A
I_{DM}	Repetitive peak drain current	150	A
T_J	Maximum junction temperature	175	°C
	Operating junction temperature range under switching conditions	-40 to 150	

1. *Pulse width limited by maximum junction temperature.*

Table 2. Thermal data

Symbol	Parameter	Value	Unit
R_{thJH}	Thermal resistance, junction-to-heat sink (TIM = 120 µm, λ = 3 W•m^{-1}•°C^{-1})	0.78	°C/W

2 Electrical characteristics

Table 3. On/off-state

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V , I_D = 1 mA	1200			V
$R_{DS(on)}$	Static drain-source on-resistance	V_{GS} = 18 V , I_D = 75 A		13	17	mΩ
		V_{GS} = 18 V , I_D = 75 A, T_J = 150 °C		20		
$V_{GS(th)}$	Gate threshold voltage	I_D = 10 mA, V_{DS} = V_{GS}	1.9	3.0	4.9	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 1200 V, V_{GS} = 0 V			200	µA
I_{GSS}	Gate-body leakage current	V_{DS} = 0, V_{GS} = -10 to 22 V			±1	µA
C_{iss}	Input capacitance	f = 1 MHz, V_{DS} = 800 V, V_{GS} = 0 V		7000		pF
C_{oss}	Output capacitance			352		pF
C_{rss}	Reverse transfer capacitance			56		pF
R_G	Intrinsic gate resistance	f = 1 MHz, I_D = 0 A		1		Ω
Q_g	Total gate charge	V_{DS} = 450 V, V_{GS} = -5 to 18 V, I_D = 100 A		298		nC
Q_{gs}	Gate-source charge			97		nC
Q_{gd}	Gate-drain charge			108		nC

Table 4. Switching energy

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
E_{on}	Turn-on switching energy	V_{DS} = 450 V, I_D = 75 A, $R_{G(on)}$ = 5.6 Ω, $R_{G(off)}$ = 1 Ω, V_{GS} = -5 to 18 V	-	0.52	-	mJ
E_{off}	Turn-off switching energy		-	0.32	-	
E_{on}	Turn-on switching energy	V_{DS} = 450 V, I_D = 75 A, $R_{G(on)}$ = 5.6 Ω, $R_{G(off)}$ = 1 Ω, V_{GS} = -5 to 18 V, T_J = 150 °C	-	0.46	-	mJ
E_{off}	Turn-off switching energy		-	0.33	-	

Table 5. Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{SD}	Forward on voltage drop	V_{GS} = 0 V, I_{SD} = 75 A	-	2.9	-	V
E_{rr}	Reverse recovery energy	V_{DD} = 450 V, I_{SD} = 75 A, V_{GS} = -5 V	-	182	-	µJ
t_{rr}	Reverse recovery time		-	20	-	ns
Q_{rr}	Reverse recovery charge		-	546	-	nC
I_{RRM}	Reverse recovery current		-	46	-	A

2.1 Electrical characteristics (curves)

Figure 1. Typical output characteristics (T_J = -40 °C)

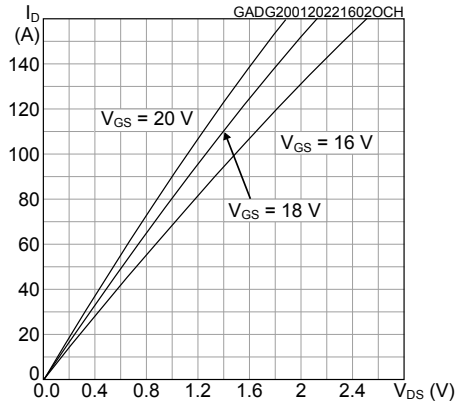


Figure 2. Typical output characteristics (T_J = 25 °C)

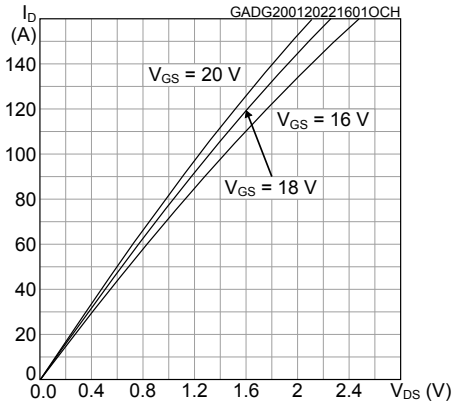


Figure 3. Typical output characteristics (T_J = 150 °C)

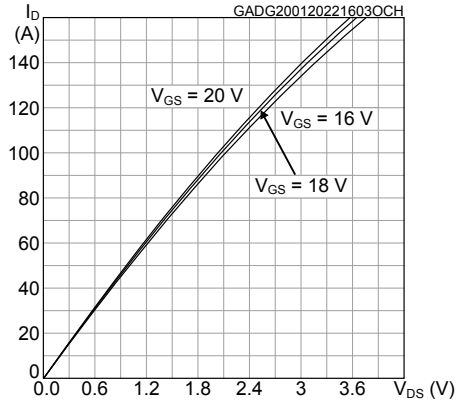


Figure 4. Typical transfer characteristics

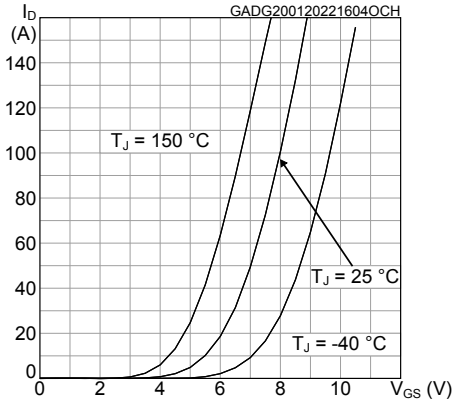


Figure 5. Typical diode foward charcteristics (terminal)

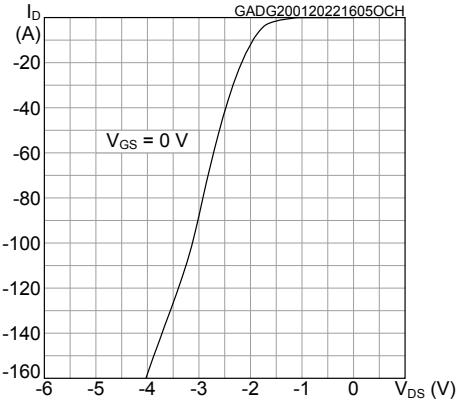


Figure 6. Typical gate charge characteristics

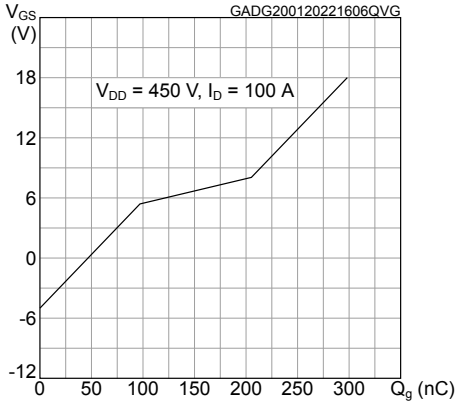


Figure 7. Typical switching energy vs drain current (T_J = 25 °C)

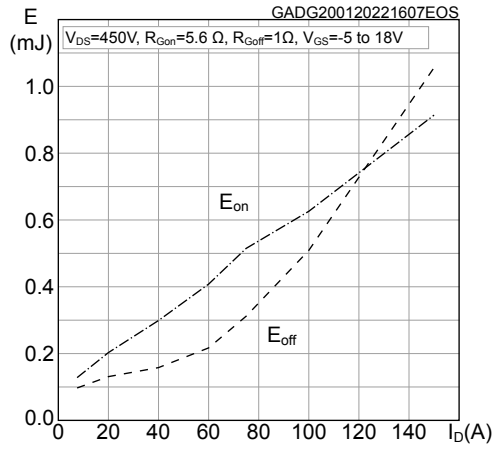


Figure 8. Typical switching energy vs drain current (T_J = 150 °C)

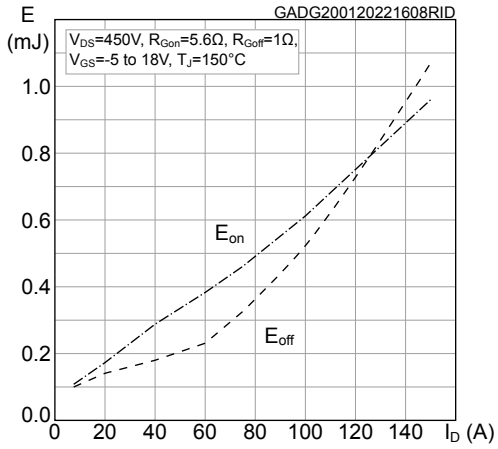


Figure 9. Typical switching energy vs gate resistance (T_J = 25 °C)

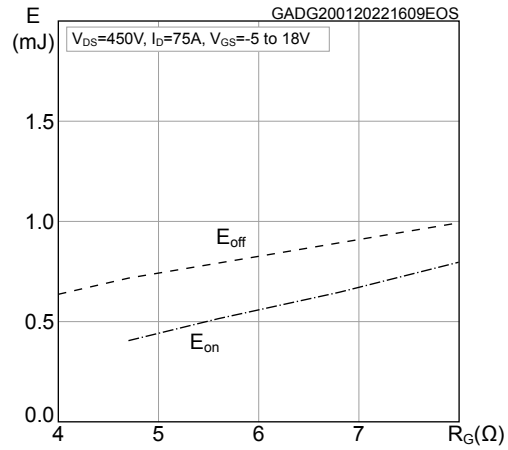


Figure 10. Typical switching energy vs gate resistance (T_J = 150 °C)

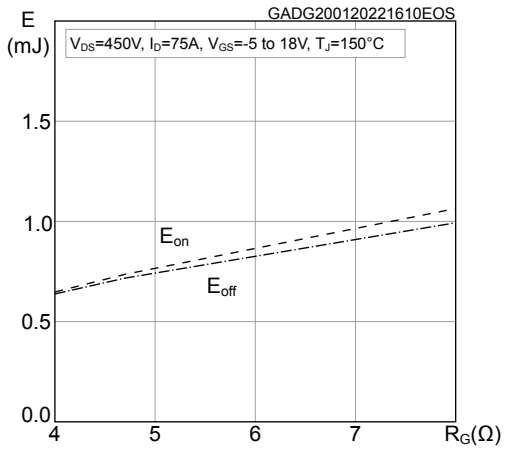


Figure 11. Typical switching energy vs temperature

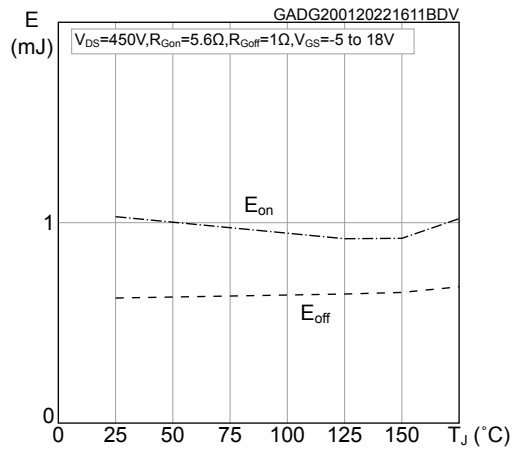


Figure 12. Typical switching energy vs V_{GS} (T_J = 25 °C)

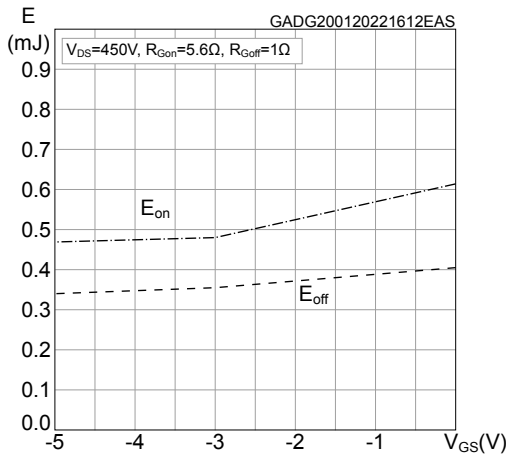


Figure 13. Typical switching energy vs V_{GS} (T_J = 150 °C)

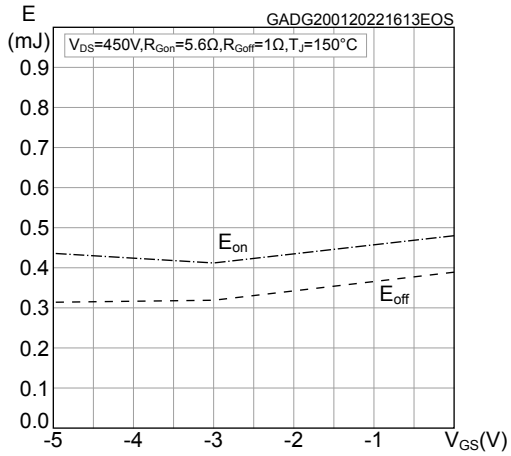
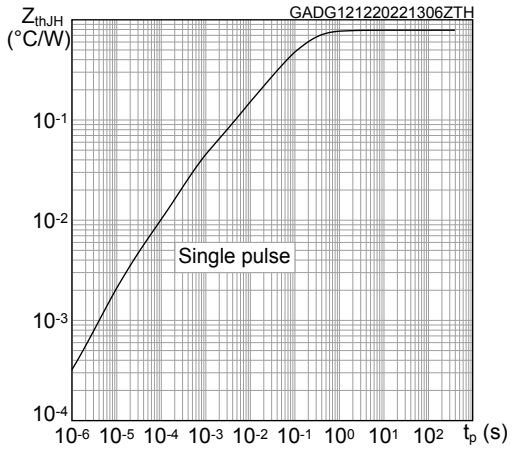


Figure 14. Maximum transient thermal impedance



3 NTC

Table 6. Absolute maximum ratings for NTC temperature sensor, considered as stand-alone

Symbol	Parameter	Test condition	Min.	Typ.	Max.	Unit
R_{25}	Resistance rating	T = 25 °C		5		kΩ
R_{100}	Resistance rating	T = 100 °C		493		Ω
$\Delta R_{100}/R$	Resistance tolerance		-5		5	%
B	B value	T = 25 to 50 °C		3375		K
		T = 25 to 85 °C		3411		
T	Operating temperature range		-40		150	°C

Figure 15. NTC typical resistance vs temperature

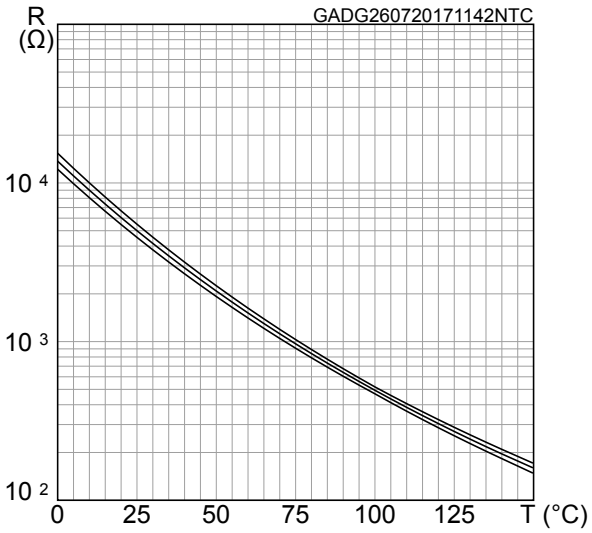
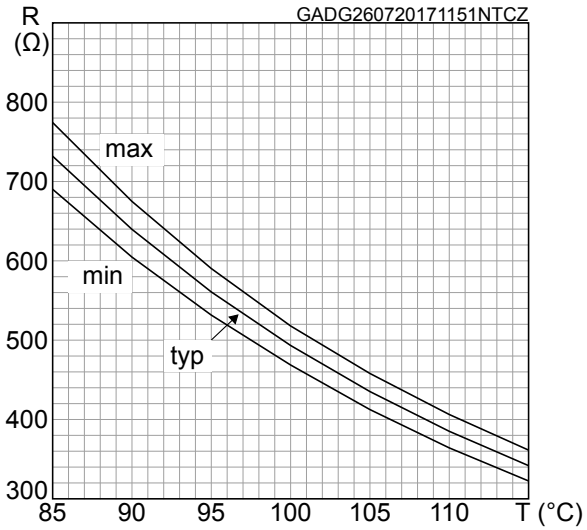


Figure 16. NTC resistance vs temperature, zoom



4 Package

Table 7. **ACEPACK 2 package**

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{ISO}	Isolation withstand voltage applied between each pin and heat sink plate (AC voltage, t = 60 s)	2.5			kVrms
M_d	Mounting torque (M4 screw)	2.0		2.3	N•m
CTI	Comparative tracking index	200			
L_s	Stray inductance module loop		10		nH
T_{stg}	Storage temperature range	-40		125	°C

5 Electrical topology and pin description

Figure 17. **Electrical topology and pin description**

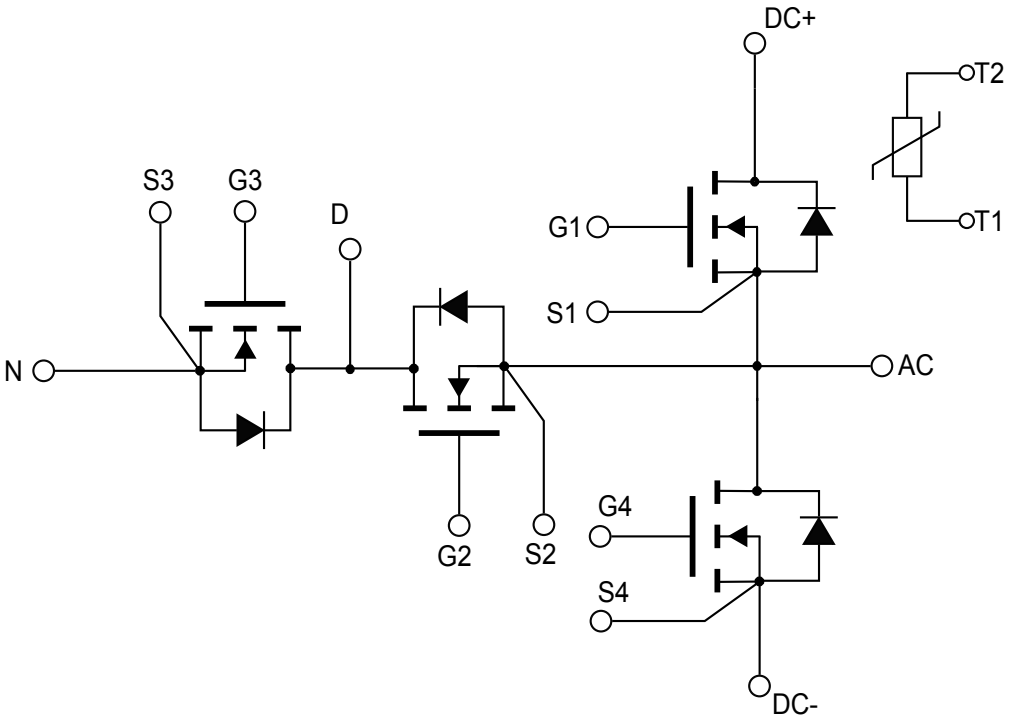


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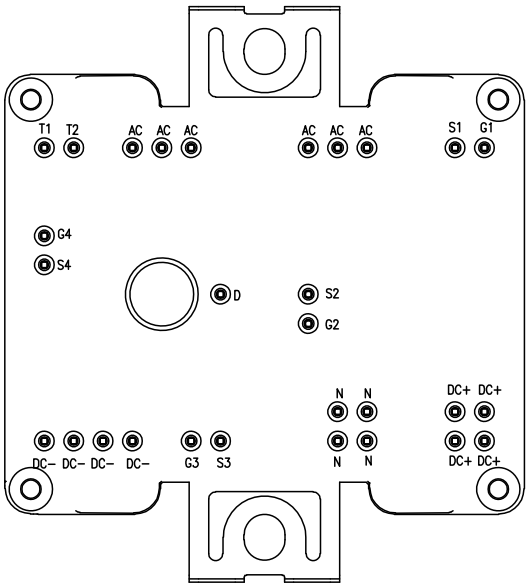
Figure 18. **Package top view with pinout**



6 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

6.1 ACEPACK 2 3-level T-type press fit package information

Figure 19. ACEPACK 2 3-level T-type press fit package outline (dimensions are in mm)

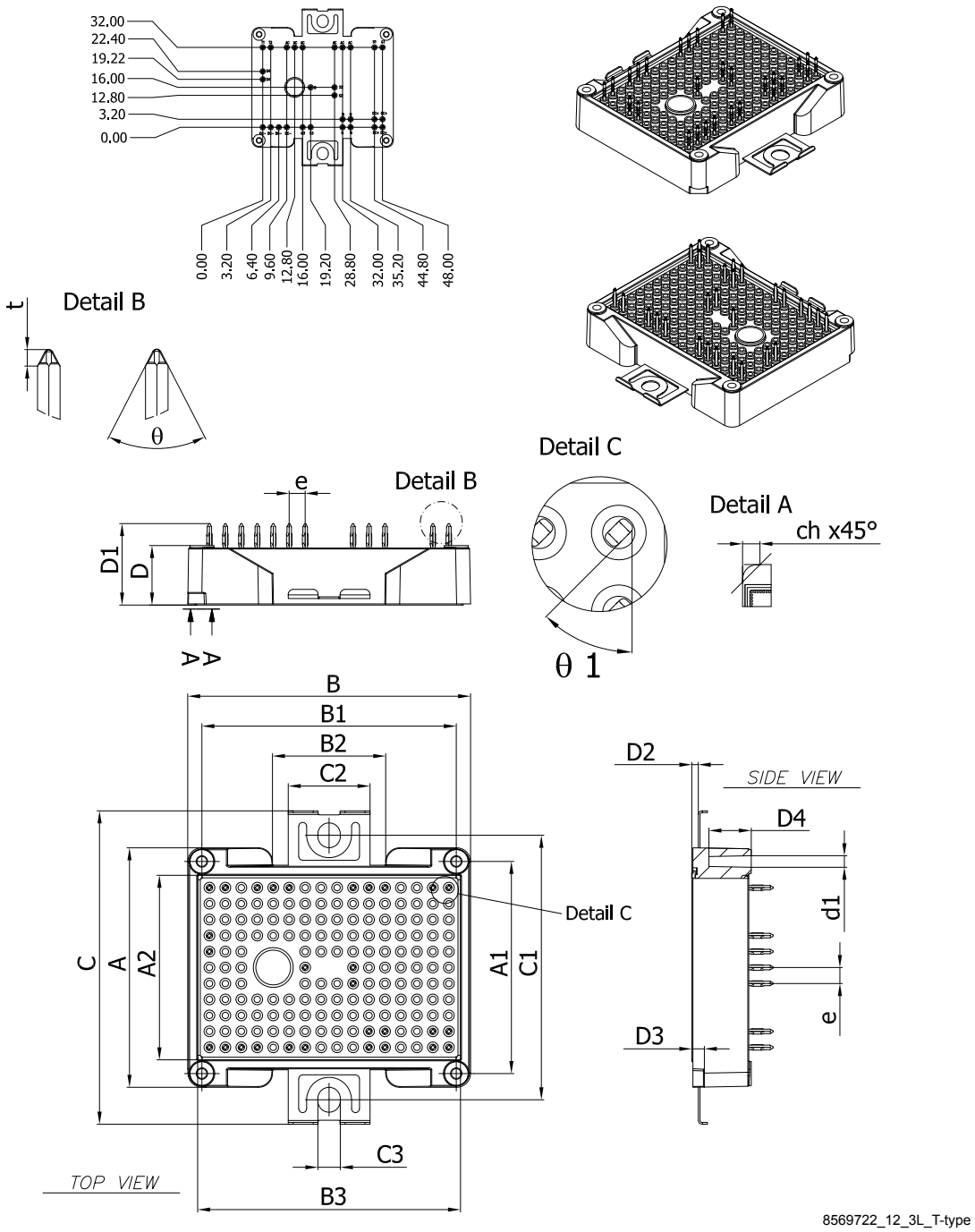
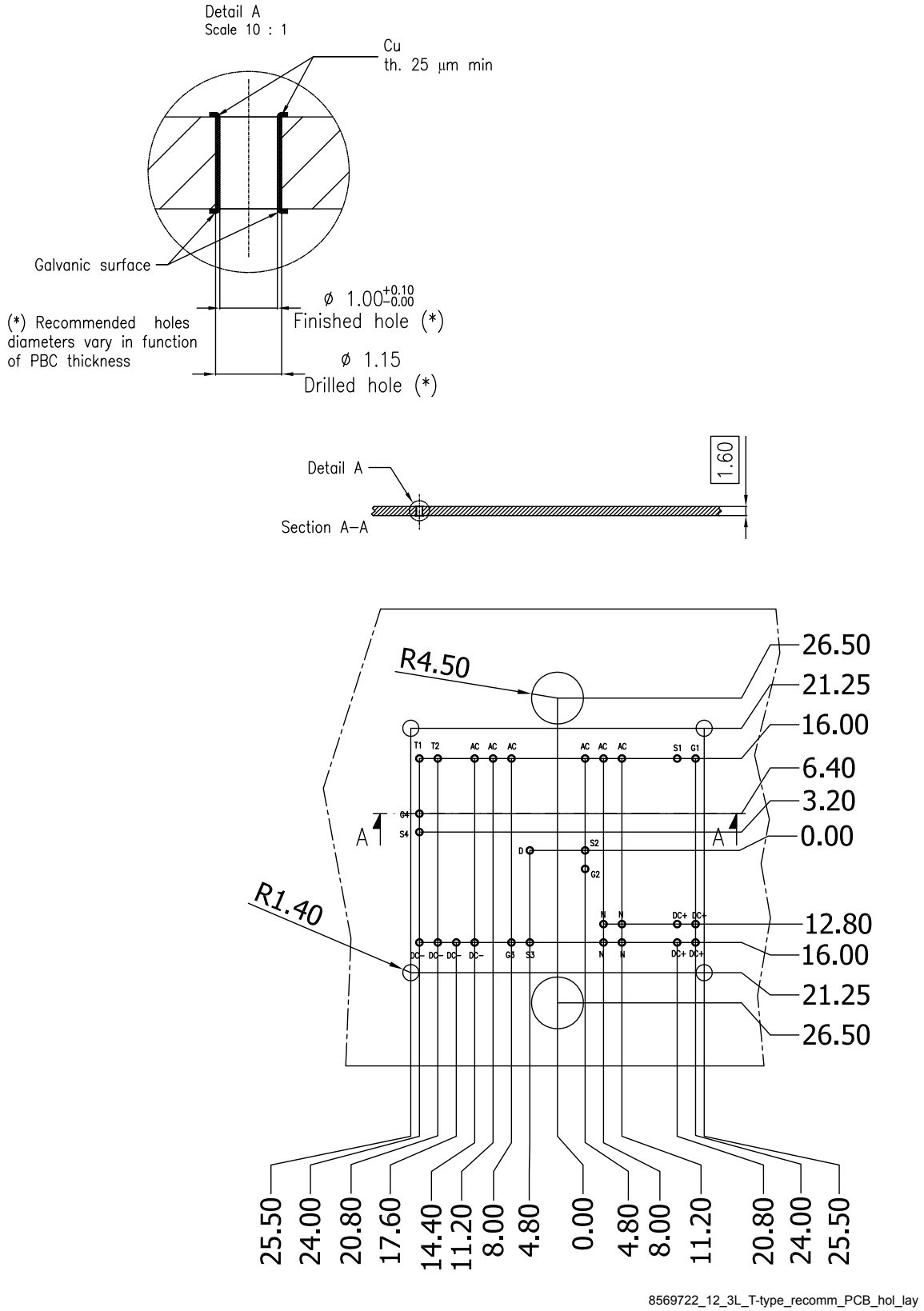


Table 8. ACEPACK 2 3-level T-type press fit mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	47.70	48.00	48.30
A1	42.30	42.50	42.70
A2		37.00 REF	
B	56.40	56.70	57.00
B1	50.85	51.00	51.15
B2	22.40	22.70	23.00
B3		52.70 REF	
C	62.30	62.80	63.30
C1	52.90	53.00	53.10
C2	16.20	16.40	16.60
C3	4.40	4.50	4.60
D	11.65	12.00	12.35
D1	15.90	16.40	16.90
D2	1.10	1.30	1.50
D3	2.30	2.50	2.70
D4			8.50
t	0.30	0.40	0.50
θ	52°	60°	68°
θ1		45°	
e		3.20 BSC	
d1		2.30 REF	
ch		3.50 REF	

Figure 20. ACEPACK 2 3-level T-type press fit recommended PCB holes layout (dimensions are in mm)



Revision history

Table 9. Document revision history

Date	Revision	Changes
14-Sep-2021	1	First release.
11-Feb-2022	2	Updated title, features and description in cover page. Updated *Table 2. Thermal data, Table 3. On/off-state,* and *Table 5. Source-drain diode.* Updated *Table 7. ACEPACK 2 package*. Updated *Section 2.1 Electrical characteristics (curves)*. Minor text changes.
16-Mar-2023	3	Modified Table 2. Thermal data. Modified Figure 14. Maximum transient thermal impedance.

Contents