ISOFACE™

ISO1H812G

Galvanic Isolated 8 Channel High-Side Switch

Datasheet

Revision 2.6, 2014-10-17

Power Management & Multimarket

Edition 2014-10-17

Published by
Infineon Technologies AG
81726 Munich, Germany

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Revision History	
Page or Item	**Subjects (major changes since previous revision)**
Revision 2.6, 2014-10-17	
Page 4	Feature list updated, Vbb Monitoring included
Page 7	Page 7 Chapter 2 Block diagram updated
Page 9	Page 9 Chapter 3.3.3 Description for repetitive short circuit corrected
Page 9	Page 9 Chapter 3.4 Vbb Monitoring included in common diagnostic output description
Page 16	Page 16 Chapter 4.5 Footnotes corrected
Page 18	Page 18 Chapter 4.8 Timing parameter for CS delay split into t_{CSD} and t_{CSDMD}
Page 19	Page 19 Chapter 4.10 Parameter Minimum Internal Gap removed
all	Correction of formats and typos
Revision 2.5	
Page 13	Page 13, Table 4.1 Extended operating temperature footnote removed
Revision 2.0	
all	Final Datasheet

Coreless Transformer Isolated Digital Output 8 Channel 0.625 A High-Side Switch

Product Highlights

- **Coreless transformer isolated data interface**
- **Galvanic isolation**
- **8 High-side output switches 0.625A**
- **µC compatible 8-bit serial peripheral**

Features

- Interface CMOS 3.3/5V operation compatible
- Serial Interface
- High common mode transient immunity
- Short circuit protection
- Maximum current internally limited
- Overload protection
- Overvoltage protection (including load dump)
- Undervoltage shutdown with autorestart and hysteresis
- Switching inductive loads
- Common output disable pin
- Thermal shutdown with restart
- Thermal independence of separate channels
- Common diagnostic output
- ESD protection
- Loss of GNDbb and loss of V_{bb} protection
- Very low standby current
- Reverse battery protection
- Isolated return path for $\overline{DIAG}$ signal
- V_{bb} monitoring
- UL508 compliant / RoHS compliant

Typical Application

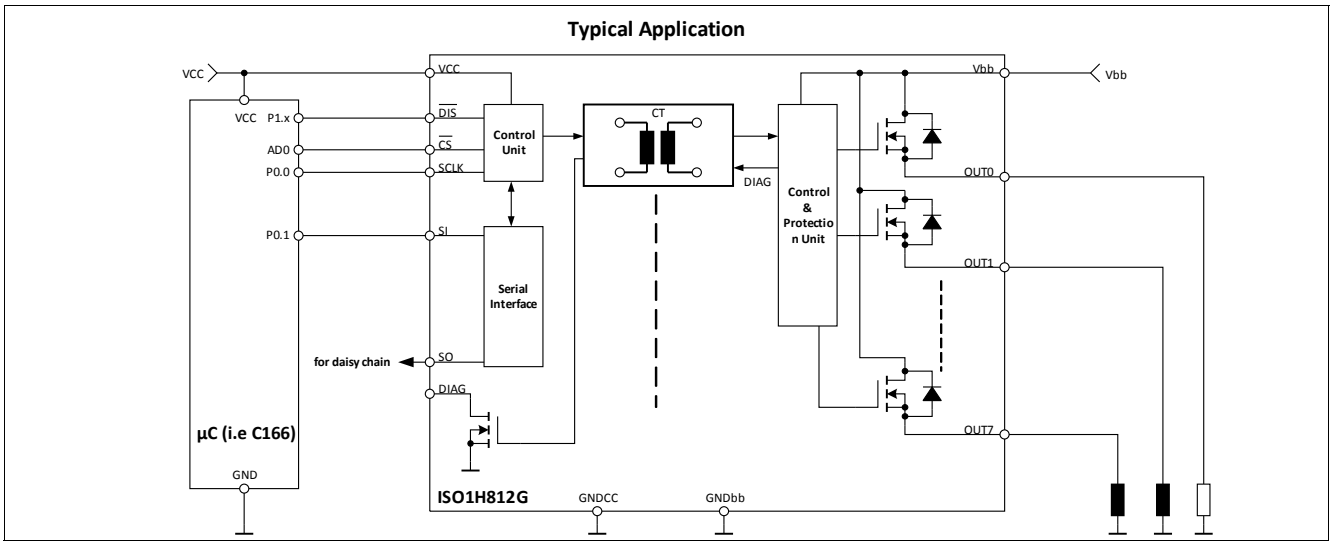
- Isolated switch for industrial applications (PLC)
- All types of resistive, inductive and capacitive loads
- µC compatible power switch for 24V DC applications
- Driver for solenoid, relays and resistive loads

Description

The ISO1H812G is a galvanically isolated 8 bit data interface in PG-DSO-36 package that provides 8 fully protected high-side power switches that are able to handle currents up to 625 mA.

A serial µC compatible interface allows to connect the IC directly to a µC system. The input interface is designed to operate with 3.3/5V CMOS compatible levels.

The data transfer from input to output side is realized by the integrated Coreless Transformer Technology.



Type		On-state Resistance	Package
ISO1H812G		200mΩ	PG-DSO36

1 Pin Configuration and Functionality

1.1 Pin Configuration

Pin	Symbol	Function
1	N.C.	Not connected
2	VCC	Positive 3.3/5V logic supply
3	$\overline{\text{DIS}}$	Output disable
4	$\overline{\text{CS}}$	Chip select
5	SCLK	Serial Clock
6	SI	Serial Data input
7	N.C.	Not connected
8	N.C.	Not connected
9	N.C.	Not connected
10	N.C.	Not connected
11	N.C.	Not connected
12	N.C.	Not connected
13	SO	Serial Data Output
14	$\overline{\text{DIAG}}$	Common diagnostic output
15	GNDCC	Input logic ground
16	N.C.	Not connected
17	N.C.	Not connected
18	N.C.	Not connected
19	GNDbb	Output driver ground
20	N.C	Not connected
21	OUT7	High-side output of channel 7
22	OUT7	High-side output of channel 7
23	OUT6	High-side output of channel 6
24	OUT6	High-side output of channel 6
25	OUT5	High-side output of channel 5
26	OUT5	High-side output of channel 5
27	OUT4	High-side output of channel 4
28	OUT4	High-side output of channel 4
29	OUT3	High-side output of channel 3
30	OUT3	High-side output of channel 3
31	OUT2	High-side output of channel 2
32	OUT2	High-side output of channel 2
33	OUT1	High-side output of channel 1
34	OUT1	High-side output of channel 1
35	OUT0	High-side output of channel 0
36	OUT0	High-side output of channel 0
TAB	Vbb	Positive driver power supply voltage

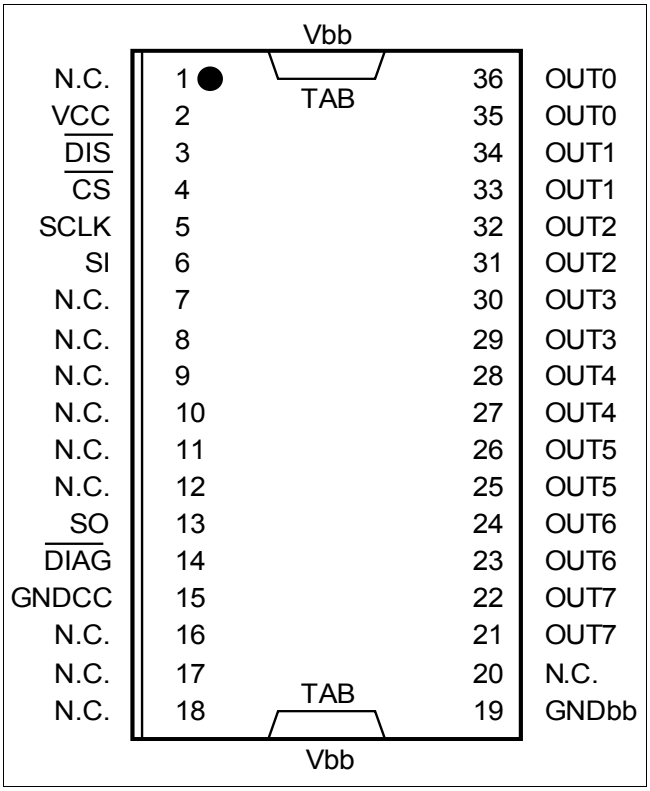


Figure 1 Power SO-36 (430mil)

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1.2 Pin Functionality

VCC (Positive 3.3/5V logic supply)

The VCC supplies the input interface that is galvanically isolated from the output driver stage. The input interface can be supplied with 3.3V / 5V.

$\overline{\text{DIS}}$ (Output disable)

The high-side outputs OUT0...OUT7 can be immediately switched off by means of the low active pin $\overline{\text{DIS}}$ that is an asynchronous signal. The input registers are also reset by the $\overline{\text{DIS}}$ signal. The output remains switched off after low-high transient of $\overline{\text{DIS}}$, till new data is written into the input interface. Current Sink to GNDCC

$\overline{\text{CS}}$ (Chip select)

The system microcontroller selects the ISO1H812G by means of the low active pin $\overline{\text{CS}}$ to activate the interface. Current Source to VCC

SCLK (Serial shift clock)

SCLK (serial clock) is used to synchronize the data transfer between the master and the ISO1H812G. Data present at the SI pin are latched on the rising edge of the serial clock input, while data at the SO pin is updated after the falling edge of SCLK.

Current Source to VCC

SI (Serial data input)

This pin is used to transfer data into the device. Data is latched on the rising edge of the serial clock.

Current Sink to GNDCC

SO (Serial data output)

SO can be connected to a serial input of a further IC to build a daisy-chain configuration. It is only actvated if $\overline{\text{CS}}$ is in low state, otherwise this output is in high impedance state.

$\overline{\text{DIAG}}$ (Common diagnostic output)

The low active $\overline{\text{DIAG}}$ signal contains the OR-wired information of the separated overtemperature detection units for each channel.The output pin $\overline{\text{DIAG}}$ provides an open drain functionality. A current source is also connected to the pin $\overline{\text{DIAG}}$. In normal operation the signal $\overline{\text{DIAG}}$ is high. When overtemperature or Vbb below ON-Limit is detected the signal $\overline{\text{DIAG}}$ changes to low.

GNDCC (Ground for VCC domain)

This pin acts as the ground reference for the input interface that is supplied by VCC.

GNDbb (Output driver ground domain)

This pin acts as the ground reference for the output driver that is supplied by Vbb.

OUT0 ... OUT7 (High side output channel 0 ... 7)

The output high side channels are internally connected to Vbb and controlled by the corresponding data input.

TAB (Vbb, Positive supply for output driver)

The heatslug is connected to the positive supply port of the output interface.

2 Blockdiagram

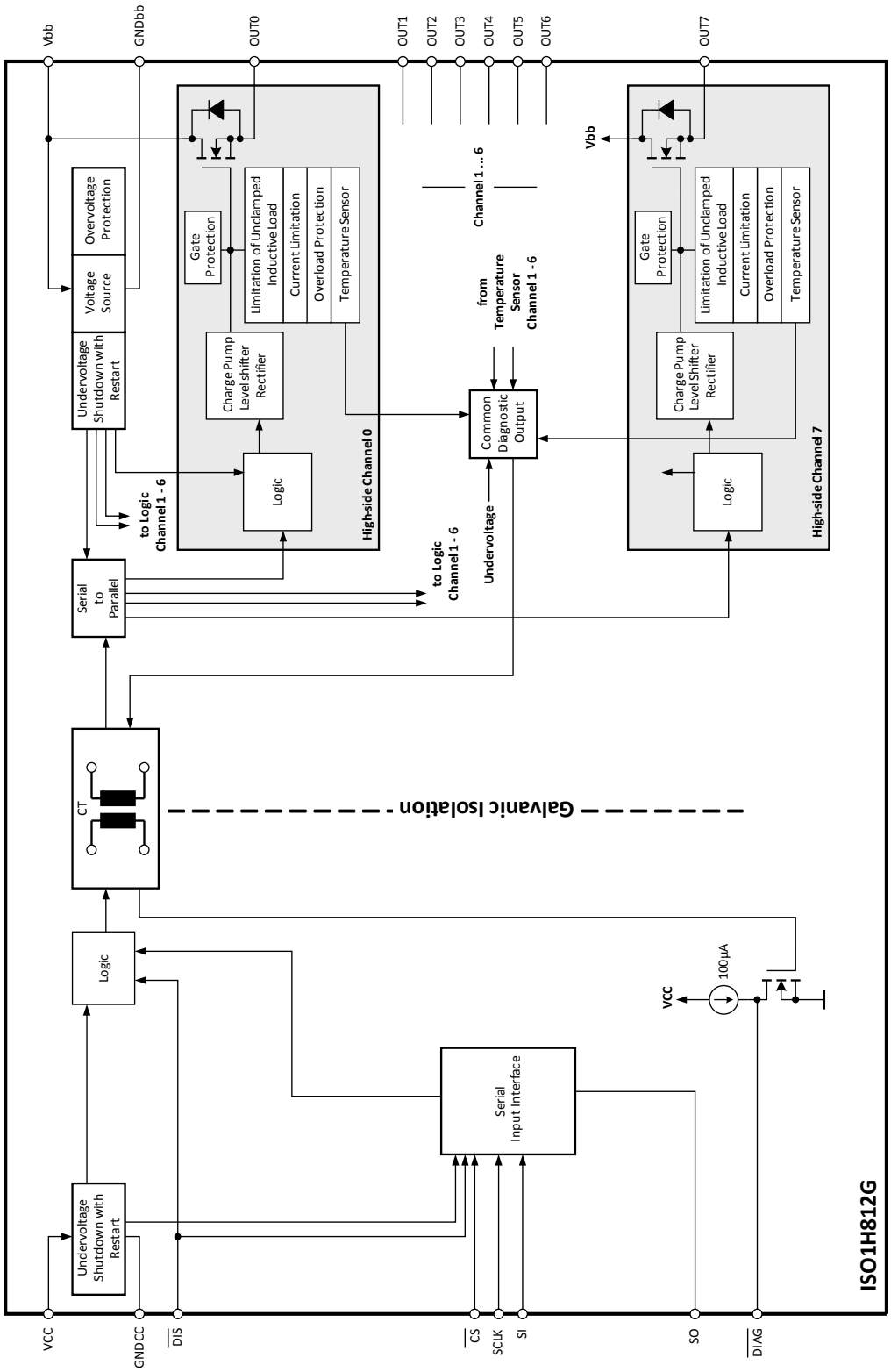


Figure 2 Blockdiagram

3 Functional Description

3.1 Introduction

The ISOface ISO1H812G includes 8 high-side power switches that are controlled by means of the integrated µC compatible SPI interface. The outputs OUT0...OUT7 are controlled by the data of the serial input SI. The IC can replace 8 optocouplers and the 8 high-side switches in conventional I/O-Applications as a galvanic isolation is implemented by means of the integrated coreless transformer technology. The µC compatible interface allows a direct connection to the ports of a microcontroller without the need for other components. Each of the 8 high-side power switches is protected against short to Vbb, overload, overtemperature and against overvoltage by an active zener clamp.

The diagnostic logic on the power chip recognizes the overtemperature information of each power transistor The information is send via the internal coreless transformer to the pin $\overline{DIAG}$ at the input interface.

3.2 Power Supply

The IC contains 2 galvanic isolated voltage domains that are independent from each other. The input interface is supplied at VCC and the output stage is supplied at Vbb. The different voltage domains can be switched on at different time. The output stage is only enabled once the input stage enters a stable state.

3.3 Output Stage

Each channel contains a high-side vertical power FET that is protected by embedded protection functions.

The continuous current for each channel is 625mA (all channels ON).

3.3.1 Output Stage Control

Each output is independently controlled by an output latch and a common reset line via the pin $\overline{DIS}$ that disables all eight outputs and resets the latches. Serial data input (SI) is read on the rising edge of the serial clock SCLK. A logic high input data bit turns the respective output channel ON, a logic low data bit turns it OFF. $\overline{CS}$ must be low whilst shifting all the serial data into the device. A low-to-high transition of $\overline{CS}$ transfers the serial data input bits to the output buffer.

3.3.2 Power Transistor Overvoltage Protection

Each of the eight output stages has its own zener clamp that causes a voltage limitation at the power transistor when solenoid loads are switched off. V_{ON} is then clamped to 47V (min.).

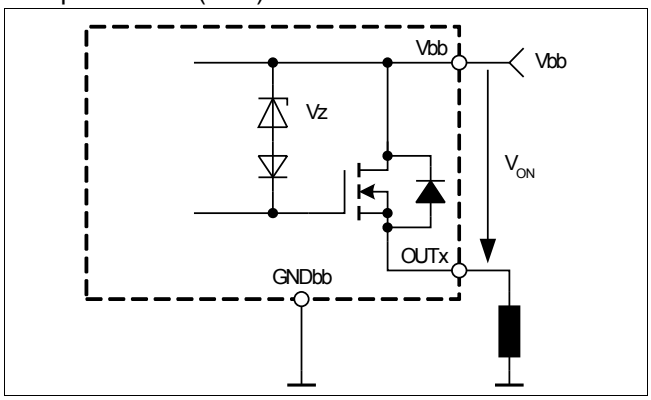


Figure 3 Inductive and overvoltage output clamp (each channel)

Energy is stored in the load inductance during an inductive load switch-off.

$$E_L = 1/2 \times L \times I_L^2$$

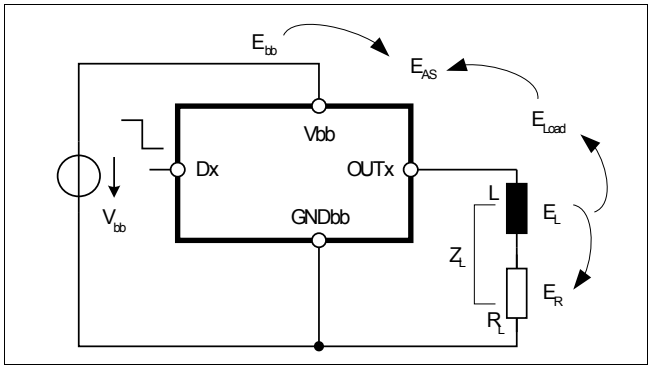


Figure 4 Inductive load switch-off energy dissipation (each channel)

While demagnetizing the load inductance, the energy dissipation in the DMOS is

$$E_{AS} = E_{bb} + E_L - E_R = V_{ON(CL)} \times i_L(t)dt$$

with an approximate solution for $R_L > 0\Omega$:

$$E_{AS} = \frac{I_L \times L}{2 \times R_L} \times (V_{bb} + |V_{ON(CL)}|) \times \ln\left(1 + \frac{I_L \times R_L}{|V_{ON(CL)}|}\right)$$

3.3.3 Power Transistor Overcurrent Protection

The outputs are provided with a current limitation that enters a repetitive switched mode after an initial peak current has been exceeded. The initial peak short circuit current limit is set to $I_{L(SCp)}$ at T_j = 125°C. During the repetitive short circuit the current limit is set to $I_{L(SCr)}$. If this operation leads to an overtemperature condition, a second protection level (T_j > 135°C) will change the output into a low duty cycle PWM (selective thermal shutdown with restart) to prevent critical chip temperatures.

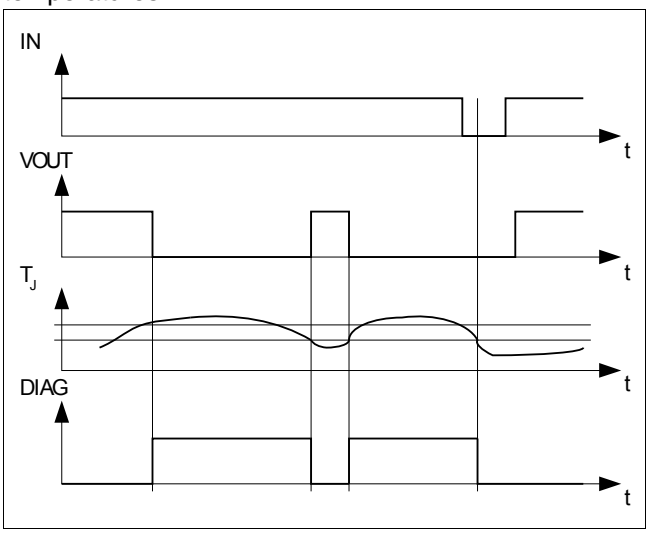


Figure 5 Overtemperature detection

The following figures show the timing for a turn on into short circuit and a short circuit in on-state. Heating up of the chip may require several milliseconds, depending on external conditions.

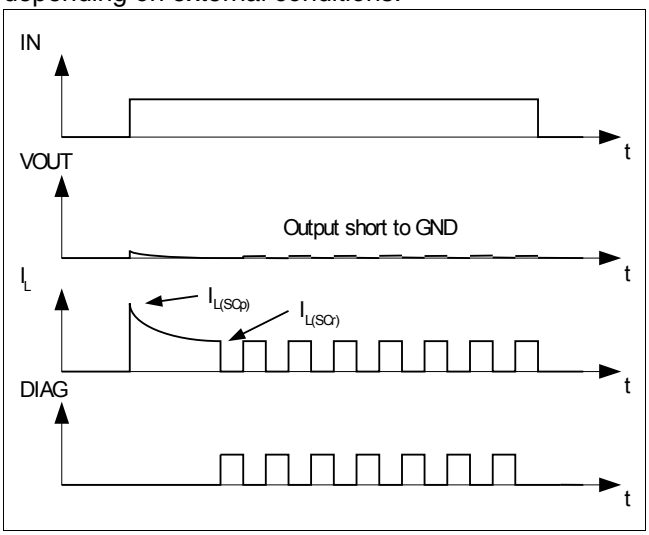


Figure 6 Turn on into short circuit, shut down by overtemperature, restart by cooling

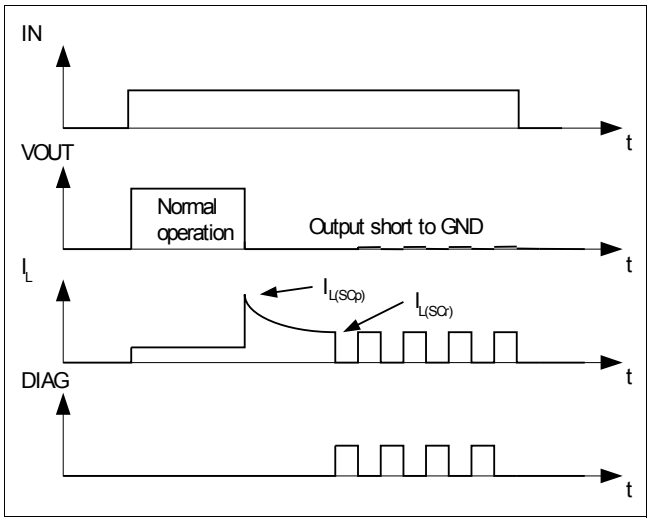


Figure 7 Short circuit in on-state, shut down down by overtemperature, restart by cooling

3.4 Common Diagnostic Output

The overtemperature detection information are OR-wired in the common diagnostic output block. The information is send via the integrated coreless transformer to the input interface. In addition Vbb undervoltage is indicated at the $\overline{\text{DIAG}}$ output.

The output stage at pin $\overline{\text{DIAG}}$ has an open drain functionality combined with a current source.

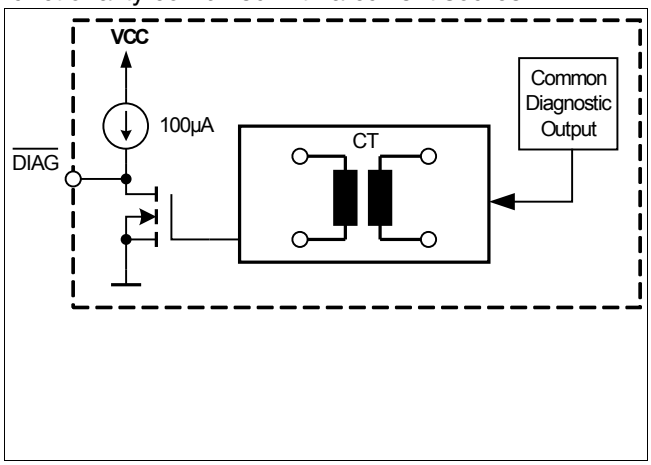


Figure 8 Common diagnostic output

3.5 Serial Interface

The ISO1H812G contains a serial interface that can be directly controlled by the microcontroller output ports.

3.5.1 SPI Signal Description

$\overline{CS}$ - Chip select. The system microcontroller selects the ISO1H812G by means of the $\overline{CS}$ pin. Whenever the pin is in a logic low state, data can be transferred from the µC.

$\overline{CS}$ High to low transition:

•Serial input data can be clocked in from then on

•SO changes from high impendance state to logic high or low state corresponding to the SO bit-state

$\overline{CS}$ Low to high transition:

•Transfer of SI bits from shift register into output buffers, if number of clock signals was an integer multiple of 8

•SO changes from the SO bit-state to high impendance state

To avoid any false clocking the serial input pin SCLK should be logic high state during high-to-low transition of $\overline{CS}$. When $\overline{CS}$ is in a logic high state, any signals at the SCLK and SI pins are ignored and SO is forced into a high impedance state. The integrated modulo counter that counts the number of clocks avoids the take over of invalid commands caused by a spike on the clock line or wrong number of clock cycles. A command is only taken over, if after the low-to-high transition of the $\overline{CS}$ signal the number of counted clock cycles is recognized as a multiple of 8.

SCLK - Serial clock. The system clock pin clocks the internal shift register of the ISO1H812G. The serial input (SI) accepts data into the input shift register on the rising edge of SCLK while the serial output (SO) shifts the output information out of the shift register on the falling edge of the serial clock. It is essential that the SCLK pin is in a logic high state whenever chip select $\overline{CS}$ makes any transition. The number of clock pulses will be counted during a chip select cycle. The received data will only be accepted, if exactly an integer multiple of 8 clock pulses were counted during $\overline{CS}$ is active.

SI - Serial input. Serial data bits are shifted in at this pin, the most significant bit first. SI information is read in on the rising edge of the SCLK. Input data is latched in the shift register and then transferred to the control buffer of the output stages.

SO - Serial output. SO is in a high impedance state until the $\overline{CS}$ pin goes to a logic low state. The data of the internal shift register are shifted out serially at this pin. The most significant bit will appear at first. The further bits will appear following the falling edge of SCLK.

3.5.2 SPI Bus Concepts

3.5.2.1 Independent Individual Control

Each IC with a SPI is controlled individually and independently by an SPI master, as in a directional point-to-point communication.The port requirements for this topology are the greatest, because for each controlled IC an individual SPI at the µC is needed (SCLK, $\overline{CS}$, SI). All ICs can be addressed simultaneously with the full SPI bandwidth.

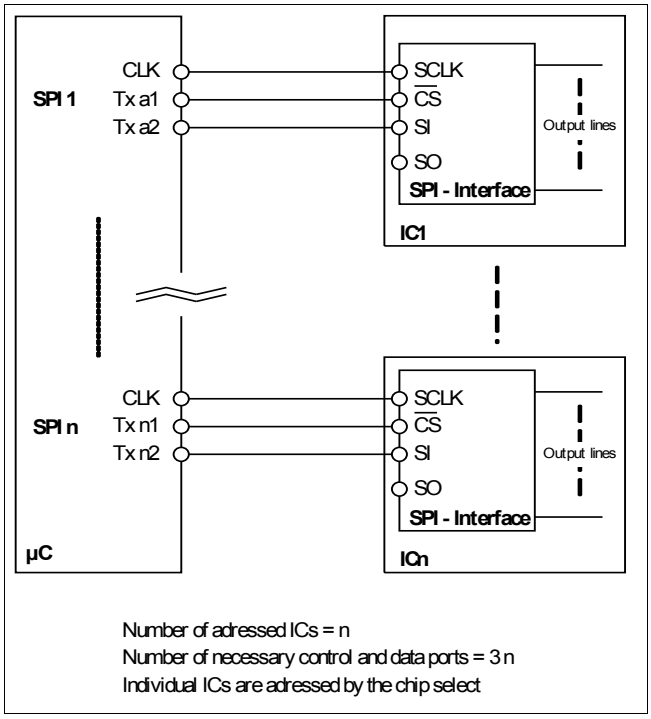


Figure 9 Individual independent control of each IC with SPI

3.5.2.2 Daisy-chain Configuration

The connection of different ICs and a µC as shown in Fig. 10 is called a daisy-chain. For this type of bus-topology only one SPI interface of the µC for two or more ICs is needed. All ICs share the same clock and chip select port of the SPI master. That is all ICs are active and addressed simultaneously. The data out of the µC is connected to the SI of the first IC in the line. Each SO of an IC is connected to the SI of the next IC in the line.

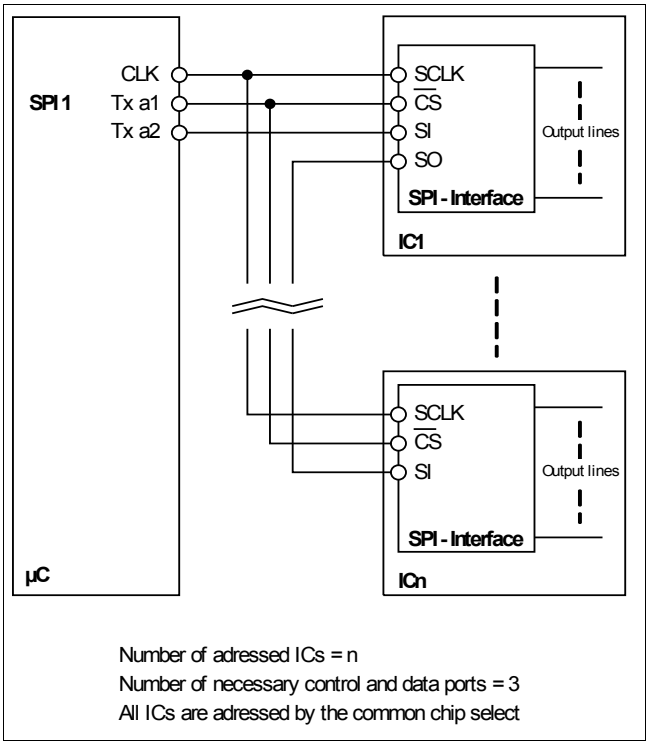


Figure 10 SPI bus all ICs in a "daisy chain" configuration

The µC feeds the data bits into the SI of IC1 (first IC in the chain). The bits coming from the SO of IC1 are directly shifted into the SI of the next IC. As long as the chip select is inactive (logic high) all the IC SPIs ignore the clock (SCLK) and input signals (SI) and all outputs (SO) are in tristate. As long as the chip select is active the SPI register works as a simple shift register. With each clock signal one input is shifted into the SPI register (SI), each bit in the shift register moves one position further within the register, and the last bit in the SPI shift register is shifted out of SO. This is continued as long as the chip select is active (logic low) and clock signals are applied. The data is then only taken over to the output buffers of each IC when the $\overline{CS}$ signal changes to high from low and recognized as valid data by the internal modulo counter.

3.6 Transmission Failure Detection

There is a failure detection unit integrated to ensure also a stable functionality during the integrated coreless transformer transmission. This unit decides whether the transmitted data is valid or not. If four times serial data coming from the internal registers is not accepted the output stages are switched off until the next valid data is received.

3.7 Serial Interface Timing

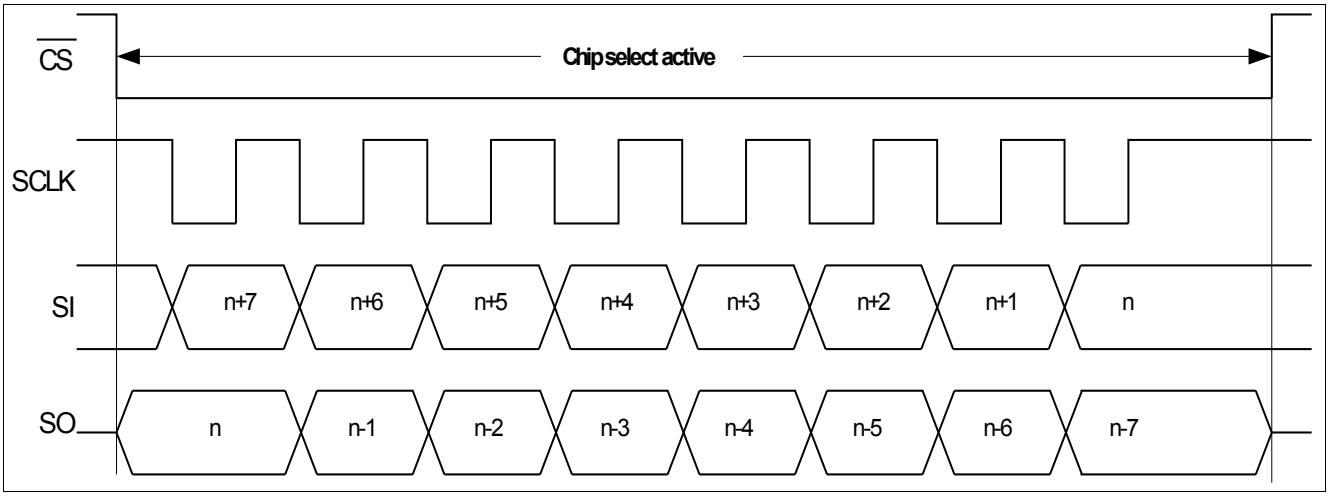


Figure 11 Serial interface

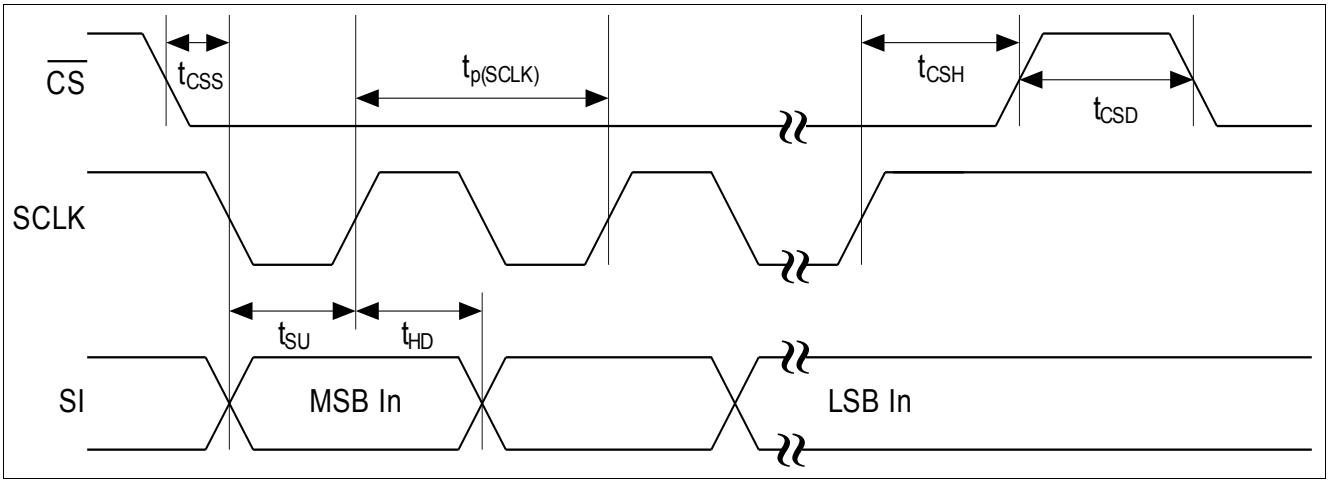


Figure 12 Serial input timing diagram

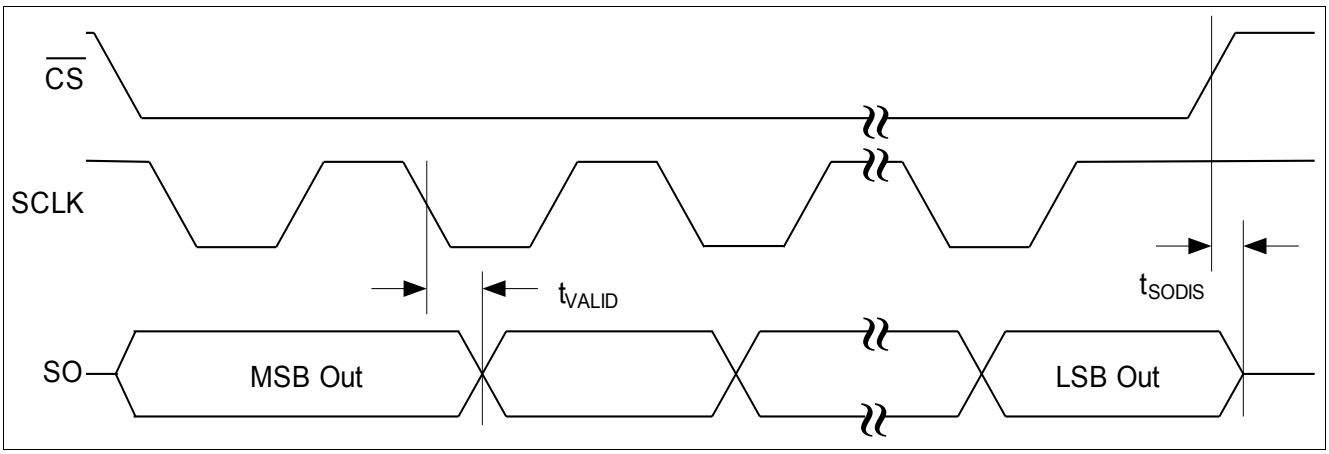


Figure 13 Serial output timing diagram

4 Electrical Characteristics

Note: All voltages at pins 2 to 14 are measured with respect to ground GNDCC (pin 15). All voltages at pin 20 to pin 36 and TAB are measured with respect to ground GNDbb (pin 19). The voltage levels are valid if other ratings are not violated. The two voltage domains V_{CC} ,GND_{CC} and V_{bb} ,GND_{bb} are internally galvanically isolated.

4.1 Absolute Maximum Ratings

Note: Absolute maximum ratings are defined as ratings, which when being exceeded may lead to destruction of the integrated circuit. For the same reason make sure, that any capacitor that will be connected to pin 2 (VCC) and TAB (Vbb) is discharged before assembling the application circuit. Supply voltages higher than $V_{bb(AZ)}$ require an external current limit for the GNDbb pin, e.g. with a 15Ω resistor in GNDbb connection. Operating at absolute maximum ratings can lead to a reduced lifetime.

Parameter at T_j = -40 ... 135°C, unless otherwise specified	**Symbol**	**Limit Values**		**Unit**
		min.	**max.**	
Supply voltage input interface (VCC)	V_{CC}	-0.5	6.5	V
Supply voltage output interface (Vbb)	V_{bb}	-1[1)]	45	
Continuos voltage at pin SI	V_{SI}	-0.5	6.5	
Continuos voltage at pin $\overline{CS}$	V_{CS}	-0.5	6.5	
Continuos voltage at pin SCLK	V_{SCLK}	-0.5	6.5	
Continuos voltage at pin $\overline{DIS}$	V_{DIS}	-0.5	6.5	
Continuos voltage at pin SO	V_{SO}	-0.5	6.5	
Continuos voltage at pin $\overline{DIAG}$	V_{DIAG}	-0.5	6.5	
Load current (short-circuit current)	I_L	---	self limited	A
Reverse current through GNDbb[1)]	I_{GNDbb}	-1.6	---	
Operating Temperature	T_j	-25	internal limited	°C
Extended Operation Temperature	T_j	-40	internal limited	
Storage Temperature	T_{stg}	-50	150	
Power Dissipation[2)]	P_{tot}	---	3.3	W
Inductive load switch-off energy dissipation[3)] single pulse, T_j = 125°C, I_L = 0.625A one channel active all channel simultaneously active (each channel)	E_{AS}	 --- 	 10 1	J
Load dump protection[3)] $V_{loadDump}$[4)]=V_A + V_S V_{IN} = low or high t_d = 400ms, R_I = 2W, R_L = 27W, V_A = 13.5V t_d = 350ms, R_I = 2W, R_L = 57W, V_A = 27V	$V_{Loaddump}$	 --- ---	 90 117	V
Electrostatic discharge voltage (Human Body Model) according to JESD22-A114-B	V_{ESD}		2	kV
Electrostatic discharge voltage (Charge Device Model) according to ESD STM5.3.1 - 1999	V_{ESD}		1	kV
Continuos reverse drain current[1)3)], each channel	I_S	---	4	A

1) defined by P_{tot}

2) Device on 50mm*50mm*1.5mm epoxy PCB FR4 with 6cm² (one layer, 70µm thick) copper area for drain connection. PCB is vertical without blown air.

3) not subject to production test, specified by design

4) $V_{Loaddump}$ is setup without the DUT connected to the generator per ISO7637-1 and DIN40839

4.2 Thermal Characteristics

Parameter at T_j = -25 ... 125°C, V_{bb}=15...30V, V_{CC}= 3.0...5.5V, unless otherwise specified	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Thermal resistance junction - case	R_{thJC}	---	---	1.5	K/W	
Thermal resistance @ min. footprint	$R_{th(JA)}$	---	---	50		
Thermal resistance @ 6cm² cooling area[1)]	$R_{th(JA)}$	---	---	38		

1) Device on 50mm*50mm*1.5mm epoxy PCB FR4 with 6cm² (one layer, 70µm thick) copper area for drain connection. PCB is vertical without blown air.

4.3 Load Switching Capabilities and Characteristics

Parameter at T_j = -25 ... 125°C, V_{bb}=15...30V, V_{CC}= 3.0...5.5V, unless otherwise specified	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
On-state resistance, I_L = 0.5A, each channel T_j = 25°C T_j = 125°C two parallel channels, T_j = 25°C:[1)] four parallel channels, T_j = 25°C:[1)]	R_{ON}	 --- ---	 150 270 75 38	 200 320 100 50	mΩ	
Nominal load current Device on PCB 38K/W, T_a = 85°C, T_j < 125°C one channel:[1)] two parallel channels:[1)] four parallel channels:[1)]	$I_{L(NOM)}$		 0.7 1.1 2.2		A	
Turn-on time to 90% V_{OUT}[2)] R_L = 47Ω, V_{Dx} = 0 to 5V	t_{on}	---	64	120	µs	
Turn-off time to 10% V_{OUT}[1)] R_L = 47Ω, V_{Dx} = 5 to 0V	t_{off}	---	89	170		
Slew rate on 10 to 30% V_{OUT} R_L = 47Ω, V_{bb} = 15V	dV/dt_{on}	---	1	2	V/µs	
Slew rate off 70 to 40% V_{OUT} R_L = 47Ω, V_{bb} = 15V	$-dV/dt_{off}$	---	1	2		
Internal data transmission period	t_{idt}			17.8	µs	[1)]
Failure shutdown time	t_{fs}			64	µs	[1)]

1) not subject to production test, specified by design

2) The turn-on and turn-off time includes the switching time of the high-side switch and the transmission time via the coreless transformer in normal operating mode. During a failure on the coreless transformer transmission turn-on or turn-off time can increase by up to 50µs.

4.4 Operating Parameters

Parameter at T_j = -25 ... 125°C, V_{bb}=15...30V, V_{CC}= 3.0...5.5V, unless otherwise specified		Symbol	Limit Values			Unit	Test Condition
			min.	typ.	max.		
Common mode transient immunity[1]		$\Delta V_{ISO}/dt$	-25	-	25	kV/µs	ΔV_{ISO} = 500V
Magnetic field immunity[1]		H_{IM}	100			A/m	IEC61000-4-8
Voltage domain V_{bb} (Output interface)	Operating voltage	V_{bb}	11	---	35	V	
	Undervoltage shutdown	$V_{bb(under)}$	7	---	10.5		
	Undervoltage restart	$V_{bb(u\_rst)}$	---	---	11		
	Undervoltage hysteresis	$\Delta V_{bb(under)}$	---	0.5	---		
	Undervoltage current	$I_{bb(uvlo)}$	---	1	2.5	mA	V_{bb} < 7V
	Operating current	I_{GNDL}	---	10	14	mA	All Channels ON - no load
	Leakage output current (included in $I_{bb(off)}$) V_{Dx} = low, each channel	$I_{L(off)}$	---	5	30	µA	
Voltage domain V_{CC} (Input interface)	Operating voltage	V_{CC}	3.0	---	5.5	V	
	Undervoltage shutdown	$V_{CC(under)}$	2.5	---	2.9		
	Undervoltage restart	$V_{CC(u\_rst)}$	---	---	3		
	Undervoltage hysteresis	$\Delta V_{CC(under)}$	---	0.1	---		
	Undervoltage current	$I_{CC(uvlo)}$	---	1	2	mA	V_{cc} < 2.5V
	Operating current	$I_{CC(on)}$	---	4.5	6	mA	

1) not subject to production test

4.5 Output Protection Functions

Parameter[1)] at T_j = -25 ... 125°C, V_{bb}=15...30V, V_{CC}=3.0...5.5V, unless otherwise specified	Symbol	Limit Values min.	Limit Values typ.	Limit Values max.	Unit	Test Condition
Initial peak short circuit current limit, each channel:	$I_{L(SCp)}$				A	
T_j = -25°C, V_{bb} = 30V, t_m = 700µs		---	---	1.9		
T_j = 25°C		---	1.4	---		
T_j = 125°C		0.7	---	---		
two parallel channels:[2)]		twice the current of one channel				
four parallel channels:[2)]		four times the current of one channel				
Repetitive short circuit current limit $T_j = T_{jt}$ (see timing diagrams)		---		---		
each channel:[2)]	$I_{L(SCr)}$		1.1			
two parallel channels:[2)]			1.1			
four parallel channels:[2)]			1.1			
Output clamp (inductive load switch off)[3)] at $V_{OUT} = V_{bb} - V_{ON(CL)}$	$V_{ON(CL)}$	47	53	60	V	
Overvoltage protection	$V_{bb(AZ)}$	47	---	---		
Thermal overload trip temperature[2) 4)]	T_{jt}	135	---	---	°C	
Thermal hysteresis[2)]	ΔT_{jt}	---	10	---	K	

1) Integrated protection functions are designed to prevent IC destruction under fault conditions described in the data sheet. Fault conditions are considered as “outside” normal operating range. Protection functions are not designed for continuos repetitive operation.

2) not subject to production test, specified by design

3) If channels are connected in parallel, output clamp is usually accomplished by the channel with the lowest $V_{ON(CL)}$

4) Higher operating temperature at normal function for each channel available

4.6 Diagnostic Characteristics at pin $\overline{\text{DIAG}}$

Parameter at T_j = -25 ... 125°C, V_{bb}=15...30V, V_{CC}=3.0...5.5V, unless otherwise specified	Symbol	Limit Values min.	Limit Values typ.	Limit Values max.	Unit	Test Condition
Common diagnostic sink current (overtemperature of any channel) T_j = 135°C	$I_{diagsink}$			5	mA	V_{DIAGON} < 0.25 x VCC
Common diagnostic source current	$I_{diagsource}$		100		µA	

4.7 Input Interface

Parameter at T_j = -25 ... 125°C, V_{bb}=15...30V, V_{CC}= 3.0...5.5V, unless otherwise specified	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Input low state voltage (SI, $\overline{DIS}$, $\overline{CS}$, SCLK)	V_{IL}	-0.3	---	0.3 x V_{CC}	V	
Input high state voltage (SI, $\overline{DIS}$, $\overline{CS}$, SCLK)	V_{IH}	0.7 x V_{CC}	---	V_{CC}+ 0.3		
Input voltage hysteresis (SI, $\overline{DIS}$, $\overline{CS}$, SCLK)	V_{IHys}		100		mV	
Output low state voltage (SO)	V_{OL}	-0.3	---	0.25 x V_{CC}	V	C_L < 50pF, R_L > 10kΩ
Output high state voltage (SO)	V_{OH}	0.75 x V_{CC}	---	V_{CC}+ 0.3		
Input pull down current (SI , $\overline{DIS}$)	I_{Idown}		100		µA	
Input pull up current ($\overline{CS}$, SCLK)	$-I_{Iup}$		100			
Output disable time (transition $\overline{DIS}$ to logic low)[1)2)] Normal operation Turn-off time to 10% V_{OUT} R_L = 47Ω	t_{DIS}	---	85	170	µs	
Output disable time (transition $\overline{DIS}$ to logic low)[1)2)3)] Disturbed operation Turn-off time to 10% V_{OUT} R_L = 47Ω	t_{DIS}	---	---	230		

1) The time includes the turn-on/off time of the high-side switch and the transmission time via the coreless transformer.

2) If Pin $\overline{DIS}$ is set to low the outputs are set to low; after $\overline{DIS}$ set to high a new write cycle is necessary to set the output again.

3) The parameter is not subject to production test - verified by design/characterization

4.8 SPI Timing

Parameter at T_j = -25 ... 125°C, V_{bb}=15...30V, V_{CC}= 3.0...5.5V, unless otherwise specified	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Serial clock frequency	f_{SCLK}	DC	---	20	MHz	
Serial clock period (1/fclk)	$t_{p(SLCK)}$	50	---	---	ns	
$\overline{CS}$ Setup time (falling edge of $\overline{CS}$ to falling edge of SCLK)	t_{CSS}	5	---	---		
$\overline{CS}$ Hold time (rising edge of SCLK to rising edge of $\overline{CS}$)	t_{CSH}	10	---	---		
$\overline{CS}$ Disable time ($\overline{CS}$ high time between two accesses)	t_{CSD}	10	---	---		
Data setup time (required time SI to rising edge of SCLK)	t_{SU}	6	---	---		
Data hold time (falling edge of SCLK to SI)	t_{HD}	6	---	---		
SO Output valid time CL = 50pF	t_{VALID}	---	---	20		
SO Output disable time	t_{SODIS}			20	ns	
Delay to next $\overline{CS}$ cycle for multiple device synchronization[1)]	t_{CSDMD}	17,8			µs	2)
Input to output data transmission jitter	t_{IOJ}	8		17,8		2)

1) necessary $\overline{CS}$ delay time to ensure a proper data update for multiple devices

2) not subject to production test, specified by design

4.9 Reverse Voltage

Parameter at T_j = -25 ... 125°C, V_{bb}=15...30V, V_{CC}= 3.0...5.5V, unless otherwise specified	Symbol	Limit Values			Unit	Test Condition
		min.	typ.	max.		
Reverse voltage[1)2)] R_{GND} = 0 Ω R_{GND} = 150 Ω	$-V_{bb}$	 --- ---	 --- ---	 1 45	V	
Diode forward on voltage IF = 1.25A, V_{Dx} = low, each channel	$-V_{ON}$	---	---	1.2		

1) defined by P_{tot}

2) not subject to production test, specified by design

4.10 Isolation and Safety-Related Specification

Parameter	Value	Unit	Conditions
Rated dielectric isolation voltage V_{ISO}	500	V_{AC}	1 - minute duration[1)]
Short term temporary overvoltage	1250	V	5s acc. DIN EN60664-1[1)]
Minimum external air gap (clearance)	2.6	mm	shortest distance through air.
Minimum external tracking (creepage)	2.6	mm	shortest distance path along body.

1) not subject to production test, verified by characterization; Production Test with 1100V, 100ms duration

Approvals:

UL508, CSA C22.2 NO.14

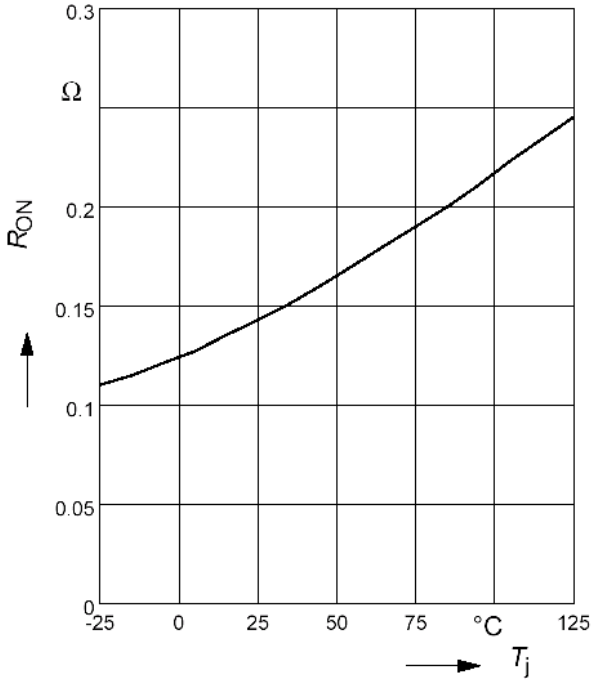
Certificate Number: 20090514-E329661

4.11 Reliability

For Qualification Report please contact your local Infineon Technologies office!

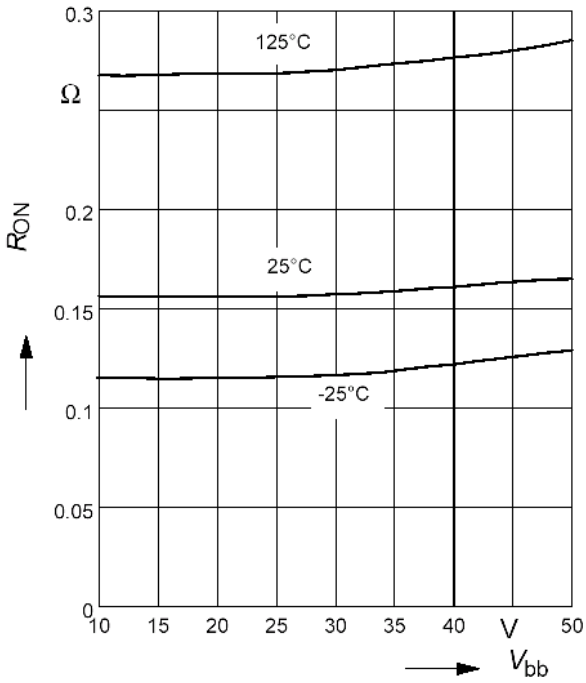
Typ. on-state resistance

$R_{ON} = f(T_j)$; V_{bb} = 15V ; V_{in} = high



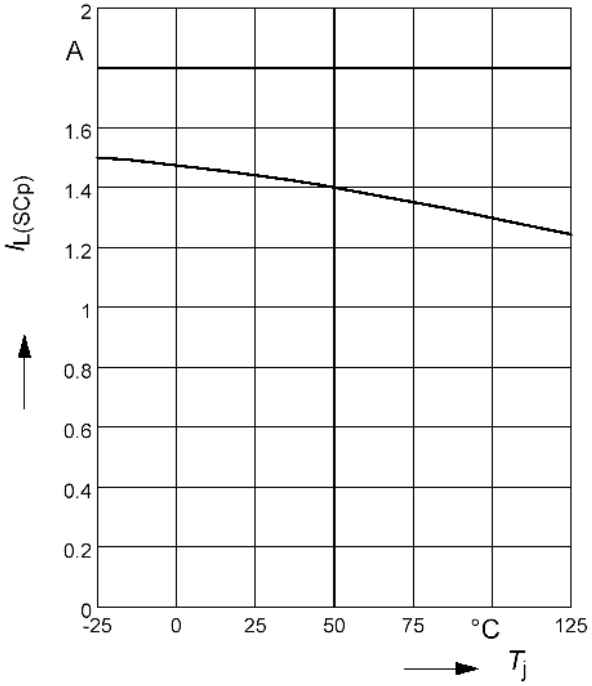
Typ. on-state resistance

$R_{ON} = f(V_{bb})$; I_L = 0.5A ; V_{in} = high



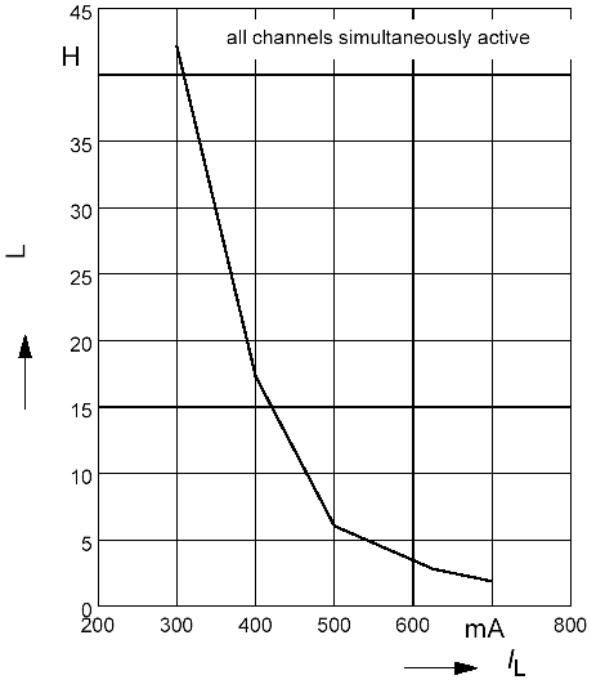
Typ. initial peak short circuit current limit

$I_{L(SCp)} = f(T_j)$; V_{bb} = 24V



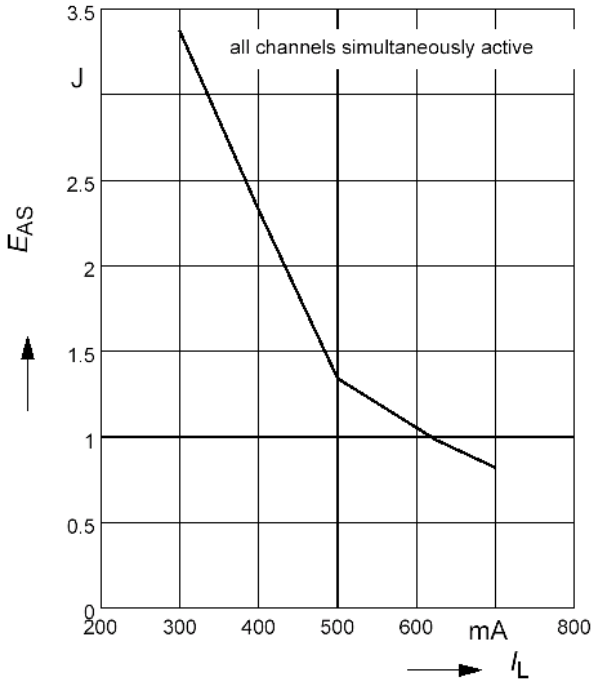
Maximum allowable load inductance for a single switch off, calculated

$L = f(I_L)$; T_{jstart}=125°C, V_{bb}=24V, R_L=0Ω



Maximum allowable inductive switch-off energy, single pulse

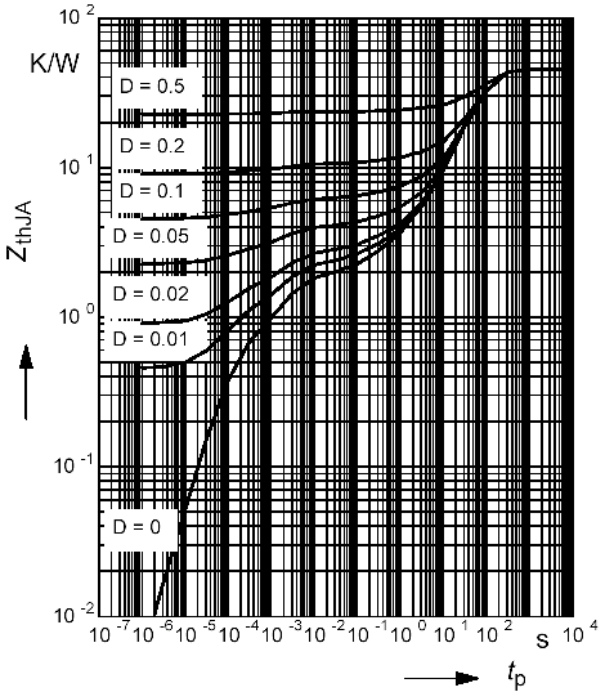
$E_{AS} = f(I_L)$; T_{jstart} = 125°C, V_{bb} = 24V



Typ. transient thermal impedance

Z_{thJA}=f(t_p) @ min. footprint

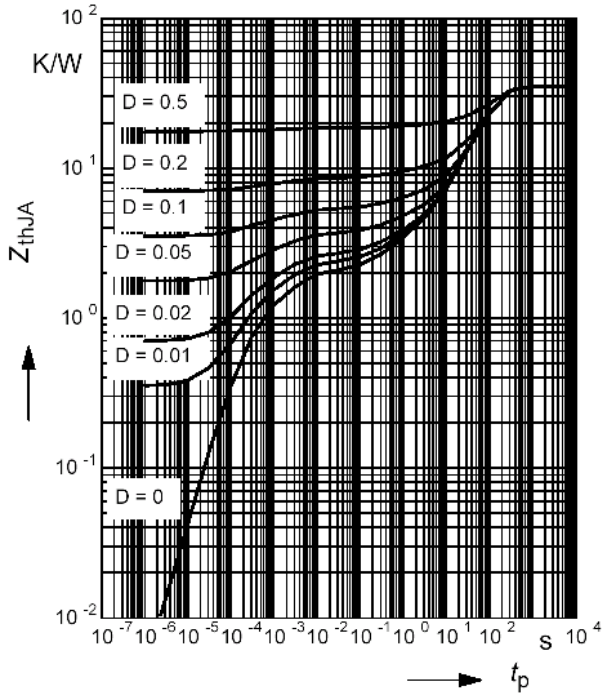
Parameter: $D=t_p/T$



Typ. transient thermal impedance

Z_{thJA}=f(t_p) @ 6cm² heatsink area

Parameter: $D=t_p/T$



5 Package Outlines

PG-DSO-36

(Plastic Dual Small Outline Package)

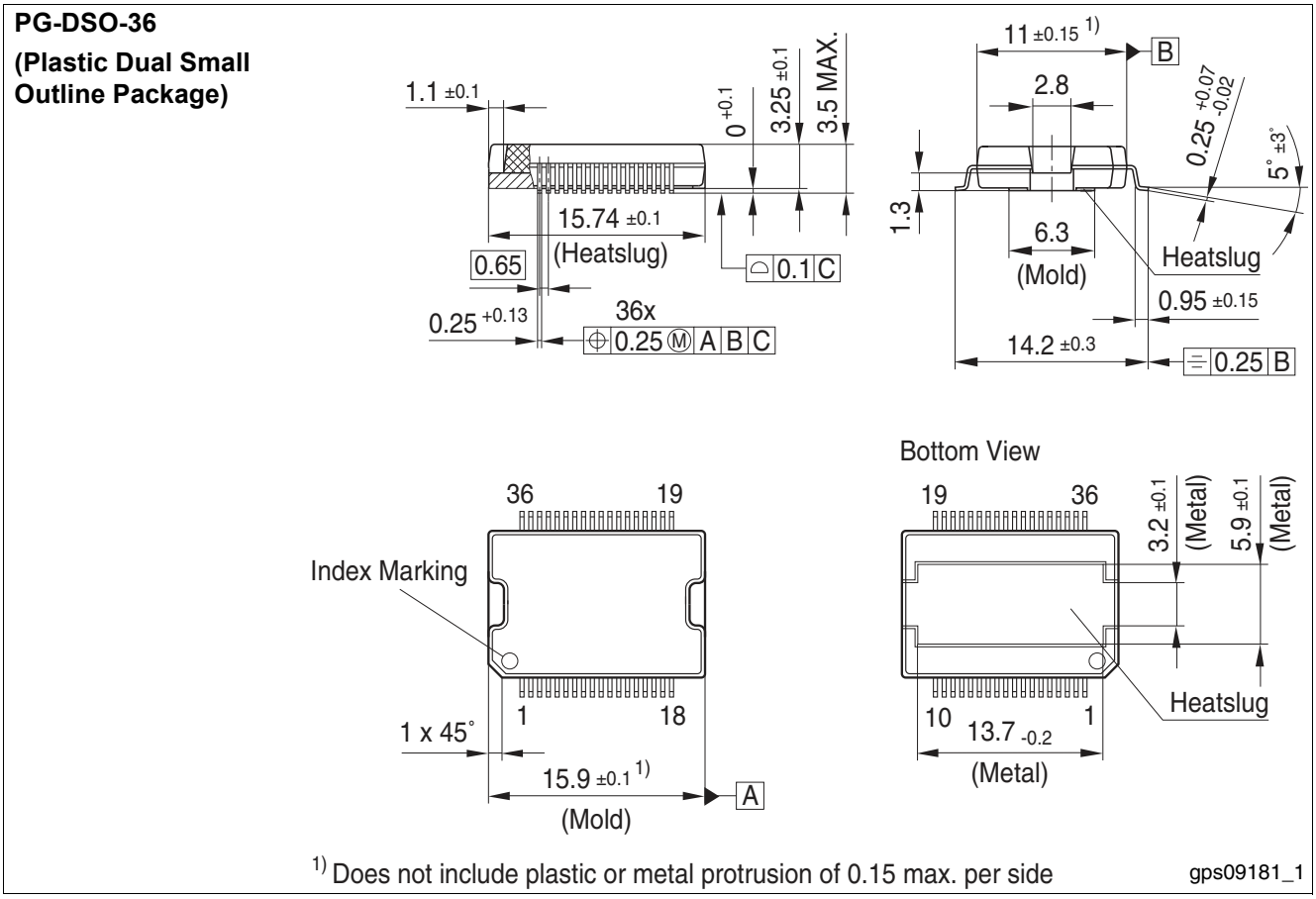


Figure 14 PG-DSO36

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