THIS SPEC IS OBSOLETE

Spec No: 38-05003

Spec Title: CY7C1046CV33 - 1M x 4 Static RAM

Sunset Owner: Anuj Chakrapani (AJU)

Replaced by: None

CY7C1046CV33

1M x 4 Static RAM

Features

- **High speed**
  - **—t_{AA} = 10ns**
- **Low active power for 10 ns speed**
  - **—324 mW (max.)**
- **2.0V data retention**
- **Automatic power-down when deselected**
- **TTL-compatible inputs and outputs**
- **Easy memory expansion with $\overline{CE}$ and $\overline{OE}$ features**

Functional Description[1]

The CY7C1046CV33 is a high-performance CMOS static RAM organized as 1,048,576 words by 4 bits. Easy memory expansion is provided by an active LOW Chip Enable ($\overline{CE}$), an active LOW Output Enable ($\overline{OE}$), and three-state drivers.

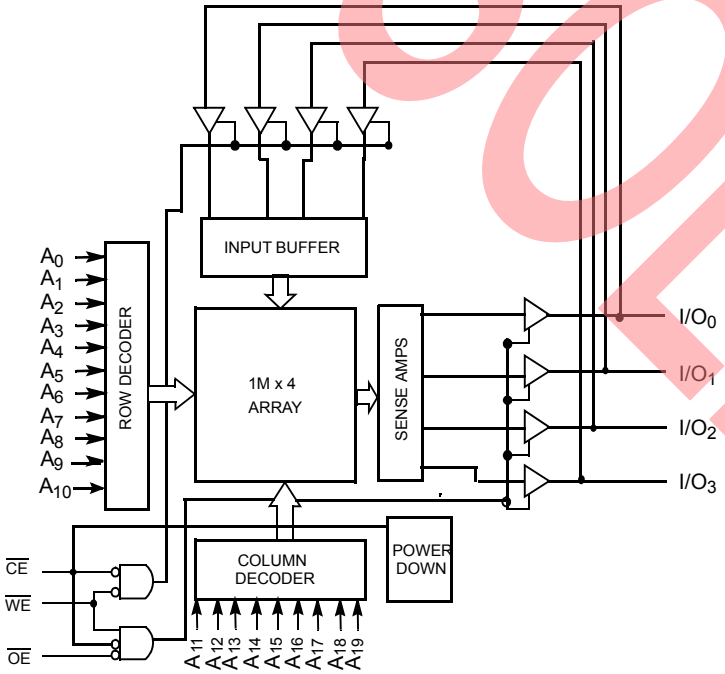
Writing to the device is accomplished by taking Chip Enable ($\overline{CE}$) and Write Enable ($\overline{WE}$) inputs LOW. Data on the four I/O pins (I/O_0 through I/O_3) is then written into the location specified on the address pins (A_0 through A_{19}).

Reading from the device is accomplished by taking Chip Enable ($\overline{CE}$) and Output Enable ($\overline{OE}$) LOW while forcing Write Enable ($\overline{WE}$) HIGH. Under these conditions, the contents of the memory location specified by the address pins will appear on the I/O pins.

The four input/output pins (I/O_0 through I/O_3) are placed in a high-impedance state when the device is deselected ($\overline{CE}$ HIGH), the outputs are disabled ($\overline{OE}$ HIGH), or during a Write operation ($\overline{CE}$ LOW, and $\overline{WE}$ LOW).

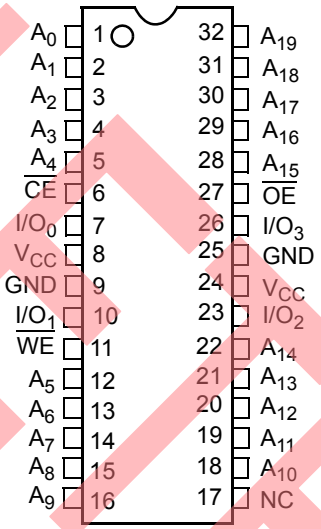
The CY7C1046CV33 is available in a standard 400-mil-wide 32-pin SOJ package with center power and ground (revolutionary) pinout.

Logic Block Diagram



Pin Configuration

SOJ
Top View



Selection Guide

	-8[2]	-10	-12	-15	Unit
Maximum Access Time	8	10	12	15	ns
Maximum Operating Current	100	90	85	80	mA
Maximum CMOS Standby Current	10	10	10	10	mA

Notes:
1. For guidelines on SRAM system design, please refer to the 'System Design Guidelines' Cypress application note, available on the internet at www.cypress.com.
2. Shaded areas contain advance information.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature .....–65°C to +150°C

Ambient Temperature with Power Applied.....–55°C to +125°C

Supply Voltage on V_{CC} to Relative GND[3] .... –0.5V to +4.6V

DC Voltage Applied to Outputs in High-Z State[3].....–0.5V to V_{CC} + 0.5V

DC Input Voltage[3].....–0.5V to V_{CC} + 0.5V

Current into Outputs (LOW)..... 20 mA

Static Discharge Voltage..... > 2001V (per MIL-STD-883, Method 3015)

Latch-up Current..... > 200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	3.0V – 3.6V
Industrial	–40°C to + 85°C	3.0V – 3.6V

DC Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions		-8[2] Min.	-8[2] Max.	-10 Min.	-10 Max.	-12 Min.	-12 Max.	-15 Min.	-15 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = –4.0 mA		2.4		2.4		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4		0.4		0.4		0.4	V
V_{IH}	Input HIGH Voltage			2.0	V_{CC} + 0.3	2.0	V_{CC} + 0.3	2.0	V_{CC} + 0.3	2.0	V_{CC} + 0.3	V
V_{IL}	Input LOW Voltage[3]			–0.3	0.8	–0.3	0.8	–0.3	0.8	–0.3	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}		–1	+1	–1	+1	–1	+1	–1	+1	µA
I_{OZ}	Output Leakage Current	GND ≤ V_{OUT} ≤ V_{CC}, Output Disabled		–1	+1	–1	+1	–1	+1	–1	+1	µA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., f = f_{MAX} = $1/t_{RC}$			100		90		85		80	mA
I_{SB1}	Automatic CE Power-Down Current —TTL Inputs	Max. V_{CC}, $\overline{CE}$ ≥ V_{IH} V_{IN} ≥ V_{IH} or V_{IN} ≤ V_{IL}, f = f_{MAX}			40		40		40		40	mA
I_{SB2}	Automatic CE Power-Down Current —CMOS Inputs	Max. V_{CC}, $\overline{CE}$ ≥ V_{CC} – 0.3V, V_{IN} ≥ V_{CC} – 0.3V, or V_{IN} ≤ 0.3V, f = 0	Commercial		10		10		10		10	mA

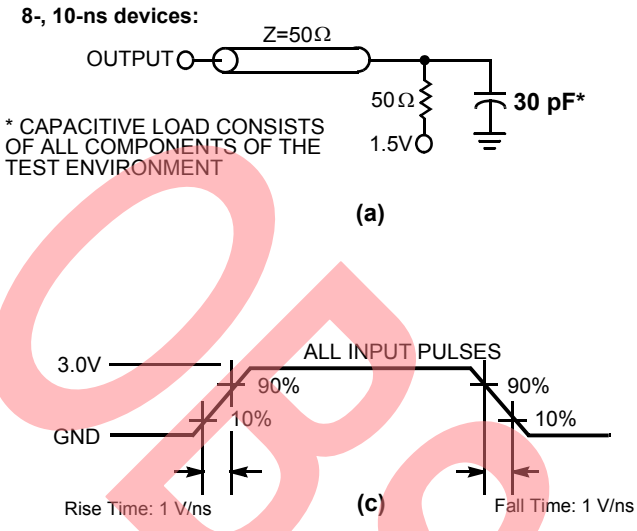
Capacitance[4]

Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 3.3V	6	pF
C_{OUT}	I/O Capacitance		6	pF

Notes:

3. V_{IL} (min.) = –2.0V for pulse durations of less than 20 ns.
4. Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms[5]



Notes:

5. AC characteristics (except High-Z) for all 8-ns and 10-ns parts are tested using the load conditions shown in Figure (a). All other speeds are tested using the Thevenin load shown in Figure (b). High-Z characteristics are tested for all speeds using the test load shown in Figure (d).

AC Switching Characteristics[6] Over the Operating Range

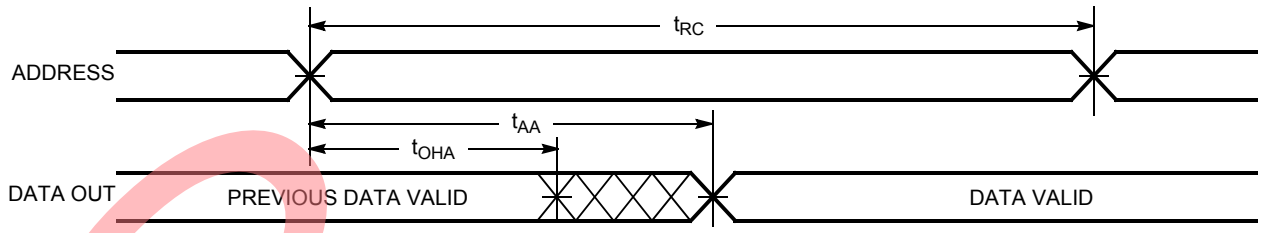
Parameter	Description	-8[2]		-10		-12		-15		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle										
t_{power}[7]	V_{CC}(typical) to the first access	1		1		1		1		µs
t_{RC}	Read Cycle Time	8		10		12		15		ns
t_{AA}	Address to Data Valid		8		10		12		15	ns
t_{OHA}	Data Hold from Address Change	3		3		3		3		ns
t_{ACE}	$\overline{CE}$ LOW to Data Valid		8		10		12		15	ns
t_{DOE}	$\overline{OE}$ LOW to Data Valid		4		5		6		7	ns
t_{LZOE}	$\overline{OE}$ LOW to Low-Z[9]	0		0		0		0		ns
t_{HZOE}	$\overline{OE}$ HIGH to High-Z[8, 9]		4		5		6		7	ns
t_{LZCE}	$\overline{CE}$ LOW to Low-Z[9]	3		3		3		3		ns
t_{HZCE}	$\overline{CE}$ HIGH to High-Z[8, 9]		4		5		6		7	ns
t_{PU}	$\overline{CE}$ LOW to Power-up	0		0		0		0		ns
t_{PD}	$\overline{CE}$ HIGH to Power-Down		8		10		12		15	ns
Write Cycle[10, 11]										
t_{WC}	Write Cycle Time	8		10		12		15		ns
t_{SCE}	$\overline{CE}$ LOW to Write End	6		7		8		10		ns
t_{AW}	Address Set-up to Write End	6		7		8		10		ns
t_{HA}	Address Hold from Write End	0		0		0		0		ns
t_{SA}	Address Set-up to Write Start	0		0		0		0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	6		7		8		10		ns
t_{SD}	Data Set-up to Write End	4		5		6		7		ns
t_{HD}	Data Hold from Write End	0		0		0		0		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low-Z[9]	3		3		3		3		ns
t_{HZWE}	$\overline{WE}$ LOW to High-Z[8, 9]		4		5		6		7	ns

Notes:

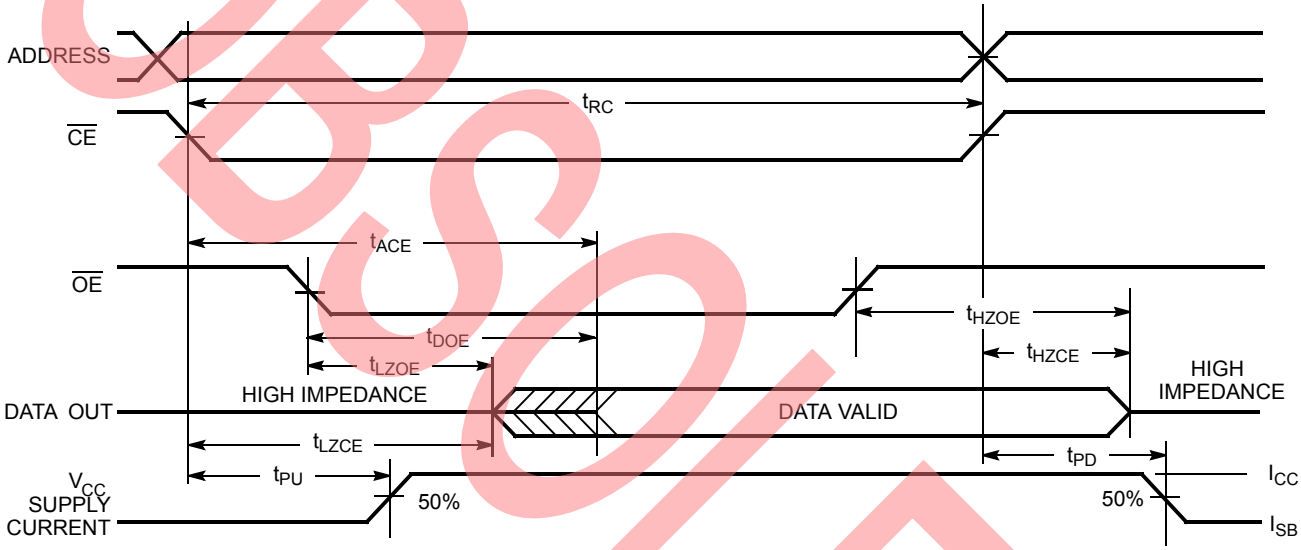
6. Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V.
7. t_{POWER} gives the minimum amount of time that the power supply should be at stable, typical Vcc values until the first memory access can be performed.
8. t_{HZOE}, t_{HZCE}, and t_{HZWE} are specified with a load capacitance of 5 pF as in part (d) of AC Test Loads. Transition is measured ±500 mV from steady-state voltage.
9. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZOE} is less than t_{LZOE}, and t_{HZWE} is less than t_{LZWE} for any given device.
10. The internal Write time of the memory is defined by the overlap of $\overline{CE}$ LOW, and $\overline{WE}$ LOW. $\overline{CE}$ and $\overline{WE}$ must be LOW to initiate a Write, and the transition of either of these signals can terminate the Write. The input data set-up and hold timing should be referenced to the leading edge of the signal that terminates the Write.
11. The minimum Write cycle time for Write Cycle no. 3 ($\overline{WE}$ controlled, $\overline{OE}$ LOW) is the sum of t_{HZWE} and t_{SD}.

Switching Waveforms

Read Cycle No. 1[14, 15]



Read Cycle No. 2 (OE Controlled)[15, 16]

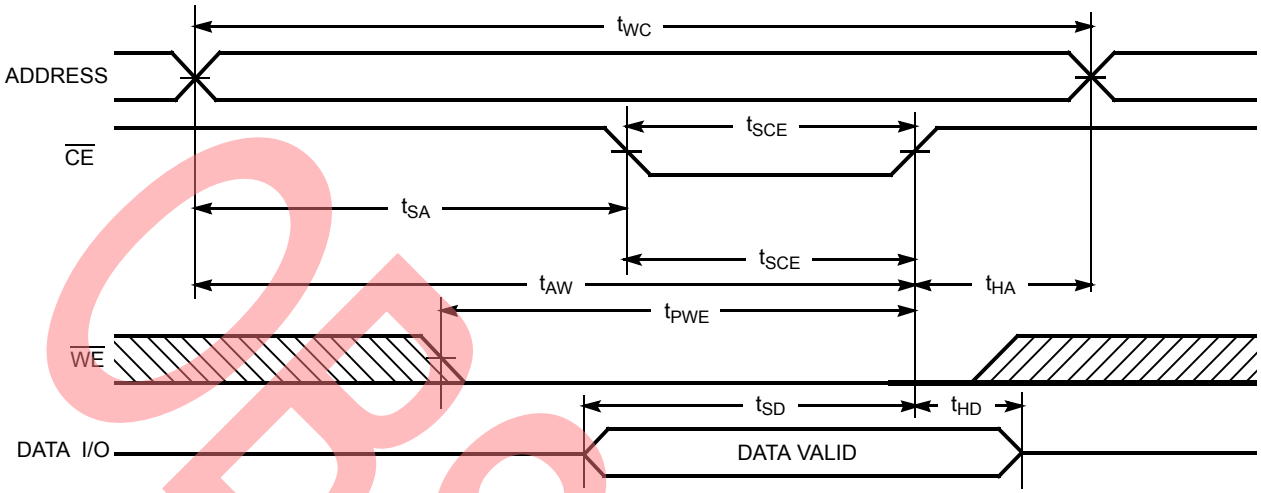


Notes:

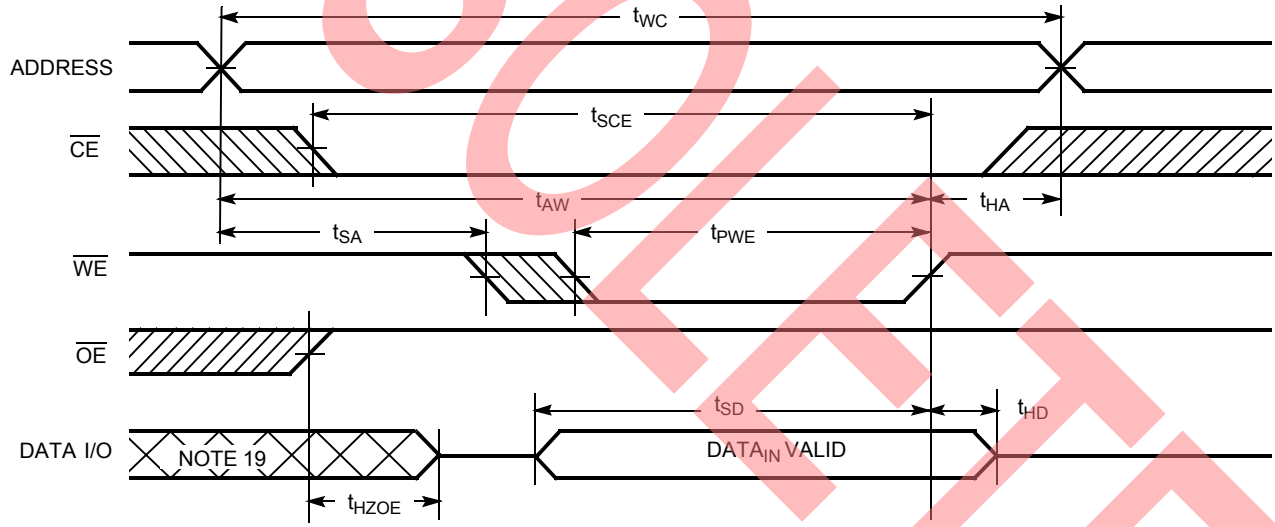
12. $t_r \leq 3$ ns for the -10, -12, and -15 speeds.
13. No input may exceed V_{CC} + 0.5V.
14. Device is continuously selected. $\overline{OE}$, $\overline{CE}$ = V_{IL}.
15. $\overline{WE}$ is HIGH for Read cycle.
16. Address valid prior to or coincident with $\overline{CE}$ transition LOW.

Switching Waveforms (continued)

Write Cycle No. 1 ($\overline{CE}$ Controlled)[17, 18]



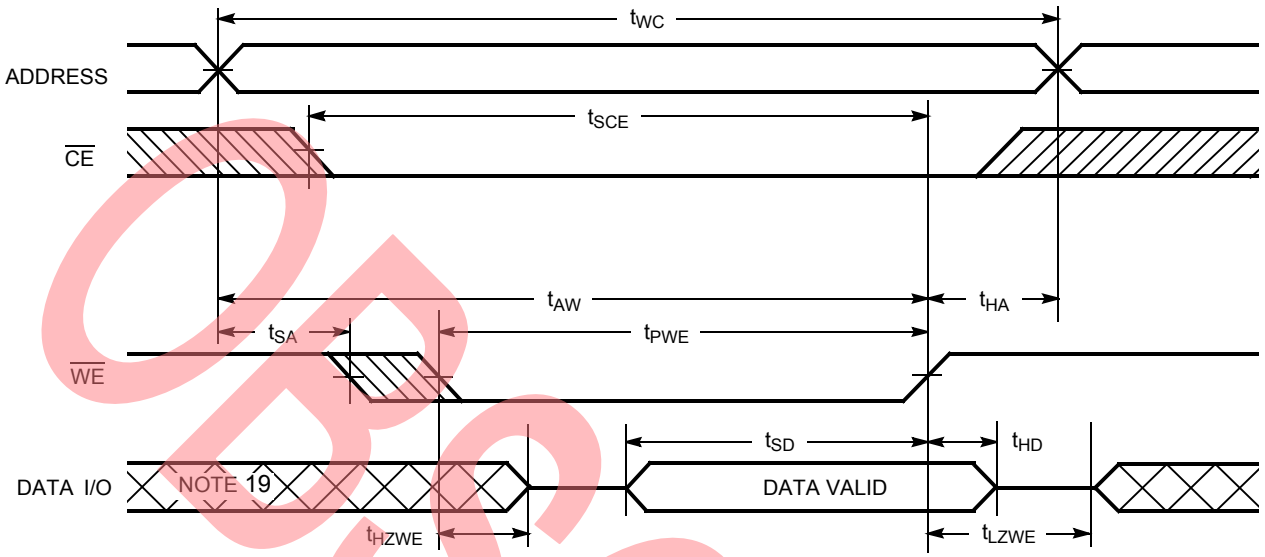
Write Cycle No. 2 ($\overline{WE}$ Controlled, $\overline{OE}$ HIGH During Write)[17, 18]



Notes:
17. Data I/O is high impedance if $\overline{OE}$ = V_{IH}.
18. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ going HIGH, the output remains in a high-impedance state.
19. During this period the I/Os are in the output state and input signals should not be applied.

Switching Waveforms (continued)

Write Cycle No. 3 ($\overline{WE}$ Controlled, $\overline{OE}$ LOW)[18]



Truth Table

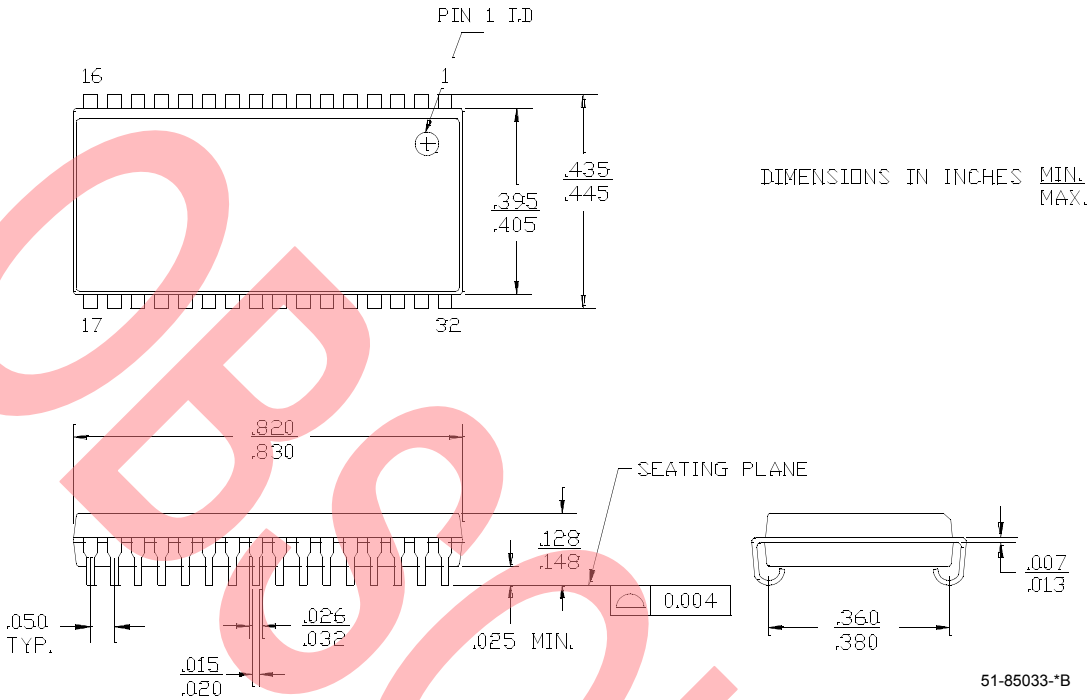
$\overline{CE}$	$\overline{OE}$	$\overline{WE}$	$I/O_0 – I/O_7$	Mode	Power
H	X	X	High-Z	Power-down	Standby (I_{SB})
L	L	H	Data Out	Read	Active (I_{CC})
L	X	L	Data In	Write	Active (I_{CC})
L	H	H	High-Z	Selected, Outputs Disabled	Active (I_{CC})

Ordering Information

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
10	CY7C1046CV33-10VC	V33	32-lead (400-mil) Molded SOJ	Commercial
	CY7C1046CV33-10VI	V33	32-lead (400-mil) Molded SOJ	Industrial
12	CY7C1046CV33-12VC	V33	32-lead (400-mil) Molded SOJ	Commercial
	CY7C1046CV33-12VI	V33	32-lead (400-mil) Molded SOJ	Industrial
15	CY7C1046CV33-15VC	V33	32-lead (400-mil) Molded SOJ	Commercial
	CY7C1046CV33-15VI	V33	32-lead (400-mil) Molded SOJ	Industrial

Package Diagram

32-Lead (400-Mil) Molded SOJ V33



Document History Page

Document Title: CY7C1046CV33 1M x 4 Static RAM Document Number: 38-05003				
REV.	**ECN NO.**	**Submission-Date**	**Orig. of Change**	**Description of Change**
**	112570	03/06/02	HGK	New data sheet for RAM 7
*A	116478	09/16/02	CEA	Add applications foot note to data sheet, page 1.
*B	2895041	03/18/2010	AJU	Inactive part numbers; obsolete data sheet.

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