SBAS249B – DECEMBER 2001 – REVISED NOVEMBER 2007

16-Bit, Voltage Output, Serial Input DIGITAL-TO-ANALOG CONVERTER

FEATURES

- LOW POWER: 150mW MAXIMUM
- +10V INTERNAL REFERENCE
- UNIPOLAR OR BIPOLAR OPERATION
- SETTLING TIME: 5μs to ±0.003% FSR
- 16-BIT MONOTONICITY, –40°C TO +85°C
- ±10V, ±5V, OR +10V CONFIGURABLE VOLTAGE OUTPUT
- RESET TO ZERO OR MID-SCALE
- DOUBLE-BUFFERED DATA INPUT
- DAISY-CHAIN FEATURE FOR MULTIPLE DAC7731s ON A SINGLE BUS
- SMALL SSOP-24 PACKAGE

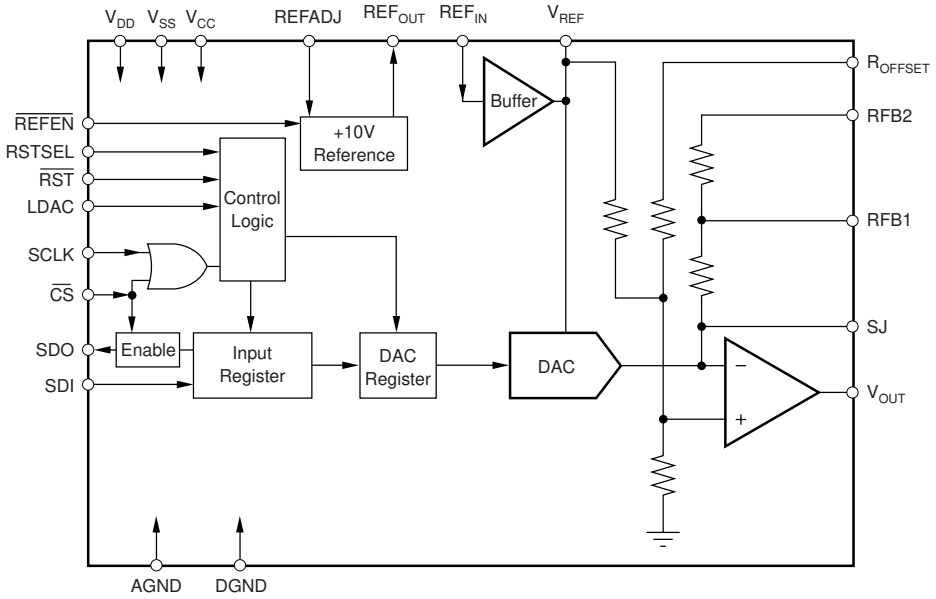
APPLICATIONS

- PROCESS CONTROL
- ATE PIN ELECTRONICS
- CLOSED-LOOP SERVO CONTROL
- MOTOR CONTROL
- DATA ACQUISITION SYSTEMS

DESCRIPTION

The DAC7731 is a 16-bit Digital-to-Analog Converter (DAC) which provides 16 bits of monotonic performance over the specified operating temperature range and offers a +10V internal reference. Designed for automatic test equipment and industrial process control applications, the DAC7731 output swing can be configured in a ±10V, ±5V, or +10V range. The flexibility of the output configuration allows the DAC7731 to provide both unipolar and bipolar operation by pin strapping. The DAC7731 includes a high-speed output amplifier with a maximum settling time of 5μs to ±0.003% FSR for a 20V full-scale change and only consumes 100mW (typical) of power.

The DAC7731 features a standard 3-wire, SPI-compatible serial interface with double buffering to allow asynchronous updates of the analog output as well as a serial data output line for daisy-chaining multiple DAC7731s. A user programmable reset control forces the DAC output to either min-scale (0000_h) or mid-scale (8000_h), overriding both the input and DAC register values. The DAC7731 is available in a SSOP-24 package and three performance grades specified to operate from –40°C to +85°C.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

ABSOLUTE MAXIMUM RATINGS(1)

V_{CC} to V_{SS}	–0.3V to +32V
V_{CC} to AGND	–0.3V to +16V
V_{SS} to AGND	–16V to +0.3V
AGND to DGND	–0.3V to 0.3V
REF_{IN} to AGND	0V to V_{CC} – 1.4V
V_{DD} to DGND	–0.3V to +6V
Digital Input Voltage to DGND	–0.3V to V_{DD} + 0.3V
Digital Output Voltage to DGND	–0.3V to V_{DD} + 0.3V
Operating Temperature Range	–40°C to +85°C
Storage Temperature Range	–65°C to +150°C
Junction Temperature (TJ Max)	+150°C

NOTE: (1) Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may affect device reliability.

ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

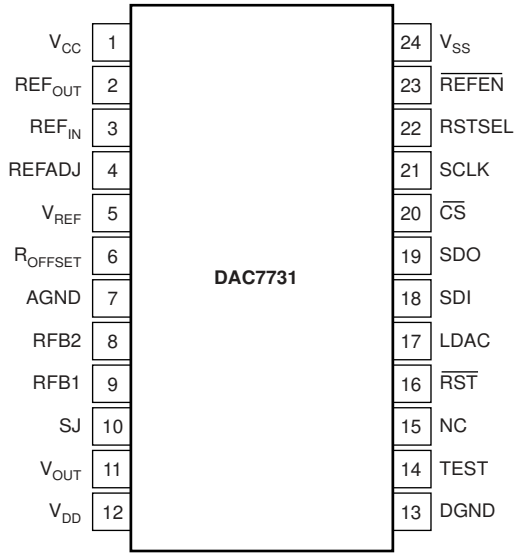
PACKAGE/ORDERING INFORMATION(1)

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER(2)	TRANSPORT MEDIA, QUANTITY
DAC7731E	SSOP-24	DB	–40°C to +85°C	DAC7731E	DAC7731E	Rails, 60
"	"	"	"	"	DAC7731E/1K	Tape and Reel,1000
DAC7731EB	SSOP-24	DB	–40°C to +85°C	DAC7731EB	DAC7731EB	Rails, 60
"	"	"	"	"	DAC7731EB/1K	Tape and Reel, 1000
DAC7731EC	SSOP-24	DB	–40°C to +85°C	DAC7731EC	DAC7731EC	Rails, 60
"	"	"	"	"	DAC7731EC/1K	Tape and Reel, 1000

NOTE: (1) For the most current package ordering information, see the Package Option Addendum at the end of this data sheet, or see the TI web site at www.ti.com.

PIN CONFIGURATION

Top View **SSOP**



NOTE: $\overline{RST}$, LDAC, SDI, $\overline{CS}$ and SCK are Schmitt-triggered inputs.

PIN DESCRIPTIONS

PIN	NAME	DESCRIPTION
1	V_{CC}	Positive Analog Power Supply
2	REF_{OUT}	Internal Reference Output
3	REF_{IN}	Reference Input
4	REFADJ	Internal Reference Trim. (Acts as a gain adjustment input when the internal reference is used.)
5	V_{REF}	Buffered Output from REF_{IN}, can be used to drive external devices. Internally, this pin directly drives the DAC's circuitry.
6	R_{OFFSET}	Offsetting Resistor
7	AGND	Analog ground
8	RFB2	Feedback Resistor 2, used to configure DAC output range.
9	RFB1	Feedback Resistor 1, used to configure DAC output range.
10	SJ	Summing Junction of the Output Amplifier
11	V_{OUT}	DAC Voltage Output
12	V_{DD}	Digital Power Supply
13	DGND	Digital Ground
14	TEST	Reserved, Connect to DGND
15	NC	No Connection
16	$\overline{RST}$	V_{OUT} reset; active LOW, depending on the state of RSTSEL, the DAC register is either reset to mid-scale or min-scale.
17	LDAC	DAC register load control, rising dege triggered. Data is loaded from the input register to the DAC register.
18	SDI	Serial Data Input. Data is latched into the input register on the rising edge of SCLK.
19	SDO	Serial Data Output, delayed 16 SCLK clock cycles.
20	$\overline{CS}$	Chip Select, Active LOW
21	SCLK	Serial Clock Input
22	RSTSEL	Reset Select; determines the action of $\overline{RST}$. If HIGH, $\overline{RST}$ will reset the DAC register to mid-scale. If LOW, $\overline{RST}$ will reset the DAC register to min-scale.
23	$\overline{REFEN}$	Enables internal +10V reference (REF_{OUT}), active LOW.
24	V_{SS}	Negative Analog Power Supply

ELECTRICAL CHARACTERISTICS

All specifications at $T_A = T_{MIN}$ to T_{MAX}, V_{CC} = +15V, V_{SS} = –15V, V_{DD} = +5V, Internal reference enabled, unless otherwise noted.

PARAMETER	CONDITIONS	DAC7731E			DAC7731EB			DAC7731EC			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
ACCURACY											
Linearity Error (INL)				±6			±4			±3	LSB
	T_A = 25°C			±5			±3			±2	LSB
Differential Linearity Error (DNL)				±4			±2			±1	LSB
Monotonicity		14			15			16			Bits
Offset Error				±0.1			*			*	% of FSR
Offset Error Drift			±2			*			*		ppm/°C
Gain Error	With Internal REF			±0.4			±0.25			±0.15	% of FSR
	With External REF			±0.25			±0.1			*	% of FSR
Gain Error Drift	With Internal REF		±15			±10			±7		ppm/°C
PSRR (V_{CC} or V_{SS})	At Full-Scale		50	200		*	*		*	*	ppm/V
ANALOG OUTPUT[1]											
Voltage Output[2]	+11.4/–4.75		0 to 10			*			*		V
	+11.4/–11.4		±10			*			*		V
	+11.4/–6.4		±5			*			*		V
Output Current		±5			*			*			mA
Output Impeadance			0.1			*			*		Ω
Maximum Load Capacitance			200			*			*		pF
Short-Circuit Current			±15			*			*		mA
Short-Circuit Duration	AGND		Indefinite			*			*		
REFERENCE											
Reference Output		9.96	10	10.04	9.975	*	10.025	*	*	*	V
REF_{OUT} Impedance			400			*			*		Ω
REF_{OUT} Voltage Drift			±15			±10			±7		ppm/°C
REF_{OUT} Voltage Adjustment[3]		±25			*			*			mV
REF_{IN} Input Range[4]		4.75		V_{CC} – 1.4	*		*	*		*	V
REF_{IN} Input Current			10			*			*		nA
REFADJ Input Range	Absolute Max Value that can be applied is V_{CC}	0		10	*		*	*		*	V
REFADJ Input Impedance			50			*			*		kΩ
V_{REF} Output Current		–2		+2	*		*	*		*	mA
V_{REF} Impedance			1			*			*		Ω
DYNAMIC PERFORMANCE											
Settling Time to ±0.003%	20V Output Step R_L = 5kΩ, C_L = 200pF, with external REF_{OUT} to REF_{IN} filter[5]		3	5		*	*		*	*	µs
Digital Feedthrough			2			*			*		nV-s
Output Noise Voltage	at 10kHz		100			*			*		nV/√Hz
DIGITAL INPUT											
V_{IH}	$\|I_H\|$ < 10µA	0.7 • V_{DD}			*			*			V
V_{IL}	$\|I_L\|$ < 10µA			0.3 • V_{DD}			*			*	V
DIGITAL OUTPUT											
V_{OH}	I_{OH} = –0.8mA	3.6			*			*			V
V_{OL}	I_{OL} = 1.6mA			0.4			*			*	V
POWER SUPPLY											
V_{DD}		+4.75	+5.0	+5.25	*	*	*	*	*	*	V
V_{CC}		+11.4		+15.75	*		*	*		*	V
V_{SS}	Bipolar Operation	–15.75		–11.4	*		*	*		*	V
	Unipolar Opeation	–15.75		–4.75	*		*	*		*	V
I_{DD}			100			*			*		µA
I_{CC}	Unloaded		4	6		*	*		*	*	mA
I_{SS}	Unloaded	–4	–2.5		*	*		*	*		mA
Power	No Load, Ext. Reference		85			*			*		mW
	No Load, Int. Reference		100	150		*	*		*	*	mW
TEMPERATURE RANGE											
Specified Performance		–40		+85	*		*	*		*	°C

* Specifications same as grade to the left.

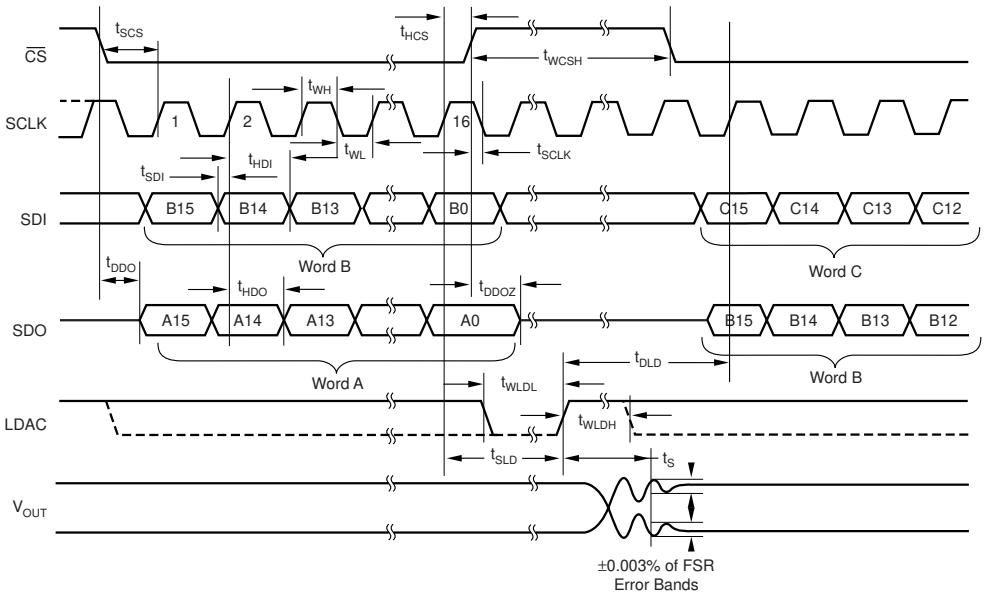
NOTES: (1) With minimum V_{CC}/V_{SS} requirements, internal reference enabled.
(2) Please refer to the *Theory of Operation* section for more information with respect to output voltage configurations.
(3) See Figure 11 for gain and offset adjustment connection diagrams when using the internal reference.
(4) The minimum value for REF_{IN} must be equal to the greater of V_{SS} +14V and +4.75V, where +4.75V is the minimum voltage allowed.
(5) Reference low-pass filter values: 100kΩ, 1.0µF (see Figure 14).

TIMING CHARACTERISTICS

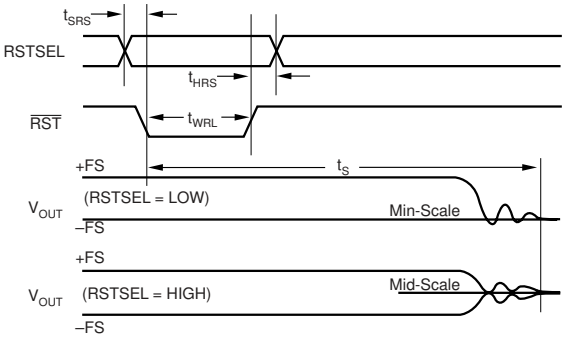
V_{CC} = +15V, V_{SS} = –15V, V_{DD} = 5V; R_L = 2kΩ to AGND; C_L = 200pF to AGND; all specifications –40°C to +85°C, unless otherwise noted.

PARAMETER	DESCRIPTION	DAC7731			UNITS
		MIN	TYP	MAX	
t_{WH}	SCLK HIGH Time	25			ns
t_{WL}	SCLK LOW Time	25			ns
t_{SDI}	Setup Time: Data in valid before rising SCLK	5			ns
t_{HDI}	Hold Time: Data in valid after rising SCLK	20			ns
t_{SCS}	Setup Time: $\overline{CS}$ falling edge before first rising SCLK	15			ns
t_{HSC}	Hold Time: $\overline{CS}$ rising edge after 16th rising SCLK	0			ns
t_{DDO}	Delay Time: $\overline{CS}$ Falling Edge to Data Out valid, C_L = 20pF on SDO	50			ns
t_{HDO}	Hold Time: Data Out valid after SCLK rising edge, C_L 20pF on SDO	50			ns
t_{DDOZ}	Delay Time: $\overline{CS}$ rising edge to SDO = High Impedance			70	ns
t_{WCSH}	$\overline{CS}$ HIGH Time	50			ns
t_{WLDL}	LDAC LOW Time	20			ns
t_{WLDH}	LDAC HIGH Time	20			ns
t_{SLD}	Setup Time: 16th Rising SCLK Before LDAC Rising Edge	15			ns
t_{DLD}	Delay Time: LDAC rising edge to first SCLK rising edge of next transfer cycle.	15			ns
t_{SCLK}	Setup Time: $\overline{CS}$ High before falling SCLK edge following 16th rising SCLK edge	5			ns
t_{SRS}	Setup Time: RSTSEL Valid Before $\overline{RST}$ LOW	0			ns
t_{HRS}	Hold Time: RSTSEL valid after $\overline{RST}$ HIGH	20			ns
t_{WRL}	$\overline{RST}$ LOW Time	30			ns
t_S	DAC V_{OUT} Settling Time			5	µs

INTERFACE TIMING



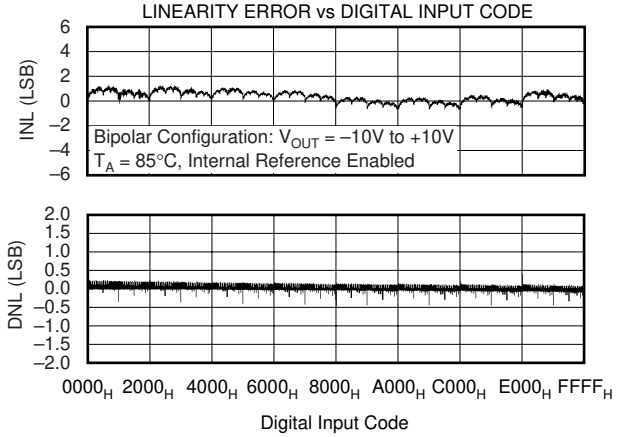
RESET TIMING



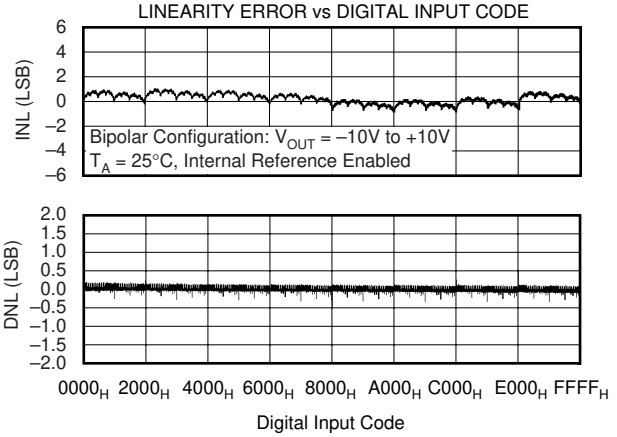
TYPICAL CHARACTERISTICS

T_A = +25°C (unless otherwise noted).

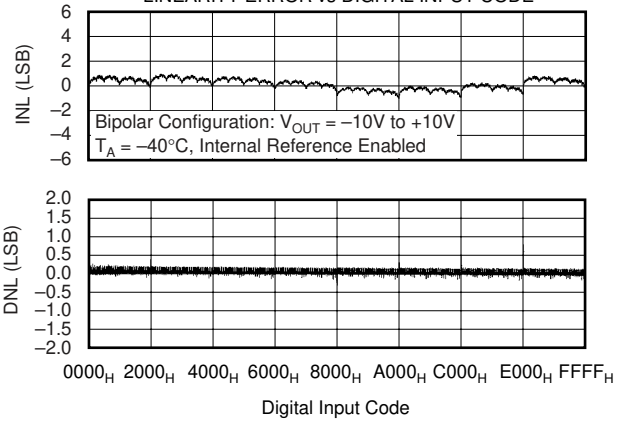
LINEARITY ERROR AND DIFFERENTIAL LINEARITY ERROR vs DIGITAL INPUT CODE



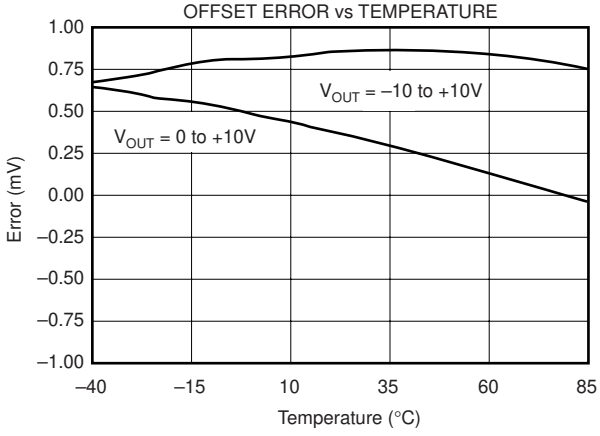
LINEARITY ERROR AND DIFFERENTIAL LINEARITY ERROR vs DIGITAL INPUT CODE



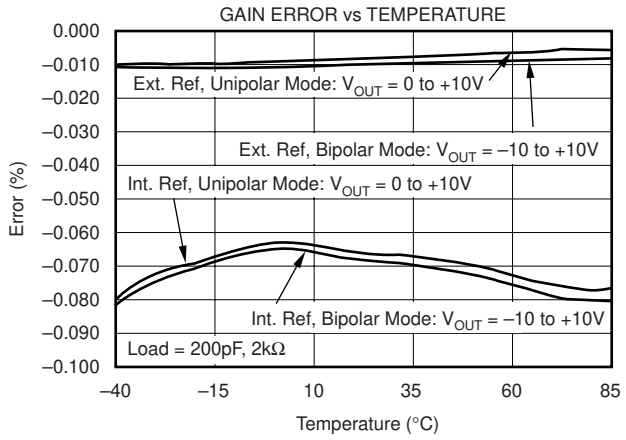
LINEARITY ERROR AND DIFFERENTIAL LINEARITY ERROR vs DIGITAL INPUT CODE



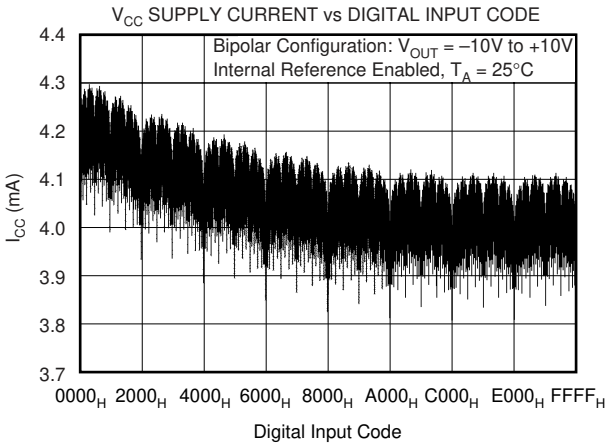
OFFSET ERROR vs TEMPERATURE



GAIN ERROR vs TEMPERATURE



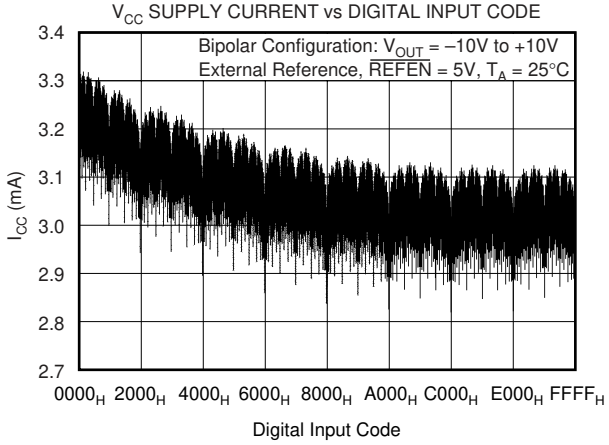
V_{CC} SUPPLY CURRENT vs DIGITAL INPUT CODE



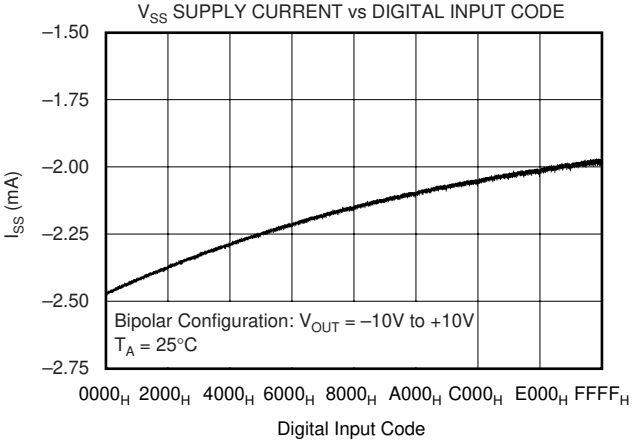
TYPICAL CHARACTERISTICS (Cont.)

T_A = +25°C (unless otherwise noted).

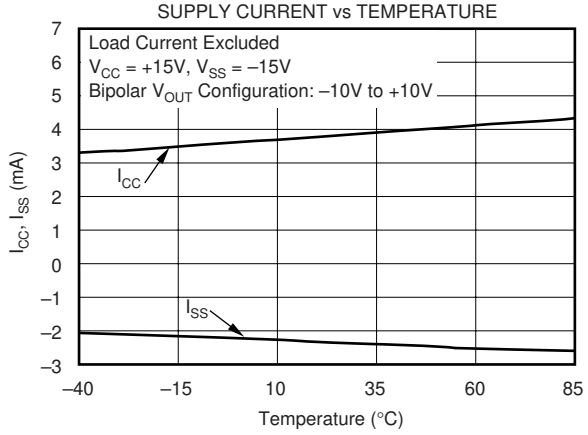
V_{CC} SUPPLY CURRENT vs DIGITAL INPUT CODE



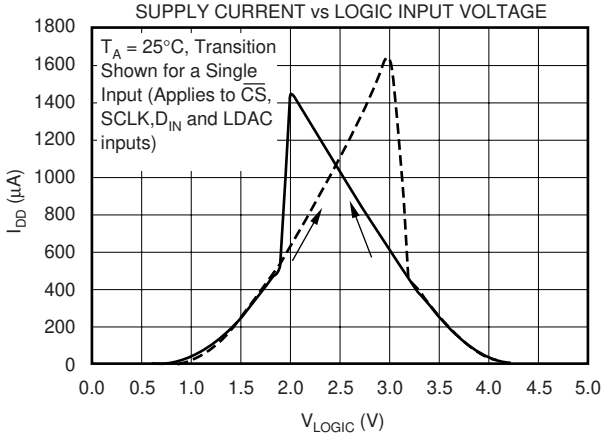
V_{SS} SUPPLY CURRENT vs DIGITAL INPUT CODE



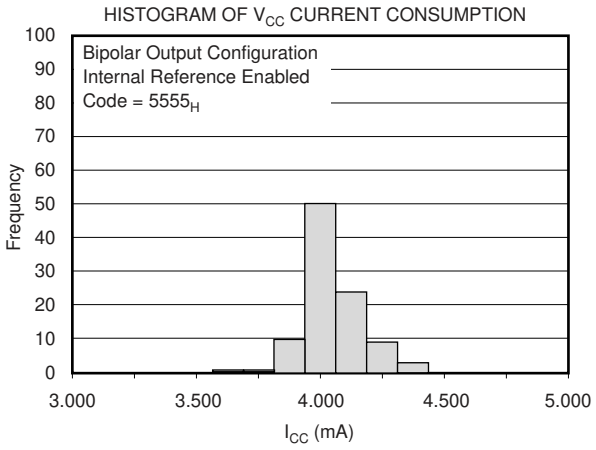
SUPPLY CURRENT vs TEMPERATURE



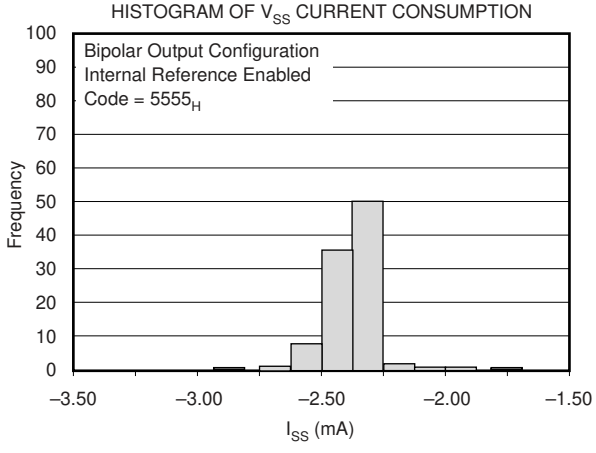
SUPPLY CURRENT vs LOGIC INPUT VOLTAGE



HISTOGRAM OF V_{CC} CURRENT CONSUMPTION



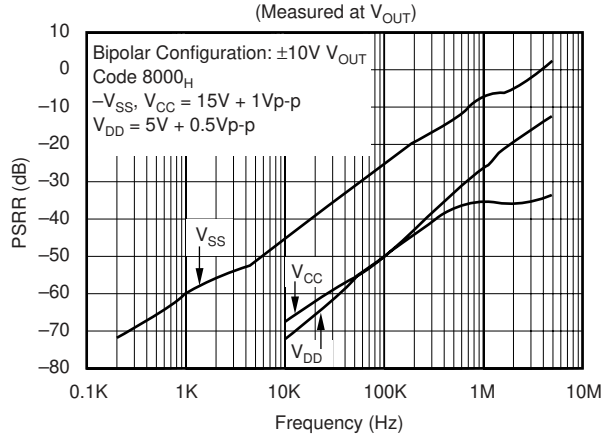
HISTOGRAM OF V_{SS} CURRENT CONSUMPTION



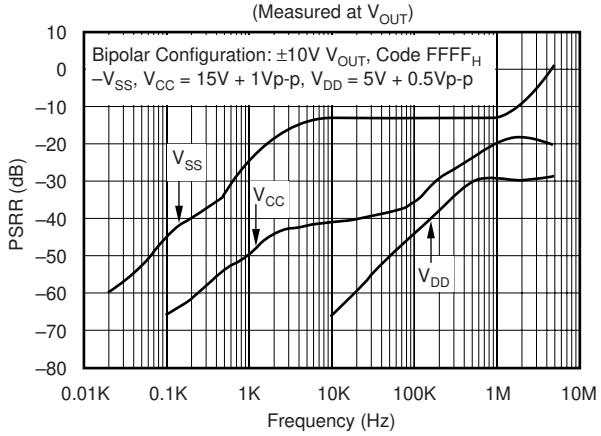
TYPICAL CHARACTERISTICS (Cont.)

T_A = +25°C (unless otherwise noted).

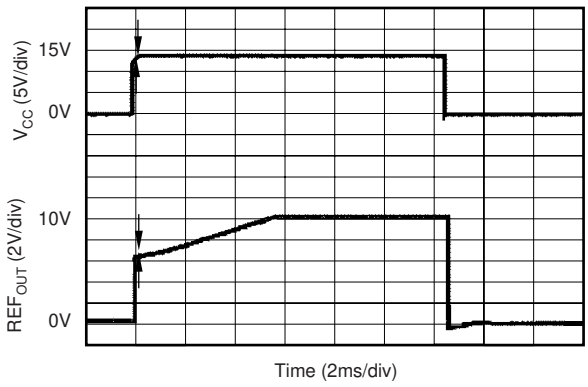
POWER-SUPPY REJECTION RATIO vs FREQUENCY
(Measured at V_{OUT})



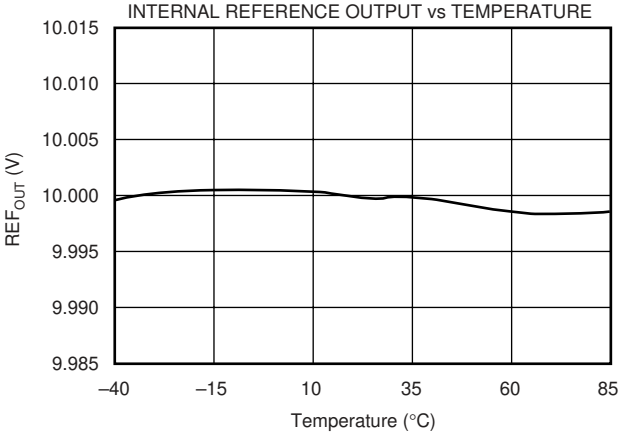
POWER-SUPPY REJECTION RATIO vs FREQUENCY
(Measured at V_{OUT})



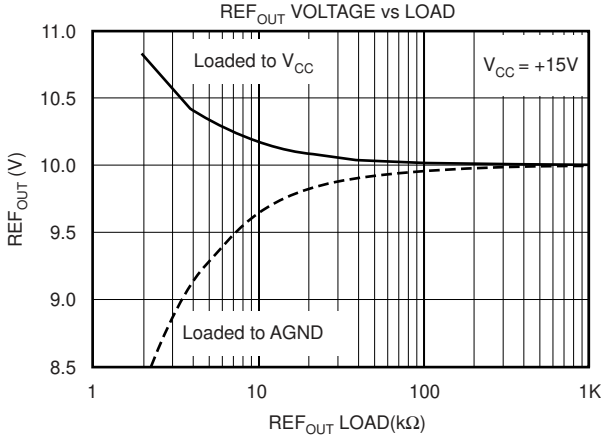
INTERNAL REFERENCE START-UP



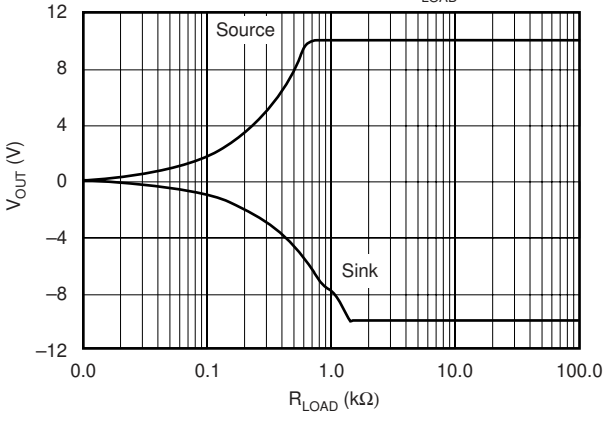
INTERNAL REFERENCE OUTPUT vs TEMPERATURE



REF_{OUT} VOLTAGE vs LOAD



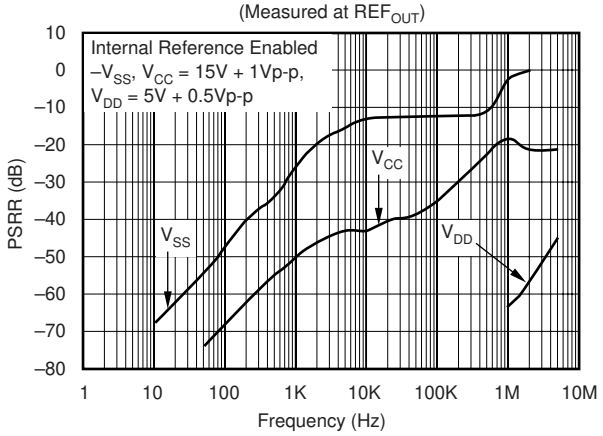
OUTPUT VOLTAGE vs R_{LOAD}



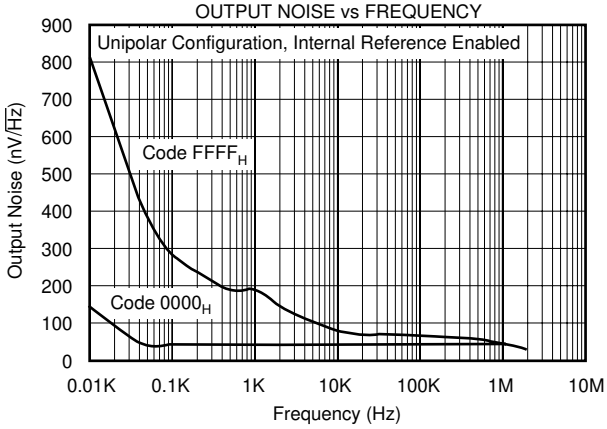
TYPICAL CHARACTERISTICS (Cont.)

T_A = +25°C (unless otherwise noted).

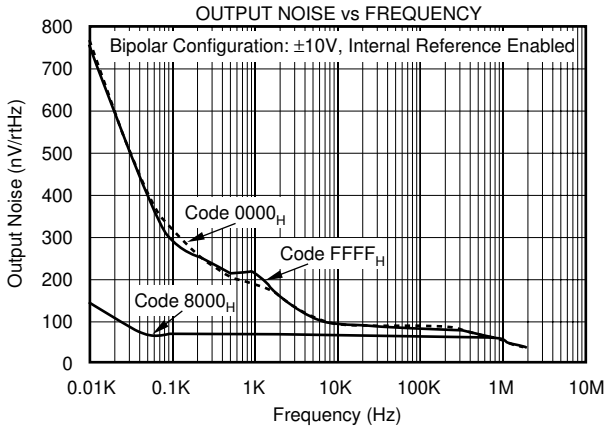
POWER-SUPPY REJECTION RATIO vs FREQUENCY
(Measured at REF_{OUT})



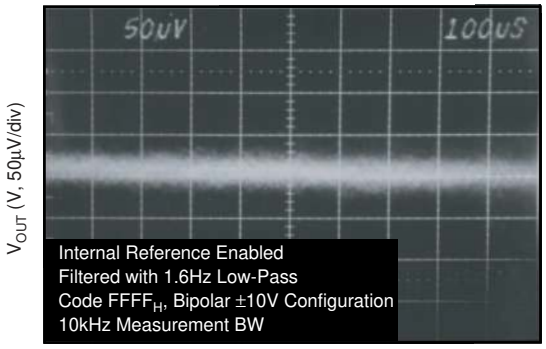
OUTPUT NOISE vs FREQUENCY



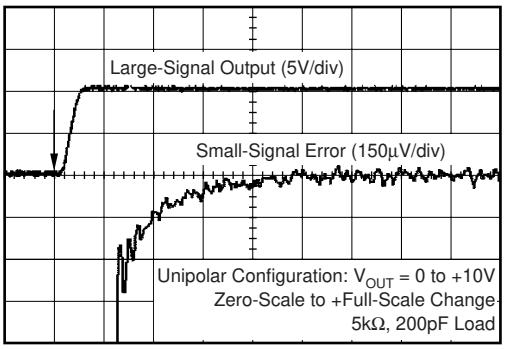
OUTPUT NOISE vs FREQUENCY



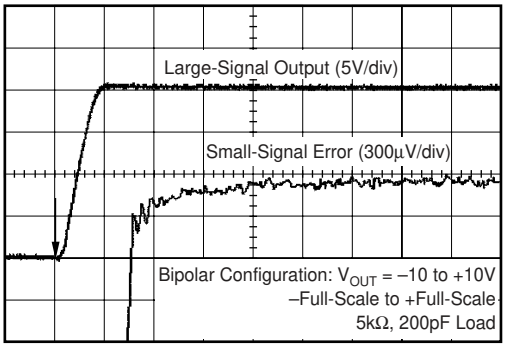
BROADBAND NOISE



UNIPOLAR FULL-SCALE SETTLING TIME



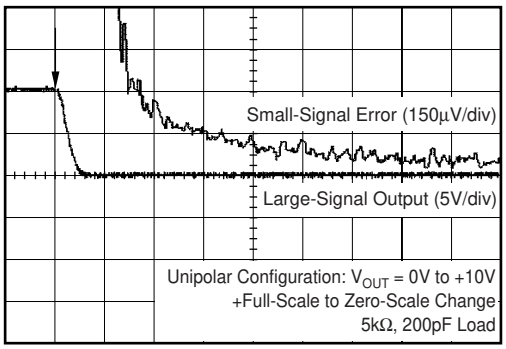
BIPOLAR FULL-SCALE SETTLING TIME



TYPICAL CHARACTERISTICS (Cont.)

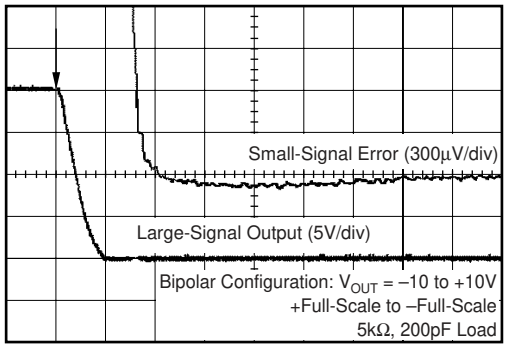
T_A = +25°C (unless otherwise noted).

UNIPOLAR FULL-SCALE SETTLING TIME



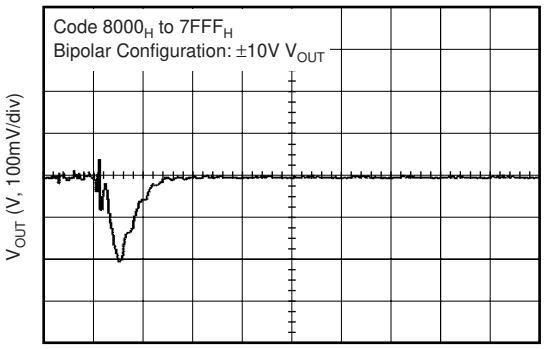
Time (2µs/div)

BIPOLAR FULL-SCALE SETTLING TIME



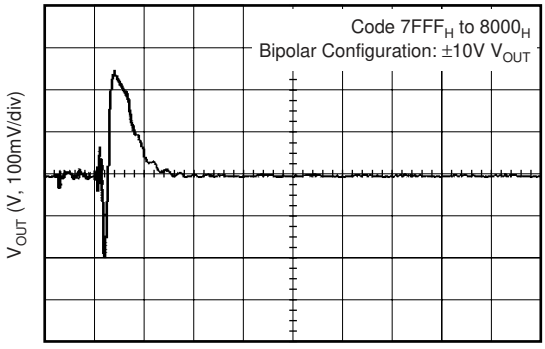
Time (2µs/div)

MID-SCALE GLITCH



Time (1µs/div)

MID-SCALE GLITCH



Time (1µs/div)

THEORY OF OPERATION

The DAC7731 is a voltage output, 16-bit DAC with a +10V built-in internal reference. The architecture is an R-2R ladder configuration with the three MSBs segmented, followed by an operational amplifier that serves as a buffer, as shown in Figure 1. The output buffer is designed to allow user-configurable output adjustments giving the DAC7731 output voltage ranges of 0V to +10V, –5V to +5V, or –10V to +10V. Please refer to Figures 2, 3, and 4 for pin configuration information.

The digital input is a serial word made up of the DAC code (MSB first) and is loaded into the DAC register using the LDAC input pin. The converter can be powered from ±12V to ±15V dual analog supplies and a +5V logic supply. The device offers a reset function, which immediately sets the DAC output voltage and DAC register to min-scale (code 0000_H) or mid-scale (code 8000_H). The data I/O and reset functions are discussed in more detail in the following sections.

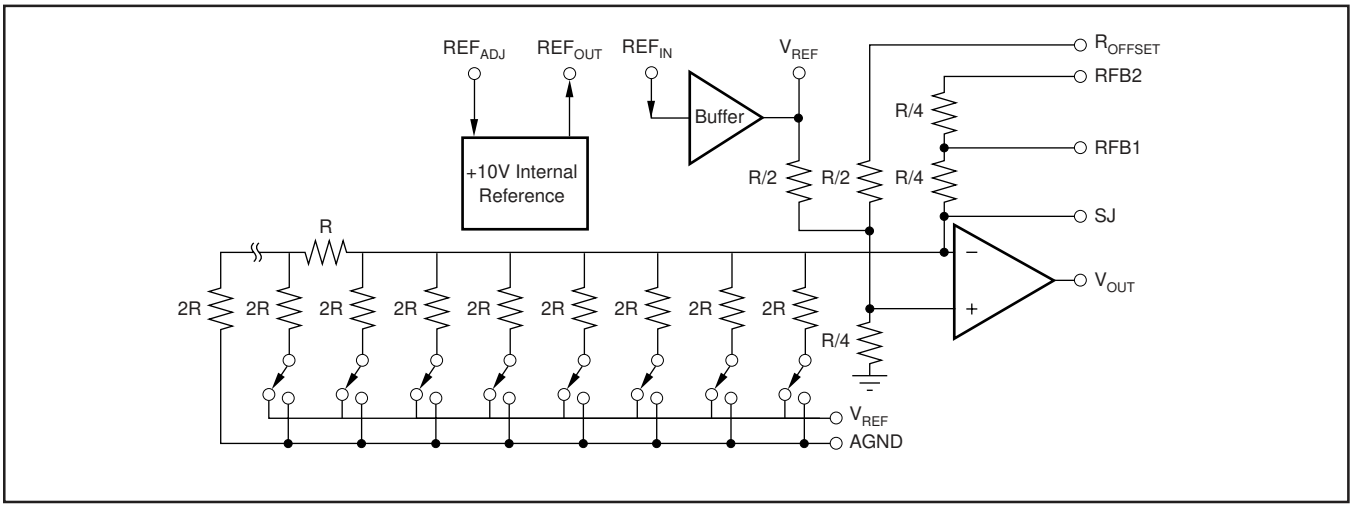


FIGURE 1. DAC7731 Architecture.

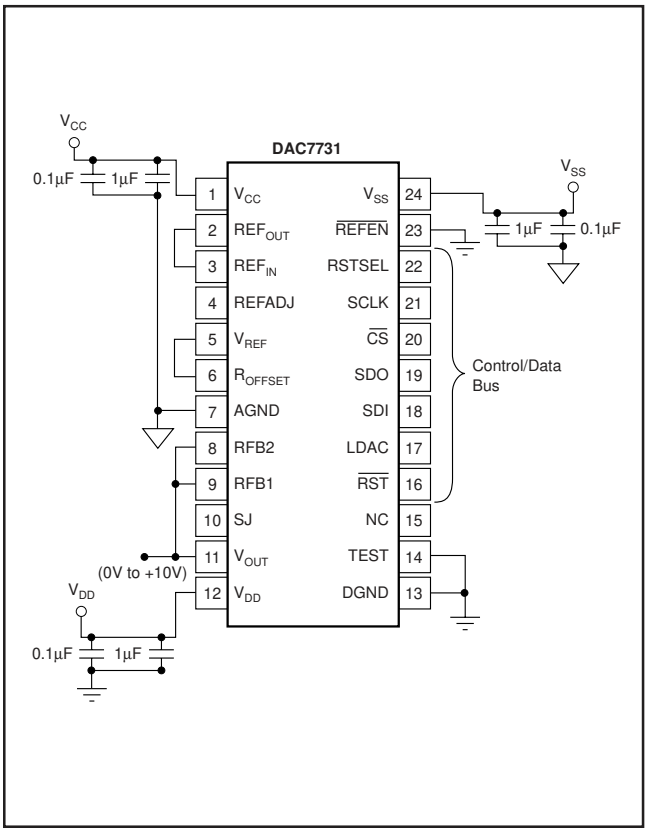


FIGURE 2. Basic Operation: V_{OUT} = 0V to +10V.

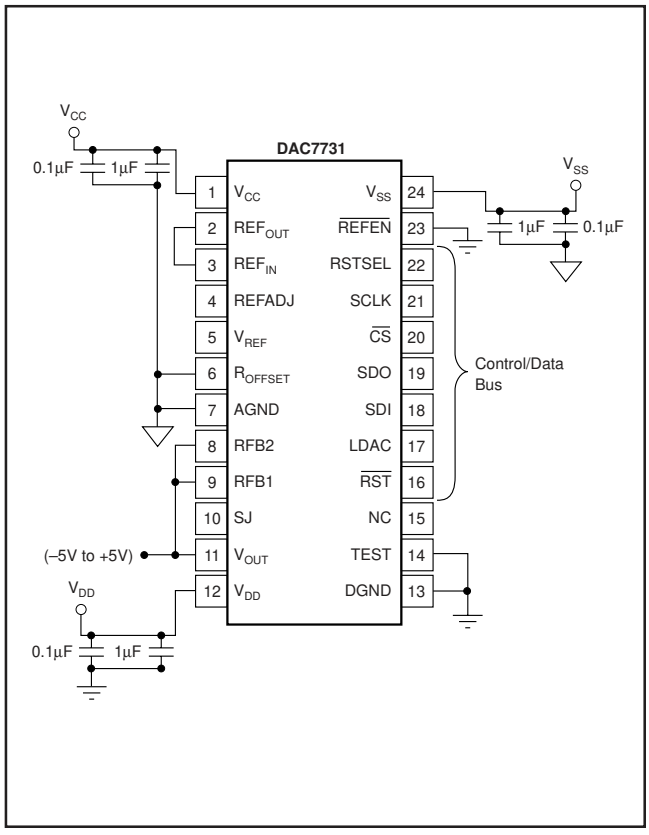


FIGURE 3. Basic Operation: V_{OUT} = –5V to +5V.

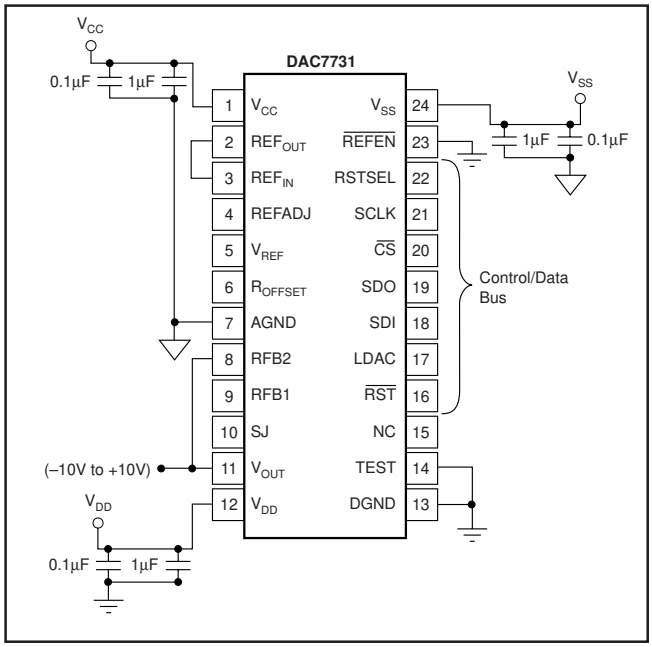


FIGURE 4. Basic Operation: V_{OUT} = –10V to +10V.

ANALOG OUTPUTS

The output amplifier can swing to within 1.4V of the supply rails, specified over the –40°C to +85°C temperature range. This allows for a ±10V DAC voltage output operation from ±12V supplies with a typical 5% tolerance.

When the DAC7731 is configured for a unipolar, 0V to 10V output, a negative voltage supply is required. This is due to internal biasing of the output stage. Please refer to the Electrical Characteristics table (see page 3) for more information.

The minimum and maximum voltage output values are dependent upon the output configuration implemented and reference voltage applied to the DAC7731. Please note that V_{SS} (the negative power supply) must be in the range of –4.75V to –15.75V for unipolar operation. The voltage on V_{SS} sets several bias points within the converter and is required in all modes of operation. If V_{SS} is not in one of these two configurations, the bias values may be in error and proper operation of the device is not ensured.

Supply sequence is important in establishing the correct startup of the DAC. The following supply sequence must be followed: V_{SS} (device substrate) first, then V_{DD} followed by V_{CC}. In addition, each supply must reach the values specified in the Electrical Characteristics table (see page 3) within 100ms of its ramp start.

REFERENCE INPUTS

The DAC7731 provides a built-in +10V voltage reference and on-chip buffer to allow external component reference drive. To use the internal reference, $\overline{REFEN}$ must be LOW, enabling the reference circuitry of the DAC7731 (as shown in Table I) and the REF_{OUT} pin must be connected to REF_{IN}. This is the input to the on-chip reference buffer. The buffer output is provided at the V_{REF} pin. In this configuration, V_{REF} is used to setup the DAC7731 output amplifier into one of three voltage output modes as discussed earlier. V_{REF} can also be used to drive other system components requiring an external reference.

$\overline{REFEN}$	ACTION
1	Internal Reference disabled; REF_{OUT} = High Impedance
0	Internal Reference enabled; REF_{OUT} = +10V

TABLE I. $\overline{REFEN}$ Action.

The internal reference of the DAC7731 can be disabled when use of an external reference is desired. When using an external reference, the reference input, REF_{IN}, can be any voltage between 4.75V (or V_{SS} + 14V, whichever is greater) and V_{CC} – 1.4V.

DIGITAL INTERFACE

Table II shows the input data format for the DAC7731 and Table III illustrates the basic control logic of the device. The serial interface consists of a chip select input ($\overline{CS}$), serial data clock input (SCLK), serial data input (SDI), serial data output (SDO), and load control input (LDAC). An asynchronous reset input ($\overline{RST}$), which is active LOW, is provided to simplify start-up conditions, periodic resets, or emergency resets to a known state, depending on the status of the reset select (RSTSEL) signal. Please refer to the *DAC Reset* section for additional information regarding the reset operation.

DIGITAL INPUT	ANALOG OUTPUT	
	Unipolar Configuration	Bipolar Configuration
	Unipolar Straight Binary	Bipolar Offset Binary
0x0000	Zero (0V)	–Full-Scale (–V_{REF} or –V_{REF}/2)
0x0001	Zero + 1LSB	–Full-Scale + 1LSB
:	:	:
0x8000	1/2 Full-Scale	Bipolar Zero
0x8001	1/2 Full-Scale + 1LSB	Bipolar Zero + 1LSB
:	:	:
0xFFFF	Full-Scale (V_{REF} – 1LSB)	+Full-Scale (+V_{REF} – 1LSB or +V_{REF}/2 – 1LSB)

TABLE II. DAC7731 Data Format.

CONTROL STATUS					COMMAND
$\overline{CS}$	$\overline{RST}$	RSTSEL	LDAC	SCLK	ACTION
H	H	X	X	X	Shift Register is disabled on the serial bus.
L	H	X	X	X	Enable SDO pin from High Impedance; enables shift operation and I/O bus (SCLK, SDI, SDO).
L	H	X	X	↑	Serial Data Shifted into Input Register
↑	H	X	X	L	Serial Data Shifted into Input Register(1)
X	H	X	↑	X	Data in Input Register is Loaded into DAC Register.
X	L	H	X	X	Resets Input and DAC Registers to mid-scale.
X	L	L	X	X	Resets Input and DAC Registers to min-scale.

NOTE: (1) In order to avoid unwanted shifting of the input register by an additional bit, care must be taken that a rising edge on $\overline{CS}$ only occurs when SCLK is HIGH.

TABLE III. DAC7731 Logic Truth Table.

The DAC code is provided via a 16-bit serial interface, as shown in Table II. The digital input word makes up the digital code to be loaded into the data input register of the device. A typical data transfer and DAC output update take place as follows: Once $\overline{CS}$ is active (LOW), the DAC7731 is enabled on the serial bus and the 16-bit serial data transfer can begin. The serial data is shifted into the device on each rising SCLK edge until all 16 bits are transferred (1 bit per 1 rising SCLK edge). Once received, the data in the input register is loaded into the DAC register upon reception of a rising edge on the LDAC input (load command). This action updates the analog output, V_{OUT}, to the desired voltage specified by the digital input word. A rising edge on LDAC is completely asynchronous to the serial interface of the device and can occur at any time. Care must be taken to ensure that the entire 16 bits of data are loaded into the input register before issuing a LDAC active edge. Additional load commands will have no effect on the DAC output if the data in the input register is unchanged between rising LDAC edges. When $\overline{CS}$ is returned HIGH, the rising edge on $\overline{CS}$ must occur when SCLK is HIGH. Application of a rising $\overline{CS}$ edge when SCLK is LOW will cause one additional shift in the serial input shift register, corrupting the desired input data.

TIMING CONSIDERATIONS

The flexible interface of the DAC7731 can operate under a number of different scenarios as is required by a host controller. Critical timing for a 16-bit data transfer cycle is shown in the Interface Timing section of the Timing Characteristics. While this is the most common method of writing to the DAC7731, the device accepts two additional modes of data transfer from the host. These are byte transfer mode and continuous transfer mode.

Byte transfer mode is especially useful when an 8-bit host is communicating with the DAC. Data transfer can occur without requiring an additional general purpose I/O pin to control the $\overline{CS}$ input of the DAC in cycles of 16 clocks. A HIGH state on $\overline{CS}$ stops data from coming into and out of the internal shift register. This provides byte-wide support for 8-bit host processors. Figure 5 is an example of the timing cycle of such a data transfer.

The remaining data transfer mode accepted by the DAC7731 is continuous transfer. The $\overline{CS}$ of the DAC7731 can be tied LOW or held LOW by the controller for an indefinite number of serial clock cycles. Each clock cycle will transfer data into the

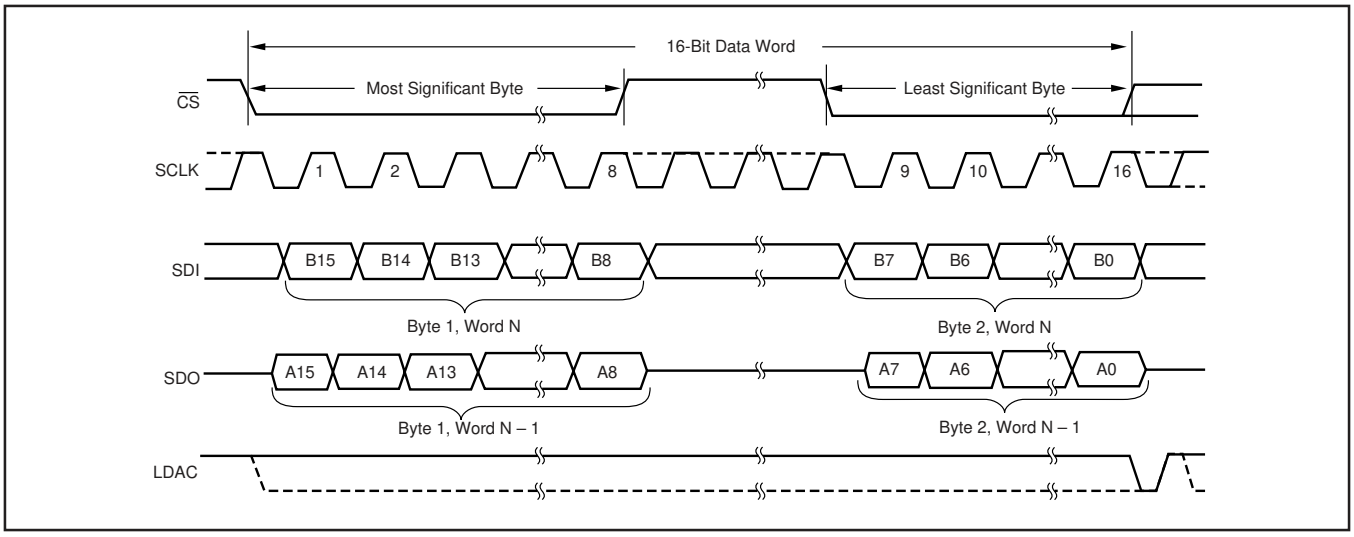


FIGURE 5. Byte-Wide Data Write Cycle.

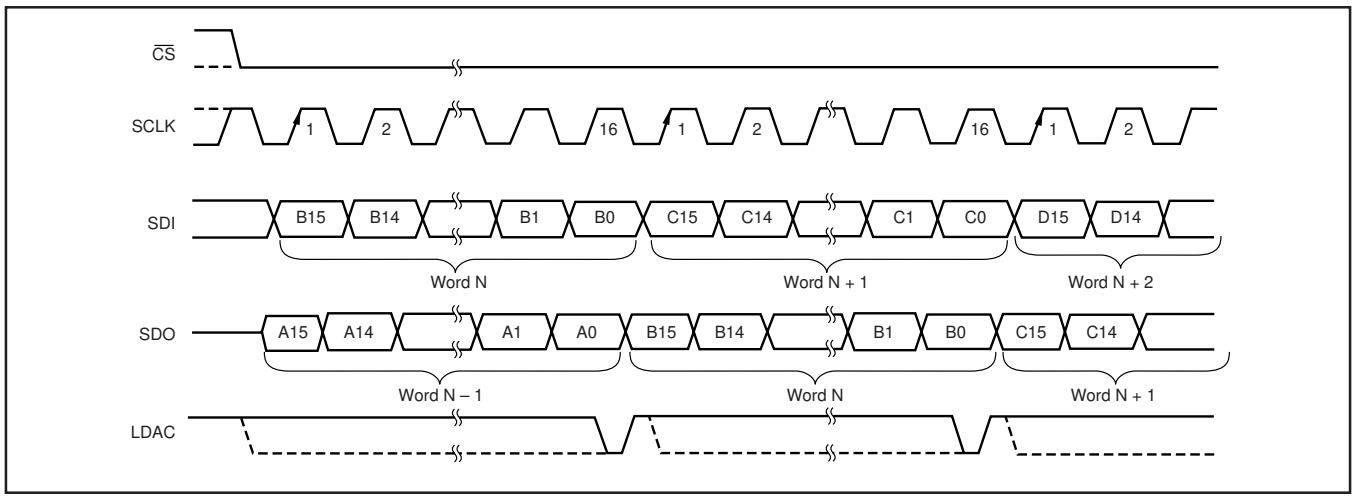


FIGURE 6. Continuous Transfer Control.

DAC via SDI and out of the DAC on SDO. Care must be taken that the LDAC signal to the DAC(s) is timed correctly so that valid data is transferred into the DAC register on each rising LDAC edge. (*Valid data* refers to the serial data latched on each of the 16 rising SCLK edges prior to the occurrence of a rising LDAC signal.) The rising edge of LDAC must occur before the first rising SCLK edge of the following 16-bit transfer. Figure 6 shows continuous transfer timing.

DAISY-CHAINING USING SDO

Multiple DAC7731s can be connected to a single serial port by attaching each of their control inputs in parallel and daisy-chaining the SDO and SDI I/Os of each device. The SDO output of the DAC7731 is active when $\overline{CS}$ is LOW and can be left unconnected when not required for use in a daisy-chain configuration.

Once a data transfer cycle begins, new data is shifted into SDI and data currently residing in the shift register (from previous cycle, power-up, or reset command) is presented on SDO, MSB first. One data transfer cycle for each DAC7731 is required to update all devices in the chain. The first data cycle written into the chain will arrive at the last DAC7731 on the final cycle of the data transfer. Upon completion of the required number of data transfer cycles (one cycle per device), each DAC voltage output is updated with a rising edge on the LDAC inputs. Figure 7 shows the required timing to properly update two DAC7731s in a daisy-chained configuration, as shown in Figure 8.

DAC RESET

The $\overline{RST}$ and RSTSEL inputs control the reset of the analog output. The reset command is level triggered by a low signal on $\overline{RST}$. Once $\overline{RST}$ is LOW, the DAC output will begin settling to the mid-scale or min-scale code depending on the state of the RSTSEL input. A HIGH value on RSTSEL will cause V_{OUT} to reset to the mid-scale code (8000_H) and a LOW value will reset V_{OUT} to min-scale (8000_H). A change in the state of the RSTSEL input while $\overline{RST}$ is LOW will cause a corresponding change in the reset command selected internally and consequently change the output value of V_{OUT} of the DAC. Note that a valid reset signal also resets the input register of the DAC to the value specified by the state of RSTSEL.

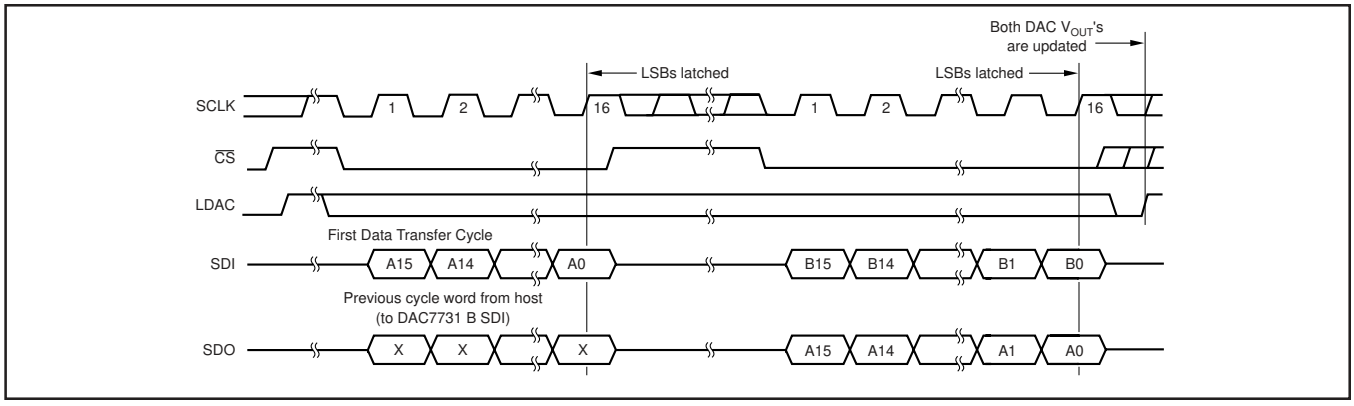


FIGURE 7. DAC7731 Daisy-Chain Timing for Figure 7.

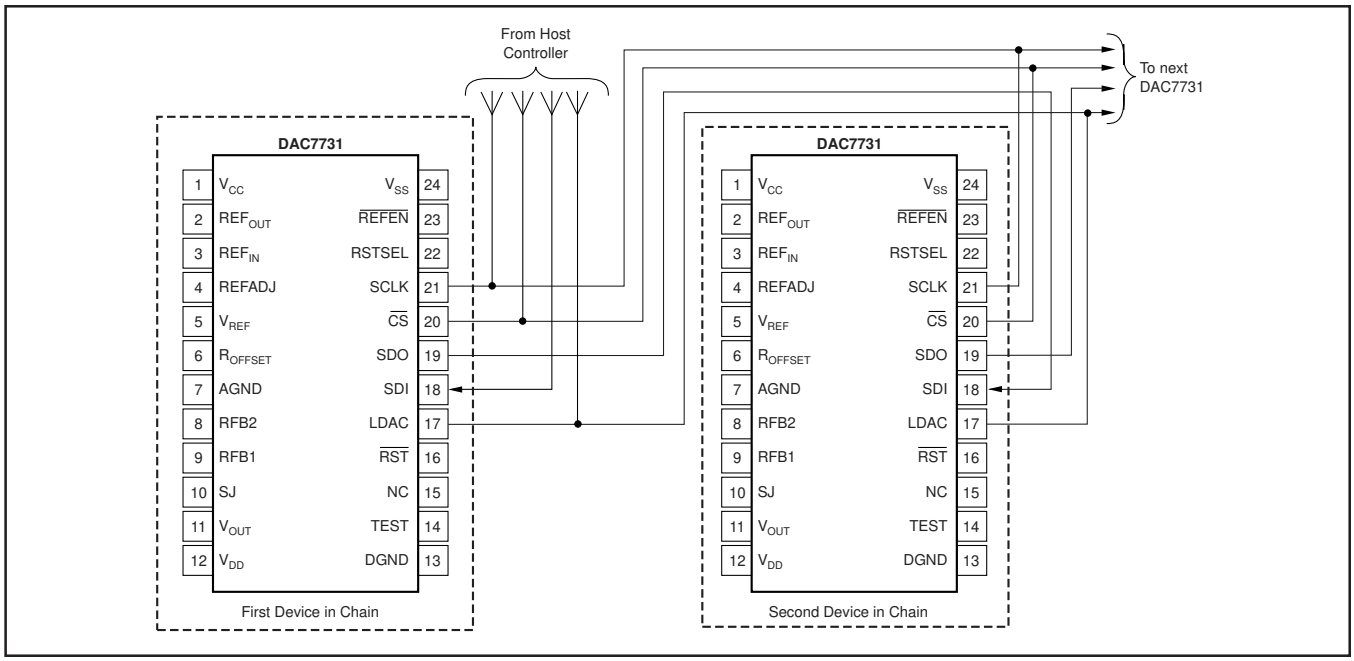


FIGURE 8. DAC7731 Daisy-Chain Schematic.

APPLICATIONS

GAIN AND OFFSET CALIBRATION

The architecture of the DAC7731 is designed in such a way as to allow for easily configurable offset and gain calibration using a minimum of external components. The DAC7731 has built-in feedback resistors and output amplifier summing points brought out of the package in order to make the absolute calibration possible. Figures 9 and 10 illustrate the relationship of offset and gain adjustments for the DAC7731 in a unipolar configuration and in a bipolar configuration, respectively.

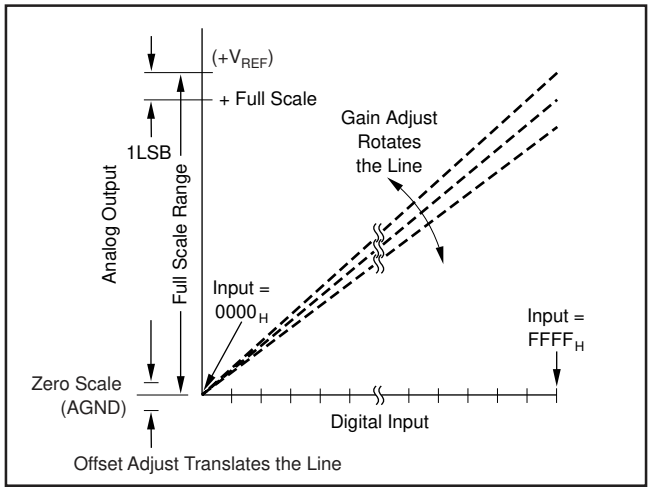


FIGURE 9. Relationship of Offset and Gain Adjustments for V_{OUT} = 0V to +10V Output Configuration.

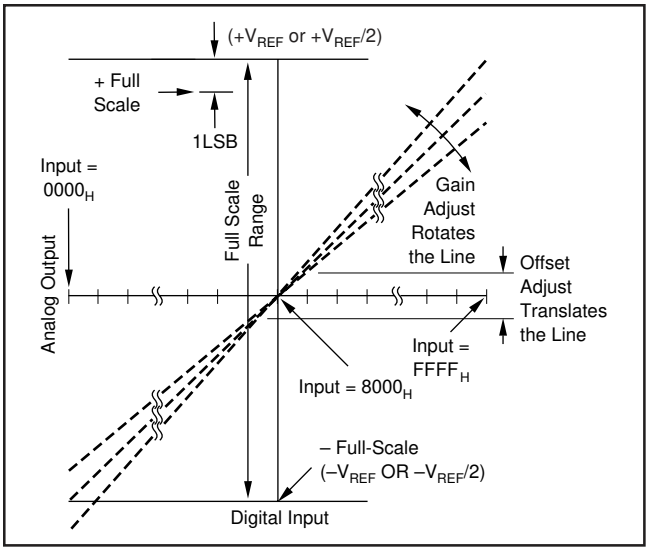


FIGURE 10. Relationship of Offset and Gain Adjustments for V_{OUT} = –10V to +10V Output Configuration. (Same Theory Applies for V_{OUT} = –5V to +5V.)

When calibrating the DAC output, offset should be adjusted first to avoid first order interaction of adjustments. In unipolar mode, the DAC7731 offset is adjusted from code 0000_H and for either bipolar mode, offset adjustments are made at code 8000_H. Gain adjustment can then be made at code $FFFF_H$ for each configuration, where the output of the DAC should be at +10V – 1LSB for the 0V to +10V or ±10V output range and +5V – 1LSB for the ±5V output range. Figure 11 shows the generalized external offset and gain adjustment circuitry using potentiometers.

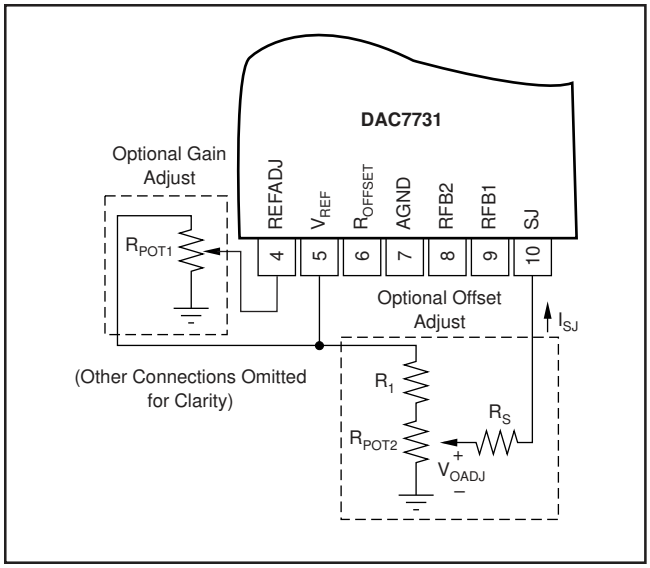


FIGURE 11. Generalized External Calibration Circuitry for Gain and Symmetrical Offset Adjustment.

OFFSET ADJUSTMENT

Offset adjustment is accomplished by introducing a small current into the summing junction (SJ) of the DAC7731. The voltage at SJ, or V_{SJ}, is dependent on the output configuration of the DAC7731. See Table IV for the required pin strapping for a given configuration and the nominal values of V_{SJ} for each output range.

REFERENCE CONFIGURATION	OUTPUT CONFIGURATION	PIN STRAPPING			V_{SJ}(1)
		R_{OFFSET}	RFB1	RFB2	
Internal Reference	0V to +10V	to V_{REF}	to V_{OUT}	to V_{OUT}	+5V
	–10V to +10V	NC	NC	to V_{OUT}	+3.333V
	–5V to +5V	to AGND	to V_{OUT}	to V_{OUT}	+1.666V
External Reference	0V to V_{REF}	to V_{REF}	to V_{OUT}	to V_{OUT}	V_{REF}/2
	–V_{REF} to V_{REF}	NC	NC	to V_{OUT}	V_{REF}/3
	–V_{REF}/2 to V_{REF}/2	to AGND	to V_{OUT}	to V_{OUT}	V_{REF}/6
NOTE: (1) Voltage measured at V_{SJ} for a given configuration.					

TABLE IV. Nominal V_{SJ} versus V_{OUT} and Reference Configuration.

The current level required to adjust the DAC7731's offset can be created by using a potentiometer divider as shown in Figure 11 Another alternative is to use a unipolar DAC in order to apply a voltage, V_{OADJ}, to the resistor R_S. A ±2uA current range applied to SJ will ensure offset adjustment coverage of the ±0.1% maximum offset specification of the DAC7731.

When in a unipolar configuration (V_{SJ} = 5V), only a single resistor, R_S, is needed for symmetrical offset adjustment with a 0V to 10V V_{OADJ} range. When in one of the two bipolar configurations, V_{SJ} is either +3.333V (±10V range) or +1.666V (±5V range), and circuit values chosen to match those given in Table V will provide symmetrical offset adjust. Please refer to Figure 11 for component configuration.

OUTPUT CONFIGURATION	R_{POT2}	R_1	R_S	I_{SJ} RANGE	NOMINAL OFFSET ADJUSTMENT
0V to +10V	10K	0	2.5M	±2µA	±25mV
–10V to +10V	10K	5K	1.5M	±2.2µA	±55mV
–5V to +5V	10K	20K	1M	±1.7µA	±21mV

TABLE V. Recommended External Component Values for Symmetrical Offset Adjustment (V_{REF} = 10V).

Figure 12 illustrates the typical minimum offset adjustment ranges provided by forcing a current at SJ for a given output voltage configuration.

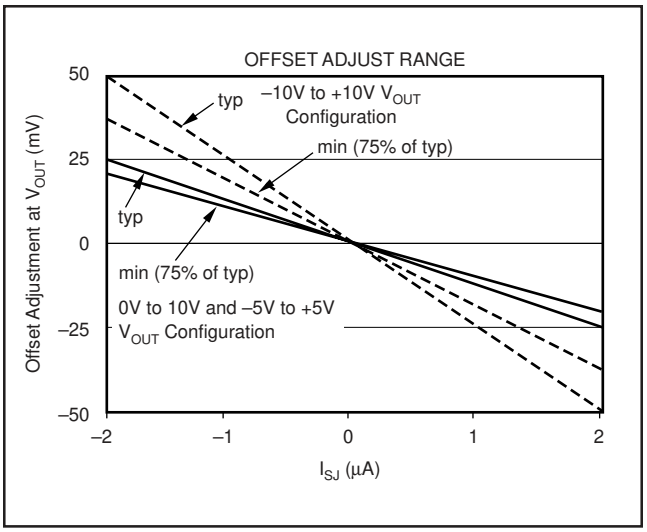


FIGURE 12. Offset Adjustment Transfer Characteristic.

GAIN ADJUSTMENT

When using the internal reference of the DAC7731, gain adjustment is performed by adjusting the device's internal reference voltage via the reference adjust pin, REFADJ. The effect of a reference voltage change on the gain of the DAC output can be seen in the generic equation (for unipolar configuration):

$$V_{OUT} = V_{REFIN} \bullet (N/65536)$$

Where N is represented in decimal format and ranges from 0 to 65535.

REFADJ can be driven by a low impedance voltage source such as a unipolar, 0V to +10V DAC or a potentiometer (less than 100kΩ), see Figure 11. Since the input impedance of REFADJ is typically 50kΩ, the smaller the resistance of the potentiometer, the more linear the adjustment will be. A 10kΩ potentiometer is suggested if linearity of the reference adjustment is of concern.

When the DAC7731's internal reference is not used, gain adjustments can be made via trimming the external reference applied to the DAC at REF_{IN}. This can be accomplished through using a potentiometer, unipolar DAC, or other means of precision voltage adjustment to control the voltage presented to the DAC7731 by the external reference. Figure 13 and Table VI summarize the range of adjustment of the internal reference via REFADJ.

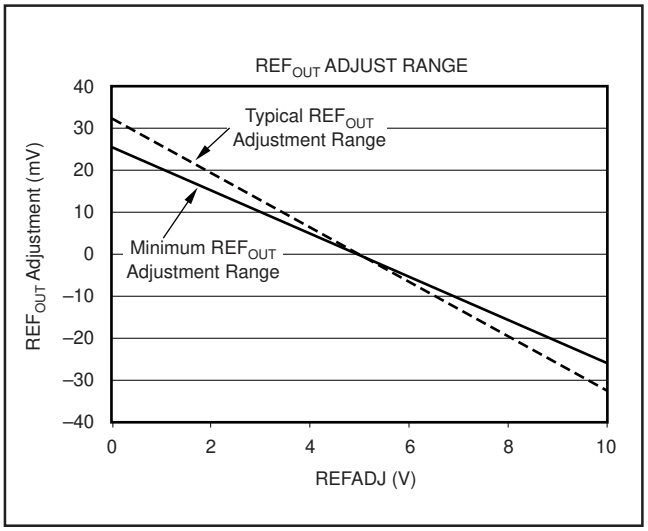


FIGURE 13. Internal Reference Adjustment Transfer Characteristic.

VOLTAGE AT REFADJ	REF_{OUT} VOLTAGE
REFADJ = 0V	10V + 25mV (min)
REFADJ = 5V or NC(1)	10V
REFADJ = 10V	10V – 25mV (max)
NOTE: NC = Not Connected.	

TABLE VI. Minimum Internal Reference Adjustment Range.

NOISE PERFORMANCE

Increased noise performance of the DAC output can be achieved by filtering the voltage reference input to the DAC7731. Figure 14 shows a typical internal reference filter schematic. A low-pass filter applied between the REF_{OUT} and REF_{IN} pins can increase noise immunity at the DAC and output amplifier. The REF_{OUT} pin can source a maximum of 50µA so care should be taken in order to avoid overloading the internal reference output.

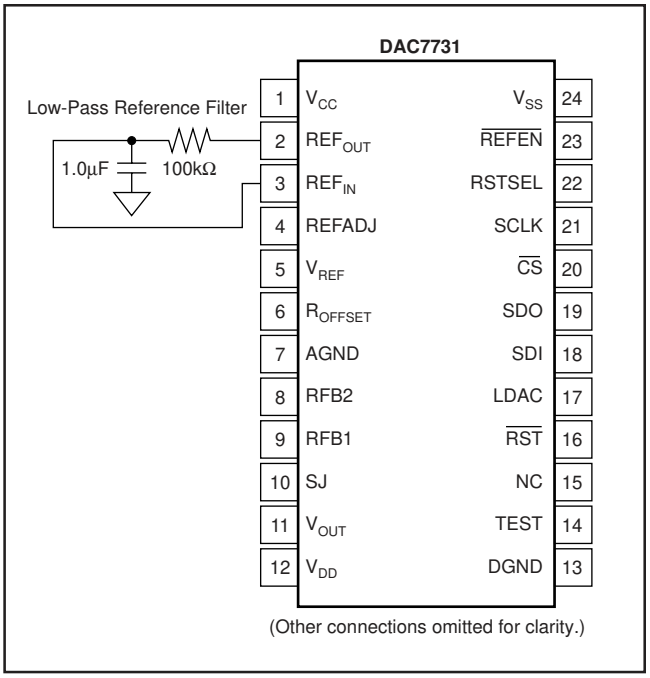


FIGURE 14. Filtering the Internal Reference.

LAYOUT

A precision analog component requires careful layout, adequate bypassing, and clean, well-regulated power supplies. The DAC7731 offers separate digital and analog supplies, as it will often be used in close proximity with digital logic, microcontrollers, microprocessors, and digital signal processors. The more digital logic present in the design and the higher the switching speed, the more important it will become to separate the analog and digital ground and supply planes at the device.

Since the DAC7731 has both analog and digital ground pins, return currents can be better controlled and have less effect on the DAC output error. Ideally, AGND would be connected directly to an analog ground plane and DGND to the digital ground plane. The analog ground plane would be separate from the ground connection for the digital components until they were connected at the power-entry point of the system.

The voltages applied to V_{CC} and V_{SS} should be well regulated and low noise. Switching power supplies and DC/DC converters will often have high-frequency glitches or spikes riding on the output voltage. In addition, digital components can create similar high-frequency spikes as their internal logic switches states. This noise can easily couple into the DAC output voltage through various paths between the power connections and analog output.

In addition, a 1μF to 10μF bypass capacitor in parallel with a 0.1μF bypass capacitor is strongly recommended for each supply input. In some situations, additional bypassing may be required, such as a 100μF electrolytic capacitor or even a Pi filter made up of inductors and capacitors–all designed to essentially low-pass filter the analog supplies, removing any high frequency noise components.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DAC7731E	ACTIVE	SSOP	DB	24	60	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	DAC7731E	Samples
DAC7731E/1K	ACTIVE	SSOP	DB	24	1000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	DAC7731E	Samples
DAC7731EB	ACTIVE	SSOP	DB	24	60	RoHS & Green	Call TI	Level-3-260C-168 HR	-40 to 85	DAC7731E B	Samples
DAC7731EB/1K	ACTIVE	SSOP	DB	24	1000	RoHS & Green	Call TI	Level-3-260C-168 HR	-40 to 85	DAC7731E B	Samples
DAC7731EC	ACTIVE	SSOP	DB	24	60	RoHS & Green	Call TI	Level-3-260C-168 HR	-40 to 85	DAC7731E C	Samples
DAC7731EC/1K	ACTIVE	SSOP	DB	24	1000	RoHS & Green	Call TI	Level-3-260C-168 HR	-40 to 85	DAC7731E C	Samples
DAC7731ECG4	ACTIVE	SSOP	DB	24	60	RoHS & Green	Call TI	Level-3-260C-168 HR	-40 to 85	DAC7731E C	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

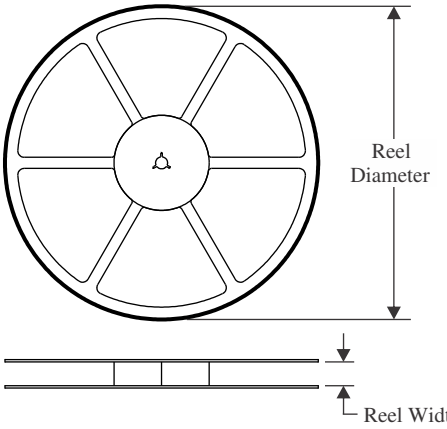
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

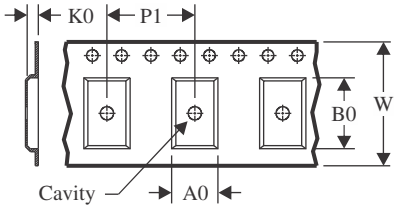
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

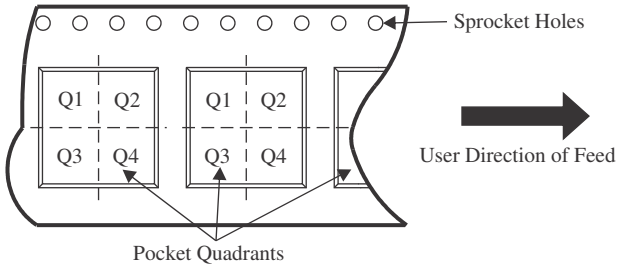


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

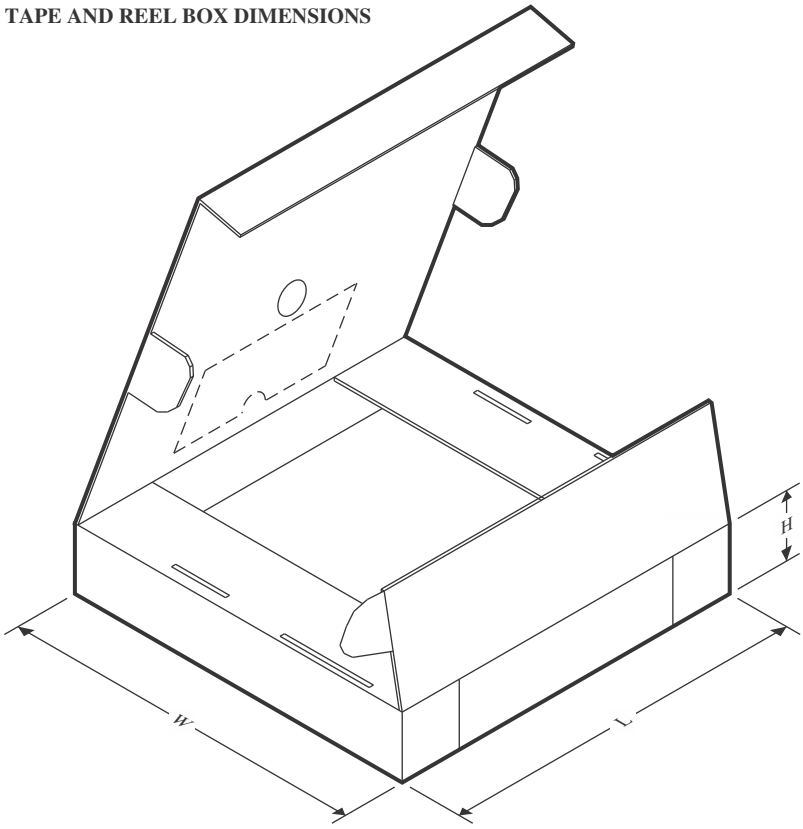
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DAC7731E/1K	SSOP	DB	24	1000	330.0	16.4	8.2	8.8	2.5	12.0	16.0	Q1
DAC7731EB/1K	SSOP	DB	24	1000	330.0	16.4	8.2	8.8	2.5	12.0	16.0	Q1
DAC7731EC/1K	SSOP	DB	24	1000	330.0	16.4	8.2	8.8	2.5	12.0	16.0	Q1

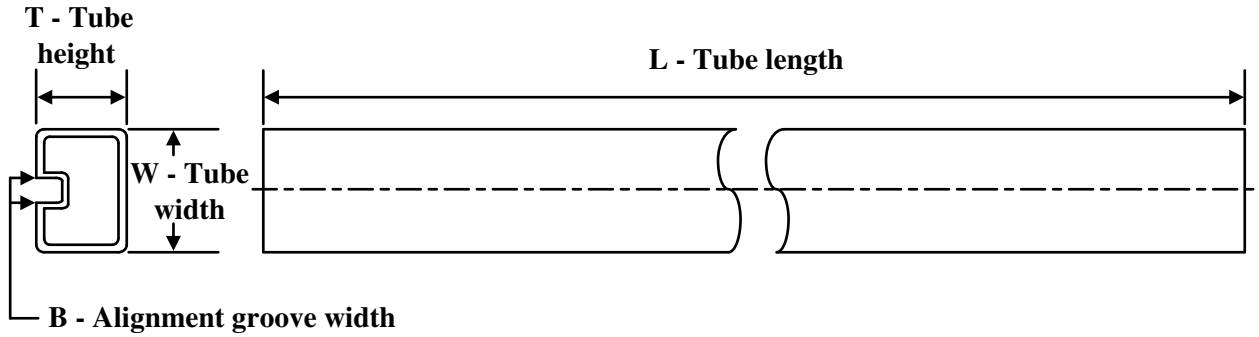
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DAC7731E/1K	SSOP	DB	24	1000	356.0	356.0	35.0
DAC7731EB/1K	SSOP	DB	24	1000	356.0	356.0	35.0
DAC7731EC/1K	SSOP	DB	24	1000	356.0	356.0	35.0

TUBE

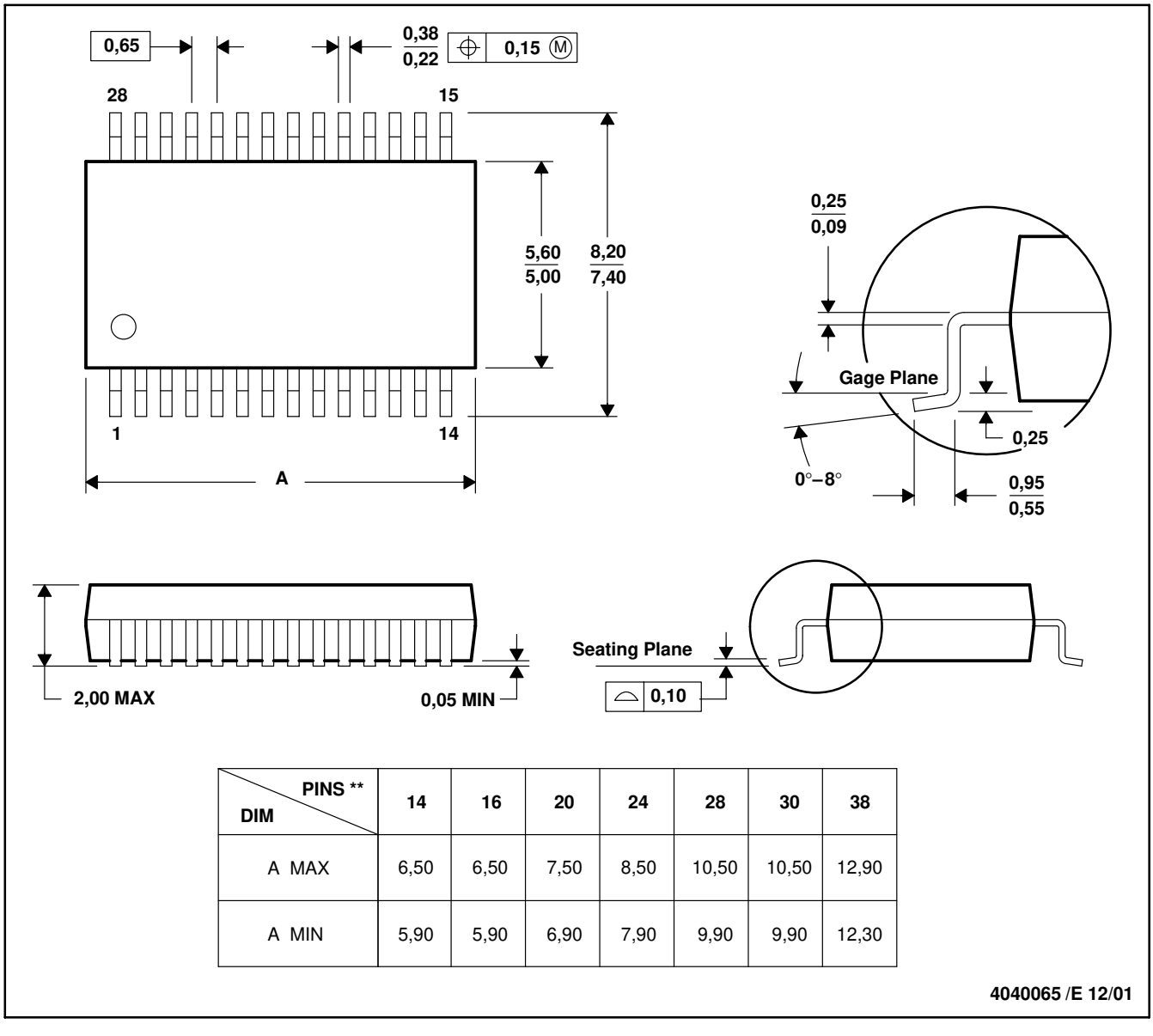


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
DAC7731E	DB	SSOP	24	60	530	10.5	4000	4.1
DAC7731EB	DB	SSOP	24	60	530	10.5	4000	4.1
DAC7731EC	DB	SSOP	24	60	530	10.5	4000	4.1
DAC7731ECG4	DB	SSOP	24	60	530	10.5	4000	4.1

DB (R-PDSO-G)** **PLASTIC SMALL-OUTLINE**

28 PINS SHOWN



DIM \ PINS **	14	16	20	24	28	30	38
A MAX	6,50	6,50	7,50	8,50	10,50	10,50	12,90
A MIN	5,90	5,90	6,90	7,90	9,90	9,90	12,30

4040065 /E 12/01

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-150

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