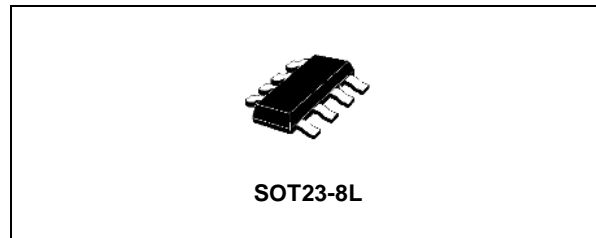


DUAL 2-INPUT AND GATE

- HIGH SPEED: $t_{PD} = 3.8\text{ns}$ (TYP.) at $V_{CC} = 5\text{V}$
- LOW POWER DISSIPATION:
 $I_{CC} = 1\mu\text{A}$ (MAX.) at $T_A = 25^\circ\text{C}$
- COMPATIBLE WITH TTL OUTPUTS
 $V_{IH} = 2\text{V}$ (MIN), $V_{IL} = 0.8\text{V}$ (MAX)
- POWER DOWN PROTECTION ON INPUTS
- SYMMETRICAL OUTPUT IMPEDANCE:
 $|I_{OH}| = I_{OL} = 8\text{mA}$ (MIN) at $V_{CC} = 4.5\text{V}$
- BALANCED PROPAGATION DELAYS:
 $t_{PLH} \cong t_{PHL}$
- OPERATING VOLTAGE RANGE:
 $V_{CC}(\text{OPR}) = 4.5\text{V}$ to 5.5V
- IMPROVED LATCH-UP IMMUNITY

DESCRIPTION

The 74V2T08 is an advanced high-speed CMOS DUAL 2-INPUT AND GATE fabricated with sub-micron silicon gate and double-layer metal wiring C²MOS technology.



ORDER CODES

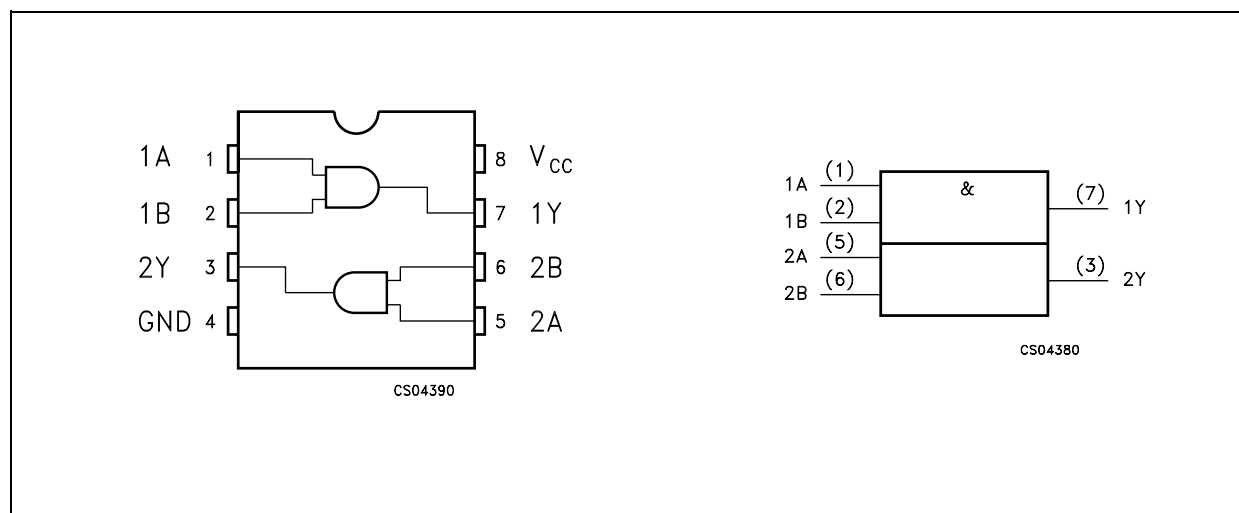
PACKAGE	T & R
SOT23-8L	74V2T08STR

The internal circuit is composed of 2 stages including buffer output, which provide high noise immunity and stable output.

Power down protection is provided on all inputs and outputs and 0 to 7V can be accepted on inputs with no regard to the supply voltage.

This device can be used to interface 5V to 3V.

PIN CONNECTION AND IEC LOGIC SYMBOLS



DC SPECIFICATION

Symbol	Parameter	Test Condition		Value						Unit	
		V _{CC} (V)		T _A = 25°C			-40 to 85°C		-55 to 125°C		
				Min.	Typ.	Max.	Min.	Max.	Min.		Max.
V _{IH}	High Level Input Voltage	4.5 to 5.5		2			2		2		V
V _{IL}	Low Level Input Voltage	4.5 to 5.5				0.8		0.8		0.8	V
V _{OH}	High Level Output Voltage	4.5	I _O =-50 μA	4.4	4.5		4.4		4.4		V
		4.5	I _O =-8 mA	3.94			3.8		3.7		
V _{OL}	Low Level Output Voltage	4.5	I _O =50 μA		0.0	0.1		0.1		0.1	V
		4.5	I _O =8 mA			0.36		0.44		0.55	
I _I	Input Leakage Current	0 to 5.5	V _I = 5.5V or GND			± 0.1		± 1		± 1	μA
I _{CC}	Quiescent Supply Current	5.5	V _I = V _{CC} or GND			1		10		20	μA
ΔI _{CC}	Additional Worst Case Supply Current	5.5	One Input at 3.4V, other input at V _{CC} or GND			1.35		1.5		1.5	mA

AC ELECTRICAL CHARACTERISTICS (Input t_r = t_f = 3ns)

Symbol	Parameter	Test Condition		Value						Unit	
		V _{CC} (V)	C _L (pF)	T _A = 25°C			-40 to 85°C		-55 to 125°C		
				Min.	Typ.	Max.	Min.	Max.	Min.		Max.
t _{PLH} t _{PHL}	Propagation Delay Time	5.0(**)	15		3.8	5.5	1.0	6.5	1.0	7.5	ns
		5.0(**)	50		4.3	6.5	1.0	7.5	1.0	8.5	

(*) Voltage range is 3.3V ± 0.3V

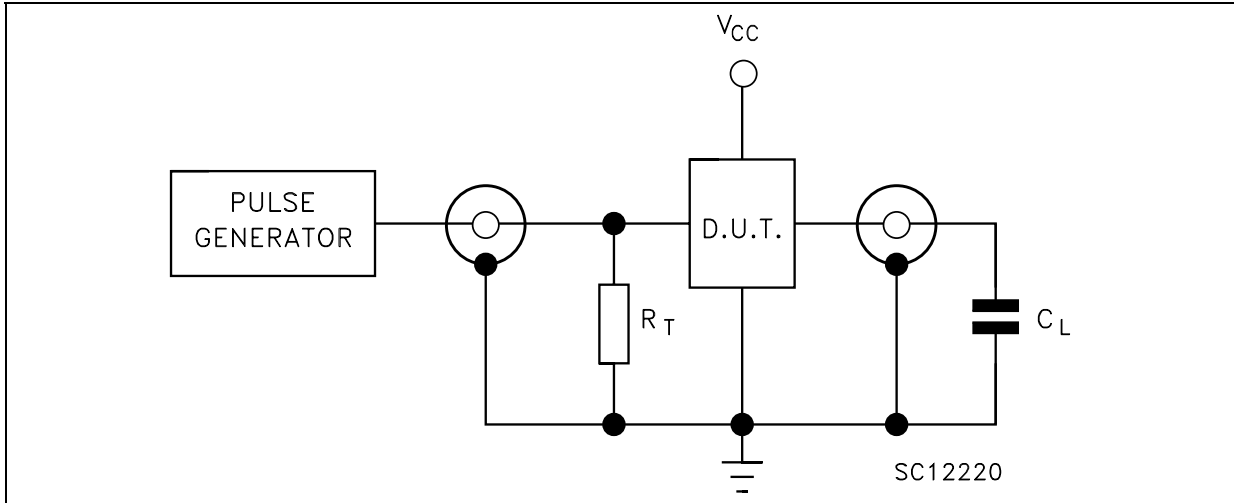
(**) Voltage range is 5.0V ± 0.5V

CAPACITANCE CHARACTERISTICS

Symbol	Parameter	Test Condition		Value						Unit	
				T _A = 25°C			-40 to 85°C		-55 to 125°C		
				Min.	Typ.	Max.	Min.	Max.	Min.		Max.
C _{IN}	Input Capacitance				4	10		10		10	pF
C _{PD}	Power Dissipation Capacitance (note 1)				19						pF

1) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average current can be obtained by the following equation. I_{CC(opr)} = C_{PD} × V_{CC} × f_{IN} + I_{CC}/2

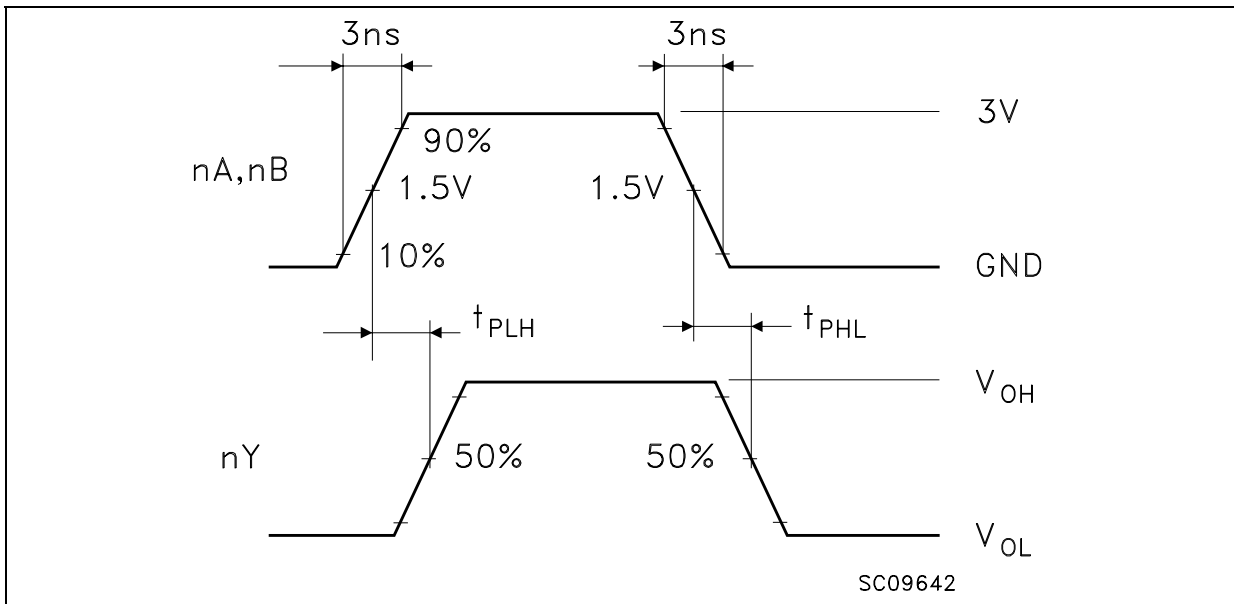
TEST CIRCUIT



$C_L = 15/50\text{pF}$ or equivalent (includes jig and probe capacitance)

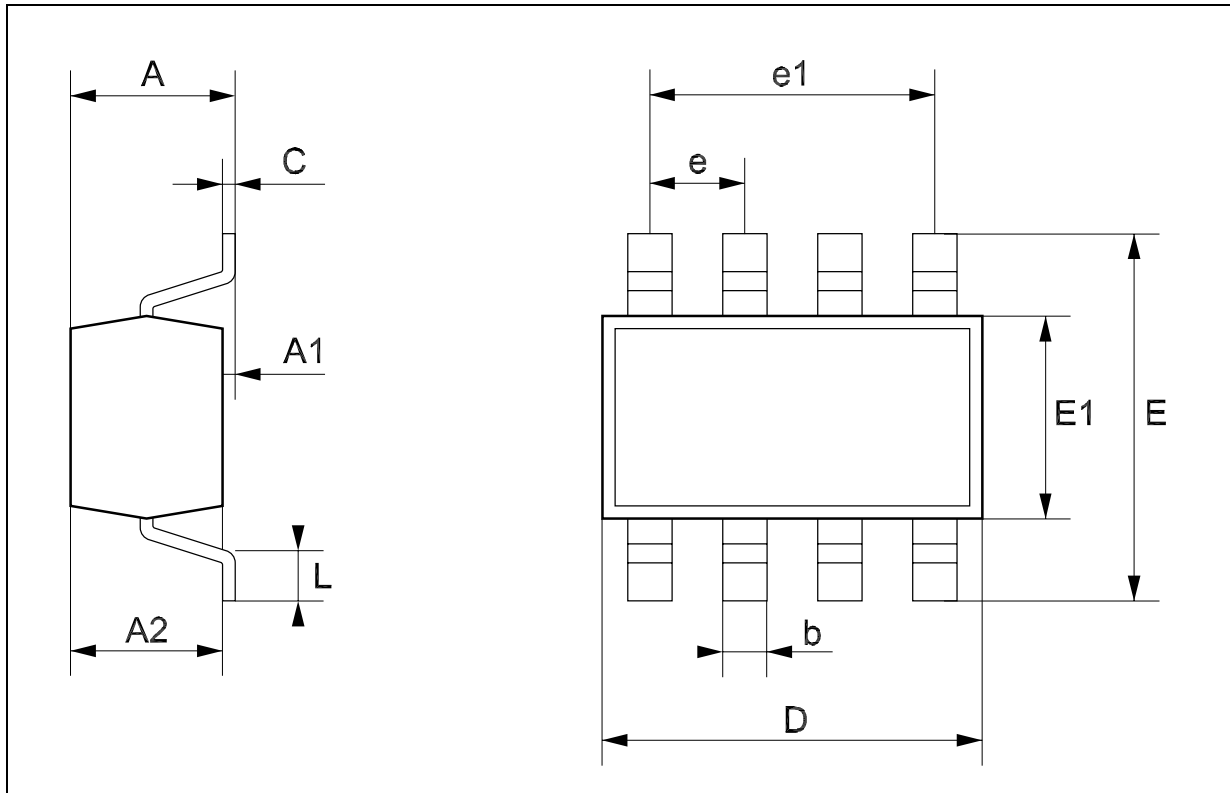
$R_T = Z_{OUT}$ of pulse generator (typically 50Ω)

WAVEFORM: PROPAGATION DELAY ($f=1\text{MHz}$; 50% duty cycle)



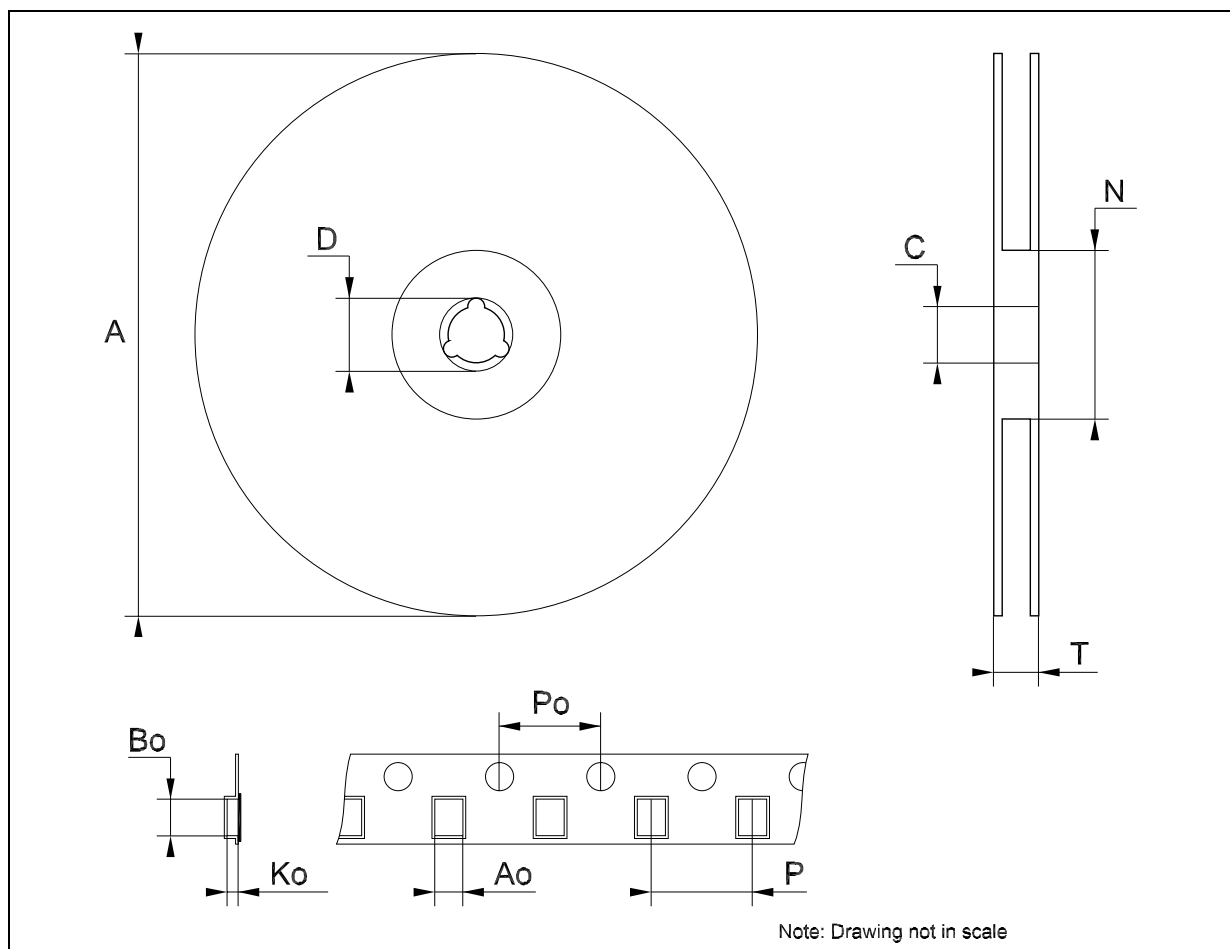
SOT23-8L MECHANICAL DATA

DIM.	mm.			mils		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A	0.90		1.45	35.4		57.1
A1	0.00		0.15	0.0		5.9
A2	0.90		1.30	35.4		51.2
b	0.22		0.38	8.6		14.9
C	0.09		0.20	3.5		7.8
D	2.80		3.00	110.2		118.1
E	2.60		3.00	102.3		118.1
E1	1.50		1.75	59.0		68.8
e	0	.65			25.6	
e1		1.95			76.7	
L	0.35		0.55	13.7		21.6



Tape & Reel SOT23-xL MECHANICAL DATA

DIM.	mm.			inch		
	MIN.	TYP	MAX.	MIN.	TYP.	MAX.
A			180			7.086
C	12.8	13.0	13.2	0.504	0.512	0.519
D	20.2			0.795		
N	60			2.362		
T			14.4			0.567
Ao	3.13	3.23	3.33	0.123	0.127	0.131
Bo	3.07	3.17	3.27	0.120	0.124	0.128
Ko	1.27	1.37	1.47	0.050	0.054	0.058
Po	3.9	4.0	4.1	0.153	0.157	0.161
P	3.9	4.0	4.1	0.153	0.157	0.161



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