

## SHDSL One Chip Rate Adaptive Transceiver with Embedded Start-up for 4 channels

The SOCRATES™-4 chip integrates all analog and digital functions of four SHDSL transceiver channels on one chip. It is fully compliant to all requirements of the ETSI TS 101524 and ITU G.991.2 (G.shdsl) standards. Unique features like the integrated hybrid and oscillator give a significant advantage in the bill of material. The unmatched power consumption of less than 700 mW per channel and its tiny package make it especially useful in high density applications. The integrated microcontroller unloads the host and makes the software design as easy as possible. SOCRATES™-4 is member of a family of SHDSL transceivers with tailor-made products for different applications. Infineon also supplies a wide range of other telecom ICs to offer complete end to end system solutions.



### Potential Applications

- DSL Access Multiplexers
- Multichannel Integrated Access Devices
- Digital Loop Carriers
- Voice Switches
- Multichannel and 4-wire repeaters
- Extended range full and fractional T1/E1 replacement
- HDSL replacement
- SDSL (2B1Q) replacement
- ISDN Primary rate access replacement
- Cellular base stations uplink
- SDH and SONET termination
- TU 12 transport
- DSL loop extension
- Leased line services
- PBX trunk lines

### Features

- Single chip 4-channel SHDSL transceiver
- Compliant with ITU G.991.2 and ETSI TS 101524 standards
- P-BGA-388 package
- Power consumption < 700 mW per channel at full speed and power
- TCPAM linecode with 2, 3 or 4 Bits/symbol
- Synchronous or plesiochronous operation
- Integrated  $\mu$ -Controller
- Built-in SHDSL Framer
- Tunable internal hybrid for best real life performance
- Internal oscillator and PLL
- Two HDLC controllers for payload and EOC per channel
- Warmstart capability

- G. handshake start-up with line probing
- Central office (COT) and remote (RT) operation
- Universal 8-Bit  $\mu$ C interface
- Universal TDM interface
- Utopia level 1/2 interface
- Supports dual bearer mode
- 2B1Q mode for SDSL interoperability
- Single 1.8 V, 3.3 V and +5 V power supply
- Inputs and Outputs TTL level
- JTAG boundary scan

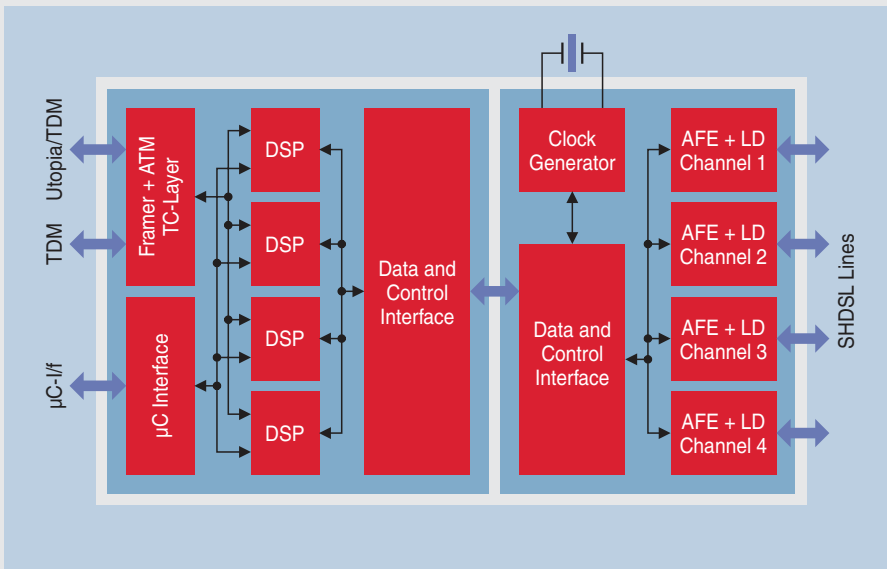
### Development and Support Tools

- SMART 2000 Evaluation package
- 32-channel density study
- DSLAM reference design
- IMA reference design

S O C R A T E S <sup>T M</sup> - 4  
P E B 2 4 6 2 2



SOCRATES PEB 24622  
High Level Block Diagram



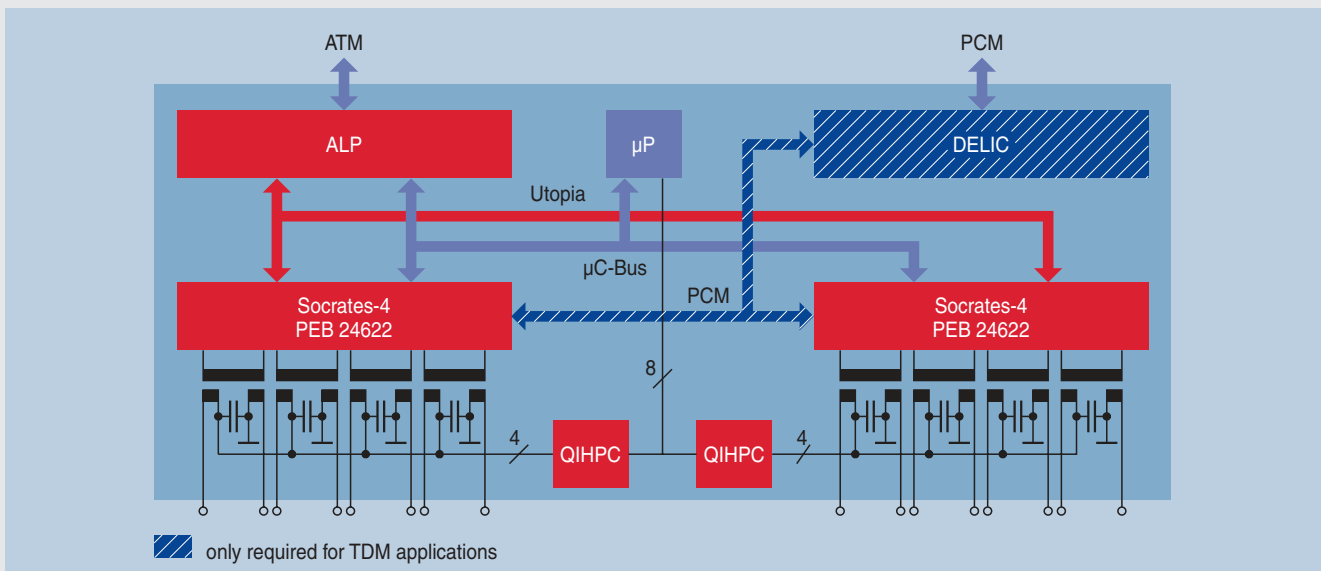
Documentation

Type	Date of Issue/Version
PEB 24622 V1.1 Product Overview	11.00
PEB 24622 V1.1 Preliminary Data Sheet	04.01

Packing

Type	Ordering Code	Package	Availability
PEB 24622 E V1.1	Q67233-H1298	P-BGA-388	ES 05.01
SMART 24622 EVM	Q67230-H1306		05.01

Application Example DSLAM with CVoDSL



How to reach us:  
<http://www.infineon.com>

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St.-Martin-Strasse 53,  
81541 München

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