AN3244
Application note

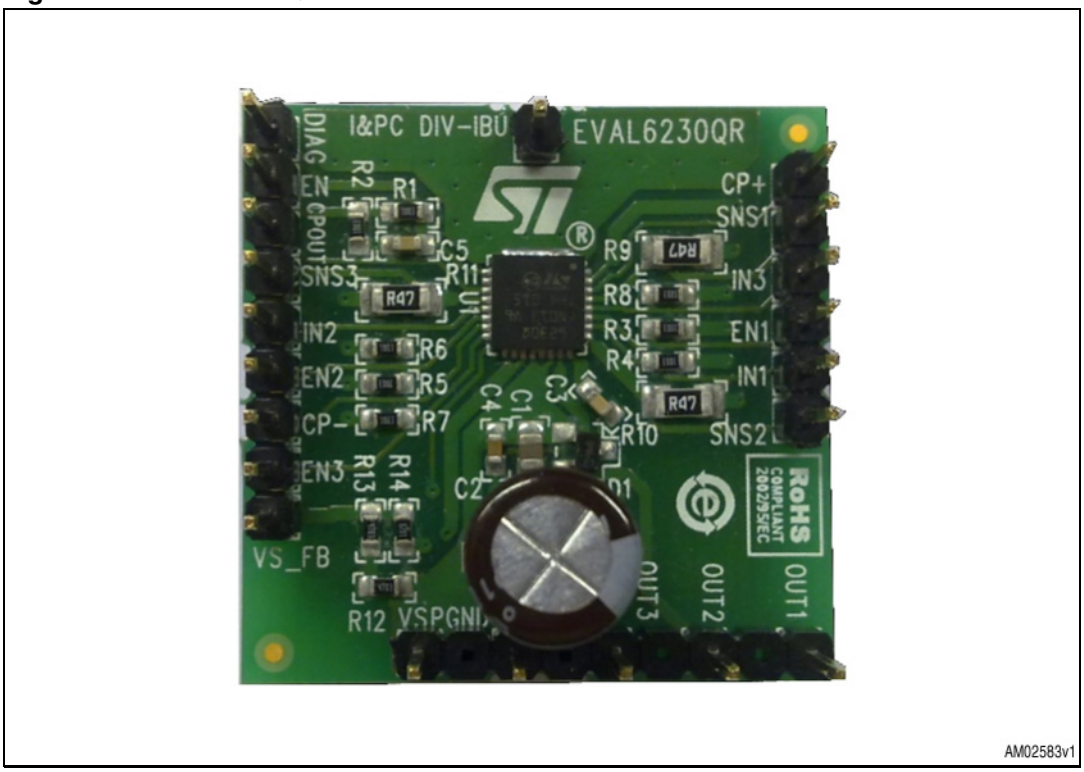
EVAL6230QR demonstration board

Introduction

This application note describes the demonstration board of the DMOS driver for the three-phase brushless DC motor driver L6230Q. The board implements a typical application which can be used as a reference design to drive three-phase brushless DC motors with currents up to 1 A DC.

Thanks to the small footprint of the L6230Q (QFN 5x5 mm) the PCB is very compact (32x31 mm).

Figure 1. EVAL6230QR demonstration board

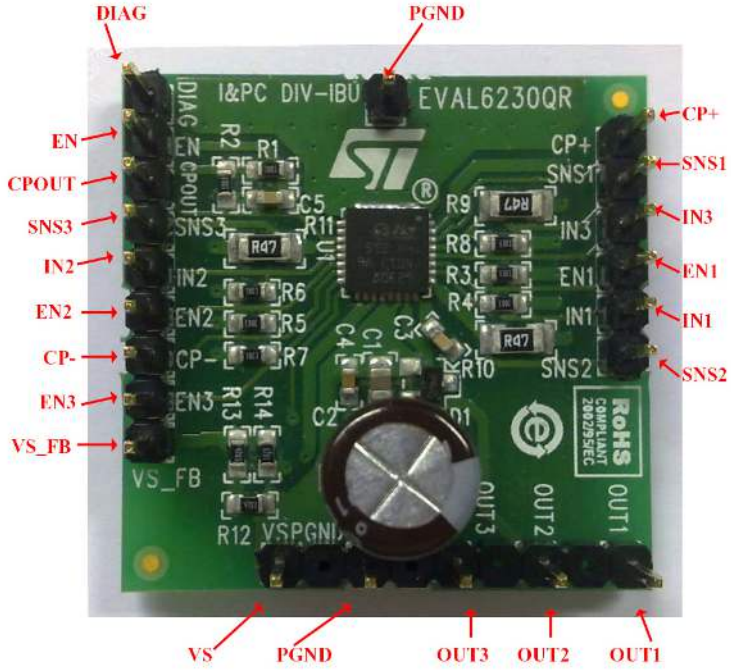


1 Demonstration board description

Table 1. EVAL6230QR: pin connections

Name	Type	Function
VS	Power supply	Power supply voltage.
PGND	Ground	Power ground terminal.
VS_FB	Analog output	Supply voltage feedback (1/115 divider ratio)
EN	Logic input	Chip enable (active 'H'). When 'L' switches OFF all power DMOS.
IN1	Logic input	Logic input half bridge 1.
EN1	Logic input	Enable input half bridge 1.
IN2	Logic input	Logic input half bridge 2.
EN2	Logic input	Enable input half bridge 2.
IN3	Logic input	Logic input half bridge 3.
EN3	Logic input	Enable input half bridge 3.
DIAG	Open-drain output	Diagnostic pin. When 'L' signals an overcurrent or overtemperature event.
CPOUT	Open-drain output	Open-drain output of internal comparator.
CP-	Analog input	Inverting input of internal comparator.
CP+	Analog input	Non-inverting input of internal comparator.
SENSE1	Analog output	Half bridge 1 source pin.
SENSE2	Analog output	Half bridge 2 source pin.
SENSE3	Analog output	Half bridge 3 source pin.
OUT1	Power output	Output half bridge 1.
OUT2	Power output	Output half bridge 2.
OUT3	Power output	Output half bridge 3.

Figure 2. EVAL6230QR connector description



The EN pin is chip enable (active high). The ENx pins enable the corresponding half-bridge. When low logic level is applied, the half bridge output is in high-impedance status (both high and low side MOS turned off).

The INx input pins drive the corresponding half bridge. When low logic level is applied, the low side MOS is switched on, whereas a high logic level turns on the high side MOS.

A general purpose comparator is integrated in the IC, its inputs and open-drain output are available on CP-, CP+, and CPOUT. It can be used for the current control or BEMF zero crossing detection (refer to the L6230; *DMOS driver for three-phase brushless DC motor,* datasheet for more details).

The power supply feedback and sensing signals are available for external conditioning, for example, to perform a field oriented control driving method.

Table 2 summarizes the electrical specification of the application, *Figure 3* shows the electrical schematic and *Table 3* contains the parts list.

Table 2. EVAL6230QR: electrical specification (recommended values)

Parameter	Value
Supply voltage range (VS)	8 to 52 Vdc
RMS output current rating (OUTx)	up to 1.4 A
Switching frequency	up to 100 kHz
Input and enable voltage range	0 to +5 V
Comparator input voltage range	0 to +5 V
Operating temperature range	-25 °C to +125 °C
L6230Q thermal resistance junction to ambient	42 °C/W

Figure 3. EVAL6230QR board schematic

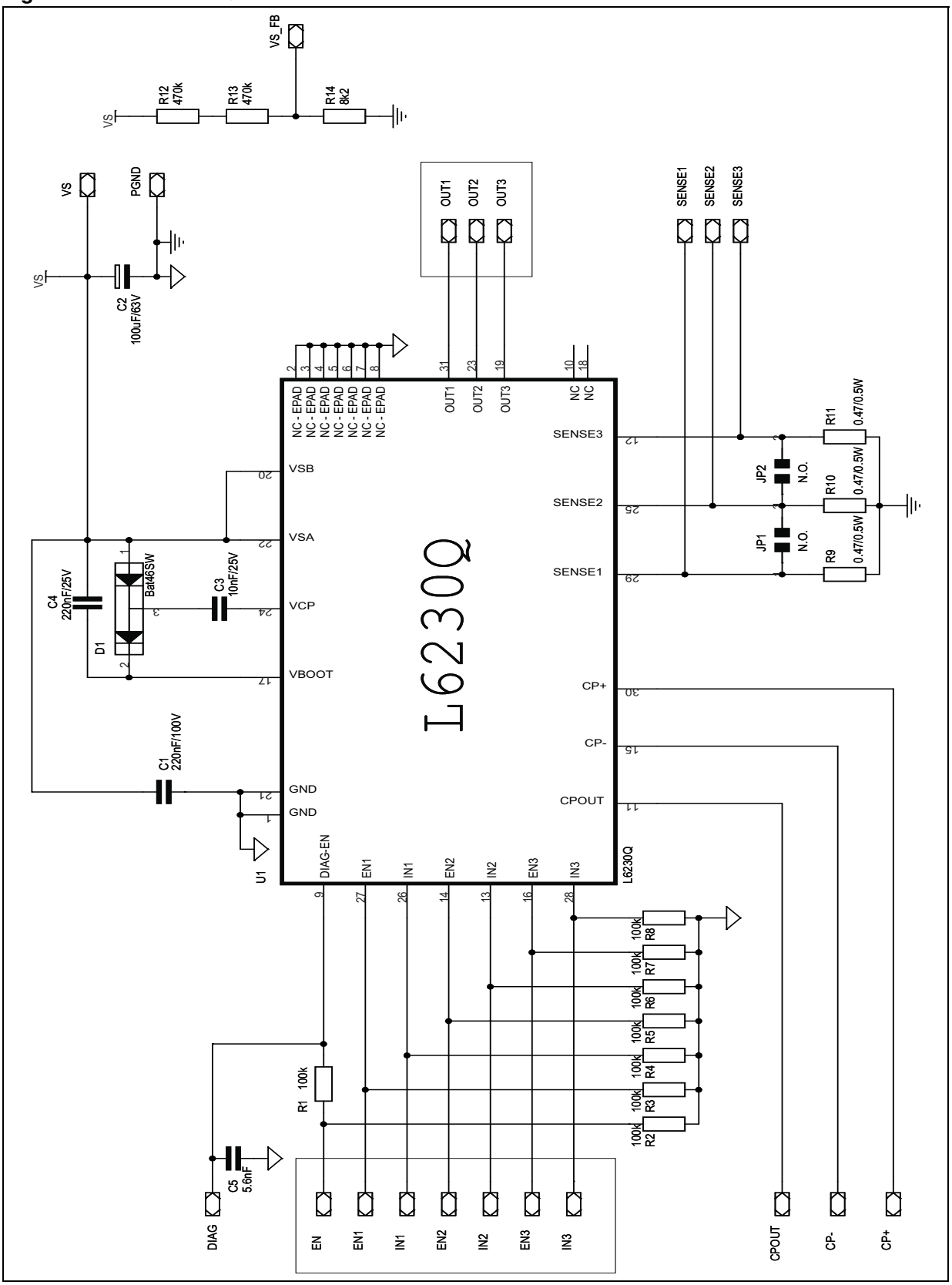


Table 3. EVAL6230QR parts list

Part reference	Part value	Part description
C1	220 nF/100 V	Capacitor
C2	100 µF/63 V	Capacitor
C3	10 nF/25 V	Capacitor
C4	220 nF/25 V	Capacitor
C5	5.6 nF	Capacitor
D1	BAT46SW	Diodes
R1 ÷ R8	100 kΩ 5 % 0.25 W	Resistor
R9, R10, R11	0.47 Ω - 0.5 W	Resistor
R12, R13	470 kΩ 5 % 0.25 W	Resistor
R14	8.2 kΩ 5 % 0.25 W	Resistor
U1	L6230Q	Three-phase BLDC motor driver in VFQFPN5x5

D1, C3, and C4 realize a charge pump circuit, which generates the supply voltage for the high side integrated MOSFETs. Due to voltage and current switching at relatively high frequency, these components are connected together through short paths in order to minimize induced noise on other circuitries.

R2 and C5 are used by the overcurrent protection integrated circuitry to set the protection timings (disable time, $t_{DISABLE}$, is about 200 µs and delay time, t_{DELAY}, is about 1 µs with the values in *Table 3*).

Figure 4, *Figure 5*, and *Figure 6* show the component placement and the two layer layout of the EVAL6230QR demonstration board. A GND area has been used for the IC power dissipation.

Figure 4. EVAL6230QR component placement

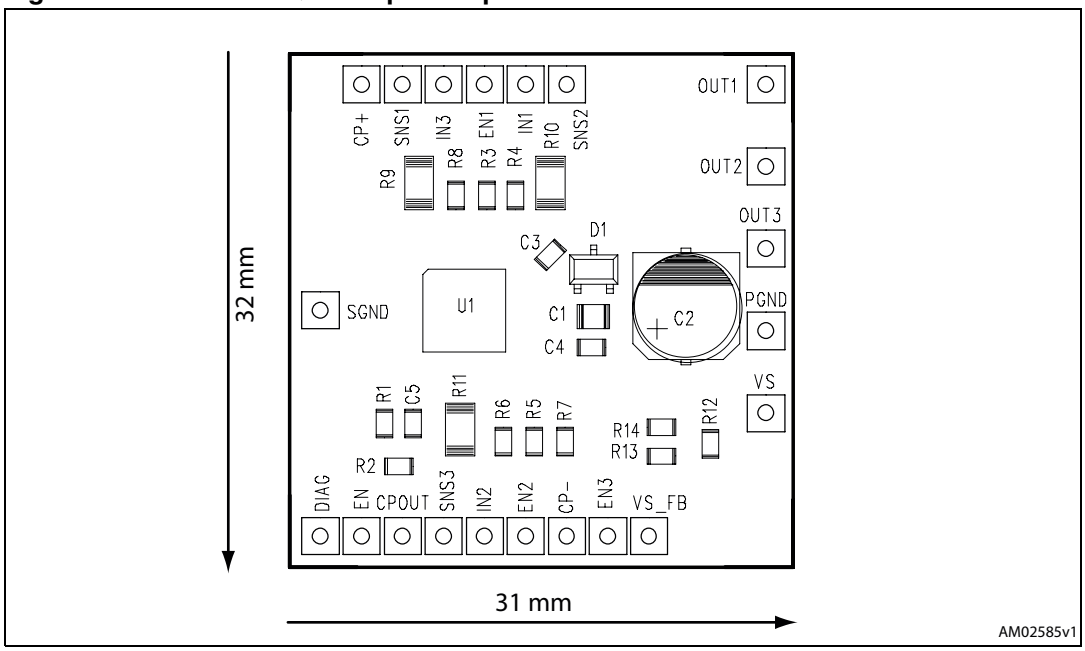


Figure 5. Top layer layout

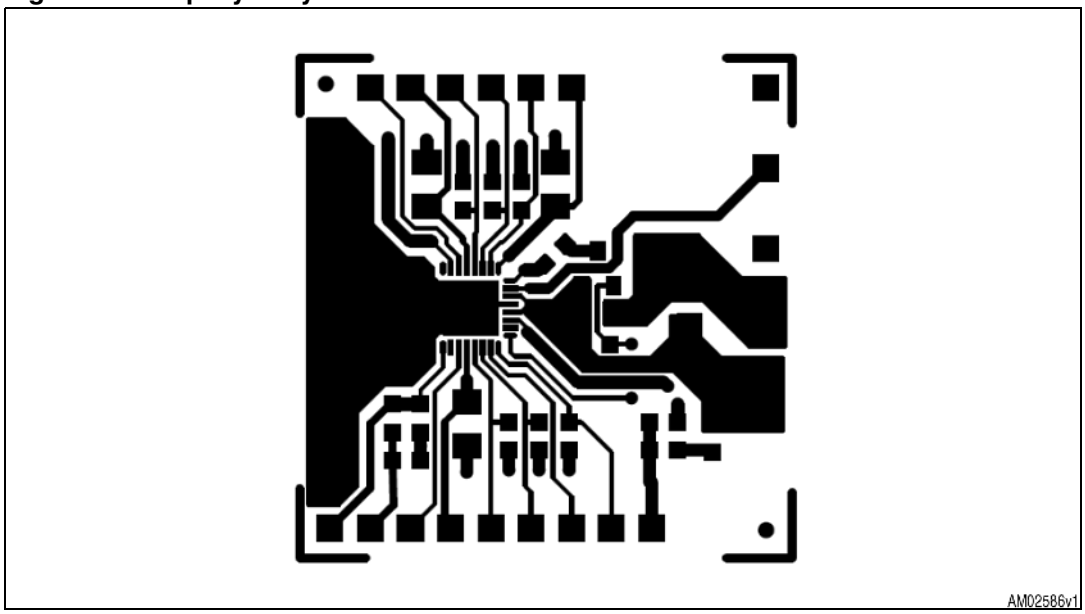
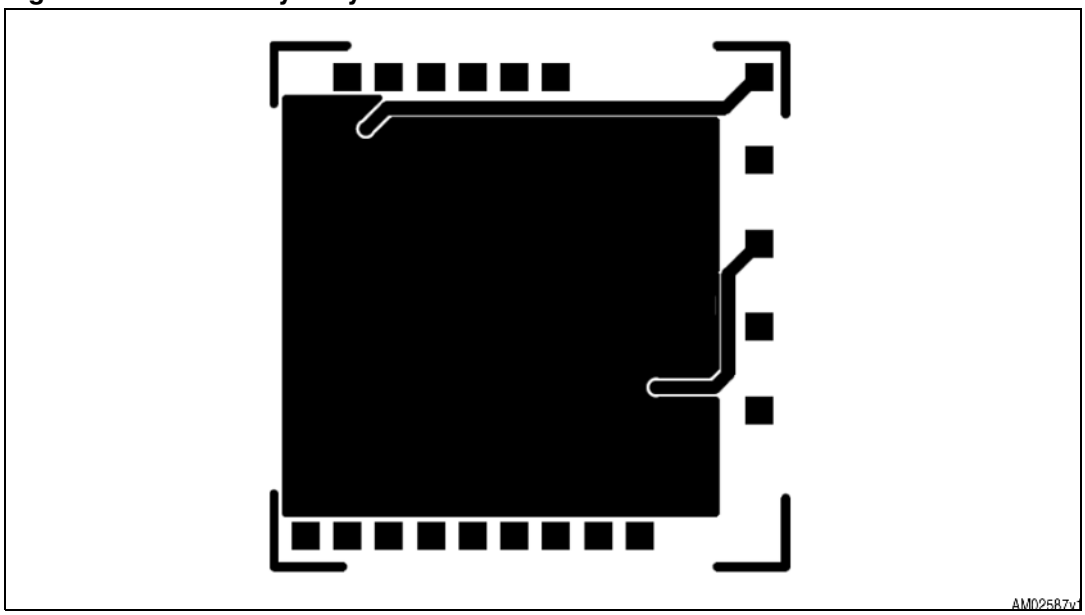


Figure 6. Bottom layer layout



2 Revision history

Table 4. Document revision history

Date	Revision	Changes
26-Nov-2010	1	Initial release