Description

The IDT P9242-R3 is a highly-integrated 15W magnetic induction wireless power transmitter with in-band, bi-directional data communication requiring no additional circuitry. The communication channel can be used for proprietary device authentication and secure system data transfer.

The P9242-R3 includes a 32-bit ARM®* Cortex®-M0 processor, foreign object detection (FOD), wide input voltage range operation, full bridge drivers, and on-chip simultaneous voltage and current demodulation.

In addition, the P9242-R3 features programmable over-current protection, programmable LED output blinking pattern, and I2C serial interface protocol to read back information such as voltage, current, and fault conditions. This standard device is compliant to the WPC-1.2 specification. Combined with the P9221-R3 receiver, the P9242-R3 forms a complete wireless power system solution for 15W applications with bi-directional data communication.

The P9242-R3 has a bootloader and application firmware pre-programmed into the internal one-time programmable (OTP) memory. The P9242-RB, which is pin-to-pin compatible with the P9242-R3, has only the bootloader pre-programmed into the internal OTP memory and uses external flash for the application firmware so that it can be changed for specific system requirements.

The P9242-R3 is available in a space-saving 48-VFQFPN package. It is rated for -40°C to +85ºC ambient operating temperature range.

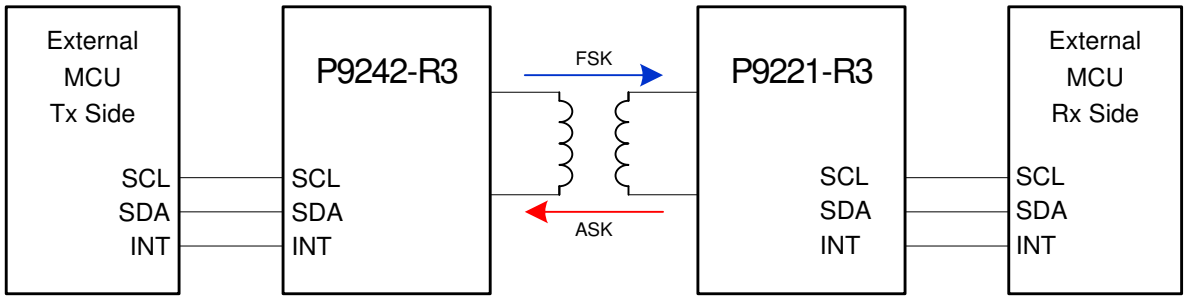
Features

- Supports bi-directional data communication
- Enables authentication and system data transfer
- Up to 15W of power transfer
- 87% end-to-end efficiency when combined with the P9221-R3
- VIN range: 4.25V to 21V
- Integrated drivers for external power FETs
- Integrated step-down switching regulator
- Simultaneous voltage and current demodulation
- Standard device compliant with the WPC-1.2 specification
- Supports the I2C interface protocol
- -40°C to +85°C ambient operating temperature range
- 6 × 6 mm, 48-VFQFPN package, Pb-free

Typical Applications

- Industrial Equipment
- Consumer Electronics
- Medical Equipment

Typical Application Circuit



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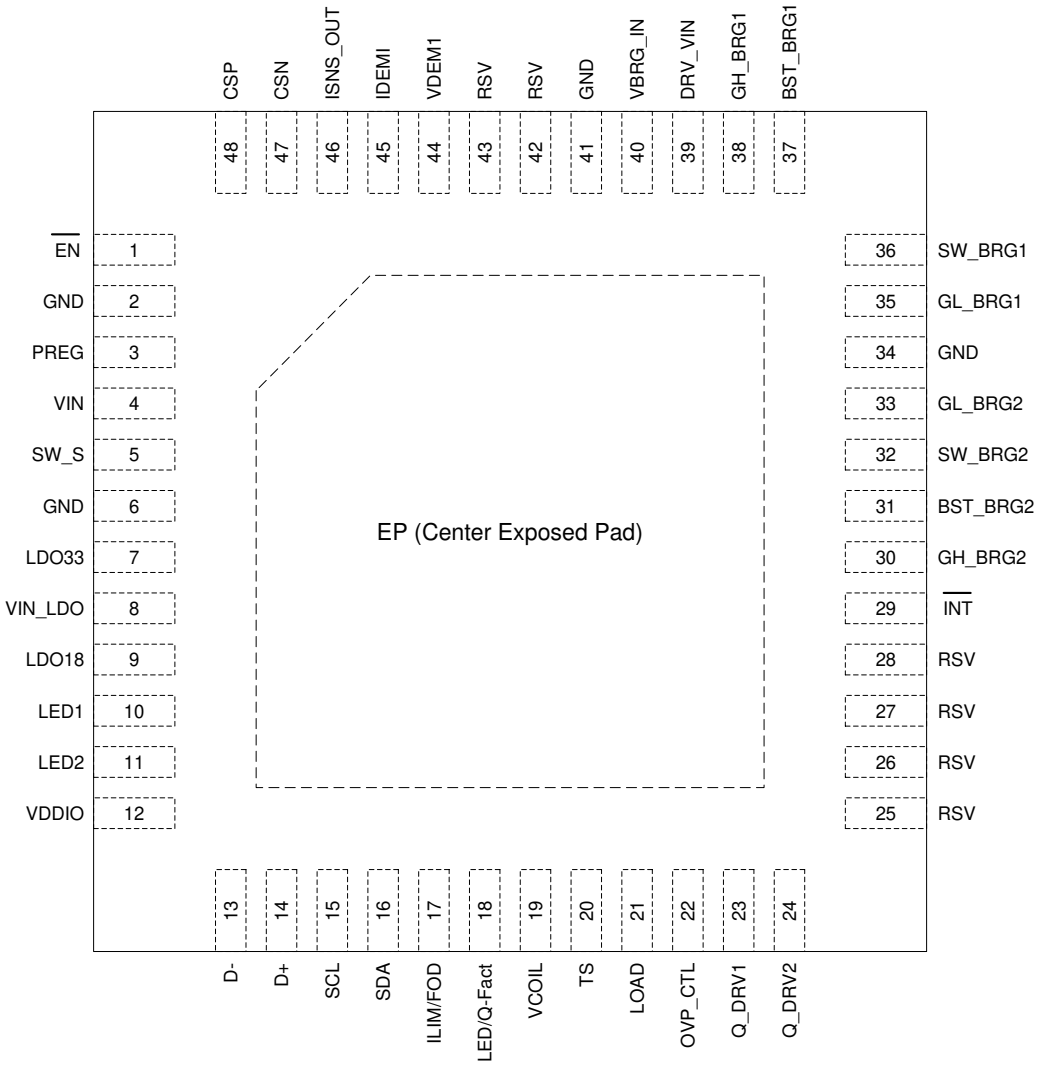
1. Pin Assignments

Figure 1. Pin Assignments



2. Pin Descriptions

Table 1. Pin Descriptions

Pins	Name	Type	Function
1	$\overline{EN}$	Input	Active-LOW enable pin. When connected to logic HIGH, the P9242-R3 enters the Shut-Down Mode, which has a typical current consumption of 25µA. When connected to logic LOW, the device is in normal operation.
2, 6, 34, 41, EP	GND	–	Ground connection.
3	PREG	Output	Regulated 5V output used for internal device biasing. Connect a 1µF capacitor from this pin to ground. This pin must not be externally loaded.
4	VIN	Input	Input power supply. Connect a 10µF capacitor from this pin to ground.
5	SW_S	Output	Step-down regulator`s switch node. Connect one of the terminals of the 4.7µH inductor to this pin.
7	LDO33	Output	Regulated 3.3V output used for internal device biasing. Connect a 1µF capacitor from this pin to ground. This pin should not be externally loaded.
8	VIN_LDO	Input	Linear regulator input power supply. Connected this pin to the 5V output of the step-down regulator.
9	LDO18	Output	Regulated 1.8V output used for internal device biasing. Connect a 1µF capacitor from this pin to ground. This pin should not be externally loaded.
10	LED1	Output	Open-drain output. Connect an LED to this pin
11	LED2	Output	Open-drain output. Connect an LED to this pin.
12	VDDIO	Input	Input power supply for internal biasing. This pin must be connected to LDO33.
13	D-	Input	Logic I/O for USB travel adaptor detection.
14	D+	Input	Logic I/O for USB travel adaptor detection.
15	SCL	Input	I2C interface clock input. Connect a 5.1kΩ pull-up resistor to the LDO33 rail.
16	SDA	I/O	I2C interface data input and data output. Connect a 5.1kΩ pull-up resistor to the LDO33 rail.
17	ILIM/FOD	Input	Programmable over-current limit and foreign object detection pin. Connect the center tap of the resistor divider to this pin to set the current-limit threshold and FOD threshold. For more information, see section 7.1.
18	LED/Q-Fact	Input	Programmable LED pattern selection and Q-factor enable/disable. Connect the center tap of a resistor divider to this pin. For more information on setting the LED pattern and Q-factor enable/disable, see section 7.8 for more details.
19	VCOIL	Input	Input for coil voltage sensing.
20	TS	Input	Remote temperature sensor for over-temperature shutdown. Connect to the NTC thermistor network. If not used, connect to the LDO33 pin through a 10kΩ resistor. Do not leave the TS pin floating.
21	LOAD	Output	An external microcontroller (MCU) can use this signal to synchronize data upload.

Pins	Name	Type	Function
22	OVP_CTL	Output	During the power transfer phase if an over-voltage has been detected on the VCOIL pin, a logic HIGH output from this pin is used to scale down the voltage by driving the external circuitry shown in Figure 30.
23	Q_DRV1	I/O	Control signal for the Q factor measurement circuit.
24	Q_DRV2	I/O	Control signal for the Q factor measurement circuit.
25, 26, 27, 28, 42, 43	RSV	Output	Reserved for internal use. Do not connect.
29	$\overline{INT}$	Output	This pin transitions from HIGH to LOW when new data is available to be read. The external MCU must reset the pin immediately after reading the user data. This pin is in a push-pull configuration; add an external FET to make it an open-drain connection.
30	GH_BRG2	Output	Gate driver output for the high-side FET of half bridge 2. Connect this pin to a series 12Ω resistor to the respective bridge FET gate.
31	BST_BRG2	Input	Bootstrap pin for half bridge 2. Connect an external capacitor from this pin to the SW_BRG2 pin to generate a drive voltage higher than the input voltage.
32	SW_BRG2	Output	Switch node for half bridge 2.
33	GL_BRG2	Output	Gate driver output for the low-side FET of half bridge 2. Connect this pin to a series 12Ω resistor to the respective bridge FET gate.
35	GL_BRG1	Output	Gate driver output for the low-side FET of half bridge 1. Connect this pin to a series 12Ω resistor to the respective bridge FET gate.
36	SW_BRG1	Output	Switch node for half bridge 1.
37	BST_BRG1	Output	Bootstrap pin for half bridge 1. Connect an external capacitor from this pin to the SW_BRG1 pin to generate a drive voltage higher than the input voltage.
38	GH_BRG1	Output	Gate driver output for the high-side FET of half bridge 1. Connect this pin to a series 12Ω resistor to the respective bridge FET gate.
39	DRV_VIN	Input	Input power supply for the internal gate drivers. Connect a 10µF capacitor from this pin to ground.
40	VBRG_IN	Input	Bridge voltage input sense.
44	VDEM1	Input	High-pass filter input. Voltage demodulation pin for data packets based on coil voltage variation; transmitted by the power receiver.
45	IDEMI	Input	High-pass filter input. Current demodulation pin for data packets based on coil current variation; transmitted by the power receiver.
46	ISNS_OUT	Output	Input current sense output.
47	CSN	Input	Low-side input current sense (VBRIDGE).
48	CSP	Input	High-side input current sense (VIN).

3. Absolute Maximum Ratings

The absolute maximum ratings are stress ratings only. Stresses beyond those listed under “Absolute Maximum Ratings” might cause permanent damage to the P9242-R3. Functional operation of the P9242-R3 at absolute maximum ratings is not implied. Exposure to absolute maximum rating conditions for extended periods could affect long-term reliability.

Table 2. Absolute Maximum Ratings

Pins [a]	Rating [b]	Units
$\overline{EN}$, VIN, SW_S, VBRG_IN, SW_BRG1, SW_BRG2, CSP, CSN, BST_BRG1, BST_BRG2, GH_BRG1, GH_BRG2	-0.3 to 28	V
PREG, LDO33, VIN_LDO, LED1, LED2, VDDIO, SCL, SDA, ILIM/FOD, LED/Q-Fact, VCOIL, TS, LOAD, OVP_CTL, D-, D+, Q_DRV1, Q_DRV2, GL_BRG1, GL_BRG2, VDEM1, IDEMI, ISNS_OUT, DRV_VIN, $\overline{INT}$	-0.3 to 6	V
LDO18	-0.3 to 2	V

[a] Absolute maximum ratings are not provided for reserved pins (RSV). These pins are not used in the application.

[b] All voltages are referred to ground unless otherwise noted. All GND pins and the exposed pad (EP) are connected together.

Table 3. Package Thermal Information

Symbol	Description	VFQFPN Rating	Units
θ_{JA}	Thermal Resistance Junction to Ambient [a], [b], [c]	27.2	°C/W
θ_{JC}	Thermal Resistance Junction to Case [b], [c]	18.8	°C/W
θ_{JB}	Thermal Resistance Junction to Board [b], [c]	1.36	°C/W
T_J	Operating Junction Temperature [a], [b]	-40 to +125	°C
T_{AMB}	Ambient Operating Temperature [a], [b]	-40 to +85	°C
T_{STG}	Storage Temperature	-55 to +150	°C
T_{LEAD}	Lead Temperature (soldering, 10s)	+300	°C

[a] The maximum power dissipation is $P_{D(MAX)} = (T_{J(MAX)} - T_{AMB}) / \theta_{JA}$ where $T_{J(MAX)}$ is 125°C. Exceeding the maximum allowable power dissipation will result in excessive die temperature, and the device will enter thermal shutdown.

[b] This thermal rating was calculated on a JEDEC 51-standard 4-layer board with the dimensions 76.2 x 114.3 mm in still air conditions.

[c] Actual thermal resistance is affected by the PCB size, solder joint quality, layer count, copper thickness, air flow, altitude, and other unlisted variables.

Table 4. ESD Information

Test Model	Pins	Ratings	Units
HBM	All pins	±2000	V
CDM	All pins	±500	V

4. Electrical Characteristics

Table 5. Electrical Characteristics

Note: V_{IN} = 5V, $\overline{EN}$ = LOW, T_{AMB} = -40°C to +85°C, unless otherwise noted. Typical values are at 25°C.

Symbol	Description	Conditions/Notes	Min	Typical	Max	Units
Input Supplies and UVLO						
V_{IN}	Input Operating Range[a]		4.25		21	V
V_{IN_UVLO}	Under-Voltage Lockout	V_{IN} rising		4.0		V
V_{IN_UVHYS}	Under-Voltage Hysteresis	V_{IN} falling		0.5		V
I_{IN}	Operating Mode Input Current	Power transfer phase, Vin = 12V		10		mA
I_{STD_BY}	Standby Mode Current	Periodic ping		1		mA
I_{SHD}	Shut-Down Current	$\overline{EN}$ = V_{IN} = 21V		25	80	µA
Enable Pin Threshold ($\overline{EN}$)						
V_{IH}	Input Threshold HIGH		2.5			V
V_{IL}	Input Threshold LOW				0.5	V
I_{EN_LKG}	$\overline{EN}$ Pin Input Leakage Current	V_{EN} = 0V	-1		1	µA
		V_{EN} = 5V		2.5		µA
Step-Down Regulator[b] with C_{OUT} = 33µF; L = 4.7µH						
V_{OUT}	Step-Down Output Voltage	Vin = 12V	4.5	5	5.5	V
N-Channel MOSFET Drivers						
$t_{LS\_ON\_OFF}$	Low-Side Gate Driver Rise and Fall Times	C_{LOAD}= 3nF; 10% to 90%, 90% to 10%		50	150	ns
$t_{HS\_ON\_OFF}$	High-Side Gate Driver Rise and Fall Times	C_{LOAD} = 3nF; 10% to 90%, 90% to 10%		150	300	ns
Input Current Sense						
V_{SEN_OFST}	Amplifier Output Offset Voltage	Measured at the ISNS_OUT pin; V_{CSP} = V_{CSN}		0.6		V
$ISEN_{ACC\_TYP}$[c]	Measured Current Sense Accuracy	V_{R_ISEN} = 25mV, I = 1.25A		±3.5		%
Analog-to-Digital Converter						
N	Resolution			12		Bit
Channel	Number of Channels			10		
$V_{IN,FS}$	Full Scale Input Voltage			2.4		V

Symbol	Description	Conditions/Notes	Min	Typical	Max	Units
LDO18[b]						
V_{LDO18}	1.8V LDO Regulator	C_{OUT} = 1µF, V_{VIN_LDO} = 5.5V	1.71	1.8	1.89	V
LDO33[b]						
V_{LDO33}	3.3V LDO Regulator	C_{OUT} = 1µF, V_{VIN_LDO} = 5.5V	3.15	3.3	3.45	V
PREG						
V_{PREG}	5V LDO Regulator			5		V
Thermal Shutdown						
T_{SD}	Thermal Shutdown	Threshold rising		140		˚C
		Threshold falling		120		˚C
Analog Input Pins Input Current Leakage (TS, VCOIL)						
I_{LKG}	Leakage Current		-1		1	µA
Open-Drain Pins Output Logic Levels (LED1, LED2, SCL, SDA)						
V_{OH}	Output Logic HIGH		4			V
V_{OL}	Output Logic LOW	I = 8mA			0.5	V
Digital Input/Output Pins Logic Levels						
V_{IH}	Input Voltage HIGH Level		0.7*VDDIO			V
V_{IL}	Input Voltage LOW Level				0.3*VDDIO	V
I_{LKG}	Leakage Current				1	µA
V_{OH}	Output Logic HIGH	I = 8mA, VDDIO = 3.3V	2.4			V
V_{OL}	Output Logic LOW	I = 8mA, VDDIO = 3.3V			0.5	V
I2C Interface (SCL, SDA)						
f_{SCL_SLV}	Clock Frequency	As I2C slave			400	kHz
C_B	Capacitive Load	For each bus line			100	pF
C_{BIN}	SCL, SDA Input Capacitance			5		pF
I_{LKG}	Input Leakage Current	V = GND and 3.3V	-1		1	µA

[a] The input voltage operating range is dependent upon the type of transmitter power stage (full-bridge, half-bridge) and transmitting coil inductance. WPC specifications should be consulted for appropriate input voltage ranges by end-product type.

[b] Do not externally load. For internal biasing only.

[c] A 20mΩ, 1% or better sense resistor and a 4.7Ω, 1% input filter resistor are required to meet the FOD specification.

5. Typical Performance Characteristics

V_{IN} = 12.0V; $\overline{EN}$ = LOW. The following performance characteristics were taken using a P9221-R3, 15W Wireless Power Receiver (RX) at T_{AMB} = +25°C unless otherwise noted.

Figure 2. Efficiency vs. Output Load: V_{OUT_RX} = 12V

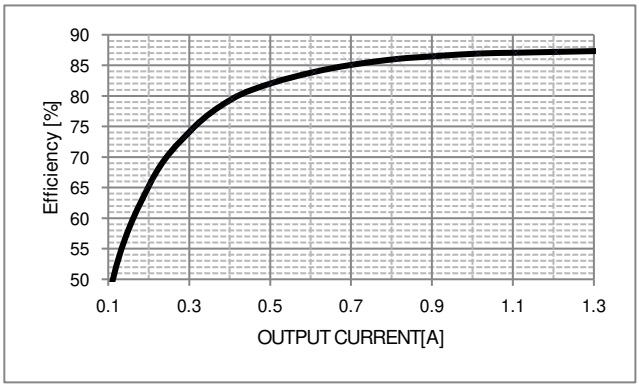


Figure 3. Efficiency vs. Output Load: V_{OUT_RX} = 9V

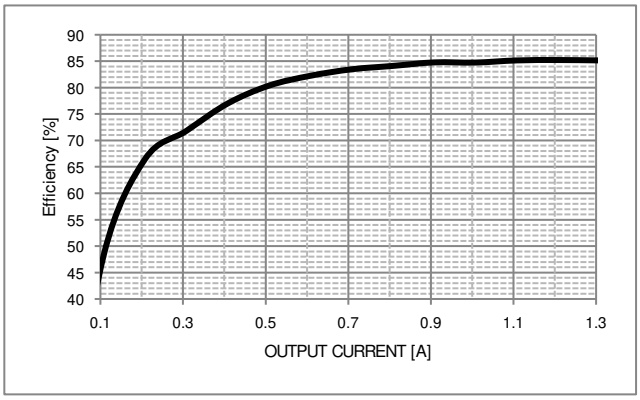


Figure 4. Efficiency vs. Output Load: V_{OUT_RX} = 5V

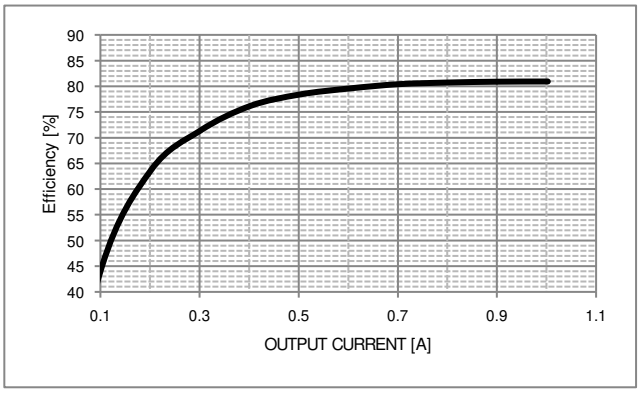


Figure 5. Load Regulation vs. Output Load: VCC_5V in Schematic Figure 30

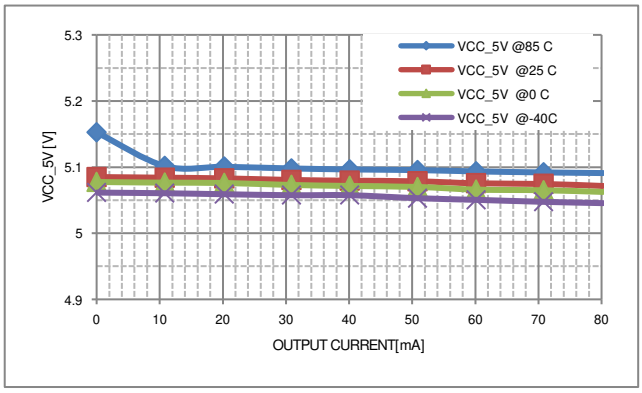


Figure 6. Load Regulation vs. Output Load: LDO33

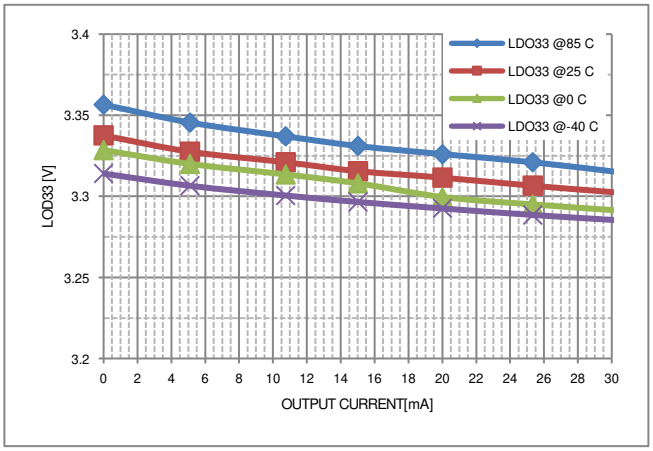


Figure 7. Load Regulation vs. Output Load: LDO18

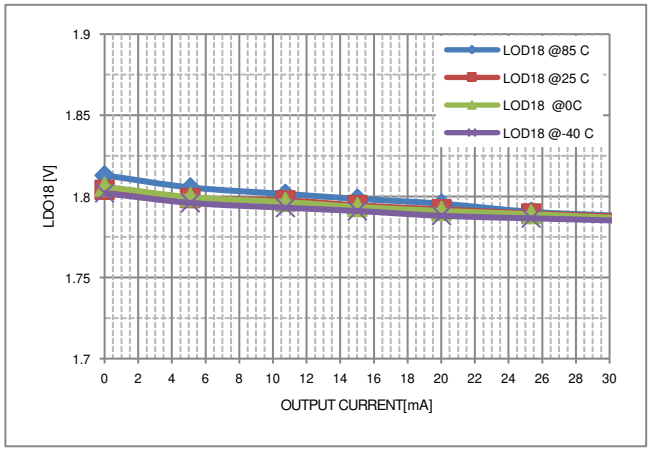


Figure 8. Over-Current Limit vs. V_{ILIM}

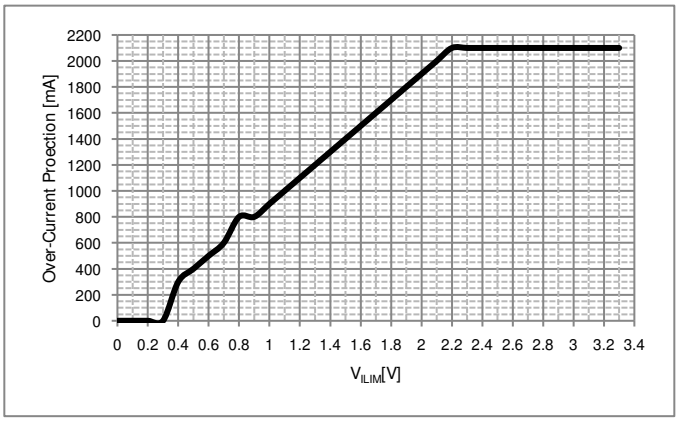


Figure 9. Voltage and Current Signal for Demodulation

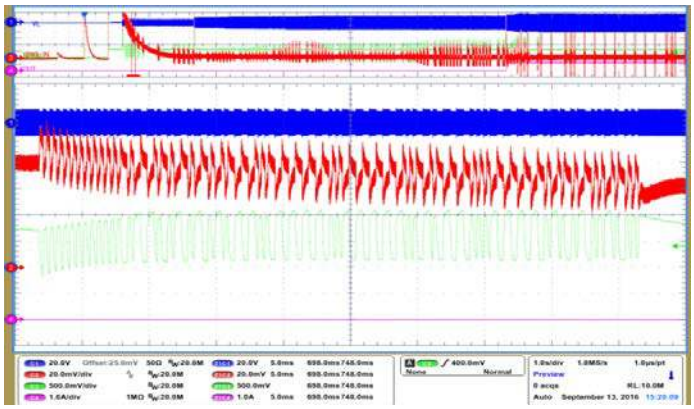


Figure 10. Enable Startup

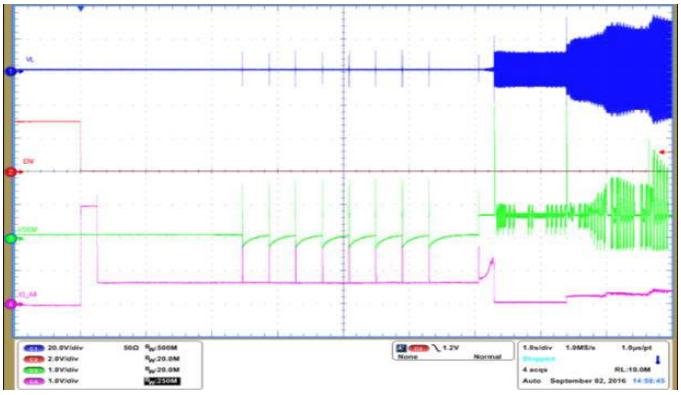


Figure 11. Communication Packet during R_X Load Step from 0 to 1.3A

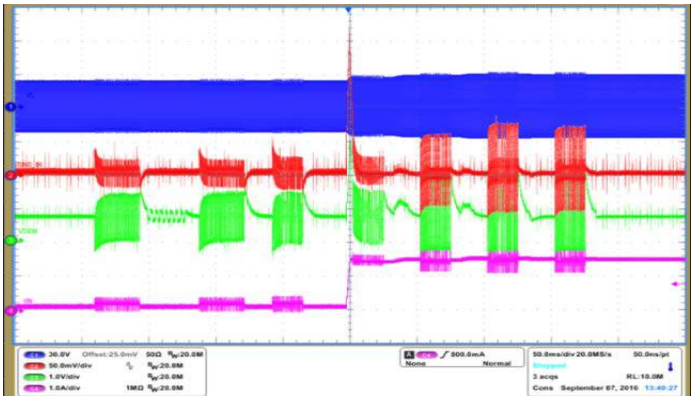
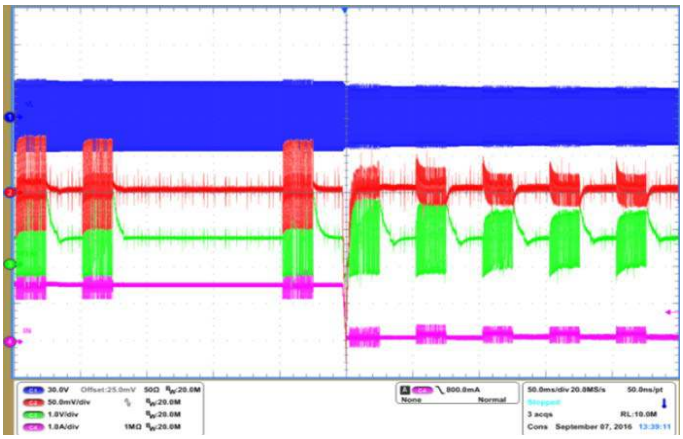
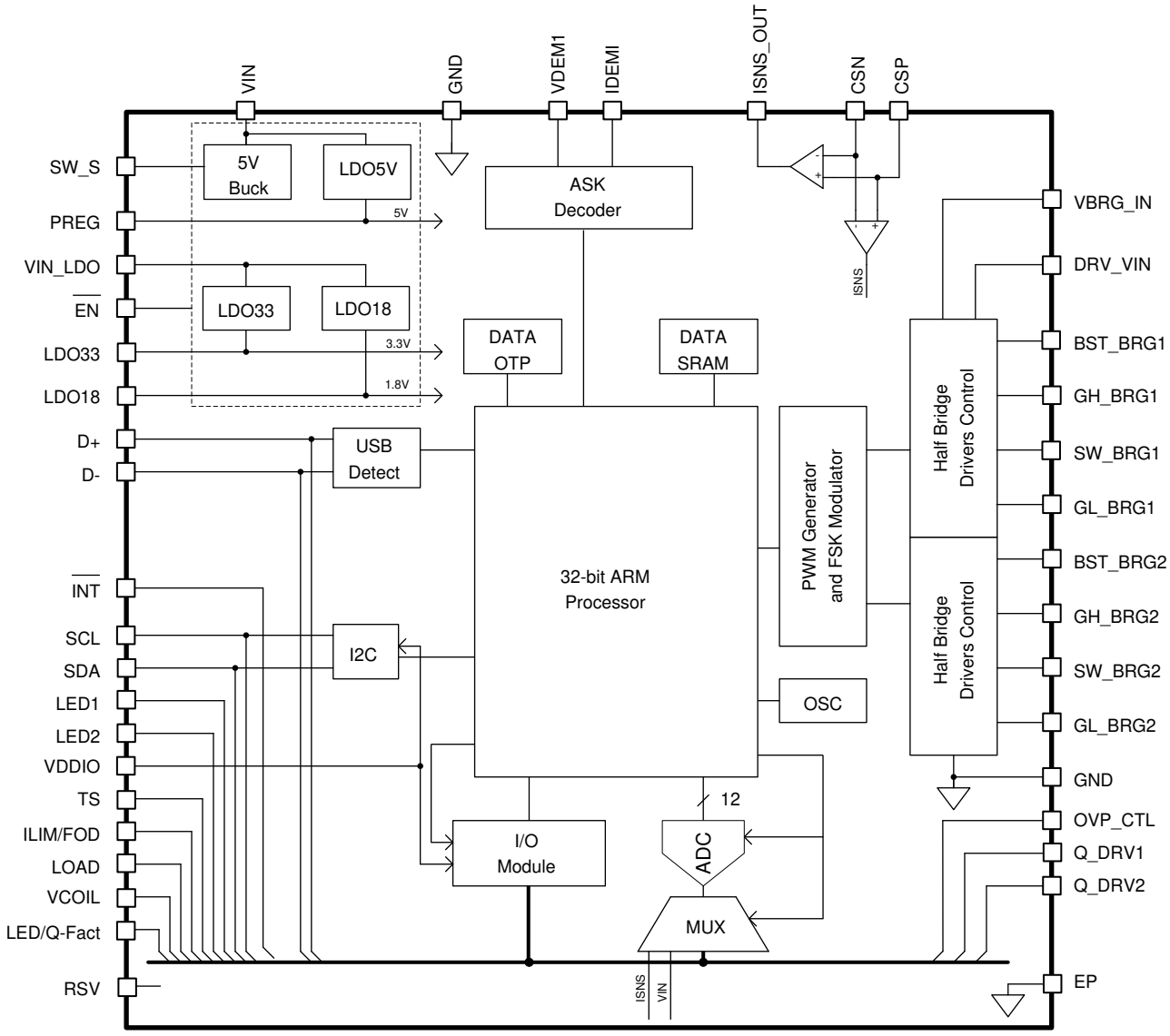


Figure 12. Communication Packet during R_X Load Step from 1.3A to 0



6. Functional Block Diagram

Figure 13. Functional Block Diagram



7. Theory of Operation

A wireless power charging system has a base station with one or more transmitters that make power available via DC-to-AC inverter(s) and transmit the power over a strongly-coupled inductor pair to a receiver in a mobile device. The amount of power transferred to the mobile device is controlled by the wireless power receiver by sending communication packets to the transmitter to increase, decrease, or maintain the power level. The communication from the receiver to the transmitter is purely binary and consists of logic 1's and 0's that ride on top of the power link that exists between the transmitter (TX) and receiver (RX) coil. The communication from the transmitter to the receiver is achieved by frequency shift keying (FSK) modulation over the power signal frequency, and amplitude shift keying (ASK) is used for the communication protocol from the receiver to the transmitter.

A feature of the wireless charging system is the fact that when it is not delivering power, the transmitter is in Standby Mode. The transmitter remains in Standby Mode and periodically pings until it detects the presence of a receiver. Once an Extended Power Profile Receiver is detected, such as the P9221-R3 or equivalent, the transmitter will provide with up to 15W of output power. If a Baseline Power Profile Receiver is present, the transmitter will deliver only up to 5W of output power.

The P9242-R3 contains features that ensure a high level of functionality and compliance with the WPC requirements, such as a power path that efficiently achieves power transfer, a simple and robust communication demodulation circuit, safety and protection circuits, configuration, and status indication circuits.

7.1 Foreign Object Detection (FOD)

When metallic objects, such as coins, keys, and paperclips, are exposed to alternating magnetic fields, the eddy current flowing through the object will heat up. The amount of heat generated is a function of the amplitude and frequency of the magnetic field, as well as the characteristics of the object, such as resistivity, size, and shape. In any wireless power system, the heat generated by the eddy current manifests itself as a power loss reducing the overall system efficiency. If appropriate measures are not taken, the heating could lead to unsafe situation.

In Extended Power Profile, there are two stages of foreign object detection (FOD). One is by measuring the system quality factor prior to entering the power transfer phase, and the other is to measure the power loss difference between the received power and the transmitted power during the power transfer phase. Prior to entering the power transfer phase, the P9242-R3 detects a change in the coil's quality factor (Q-factor) when a wireless power receiver or metal object has been placed on its surface. The transmitter measures the Q-factor and compares it with the reference Q-factor provided by the receiver. If the difference is higher than the reference Q-factor, the P9242 will identify it as FOD and shut down the system.

The second stage of the foreign object detection is during the power transfer where the power loss difference between the received power and transmitted power is constantly measured and compared to the WPC-1.2 -specified threshold. If the difference is higher than the threshold set by the WPC specification, the system will shut down to avoid over-heating.

See Table 6, Table 7, and Table 8 in section 7.2 for details for configuring the FOD threshold via external resistors.

7.2 Configuring Foreign Object Detection and Over-Current Limit – ILIM/FOD Pin

The over-current protection (OCP) is designed to protect the half-bridge and wireless receiver unit from becoming exposed to operating conditions that could potentially cause damage or unexpected behavior from the system. The input current is continuously monitored during the power transfer stage. If the input current goes above the OCP threshold, the P9242-R3 will increase the switching frequency or reduce the duty cycle in order to keep the input current below the OCP value.

External resistors can be used to select the OCP threshold (ILIM). The same resistors are also used to set the FOD threshold (refer to section 7.1 for FOD details). See Table 6, Table 7, and Table 8 for the resistor values. See the typical application schematic in Figure 30 for the location of the resistors.

Table 6. External Resistor Values for Setting Current Limiting (ILIM) to 1.5A and FOD Threshold

ILIM [mA]	R48 [KΩ]	R40 [KΩ]	Tuned FOD Threshold [%]
1500	Open	10	-40
	10	0.232	-30
	10	0.487	-20
	10	0.732	-10
	10	1	0
	10	1.27	10
	10	1.58	20
	10	1.87	30
	10	2.21	40

Table 7. External Resistor Values for Setting Current Limiting (ILIM) to 2.0A and FOD Threshold

ILIM [mA]	R48 [KΩ]	R40 [KΩ]	Tuned FOD Threshold [%]
2000	10	2.55	-40
	10	2.94	-30
	10	3.32	-20
	10	3.74	-10
	10	4.12	0
	10	4.64	10
	10	5.11	20
	10	5.76	30
	10	6.34	40

Table 8. External Resistor Values for Setting Current Limiting (ILIM) to 2.5A and FOD Threshold

ILIM[mA]	R48[KΩ]	R40[KΩ]	Tuned FOD Threshold [%]
2500	10	6.98	-40
	10	7.68	-30
	10	8.25	-20
	10	9.09	-10
	10	Open	0
	10	11	10
	10	12.1	20
	10	13.3	30
	10	14.3	40

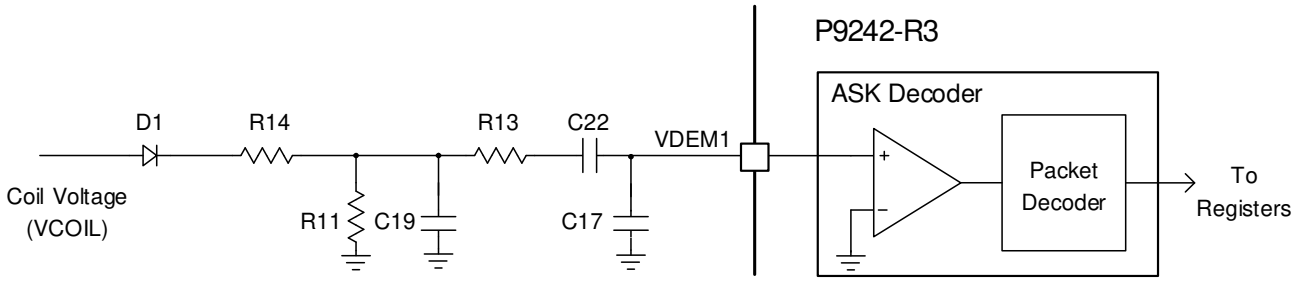
7.3 Enable Pin – $\overline{EN}$

The P9242-R3 can be disabled by applying a logic HIGH to the $\overline{EN}$ pin. When the voltage on the $\overline{EN}$ pin is pulled high, operation is suspended and the P9242-R3 is placed in the low-current Shut-Down Mode. If pulled low, the P9242-R3 is active.

7.4 Voltage Demodulation – VDEM1 Pin

In order to increase the communication reliability in any load condition, the P9242-R3 has integrated two demodulation schemes, one based on coil current information and the other based on coil voltage modulation. The voltage mode envelope detector is implemented using a discrete solution as depicted on Figure 14. This simple implementation achieves the envelope detector function low-pass filter as well as the DC filter function.

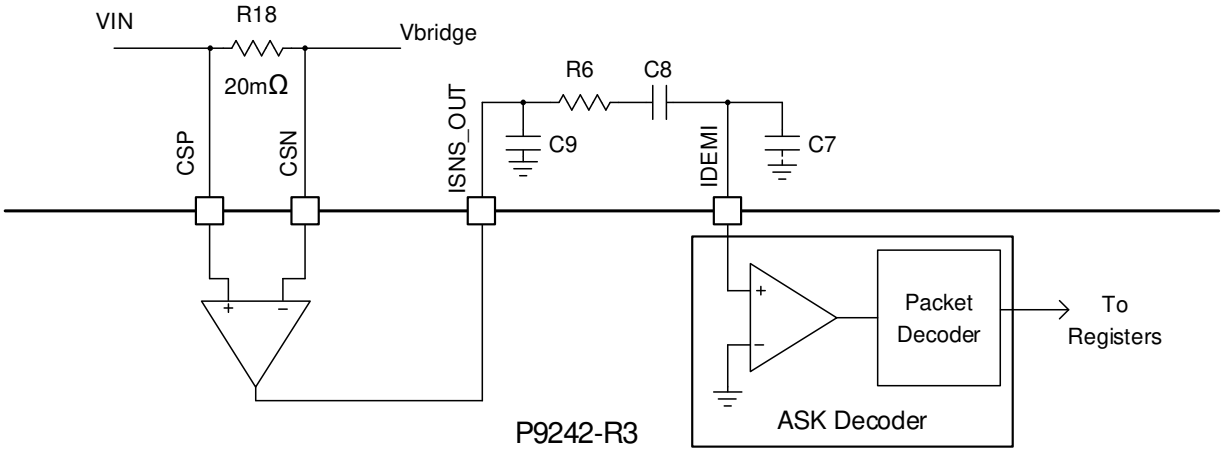
Figure 14. Voltage Mode Envelope Detector



7.5 Current Demodulation – IDEMI Pin

The current-mode detector takes the modulation information from the current sense resistor, which carries the coil current modulation information in addition to the averaged input current. There is an additional discrete low-pass filter and DC filter between the ISNS_OUT and IDEMI pins. The packet decoder block is shared between the voltage-mode and current-mode detectors. The packet decoder selects either voltage-mode or current-mode signals depending upon which produces the best demodulated signal.

Figure 15. Current Mode Envelope Detector



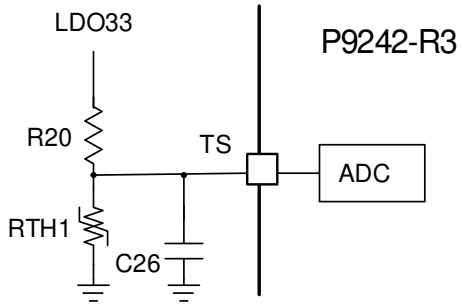
7.6 Thermal Protection

The P9242-R3 integrates thermal shutdown circuitry to prevent damage resulting from excessive thermal stress that may be encountered under fault conditions. This circuitry will shut down or reset the P9242-R3 if the die temperature exceeds a threshold to prevent damage resulting from excessive thermal stress. An internal temperature protection block is enabled in the P9242-R3 that monitors the temperature inside the chip. If the die temperature exceeds 140°C, the chip shuts down and resumes when the internal temperature drops below 120°C.

7.7 External Temperature Sensing – TS Pin

The P9242-R3 has a temperature sensor input, TS, which can be used to monitor an external temperature by using a thermistor. The built-in comparator's reference voltage was chosen to be 0.6V in the P9242-R3, and it is used for monitoring the voltage level on the TS pin. To disable the thermistor, the TS pin should be connected to the LDO33 pin through a 10K resistor. Do not leave the TS pin floating.

Figure 16. NTC Thermistor Connection to TS Pin



7.8 Q-Factor and LED Pattern Selection – LED/Q-Fact Pin

The P9242-R3 uses two LEDs to indicate the power transfer status, faults, and various operating modes depending on the voltage level at the LED/Q-Fact pin. In addition, this pin enables or disables the Q-factor used for FOD (see section 7.1). The LEDs are connected to the LED1 and LED2 pins as shown in the typical application schematic in Figure 30. The Q-factor can be enabled or disabled by the voltage on the LED/Q-fact pin as determined by the resistor divider R43 and R44 as shown in Figure 30.

Table 9. Resistors for Setting the LED Pattern and Enabling/Disabling the Q-factor Detection for FOD

Q-Factor Detection	Option	LED/Q-Fact Pin Voltage	R43 [kΩ]	R44 [kΩ]	LED1/LED2 Pin	Status			
						Standby	Transfer	Complete	Fault
Enabled	1	Pull-Down	Open	10	LED1 – GREEN	Off	On	Off	Off
					LED2 – RED	Off	Off	Off	Blink 4Hz
	2	0.225V	10	0.732	LED1 – GREEN	On	On	Off	Off
					LED2 – RED	On	Off	Off	Blink 4Hz
	3	0.375V	10	1.27	LED1 – GREEN	Off	Blink 1Hz	On	Blink 4Hz
					LED2 – RED	Off	Off	Off	Off
	4	0.525V	10	1.87	LED1 – GREEN	Off	On	Off	Blink 4Hz
					LED2 – RED	Off	Off	Off	Off
	5	0.675V	10	2.55	LED1 – GREEN	On	Blink 1Hz	On	Off
					LED2 – RED	On	Off	Off	Blink 4Hz
	6	0.825V	10	3.32	LED1 – GREEN	Off	Off	On	Off
					LED2 – RED	Off	On	Off	Blink 4Hz
	7	Pull-Up	10	Open	LED1 – GREEN	Off	Blink 1Hz	On	Off
					LED2 – RED	Off	Off	Off	Blink 4Hz
Disabled	1	1.125	10	5.11	LED1 – GREEN	Off	On	Off	Off
					LED2 – RED	Off	Off	Off	Blink 4Hz
	2	1.275	10	6.34	LED1 – GREEN	On	On	Off	Off
					LED2 – RED	On	Off	Off	Blink 4Hz
	3	1.425	10	7.68	LED1 – GREEN	Off	Blink 1Hz	On	Blink 4Hz
					LED2 – RED	Off	Off	Off	Off
	4	1.575	10	9.09	LED1 – GREEN	Off	On	Off	Blink 4Hz
					LED2 – RED	Off	Off	Off	Off
	5	1.725	10	11	LED1 – GREEN	On	Blink 1Hz	On	Off
					LED2 – RED	On	Off	Off	Blink 4Hz
	6	1.875	10	13	LED1 – GREEN	Off	Off	On	Off
					LED2 – RED	Off	On	Off	Blink 4Hz
	7	2.025	10	15.8	LED1 – GREEN	Off	Blink 1Hz	On	Off
					LED2 – RED	Off	Off	Off	Blink 4Hz

7.9 Step-Down Regulator

The input capacitors (C14 and C15 in Figure 30) must be connected as close as possible between the VIN pin and GND pin. Similarly, the output capacitor (C4 and C5 in Figure 30) must be placed close to the inductor and GND. The output voltage is sensed by the VIN_LDO pin; therefore, the connection from the step-down output (VCC_5V; see Figure 30) to the VIN_LDO pin should be made as wide and short as possible to minimize output voltage errors. The step-down regulator is the input voltage to the LDO18 and LDO33 linear regulators and is not recommended for powering an external load.

7.10 Linear Regulators – PREG, LDO33, and LDO18 Pins

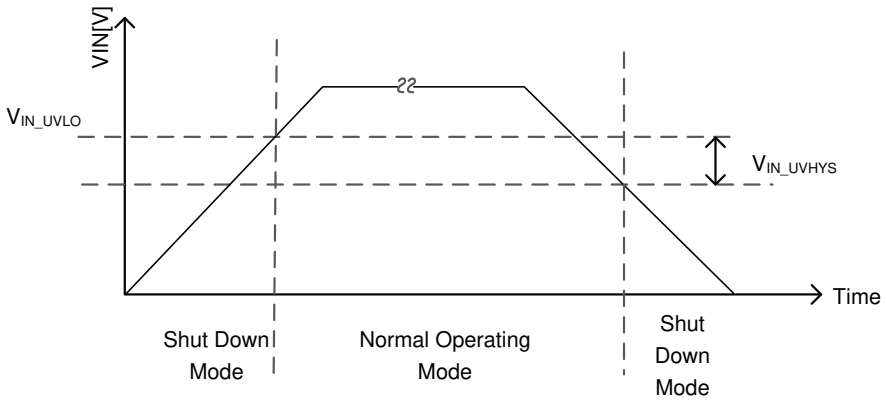
The P9242 has three low-dropout (LDO) regulators used to bias the internal circuitry. The 5V pre-regulator (PREG) provides bias for the entire internal power management. The PREG requires a 1µF ceramic bypass capacitor connected from the PREG pin to GND. This capacitor must be placed very close to the PREG pin. The voltage regulator must not be externally loaded.

The LDO33 and LDO18 are used to bias the internal digital circuit. The regulator's input voltage is supplied through the VIN_LDO pin. Both regulators require a 1µF ceramic capacitor from the pin to GND. The voltage regulators must not be externally loaded.

7.11 Under-Voltage Lock-Out (UVLO) Protection

The P9242-R3 has 4V (typical, rising) under-voltage lockout circuit on the VIN pin. To guarantee proper functionality, the voltage on the VIN pin must rise above the UVLO threshold. If the input voltage stays below the UVLO threshold, the P9242-R3 is in Shut-Down Mode.

Figure 17. UVLO Threshold Definition

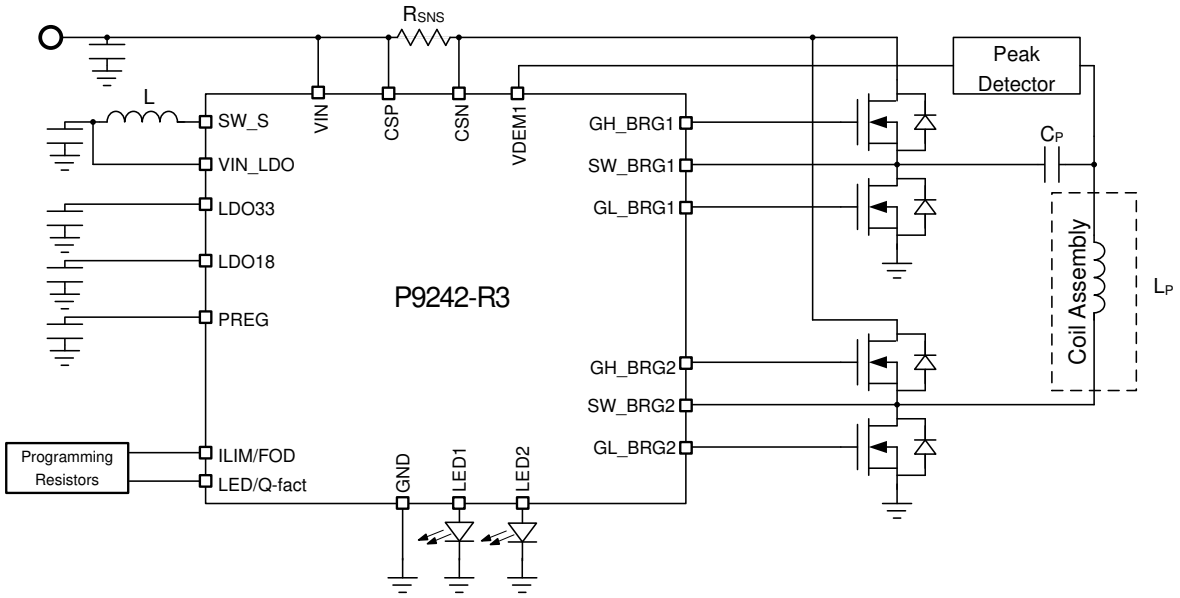


7.12 LC Resonant Circuit

The LC resonant circuit comprises the series primary resonant coil (L_P) and series capacitance (C_P) in the typical application circuit as shown in Figure 18. The transmitter coil assembly is vendor specific, and it must comply with the WPC recommendation. The WPC recommendations include the self-inductance value, DC resistance (DCR), Q-factor, size, and number of turns.

The P9242-R3 is designed to support various Extended Power Profile (EPP) coil configurations (see section 12.2) using half-bridge and full-bridge inverter topologies to drive the primary coil (L_P) and a series capacitance (C_P). Depending on the WPC coil configuration selection, the coil inductance and series capacitance will change. Near resonance, the voltage developed across the C_P series capacitance could reach 70V peak (voltage may change depending on the coil configuration). High-voltage (100V) COG-type ceramic capacitors are highly recommended for their AC and DC characteristics and temperature stability. The recommended parts are listed on the bill of materials (BOM) in Table 27.

Figure 18. Typical Application Diagram with Resonant Circuit



7.13 External Memory

The P9242-R3 has the bootloader and application firmware pre-programmed into the internal one-time programmable (OTP) memory and does not allow users to customize the firmware. The P9242-RB, which is pin-to-pin compatible with the P9242-R3, has only a bootloader pre-programmed into the internal OTP memory. Therefore, the P9242-RB must be used in conjunction with an external flash memory. Application firmware is loaded into the external flash for specific system requirements.

The P9242-RB fetches the application firmware from the external flash memory using an SPI interface and executes the code. Users can customize the firmware in external flash and load the new firmware in the flash via the P9242-RB I2C port. There is no functionality difference between the P9242-R3 IC and the P9242-RB with an external flash. The Winbond W25X20CLUXIG or any other Winbond W25X series flash device is the recommended external flash memory to be used with the P9242-RB.

8. Communication Interface

8.1 Modulation/Communication

Wireless medium-power charging systems implementing the P9242-R3 as the transmitter with the WPC-1.2 Extended Power Profile use two-way communication for power transfer: receiver-to-transmitter and transmitter-to receiver. Receiver-to-transmitter communication is accomplished by modulating the load seen by the receiver's coil; the communication is purely digital and logic 1's and 0's are carried on the power signal. Modulation is done with amplitude-shift keying (ASK) modulation using with a bit-rate of 2Kbps (for details, see sections 8.3 and 8.4). To the transmitter, this appears as an impedance change, which results in measurable variations of the transmitter's coil. The power transmitter demodulates this variation of the coil current or voltage to receive the packets.

8.2 Bit Encoding Scheme for FSK

Transmitter-to-receiver communication is accomplished by frequency-shift keying (FSK) modulation over the power signal frequency. The power transmitter P9242-R3 can modulate FSK data in the power signal frequency and use it in order to establish the handshaking protocol with the power receiver.

The P9242-R3 implements FSK communication when used in conjunction with WPC-compliant receivers, such as the P9221-R3. The FSK communication protocol allows the transmitter to send data to the receiver using the power transfer link in the form of modulating the power transfer signal. This modulation appears in the form of a change in the base operating frequency (f_{OP}) to the modulated operating frequency (f_{MOD}) in periods of 256 consecutive cycles.

Communication packets are transmitted from the transmitter to the receiver with less than 1% positive frequency deviation following any receiver-to-transmitter communication packet. The frequency deviation based on any given operating frequency is calculated using Equation 1.

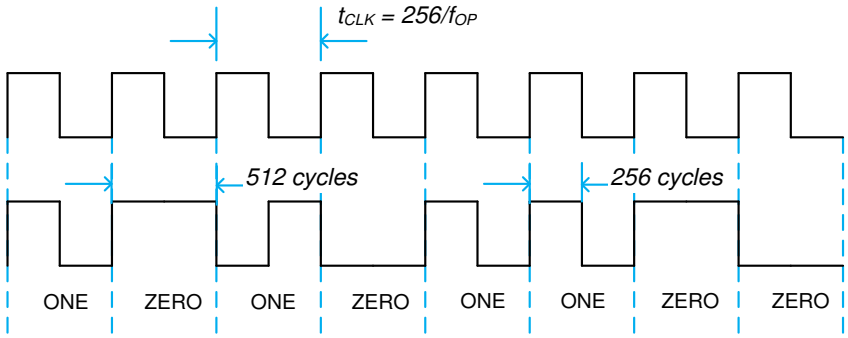
$$f_{MOD} = \frac{60000}{\frac{60000}{f_{OP}} - 3} \text{ [KHz]}$$

Equation 1

Where f_{MOD} is the change in frequency in the power signal frequency; f_{OP} is the base operating frequency of power transfer; and 60000kHz is the frequency of the internal oscillator that handles counting the period of the power transfer signal.

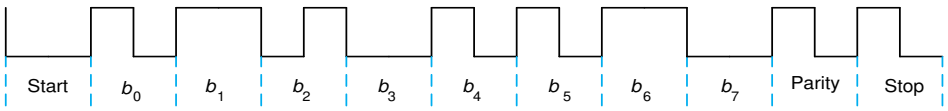
The FSK byte-encoding scheme and packet structure comply with the WPC specification revision 1.2. The FSK communication uses a bi-phase encoding scheme to modulate data bits into the power transfer signal. The start bit will consist of 512 consecutive f_{MOD} cycles (or logic '0'). A logic '1' value will be sent by sending 256 consecutive f_{OP} cycles followed by 256 f_{MOD} cycles or vice versa, and a logic '0' is sent by sending 512 consecutive f_{MOD} or f_{OP} cycles.

Figure 19. Example of Differential Bi-phase Encoding for FSK



Each byte will comply with the start, data, parity, and stop asynchronous serial format structure shown in Figure 20:

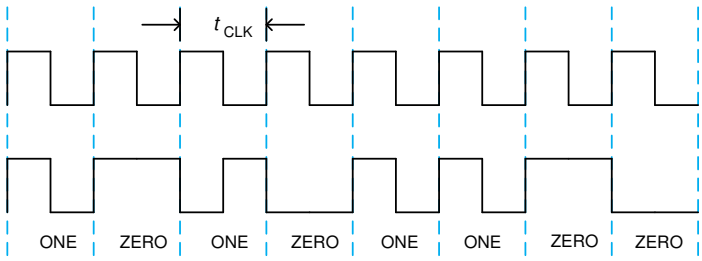
Figure 20. Example of Asynchronous Serial Byte Format for FSK



8.3 Bit Decoding Scheme for ASK

As required by the WPC, the P9242-R3 uses a differential bi-phase coding scheme to demodulate data bits from the power signal. A clock frequency of 2kHz is used for this purpose. A logic ONE bit is encoded using two narrow transitions, whereas a logic ZERO bit is encoded using one wider transition as shown in Figure 21.

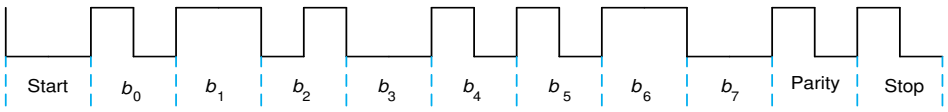
Figure 21. Bit Decoding Scheme



8.4 Byte Decoding for ASK

Each byte in the communication packet comprises 11 bits in an asynchronous serial format, as shown in Figure 22. Each byte has a start bit, 8 data bits, a parity bit, and a single stop bit.

Figure 22. Byte Decoding Scheme



8.5 Packet Structure

The P9242-R3 communicates with the base station via communication packets. Each communication packet has the following structure:

Figure 23. Communication Packet Structure

Preamble	Header	Message	Checksum

9. Bi-Directional User Data Communication

In customer-end systems, the transmitter and receiver boards must have an external microcontroller (MCU) or leverage an existing, onboard application processor to orchestrate bi-directional communication. Using the I2C communication, the MCU on the transmitter board loads the user data into specific registers and triggers the communication. The P9242-R3 sends the data to the P9221-R3 using frequency shift keying (FSK) modulation. The P9221-R3 will receive the data and interrupt the MCU on the receiver when the data is ready to be read. The external MCU on the receiver follows the same procedure to send the data to the P9242-R3 using amplitude-shift keying (ASK) modulation. When new data is available to read, the P9242-R3 will interrupt the external MCU on the transmitter board.

Bi-directional user data communication is enabled only in the power transfer phase of the WPC standard. The external MCU on the transmitter board can read the *State* register $06E0_{HEX}$ to determine whether the P9242-R3 is in the power transfer phase. Register $06E0_{HEX}$ will be set to 09_{HEX} when the device is in the power transfer phase.

See Figure 26 for a state diagram that illustrates the procedure that the external MCU on the transmitter board follows when sending the user data from the P9242-R3 to the P9221-R3 as described in section 9.1. See Figure 27 for a state diagram that illustrates the procedure that the external MCU on the transmitter follows to read the data received by the P9242-R3 from the P9221-R3 as described in section 9.2.

9.1 Transferring Data from the P9242-R3 to the P9221-R3

The external MCU on the transmitter board should read bit 0 in register 0800_{HEX} in the P9242-R3 to determine the status of the communication channel before initiating a new transfer. If the communication channel is free, bit 0 in register 0800_{HEX} is set to 0_{BIN}. If the communication channel is busy, bit 0 in register 0800_{HEX} is set to 1_{BIN}.

The P9242-R3 provides registers 0805_{HEX} to $080E_{HEX}$ for 10 bytes of outgoing user data loaded by the external MCU on the transmitter board; however, the P9242-R3 can send only 2 bytes of information at a time and the P9221-R3 can receive only 2 bytes at a time. If the external MCU on the transmitter loads more than 2 bytes into the outgoing data registers, the P9242-R3 will take 2 bytes of information at a time starting with register 0805_{HEX} and send the user data consecutively.

Important: When the P9242-R3 is sending multiple bytes of information consecutively, the external MCU on the receiver must monitor the transmission very closely and must read incoming data immediately after the interrupt is received to prevent data corruption. The P9221-R3 does not reject new incoming data because old data was not read by the external MCU on the receiver.

The external MCU on the transmitter should write an even number of data bytes to outgoing data registers 0805_{HEX} to $080E_{HEX}$ and set the number of bytes to be transferred in the register 0800_{HEX} bits [6:3] accordingly. If the external MCU on the transmitter is sending an odd number of bytes of user data, it must add one more byte of zeros or a padding byte and write an even number of registers to the outgoing data registers. For example, if the external MCU on the transmitter is transferring 3 bytes of information, it should add one byte of zeros as the fourth byte, write the 4 bytes to registers 0805_{HEX} to 0808_{HEX}, and set register 0800_{HEX} bits [6:3] to 0001_{BIN}. The P9242-R3 will not transfer the registers 0809_{HEX} to $080E_{HEX}$ when the register 0800_{HEX} bits [6:3] are set to 0001_{BIN}.

Table 10. Registers Used for Data Transmission from the P9242-R3 to the P9221-R3

Register Name	Register Address
Command register	0800_{HEX}
Outgoing user data registers	0805_{HEX} to $080E_{HEX}$ (10 bytes)
State register	$06E0_{HEX}$

The P9242-R3 does not add any checksum to the user data. The external MCU on the transmitter must construct a data packet with the user data, checksum, header, and other helpful information and load it into the outgoing user registers. For example, if the external MCU on the transmitter is sending 2 bytes of user data, it must load at least 4 bytes (header byte, checksum byte, and 2 user data bytes) into the outgoing user data registers. This will help the external MCU on the receiver to decode the data. Figure 24 shows the recommended message structure, which is consistent with the WPC standard.

Figure 24. Recommended Message Structure for the User Data Transfer from the P9242-R3 to the P9221-R3 for 8 Bytes of User Data

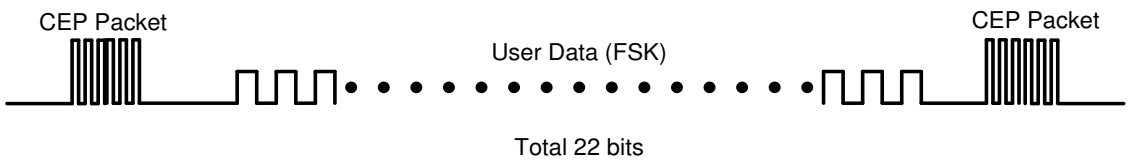
Byte 1	Byte2	Byte 3	Byte 4	Byte 5	Byte 6	Byte 7	Byte 8	Byte 9	Byte 10
Header	Data 0	Data 1	Data 2	Data 3	Data 4	Data 5	Data 6	Data 7	Checksum

The P9242-R3 also has the flexibility to send the same data multiple times based on the setting in register 0800_{HEX} bits [2:1]. For example, if register 0800_{HEX} bits [2:1] are set to 01_{BIN}, the P9242-R3 sends the data two times. It starts the second data transfer immediately after finishing the first data transfer.

The external MCU on the transmitter should set *Command* register 0800_{HEX} bit [0] to 1_{BIN} to trigger the communication after loading the user data into the outgoing user data registers and setting the *Command* register 0800_{HEX} bits [7:1] appropriately. After receiving the communication trigger from the control register, the P9242-R3 waits for the end of the next Control Error Packet (CEP; see section 10.6) and sends the data into the channel by modulating the operating frequency. Figure 25 shows the timing diagram for the user data transfer from the P9242-R3 to the P9221-R3.

The P9221-R3 and P9242-R3 cannot both send data into the channel at the same time. If two devices send data into the channel at the same time, the data will be corrupted; therefore the MCUs on the transmitter and receiver must establish an algorithm to avoid conflicting messages on the channel.

Figure 25. Timing Diagram for the User Data Transfer from the P9242-R3 to the P9221-R3



The LOAD pin on the P9242-R3 helps the external MCU to synchronize the data upload into the outgoing user data registers. In the power transfer phase, the external MCU can load the data into the outgoing user data registers on the falling edge of the LOAD pin.

The P9242-R3 will reset register 0800_{HEX} bit 0 to 0_{BIN} immediately after sending the data into the channel. The external MCU on the transmitter can periodically check bit 0 in the P9242-R3 register 0800_{HEX} to get an acknowledgment of successful data transmission into the channel. When the external MCU on the transmitter loads more than 2 bytes of user data into the outgoing registers, the P9242-R3 will reset register 0800_{HEX} bit 0 to 0_{BIN} after sending all the bytes into the channel. The P9242-R3 gives the WPC standard communication packets priority over the user data packets. The user data packets have the lowest priority. Therefore during the load transients, the P9242-R3 might skip sending the user data packets and give priority to the WPC communication packets.

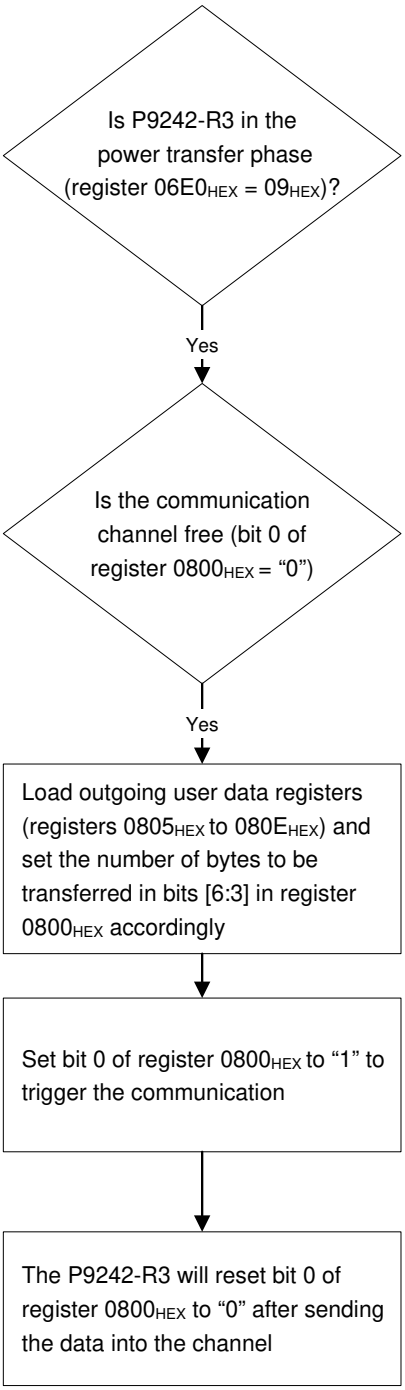
The P9242-R3 transfers the data into the channel at 200bps; however, the channel is usually busy transmitting the WPC standard communication packets. There is a very small window in which the user data can be transferred. Typically in the power transfer phase, a CEP packet is sent every 150msec. In one second, there will be only 6 to 7 time slots in which the P9242-R3 can send a maximum of 2 bytes of user data in each slot. As a result the effective maximum data transfer rate achieved for transfers from the P9242-R3 to the P9221-R3 is 110bps.

The P9242-R3 does not wait for acknowledgement from the P9221-R3 or keep track of successful delivery of the data to the P9221-R3. The P9242-R3 only acts as a messenger and relies upon the external MCU on the receiver and transmitter to craft a lossless communication protocol by adding intelligence into the data they are transferring.

Figure 26. Typical P9242-R3 to P9221-R3 Data Transfer using the WP15WBD-RK Evaluation Kit

Note: The WP15WBD-RK is the evaluation kit available for the P9242-R3 and P9221-R3, which implements the typical application schematic shown in Figure 30.

Figure 27. State Diagram for User Data Transmission from the P9242-R3 to the P9221-R3



9.2 Reading Data Sent from the P9221-R3

The 9242-R3 can receive 8 bytes of information at a time. When the P9242-R3 receives data from the P9221-R3, it will generate an interrupt to the external MCU on the transmitter by pulling down the interrupt pin. The MCU can respond to the interrupt and read the data received flag in register 0801_{HEX} bit 0 to confirm that the interrupt is generated because of the new incoming data. The *Data_Received_Flag (*register 0801_{HEX} bit [0]) is set to 1_{BIN} when there is new incoming data.

After confirming that the new data is available to be read, the external MCU should read register $080F_{HEX}$, which indicates the number of incoming data bytes received. Based on the information, the MCU on transmitter should read the number of bytes indicated from user incoming data registers 0810_{HEX} to 0817_{HEX}. For example, if the external MCU on the transmitter receives 3 bytes of information, register $080F_{HEX}$ will indicate 38_{HEX}; therefore the external MCU on the transmitter should read only registers 0810_{HEX} to 0812_{HEX} (3 bytes) and ignore 0813_{HEX} to 0817_{HEX}.

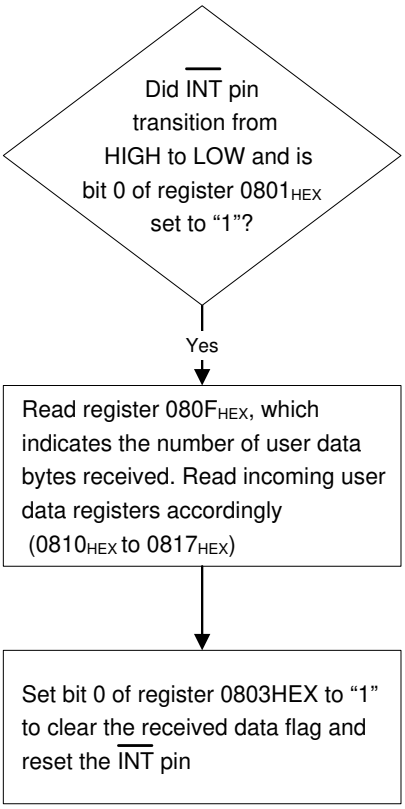
Table 11. Registers Used for Reading User Data from the P9242-R3

Register Name	Register Address
Data Received Status	0801_{HEX}
Clear Interrupt	0803_{HEX}
Incoming Data Header	$080F_{HEX}$
Incoming User Data	0810_{HEX} to 0817_{HEX}

After reading the data, the external MCU on the transmitter should clear the interrupt by writing 01_{HEX} to register 0803_{HEX}. If the external MCU on the transmitter does not handle interrupts, it should constantly poll the data received flag to check whether there is any new incoming data.

If the external MCU on the transmitter does not read data immediately after the interrupt is received, there is a risk that data could become corrupted because of new incoming data. The 9242-R3 does not reject new incoming data because the old data was not read by the MCU on the transmitter. The user can implement a higher level handshaking protocol between the external MCU on transmitter and receiver to avoid data corruption.

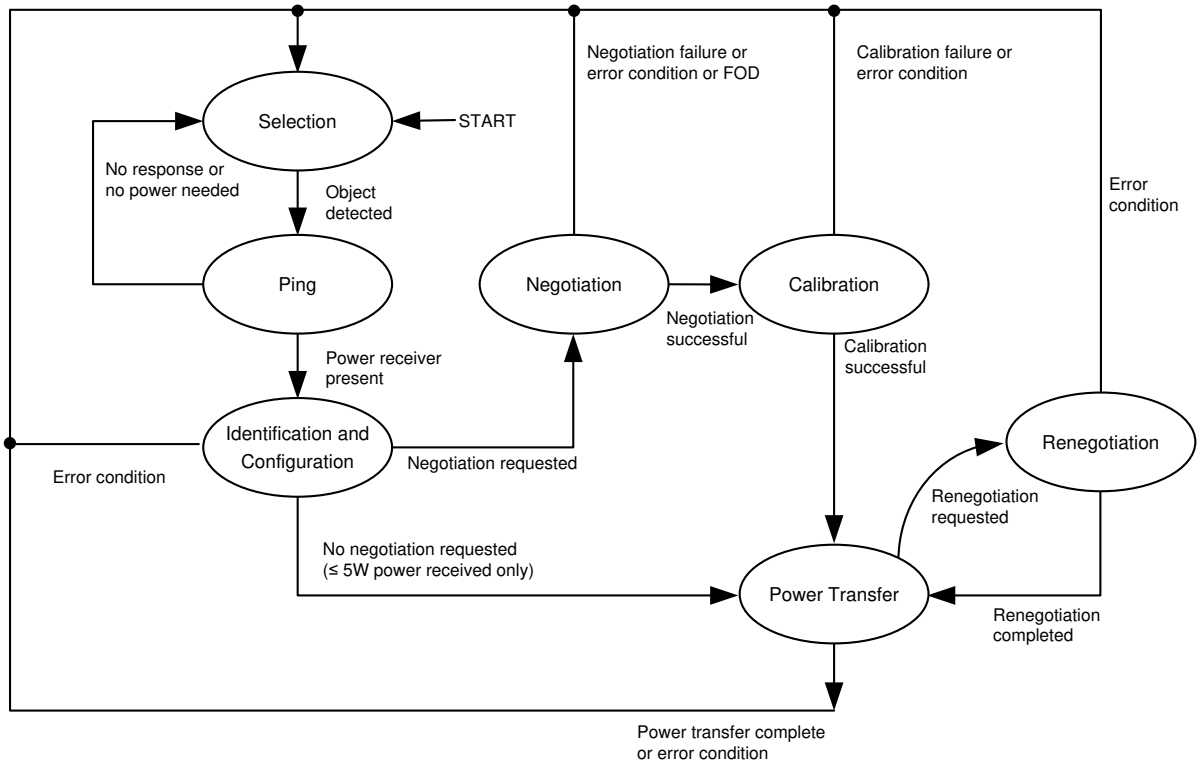
Figure 28. State Diagram for Reading Data Sent from the P9221-R3



10. WPC Mode Characteristics

The WPC-1.2 extended power profile wireless power specification has a negotiation phase, calibration phase, and renegotiation phase, as shown in Figure 29.

Figure 29. WPC Power Transfer Phases Flow Chart



10.1 Selection Phase

In the selection phase, the power transmitter determines if it will proceed to the ping phase after detecting the placement of an object. In this phase, the power transmitter typically monitors the interface surface for the placement and removal of objects using a small measurement signal. This measurement signal should not wake up a power receiver that is positioned on the interface surface.

10.2 Ping Phase (Digital Ping)

In the ping phase, the power transmitter will transmit power and will detect the response from a possible power receiver. This response assures the power transmitter that it is dealing with a power receiver rather than some unknown object. When a power receiver is placed on a WPC “Qi” charging pad, it responds to the application of a power signal by rectifying this power signal. When the internal bias voltage is greater than a specific threshold level, then the receiver is initiated enabling the WPC communication protocol.

If the power transmitter correctly receives a signal strength packet, the power transmitter proceeds to the identification and configuration phase of the power transfer, maintaining the power signal output.

10.3 Identification and Configuration Phase

The identification and configuration phase is the part of the protocol that the power transmitter executes in order to identify the power receiver and establish a default power transfer contract. This protocol extends the digital ping in order to enable the power receiver to communicate the relevant information.

In this phase, the power transmitter identifies itself and receives information for a default power transfer contract as follows:

- It receives the configuration packet.
- If the power transmitter does not acknowledge the request (does not transmit FSK modulation), the power receiver will assume 5W output power.

10.4 Negotiation Phase

In the negotiation phase, the power receiver negotiates changes to the default power transfer contract. In addition, the power receiver verifies that the power transmitter has not detected a foreign object.

10.5 Calibration Phase

In the calibration phase, the power receiver provides information that the power transmitter can use to improve its ability to detect foreign objects during power transfer.

10.6 Power Transfer Phase

In this phase, the P9242-R3 controls the power transfer by means of the following control data packets:

- Control Error Packets (CEP)
- Received Power Packet (RPP, FOD-related)
- End Power Transfer (EPT) Packet

Once the “identification and configuration” phase is completed, the transmitter initiates the power transfer mode. The receiver’s control circuit sends error packets to the transmitter to adjust the rectifier voltage to the level required to maximize the efficiency of the linear regulator and to send to the transmitter the actual received power packet for foreign object detection (FOD) to guarantee safe, efficient power transfer.

In the event of an EPT issued by the application, when the receiver sends EPT packets, the transmitter terminates the power transfer.

11. Functional Registers

The following tables provide address locations, field names, available operations (R or RW), default values, and functional descriptions of all internally accessible registers contained within the P9242-R3. The default I2C slave address is 61_{HEX}.

Table 12. State Register

Address and Bits	Register Field Name	R/W	Default	Function and Description
$06E0_{HEX}$	System_State	R	00_{HEX}	0_{DEC} = Startup 1_{DEC} = Idle 2_{DEC} = Analog Ping Phase 4_{DEC} = Digital Ping Phase 5_{DEC} = WPC Identification 7_{DEC} = WPC Configuration 8_{DEC} = Power Transfer Initialization 9_{DEC} = Power Transfer State 11_{DEC} = Remove Power 12_{DEC} = Restart 13_{DEC} = WPC Negotiation

Table 13. Status Register

Address and Bits	Register Field Name	R/W	Default	Function and Description
$06E1_{HEX}$	System_Status	R	00_{HEX}	0_{DEC} = System Normal 1_{DEC} = FOD Alarm 2_{DEC} = EPT Charge Complete 4_{DEC} = EPT No Response 5_{DEC} = EPT Internal Fault 6_{DEC} = Over-Temperature Alarm 7_{DEC} = Over-Current 9_{DEC} = EPT Other Rx Fault 10_{DEC} = Negotiation Fail

Table 14. Read Register – Coil Current

Address and Bits	Register Field Name	R/W	Default	Function and Description
$06E2_{HEX}$ [7:0]	Coil_current [7:0]	R	–	8 LSB of coil current value in mA.
$06E3_{HEX}$ [7:0]	Coil_current [15:8]	R	–	8 MSB of coil current value in mA.

Table 15. Read Register – Coil Voltage

Address and Bits	Register Field Name	R/W	Default	Function and Description
$06E4_{HEX}$ [7:0]	Coil_voltage [7:0]	R	–	8 LSB of coil voltage value in mV.
$06E5_{HEX}$ [7:0]	Coil_voltage [15:8]	R	–	8 MSB of coil voltage value in mV.

Table 16. Read Register – Remote Temperature Sensing Voltage

$$Sensing\ Voltage = \frac{Thermistor\_ADC\_Value[15:0] * 2.4V}{4095}$$

Address and Bits	Register Field Name	R/W	Default	Function and Description
$06E8_{HEX}$ [7:0]	Thermistor_ADC_Value [7:0]	R	–	8 LSB of thermistor ADC value.
$06E9_{HEX}$ [7:0]	Thermistor_ADC_Value [15:8]	R	–	8 MSB of thermistor ADC value.

Table 17. Read Register – Operating Frequency

$$f_{OP} = \frac{60\ MHz}{FRE\_CNT[15:0]}$$

Address and Bits	Register Field Name	R/W	Default	Function and Description
$06EA_{HEX}$ [7:0]	FRE_CNT [7:0]	R	–	8 LSB of operating frequency count.
$06EB_{HEX}$ [7:0]	FRQ_CNT [15:8]	R	–	8 MSB of operating frequency count.

Table 18. Read Register – Operating Duty Cycle

$$DUTY\ CYCLE = \frac{DUTY\_CNT * 50\%}{255}$$

Address and Bits	Register Field Name	R/W	Default	Function and Description
$06EC_{HEX}$ [7:0]	DUTY_CNT [7:0]	R	–	8 LSB of operating duty count.
$06ED_{HEX}$ [7:0]	DUTY_CNT [15:8]	R	–	8 MSB of operating duty count.

Table 19. Read Register – Full/Half Bridge Status

Address and Bits	Register Field Name	R/W	Default	Function and Description
$06EE_{HEX}$ [7:0]	Full/half_bridge_status [7:0]	R	–	“0” = Half bridge. "1" = Full bridge.

Table 20. Command Register

Address and Bits	Register Field Name	R/W	Default	Function and Description
$0800[7]_{HEX}$	Reserved	R	0_{BIN}	
$0800[6:3]_{HEX}$	Number_of_bytes_ to_be_ transferred	RW	0000_{BIN}	0100_{BIN} = Transfer 10 bytes 0011_{BIN} = Transfer 8 bytes 0010_{BIN} = Transfer 6 bytes 0001_{BIN} = Transfer 4 bytes 0000_{BIN} = Transfer 2 bytes
$0800[2:1]_{HEX}$	Number_of_repeats	RW	00_{BIN}	11_{BIN} = Send 4 times 10_{BIN} = Send 3 times 01_{BIN} = Send 2 times 00_{BIN} = Send only 1 time
$0800[0]_{HEX}$	Communication_Trigger	RW	0_{BIN}	If the communication channel is free, this bit is set to “0.” The external MCU sets this bit to "1” to trigger the communication. The P9242-R3 will reset this bit to 0 immediately after sending the data into the channel.

Table 21. Data Received Status Register

Address and Bits	Register Field Name	R/W	Default	Function and Description
$0801[7:1]_{HEX}$	Reserved	R	$0000\ 000_{BIN}$	
$0801[0]_{HEX}$	Data_Received_Flag	RW	0_{BIN}	0_{BIN} = No new data received 1_{BIN} = Received new data

Table 22. Clear Interrupt Register

Address and Bits	Register Field Name	R/W	Default	Function and Description
$0803[7:1]_{HEX}$	Reserved	R	$000\ 0000_{BIN}$	
$0803[0]_{HEX}$	Clear_interrupt_pin	RW	0_{BIN}	The external MCU sets this bit to "1” to clear interrupt pin. P9242-R3 will reset this bit to “0” soon after clearing the interrupt pin

Table 23. Outgoing User Data Registers

Address and Bit	Register Field Name	R/W	Default	Function and Description
0805_{HEX}	Outgoing_User_Data_0	RW	00_{HEX}	The external MCU writes into this register the data it will send to the P9221-R3.
0806_{HEX}	Outgoing_User_Data_1	RW	00_{HEX}	The external MCU writes into this register the data it will send to the P9221-R3.
0807_{HEX}	Outgoing_User_Data_2	RW	00_{HEX}	The external MCU writes into this register the data it will send to the P9221-R3.
0808_{HEX}	Outgoing_User_Data_3	RW	00_{HEX}	The external MCU writes into this register the data it will send to the P9221-R3.
0809_{HEX}	Outgoing_User_Data_4	RW	00_{HEX}	The external MCU writes into this register the data it will send to the P9221-R3.
$080A_{HEX}$	Outgoing_User_Data_5	RW	00_{HEX}	The external MCU writes into this register the data it will send to the P9221-R3.
$080B_{HEX}$	Outgoing_User_Data_6	RW	00_{HEX}	The external MCU writes into this register the data it will send to the P9221-R3.
$080C_{HEX}$	Outgoing_User_Data_7	RW	00_{HEX}	The external MCU writes into this register the data it will send to the P9221-R3.
$080D_{HEX}$	Outgoing_User_Data_8	RW	00_{HEX}	The external MCU writes into this register the data it will send to the P9221-R3.
$080E_{HEX}$	Outgoing_User_Data_9	RW	00_{HEX}	The external MCU writes into this register the data it will send to the P9221-R3.

Table 24. Incoming Data Header Register

Address and Bit	Register or Bit Field Name	R/W	Default	Function and Description
$080F_{HEX}$	Incoming_Number_of_Bytes	R	00_{HEX}	Indicates number of incoming registers received 18_{HEX} = Received 1 byte of user data 28_{HEX} = Received 2 bytes of user data 38_{HEX} = Received 3 bytes of user data 48_{HEX} = Received 4 bytes of user data 58_{HEX} = Received 5 bytes of user data 68_{HEX} = Received 6 bytes of user data 78_{HEX} = Received 7 bytes of user data 84_{HEX} = Received 8 bytes of user data

Table 25. Incoming User Data Registers

Address and Bit	Register Field Name	R/W	Default	Function and Description
0810_{HEX}	Incoming_User_Data_0	RW	00_{HEX}	The external MCU reads this register to get the data that the P9242-R3 received from the P9221-R3.
0811_{HEX}	Incoming_User_Data_1	RW	00_{HEX}	The external MCU reads this register to get the data that the P9242-R3 received from the P9221-R3.
0812_{HEX}	Incoming_User_Data_2	RW	00_{HEX}	The external MCU reads this register to get the data that the P9242-R3 received from the P9221-R3.
0813_{HEX}	Incoming_User_Data_3	RW	00_{HEX}	The external MCU reads this register to get the data that the P9242-R3 received from the P9221-R3.
0814_{HEX}	Incoming_User_Data_4	RW	00_{HEX}	The external MCU reads this register to get the data that the P9242-R3 received from the P9221-R3.
0815_{HEX}	Incoming_User_Data_5	RW	00_{HEX}	The external MCU reads this register to get the data that the P9242-R3 received from the P9221-R3.
0816_{HEX}	Incoming_User_Data_6	RW	00_{HEX}	The external MCU reads this register to get the data that the P9242-R3 received from the P9221-R3.
0817_{HEX}	Incoming_User_Data_7	RW	00_{HEX}	The external MCU reads this register to get the data that the P9242-R3 received from the P9221-R3.

12. Application Information

12.1 Power Dissipation and Thermal Requirements

The P9242-R3 is offered in a 48-VFQFPN package that has a maximum power dissipation capability of about 1.47W. The maximum power dissipation of the package is determined by the number of thermal vias between the package and the printed circuit board (PCB). The maximum power dissipation of the package is defined by the die's specified maximum operating junction temperature, $T_{J(MAX)}$ of 125°C. The junction temperature rises when the heat generated by the device's power dissipation flow is impeded by the package-to-PCB thermal resistance.

The VFQFPN package offers a typical thermal resistance, junction to ambient (θ_{JA}), of 27.2°C/W when the PCB layout design is optimized as described in the *P9242-R3 Layout Guide* document. The techniques noted in the PCB layout section must be followed when designing the printed circuit board layout. Take into consideration possible proximity to other heat-generating devices when placing the P9242-R3 and the bridge FET packages in a given application design. The ambient temperature around the power IC will also have an effect on the thermal limits of an application. The main factors influencing θ_{JA} (in the order of decreasing influence) are PCB characteristics, die/package attached thermal pad size (VFQFPN), thermal vias, and the final system hardware construction. Board designers should keep in mind that the package thermal metric θ_{JA} is impacted by the characteristics of the PCB. Changing the design or configuration of the PCB changes the overall thermal resistivity and the board's heat-sinking efficiency.

Three basic approaches for enhancing thermal performance are listed below:

- Improving the power dissipation capability of the PCB design.
- Improving the thermal coupling of the component to the PCB.
- Introducing airflow into the system.

First, the maximum power dissipation for a given situation should be calculated using Equation 2:

$$P_{D(MAX)} = \frac{\left(T_{J(MAX)} - T_{AMB}\right)}{\theta_{JA}} \qquad \text{Equation 2}$$

Where:

$P_{D(MAX)}$ = Maximum power dissipation

θ_{JA} = Package thermal resistance (°C/W)

$T_{J(MAX)}$ = Maximum device junction temperature (°C)

T_{AMB} = Ambient temperature (°C)

The maximum recommended operating junction temperature ($T_{J(MAX)}$) for the P9242-R3 is 125°C. The thermal resistance of the 48-pin VFQFPN package (NDG48) is optimally θ_{JA}=27.2°C/W. Operation is specified to a maximum steady-state ambient temperature (T_{AMB}) of 85°C. Therefore, the maximum recommended power dissipation is given by Equation 3:

$$P_{D(MAX)} = \frac{(125°C - 85°C)}{27.2°C/W} \cong 1.47 \text{ Watt} \qquad \text{Equation 3}$$

All the above-mentioned thermal resistances were determined with the P9242-R3 mounted on a standard board of the dimensions and characteristics specified by the JEDEC 51 standard.

12.2 Recommended Coils

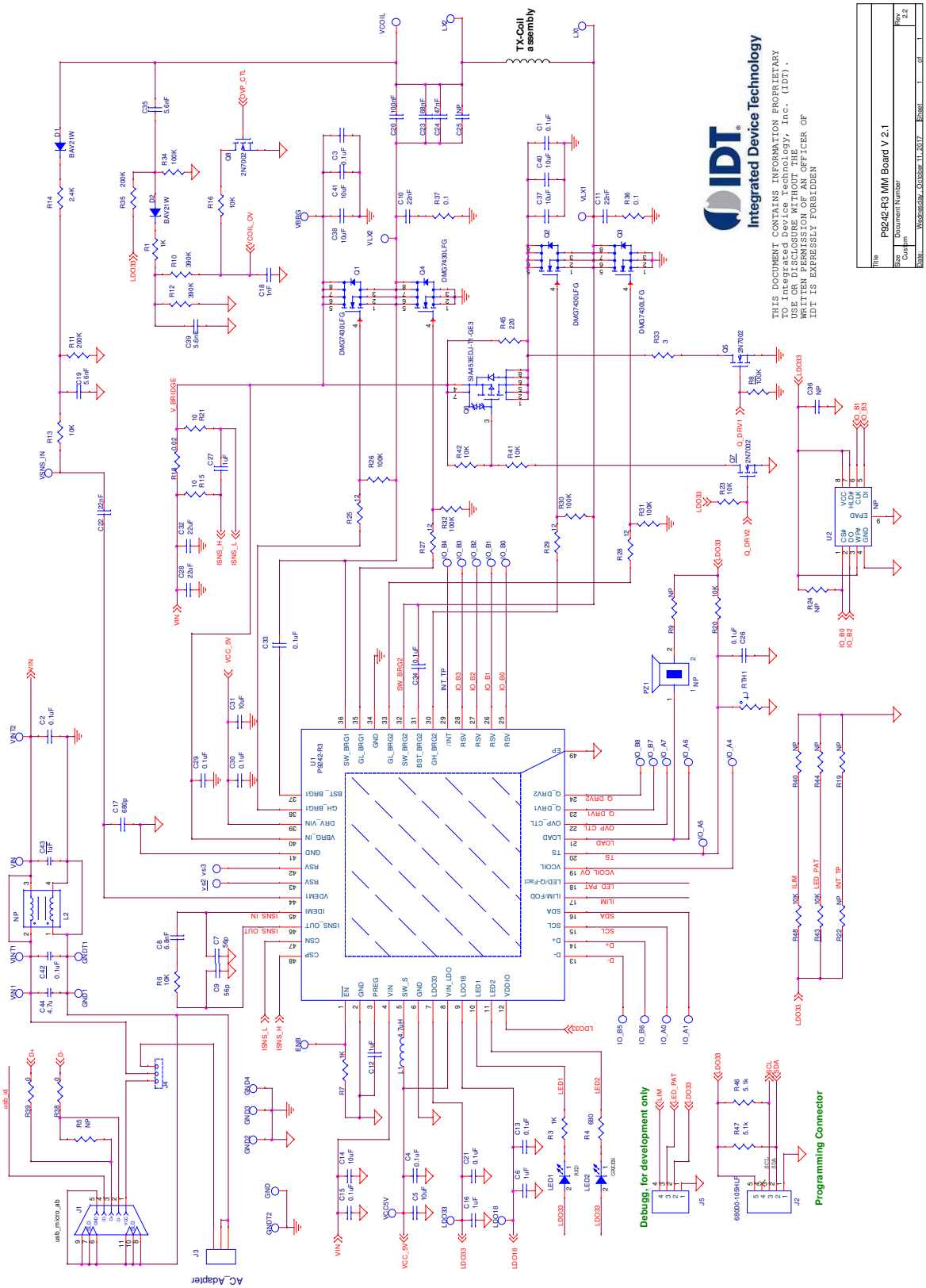
Table 26. Recommended Coil Manufactures

Output Power	Vendor	Part number	Inductance at 100kHz	DCR at 20°C
15W	SUNLORD	SWA53N53H30C11B	10µH	50mΩ
15W	TDK	WT525225-12F2-MA2-G	10.6µH	40mΩ
15W	WURTH	760308103102	10µH	55mΩ

12.3 Typical Application Schematic – P9242-R3-EVK included in WP15WBD-RK Kit

Note: The typical application schematic provides a basic guideline to understanding and building a functional medium-power wireless power transmitter type MP-A2 as described in the WPC specifications. Other components, not shown on the typical application schematic, might be needed in order to comply with other requirements, such as EMC or thermal specifications.

Figure 30. P9242-R3-EVK Typical Application Schematic



12.4 Bill of Materials (BOM)

Table 27. P9242-R3-EVK Evaluation Kit V2.1 Bill of Materials

Item	Quantity	Reference	Value	Description	Part Number	PCB Footprint
1	12	C1, C2, C3, C4, C13, C15, C21, C26, C29, C30, C33, C34	0.1µF	CAP CER 0.1µF 25V 10% X7R 0402	C1005X7R1E104K050BB	0402
2	7	C5, C14, C31, C37, C38, C40, C41	10µF	CAP CER 10µF 25V 20% X5R 0603	C1608X5R1E106M080AC	0603
3	4	C6, C12, C16, C27	1µF	CAP CER 1µF 25V 20% X5R 0402	C1005X5R1E105M050BC	0402
4	2	C7, C9	56pF	CAP CER 56PF 50V NP0 0402	CL05C560JB5NNNC	0402
5	1	C8	6.8nF	CAP CER 6800PF 25V X7R 0402	GRM155R71E682KA01D	0402
6	2	C10, C11	22nF	0.022µF 50V Ceramic Capacitor X7R 0603	GCM188R71H223KA37D	0603
7	1	C17	680pF	CAP CER 680PF 50V X7R 0402	CL05B681KB5NNNC	0402
8	1	C18	1nF	CAP CER 1000pF ±10% 50V X7R 0402	GRM155R71H102KA01D	0402
9	3	C19, C35, C39	5.6nF	5600pF 100V Ceramic Capacitor C0G, NP0 0603	C1608C0G2A562J080AC	0603
10	1	C20	100nF	CAP CER 0.1µF 100V C0G 1206	C3216C0G2A104K160AC	1206
11	1	C22	22nF	CAP CER 0.022µF 50V 10% X7R 0402	GRM155R71H223KA12D	0402
12	1	C23	68nF	CAP CER 0.068µF 100V NP0 1206	C3216C0G2A683K160AC	1206
13	1	C24	47nF	CAP CER 0.047µF 100V NP0 1206	C3216C0G2A473J115AC	1206
14	1	C25	NP	CAP CER 10000PF 100V C0G 1206	C3216C0G2A103J115AA	1206
15	2	C28, C32	22µF	CAP CER 22µF 25V 20% X5R 1206	GRM31CR61E226KE15L	1206
16	1	C36	0.1µF	CAP CER 0.1µF 25V 10% X7R 0402	C1005X7R1E104K050BB	0402
17	1	C42	0.1µF	0.10µF 50V Ceramic Capacitor X7R 0603	GRM188R71H104KA93D	0603
18	1	C43	1µF	1µF 25V Ceramic Capacitor X5R 0603	GRM188R61E105KA12D	0603
19	1	C44	4.7µF	4.7µF 25V Ceramic Capacitor X5R 0603	GRM188R61E475KE11D	0603
20	2	D1, D2	BAV21W	DIODE GEN PURP 80V 125MA DFN	BAV21W-7-F	sod123

Item	Quantity	Reference	Value	Description	Part Number	PCB Footprint
21	30	VLX1, VINT1, IO_B1, IO_A1, GNDT1, vs2, VLX2, VINT2, IO_B2, GNDT2, vs3, IO_B3, IO_B4, IO_A4, VCC5V, IO_B5, IO_A5, IO_B6, IO_A6, IO_B7, IO_A7, IO_B8, LDO18, LDO33, VSNS_IN, VCOIL, VBRG, IO_B0, IO_A0, ENB	PTH_TP	30 GAUGE WIRE PAD	NP	TEST_PT30DPAD
22	7	VIN1, GND1, GND2, GND3, GND4, VIN, GND	TP	TEST POINT PC MINIATURE SMT	5015	test_pt_sm_135x70
23	1	J1	5P	CONN RCPT MCR USB AB SMD TH SHLL	ZX62D-AB-5P8	usb_micro_ab
24	1	J2	68000-105HLF	BERGSTIK II .100" SR STRAIGHT	68000-105HLF	sip5
25	1	J3	AC Adapter	CONN POWER JACK 2.5X5.5MM HI CUR	PJ-002AH	CONN_POWER_JACK5_5MM
26	1	J4	TP	CONN HEADER 3POS .100" STR GOLD	901200763	sip3
27	1	J5	SIP con	4-position header	961104-6404-AR	sip-4
28	1	LED1	LED	LED RED CLEAR 0603 SMD	150060RS75000	0603_diode
29	1	LED2	LED	LED GREEN CLEAR 0603 SMD	150060GS75000	0603_diode
30	2	LX1, LX2	NP	Tx coil assemble through hole	NA	TP_TXCoil
31	1	L1	4.7µH	FIXED IND 4.7µH 620MA 500 MOHM	CIG10W4R7MNC	L0603
32	1	L2	NP	Common mode EMI choke	ACM4520-901-2P-T-000	EMI_TDK_ACM4520L
33	1	PZ1	NP	BUZZER PIEZO 4KHZ 12.2MM PC MNT	PS1240P02CT3	9235_buzzer
34	4	Q1, Q2, Q3, Q4	DMG7430LFG	MOSFET N-CH 30V 10.5A PWRDI3333	DMG7430LFG-7	powerdi3333_8ld_fet
35	3	Q5, Q7, Q8	2N7002	N-Channel 60-V (D-S) MOSFET	2N7002KT1G	SOT23_3
36	1	Q6	MOSFET	MOSFET P-CH 30V SC-70-6	SIA449DJ-T1-GE3	sc70_6ld_fet
37	1	RTH1	NP	NTC thermistor 10k bead	NTCLE203E3103JB0	0805
38	3	R1, R3, R7	1kΩ	RES SMD 1K OHM 5% 1/16W 0402	RC0402JR-071KL	0402
39	1	R4	680Ω	RES SMD 680 OHM 5% 1/16W 0402	RC0402JR-07680RL	0402
40	1	R5	NP	RES SMD 0.0 OHM JUMPER 1/10W	RC0402JR-070RL	0402
41	9	R6, R13, , R16, R20, R23, R41, R42, R43, R48	10kΩ	RES SMD 10K OHM 1% 1/10W 0402	RC0402FR-0710KL	0402
42	5	R8, R26, R30, R31, R32	100kΩ	RES SMD 100K OHM 5% 1/10W 0402	ERJ-2GEJ104X	0402
43	1	R24	100kΩ	RES SMD 100K OHM 5% 1/10W 0402	ERJ-2GEJ104X	0402

Item	Quantity	Reference	Value	Description	Part Number	PCB Footprint
44	1	R9	NP	RES SMD 100 OHM 5% 1/10W 0603	RC0603JR-07100RL	0603
45	2	R10, R12	390kΩ	RES SMD 390K OHM 5% 1/10W 0603	ERJ-3GEYJ394V	0603
46	1	R14	2.4kΩ	RES SMD 2.4K OHM 5% 1/10W 0402	ERJ-2GEJ242X	0402
47	2	R11, R35	200kΩ	RES SMD 200K OHM 1% 1/10W 0603	RC1608F204CS	0603
48	2	R15, R21	10Ω	RES SMD 10 OHM 1% 1/10W 0402	ERJ-2RKF10R0X	0402
49	1	R18	0.02Ω	RES SMD 0.02 OHM 1% 1/8W 0805	WSL0805R0200FEA	0805
50	4	R19, R22, R40, R44	NP	RES SMD 10K OHM 1% 1/10W 0402	RC0402FR-0710KL	0402
51	4	R25, R27, R28, R29	12Ω	RES SMD 12 OHM 5% 1/10W 0402	ERJ-2GEJ120X	0402
52	1	R33	3Ω	RES SMD 3 OHM 1% 1/8W 0805	RC0805FR-073RL	0805
53	1	R34	100kΩ	RES SMD 100K OHM 1% 1/10W 0603	ERJ-3EKF1003V	0603
54	2	R36, R37	0.1Ω	RES SMD 0.1 OHM 5% 1/6W 0402	ERJ-2BSJR10X	0402
55	2	R38, R39	0Ω	RES SMD 0.0 OHM JUMPER 1/10W	RC0402JR-070RL	0402
56	1	R45	220Ω	RES SMD 220 OHM 1% 0.4W 0805	RC1206FR-07220RL	1206
57	2	R46, R47	5.1kΩ	RES SMD 5.1K OHM 5% 1/16W 0402	MCR01MRTJ512	0402
58	1	U1	P9242-RB	Medium Power Transmitter	P9242-RB	socketqfn_48_6x6_0p4
59	1	U2	W25X20CLUXIG	SPIFLASH 2M-BIT 4KB UNIFORM SECT	W25X20CLUXIG TR	uson_2x3_8LD

13. Package Outline Drawing

The package outline drawings are appended at the end of this document and are accessible from the link below. The package information is the most current data available.

www.idt.com/document/psc/48-vfqfpn-package-outline-drawing-60-x-60-x-090-mm-body-epad-42-x-42-mm-040mm-pitch-ndg48p2

14. Special Notes: NDG 48-VFQFPN Package Assembly

Unopened dry packaged parts have a one-year shelf life.

The HIC indicator card for newly-opened dry packaged parts should be checked. If there is any moisture content, the parts must be baked for a minimum of 8 hours at 125˚C within 24 hours prior to the assembly reflow process.

15. Marking Diagrams

- Line 1: Company name and part number.
- Line 2: -R3 is part of the part number, which is followed by the package code.
- Line 3: “YYWW” is the last two digits of the year and two digits for the week that the part was assembled. # is the device step. “$” denotes the mark code.

- Line 1: Company name and part number.
- Line 2: -RB is part of the part number, which is followed by the package code.
- Line 3: “YYWW” is the last two digits of the year and two digits for the week that the part was assembled. # is the device step. “$” denotes the mark code.

16. Ordering Information

Orderable Part Number	Description and Package	MSL Rating	Shipping Package	Ambient Temperature
P9242-R3NDGI	P9242-R3 Wireless Power Receiver for 15W Applications, 48-VFQFPN (6 x 6 mm) package (NDG48P2)	MSL1	Tray	-40°C to +85°C
P9242-R3NDGI8	P9242-R3 Wireless Power Receiver for 15W Applications, 48-VFQFPN (6 x 6 mm) package (NDG48P2)	MSL1	Reel	-40°C to +85°C
P9242-RBNDGI[a]	P9242-RB Wireless Power Transmitter for 15W Applications with only bootloader pre-programmed, 48-VFQFPN (6 × 6 mm) package	MSL1	Tray	-40°C to +85°C
P9242-RBNDGI8[a]	P9242-RB Wireless Power Transmitter for 15W Applications with only bootloader pre-programmed, 48-VFQFPN (6 × 6 mm) package	MSL1	Reel	-40°C to +85°C
WP15WBD-RK	WP15WBD-RK Bi-directional Data Transfer Evaluation Kit including P9242-R3-EVK Transmitter Evaluation Board, P9221-R3-EVK Receiver Evaluation Board, two USB to I2C dongles, and one 12V/2A AC adapter.			

[a] The P9242-R3 has the bootloader and application firmware pre-programmed into internal one-time programmable (OTP) memory. The P9242-RB, which is pin compatible with the P9242-R3, has only the bootloader pre-programmed into OTP memory. The P9242-RB must be used in conjunction with an external flash; however, there is no functionality difference of the P9242-R3 IC or the P9242-RB with external flash.

17. Revision History

Revision Date	Description of Change
May 17, 2019	Added P9242-RB information. Updated Package Outline Drawings section.
October 20, 2017	Initial release.

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