5.6 GHz to 8.6 GHz, GaAs, MMIC, I/Q Downconverter

Data Sheet **HMC951A**

FEATURES

Conversion gain: 13 dB typical
Image rejection: 32 dBc typical
Input P1dB compression: −6 dBm typical
Input IP3: 3 dBm typical, 6.0 GHz to 8.6 GHz
Noise figure: 2 dB typical
LO to RF isolation: 48 dBm typical
LO to IF isolation: 13 dBm typical
RF to IF isolation: 10 dBm typical
Amplitude balance: 0.2 dB typical
Phase balance: −2° typical
RF return loss: 10 dB typical
LO return loss: 15 dB typical
IF return loss: 15 dB typical
Exposed paddle, 4 mm × 4 mm, 24-lead, LFCSP

APPLICATIONS

Point to point and point to multipoint radios
Military radars, electronic warfare, and electronic intelligence
Satellite communications
Sensors

FUNCTIONAL BLOCK DIAGRAM

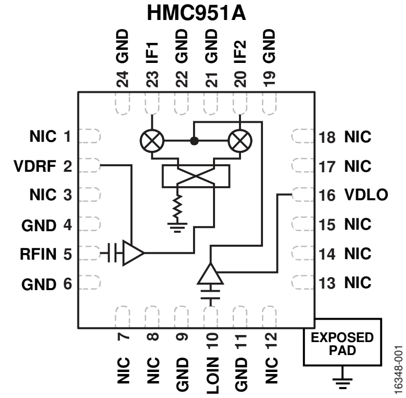

Figure 1.

GENERAL DESCRIPTION

The HMC951A is a compact gallium arsenide (GaAs), monolithic microwave integrated circuit (MMIC), in-phase quadrature (I/Q) downconverter in a RoHS compliant package that operates from 5.6 GHz to 8.6 GHz. This device provides a small signal conversion gain of 13 dB with a noise figure of 2 dB and an image rejection of 32 dBc. The HMC951A uses a low noise amplifier (LNA) followed by an image mixer that is driven by a local oscillator (LO) buffer amplifier. The image reject mixer eliminates the need for a filter following the LNA and removes thermal noise at the image frequency. The IF1 and IF2 mixer outputs are provided and an external 90° hybrid is needed to select the required sideband. The I/Q mixer topology reduces the need for filtering of unwanted sideband. The HMC951A is a smaller alternative to hybrid style, single sideband (SSB) downconverter assemblies, and it eliminates the need for wire bonding by allowing the use of surface-mount manufacturing techniques.

The HMC951A is available in 4 mm × 4 mm, 24-lead lead frame chip scale package (LFCSP) and operates over the −40°C to +85°C temperature range. An evaluation board for the HMC951A is also available upon request.

Rev. A Document Feedback

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Technical Support www.analog.com

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REVISION HISTORY

4/2018—Rev. 0 to Rev. A

Changes to Performance at Lower IF Frequencies Section ... 29
Removed Figure 99; Renumbered Sequentially ... 29

3/2018—Revision 0: Initial Version

SPECIFICATIONS

5.6 GHz TO 6.0 GHz

T_A = 25°C, intermediate frequency (IF) = 1000 MHz, VDRF = VDLO = 5 V, local oscillator (LO) power = 0 dBm, unless otherwise noted. Measurements performed with lower sideband selected and an external 90° hybrid at the IF ports, unless otherwise noted.

Table 1.

Parameter	Min	Typ	Max	Unit
OPERATING CONDITIONS				
Frequency Range				
Radio Frequency (RF)	5.6		6.0	GHz
LO	4.5		12.1	GHz
IF	DC		3.5	GHz
LO Drive Range	−4	0	+4	dBm
PERFORMANCE				
Conversion Gain	10	13		dB
Image Rejection	20	32		dBc
Input Power for 1 dB Compression (P1dB)		−6		dBm
Input Third-Order Intercept (IP3)	0	2		dBm
Amplitude Balance		0.2		dB
Phase Balance		−2		Degree
Isolation				
LO to RF	40	48		dB
LO to IF	9	13		dB
RF to IF		10		dB
Noise Figure		2	2.5	dB
Return Loss				
RF		10		dB
LO		15		dB
IF		15		dB
POWER SUPPLY				
Drain Current				
Low Noise Amplifier (I_{DD1})		75	85	mA
LO Amplifier (I_{DD2})		80	95	mA
Total Drain Current (I_{DD})		155		mA

6.0 GHz TO 8.6 GHz

T_A = 25°C, intermediate frequency (IF) = 1000 MHz, VDRF = VDLO = 5 V, local oscillator (LO) power = 0 dBm, unless otherwise noted. Measurements performed with lower sideband selected and an external 90° hybrid at the IF ports, unless otherwise noted.

Table 2.

Parameter	Min	Typ	Max	Unit
OPERATING CONDITIONS				
Frequency Range				
Radio Frequency (RF)	6.0		8.6	GHz
LO	4.5		12.1	GHz
IF	DC		3.5	GHz
LO Drive Range	−4	0	+4	dBm
PERFORMANCE				
Conversion Gain	10	13		dB
Image Rejection	20	32		dBc
Input Power for 1 dB Compression (P1dB)		−6		dBm
Input Third-Order Intercept (IP3)	1	3		dBm
Amplitude Balance		0.2		dB
Phase Balance		−2		Degree
Isolation				
LO to RF	40	48		dB
LO to IF	9	13		dB
RF to IF		10		dB
Noise Figure		2	2.5	dB
Return Loss				
RF		10		dB
LO		15		dB
IF		15		dB
POWER SUPPLY				
Drain Current				
Low Noise Amplifier (I_{DD1})		75	85	mA
LO Amplifier (I_{DD2})		80	95	mA
Total Drain Current (I_{DD})		155		mA

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
Drain Bias Voltage (VDRF, VDLO)	5.5 V
Input Power	
LO	20 dBm
RF	15 dBm
Moisture Sensitivity Level (MSL) Rating[1]	MSL3
Maximum Junction Temperature	175°C
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−40°C to +85°C
Reflow Temperature	260°C
Electrostatic Discharge Sensitivity	
Human Body Model (HBM)	1000 V
Field Induced Charged Device Model (FICDM)	750 V

[1] See the Ordering Guide.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Careful attention to PCB thermal design is required.

θ_{JA} is the junction to ambient (or die to ambient) thermal resistance measured in a one cubic foot sealed enclosure, and θ_{JC} is the junction to case (or die to package) thermal resistance.

Table 4. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
HCP-24-3[1]	40.9	46.4	°C/W

[1] Thermal impedance simulated values are based on a JEDEC 2S2P test board with 4 × 4 thermal vias. Refer to JEDEC standard JESD51-2 for additional information.

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

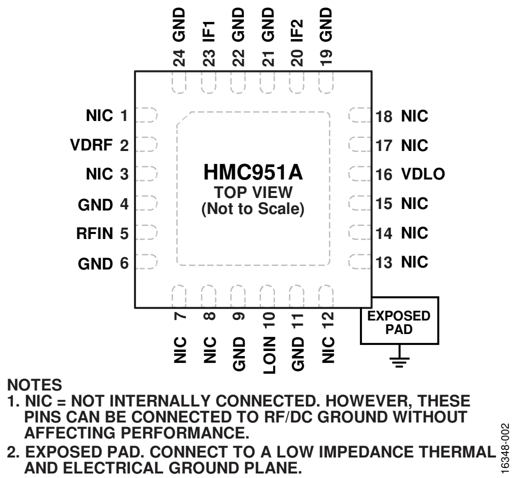

Figure 2. Pin Configuration

Table 5. Pin Function Descriptions

Pin No.	Mnemonic	Description
1, 3, 7, 8, 12 to 15, 17, 18	NIC	Not Internally Connected. However, these pins can be connected to RF/dc ground without affecting performance.
2	VDRF	Power Supply Voltage for the RF Amplifier. See Figure 3 for the interface schematic. Refer to the typical application circuit (see Figure 96) for the required external components.
4, 6, 9, 11, 19, 21, 22, 24	GND	Ground Connect. See Figure 4 for the interface schematic. These pins and package bottom must be connected to RF/dc ground.
5	RFIN	Radio Frequency Input. See Figure 5 for the interface schematic. This pin is ac-coupled and matched to 50 Ω.
10	LOIN	Local Oscillator Input. See Figure 6 for the interface schematic. This pin is ac-coupled and matched to 50 Ω.
16	VDLO	Power Supply Voltage for the LO Amplifier. See Figure 3 for the interface schematic. Refer to the typical application circuit (see Figure 96) for the required external components.
20, 23	IF2, IF1	Quadrature Intermediate Frequency Outputs. See Figure 7 for the interface schematic. For applications not requiring operation to dc, use an off chip dc blocking capacitor. For operation to dc, these pins must not source or sink more than 3 mA of current or device malfunction and failure can result.
	EPAD	Exposed Pad. Connect to a low impedance thermal and electrical ground plane.

INTERFACE SCHEMATICS

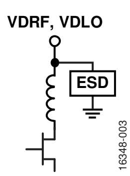

Figure 3. VDRF, VDLO Interface

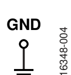

Figure 4. GND Interface

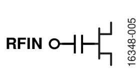

Figure 5. RFIN Interface

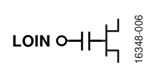

Figure 6. LOIN Interface

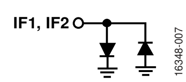

Figure 7. IF2, IF1 Interface

TYPICAL PERFORMANCE CHARACTERISTICS

LOWER SIDEBAND (HIGH-SIDE LO)

IF = 1000 MHz and RF input power = −20 dBm. Data de-embedded for RF trace loss, unless otherwise noted.

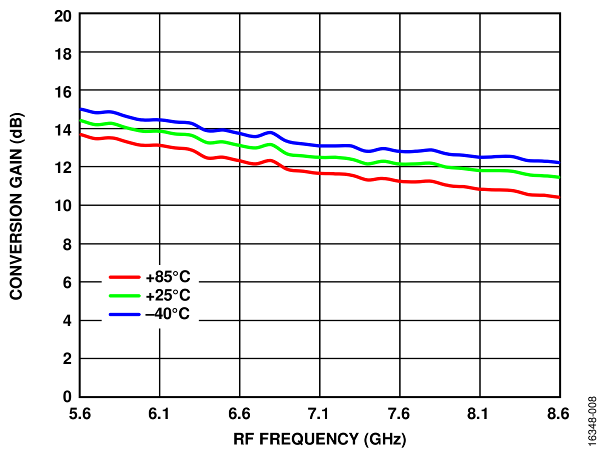

Figure 8. Conversion Gain vs. RF Frequency over Temperatures, LO Power = 0 dBm

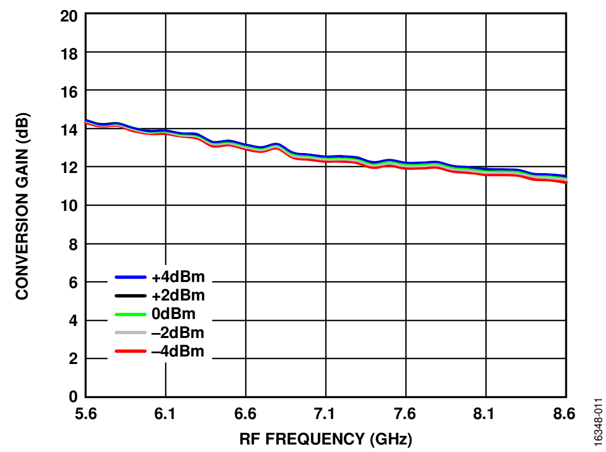

Figure 11. Conversion Gain vs. RF Frequency over LO Powers, T_A = 25°C

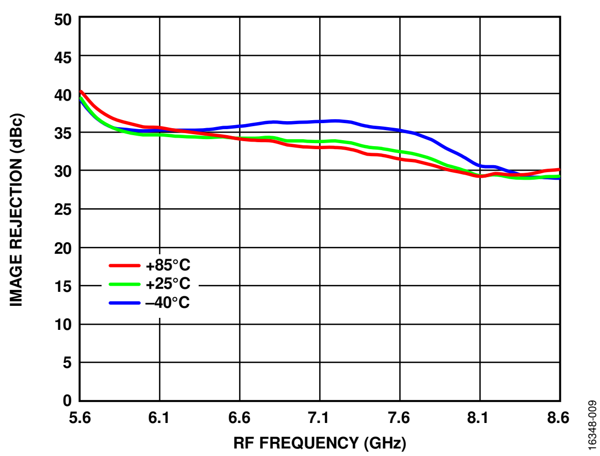

Figure 9. Image Rejection vs. RF Frequency over Temperatures, LO Power = 0 dBm

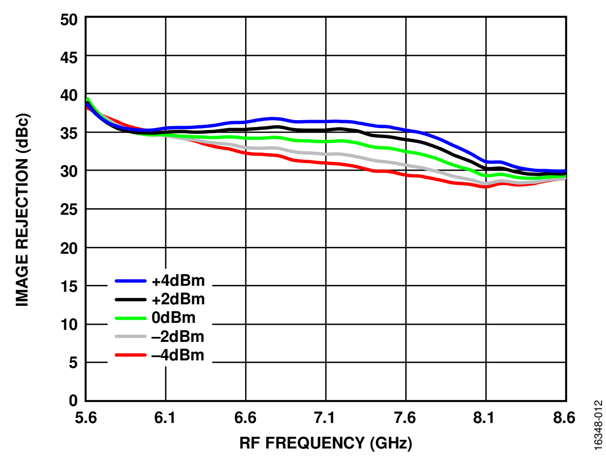

Figure 12. Image Rejection vs. RF Frequency over LO Powers, T_A = 25°C

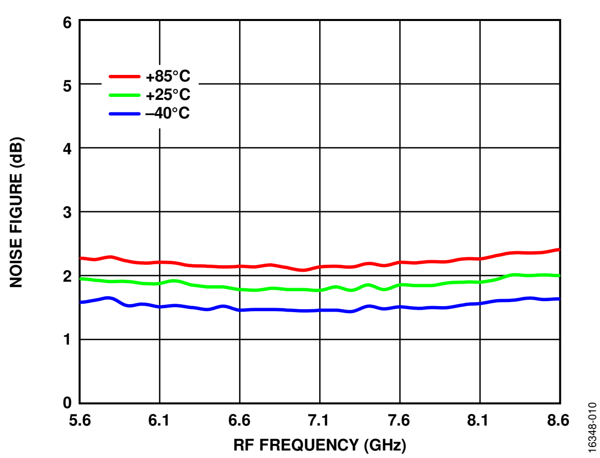

Figure 10. Noise Figure vs. RF Frequency over Temperatures, LO Power = 0 dBm

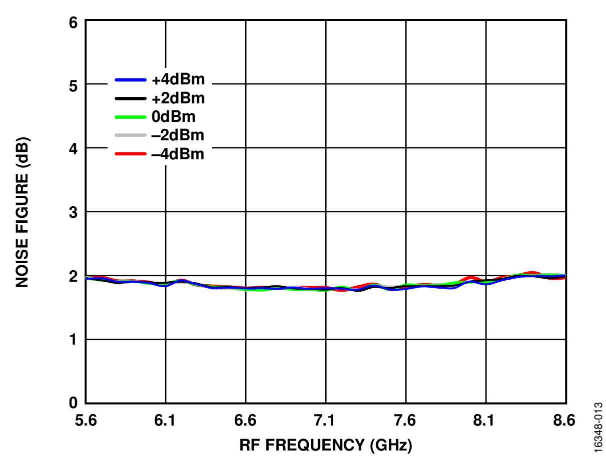

Figure 13. Noise Figure vs. RF Frequency over LO Powers, T_A = 25°C

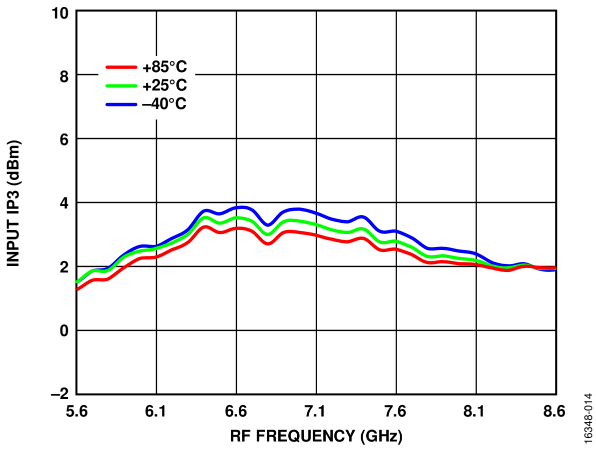

Figure 14. Input IP3 vs. RF Frequency over Temperatures, LO Power = 0 dBm

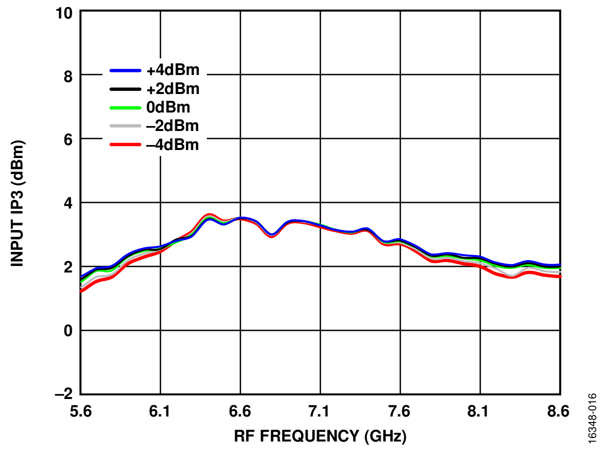

Figure 16. Input IP3 vs. RF Frequency over LO Powers, T_A = 25°C

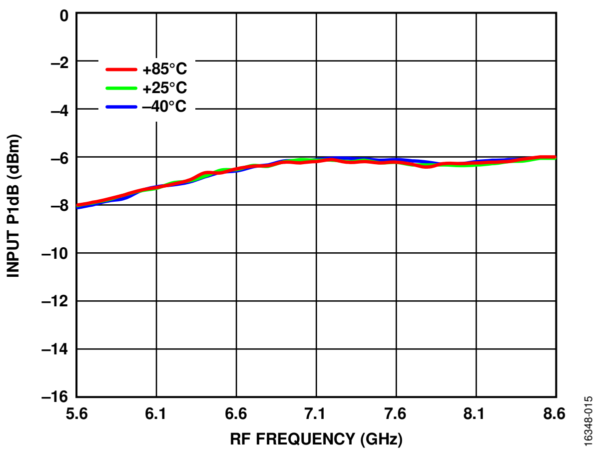

Figure 15. Input P1dB vs. RF Frequency over Temperatures, LO Power = 0 dBm

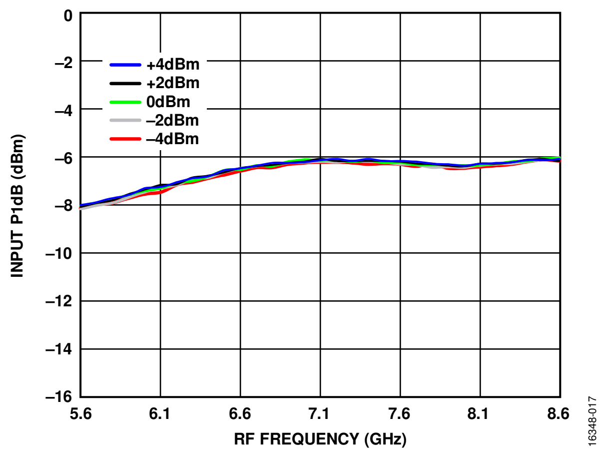

Figure 17. Input P1dB vs. RF Frequency over LO Powers, T_A = 25°C

IF = 150 MHz and RF input power = −20 dBm. Data de-embedded for RF trace loss, unless otherwise noted.

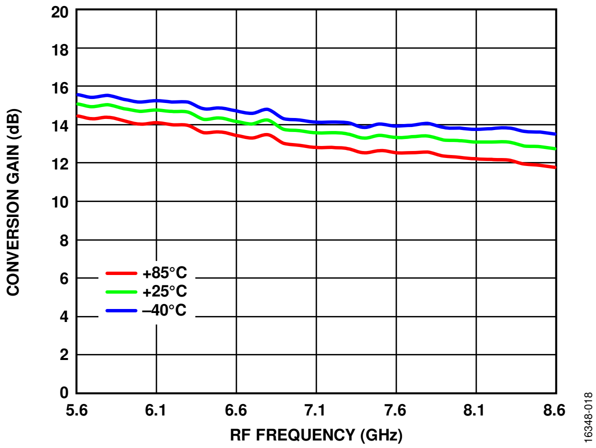

Figure 18. Conversion Gain vs. RF Frequency over Temperatures, LO Power = 0 dBm

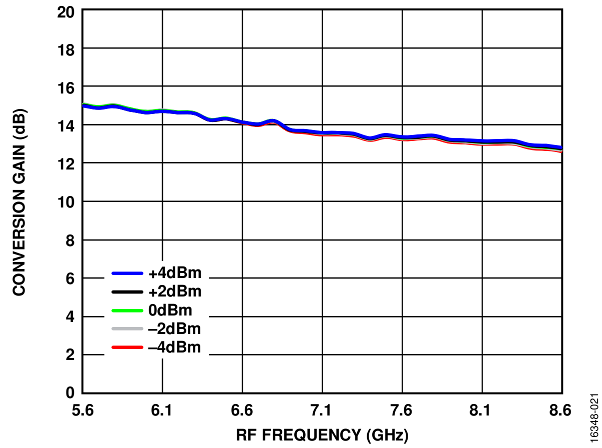

Figure 21. Conversion Gain vs. RF Frequency over LO Powers, T_A = 25°C

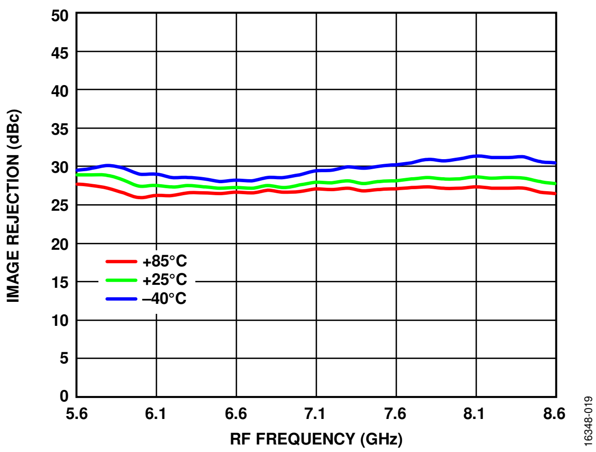

Figure 19. Image Rejection vs. RF Frequency over Temperatures, LO Power = 0 dBm

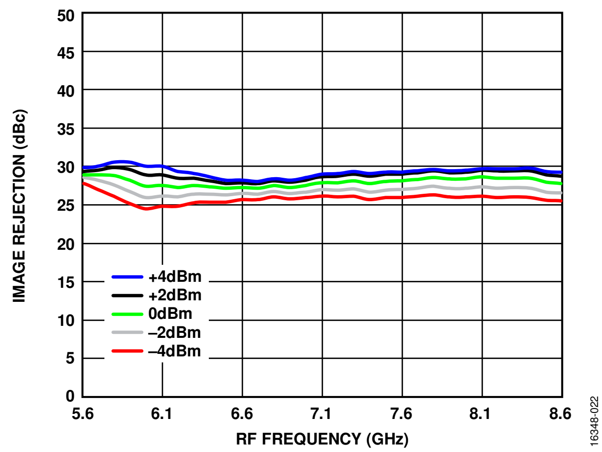

Figure 22. Image Rejection vs. RF Frequency over LO Powers, T_A = 25°C

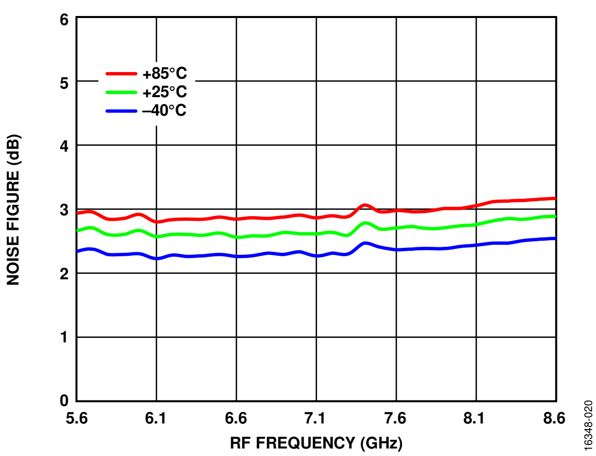

Figure 20. Noise Figure vs. RF Frequency over Temperatures, LO Power = 0 dBm

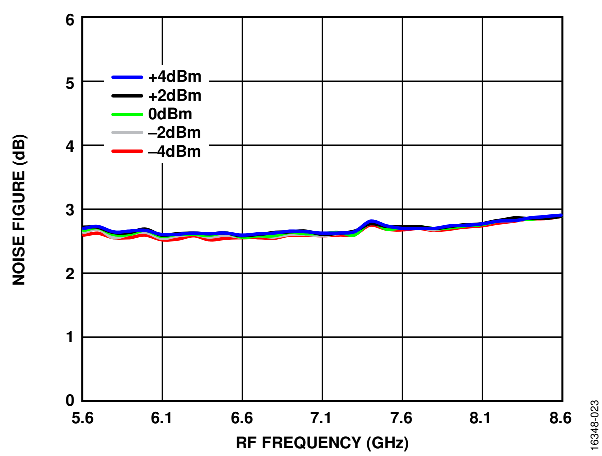

Figure 23. Noise Figure vs. RF Frequency over LO Powers, T_A = 25°C

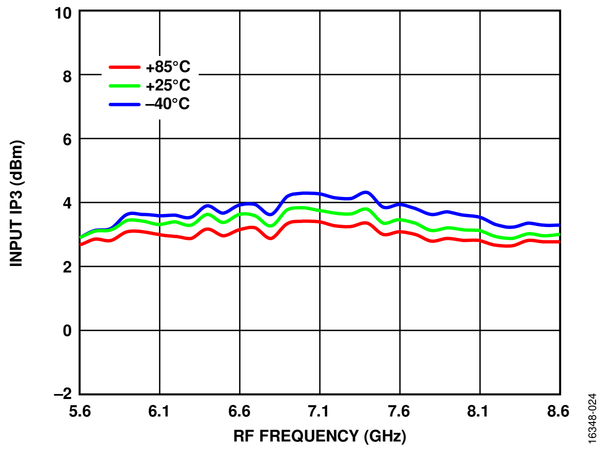

Figure 24. Input IP3 vs. RF Frequency over Temperatures, LO Power = 0 dBm

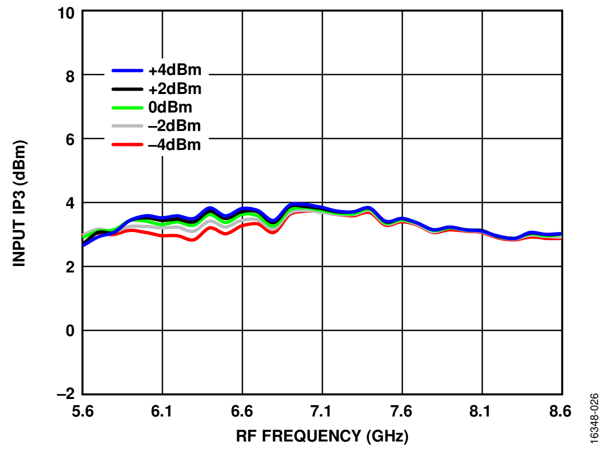

Figure 26. Input IP3 vs. RF Frequency over LO Powers, T_A = 25°C

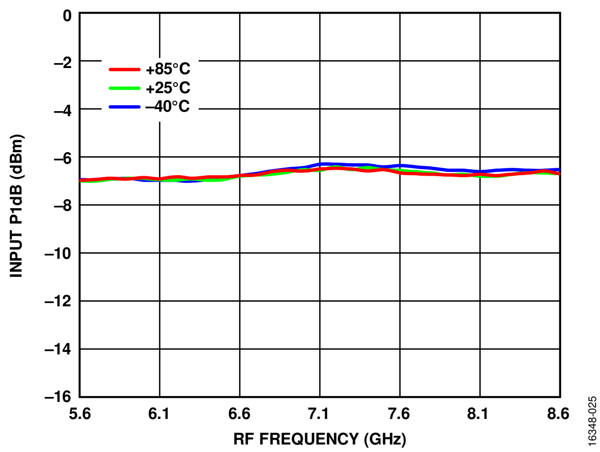

Figure 25. Input P1dB vs. RF Frequency over Temperatures, LO Power = 0 dBm

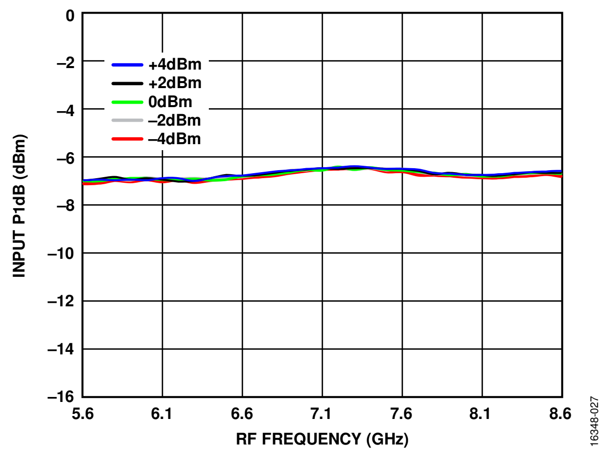

Figure 27. Input P1dB vs. RF Frequency over LO Powers, T_A = 25°C

IF = 3100 MHz and RF input power = −20 dBm. Data de-embedded for RF trace loss, unless otherwise noted.

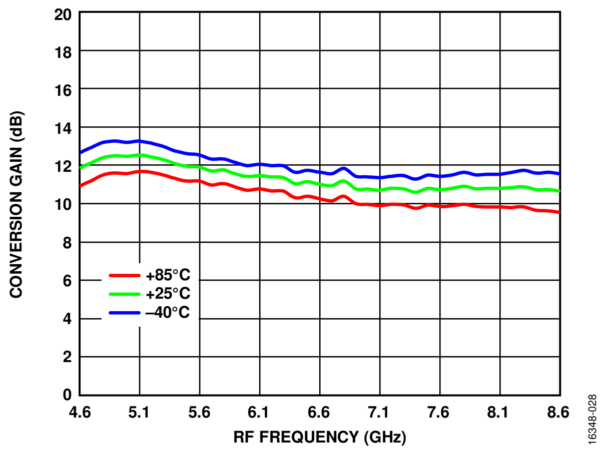

Figure 28. Conversion Gain vs. RF Frequency over Temperatures, LO Power = 0 dBm

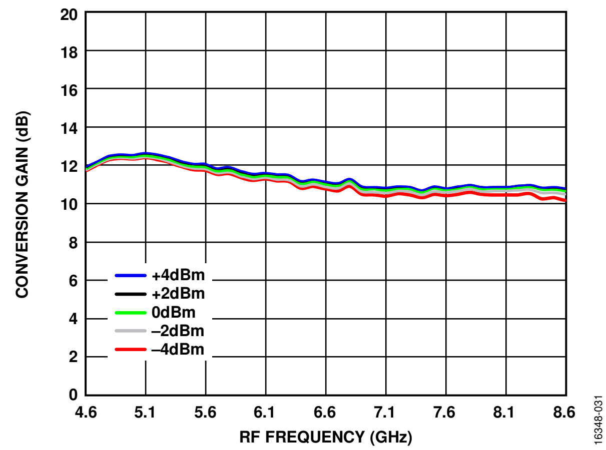

Figure 31. Conversion Gain vs. RF Frequency over LO Powers, T_A = 25°C

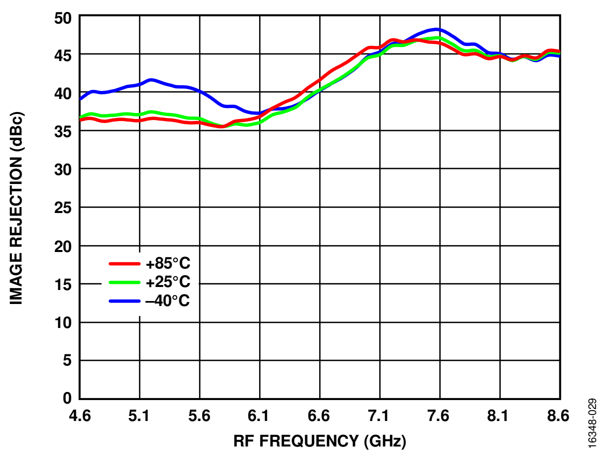

Figure 29. Image Rejection vs. RF Frequency over Temperatures, LO Power = 0 dBm

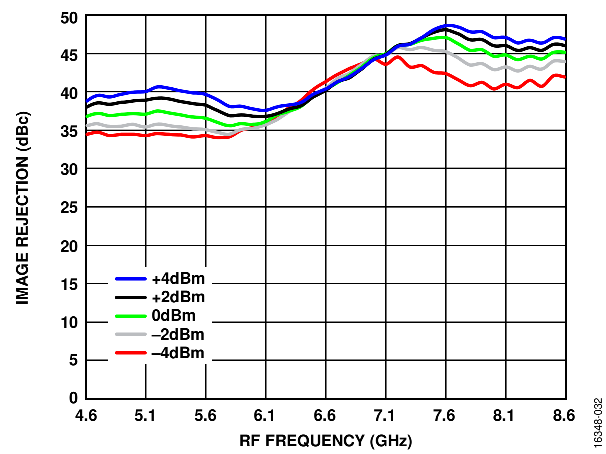

Figure 32. Image Rejection vs. RF Frequency over LO Powers, T_A = 25°C

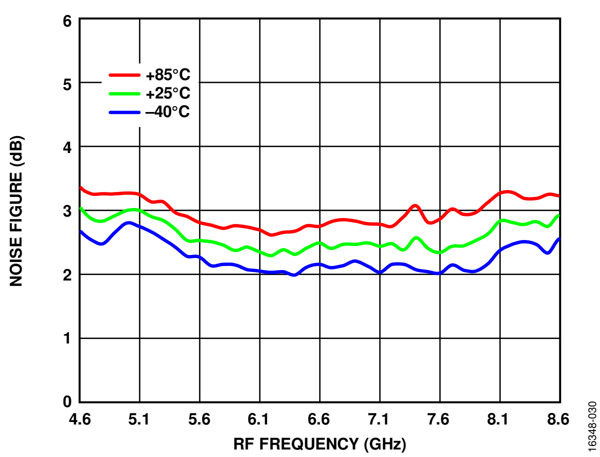

Figure 30. Noise Figure vs. RF Frequency over Temperatures, LO Power = 0 dBm

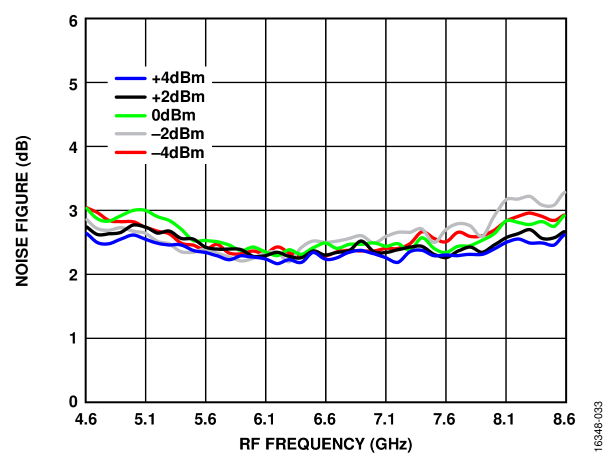

Figure 33. Noise Figure vs. RF Frequency over LO Powers, T_A = 25°C

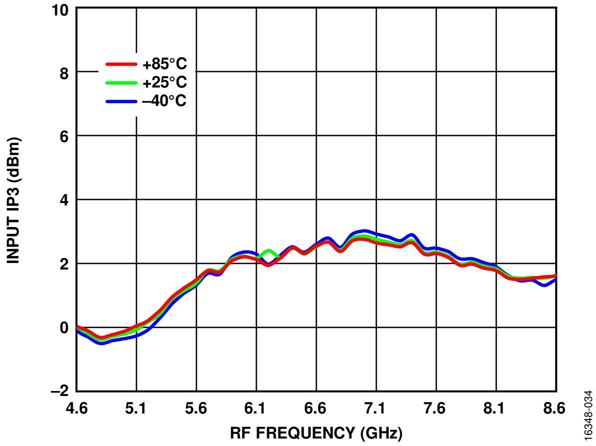

Figure 34. Input IP3 vs. RF Frequency over Temperatures, LO Power = 0 dBm

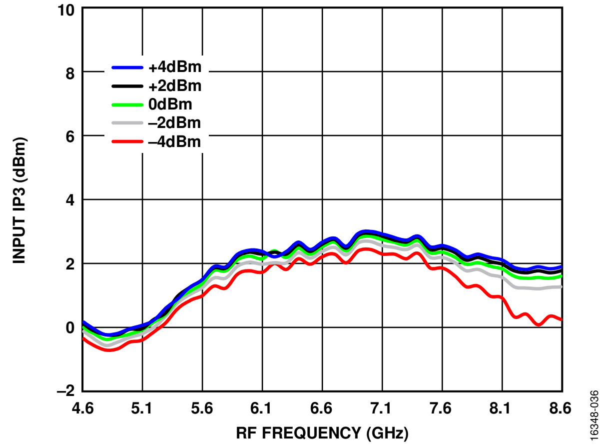

Figure 36. Input IP3 vs. RF Frequency over LO Powers, T_A = 25°C

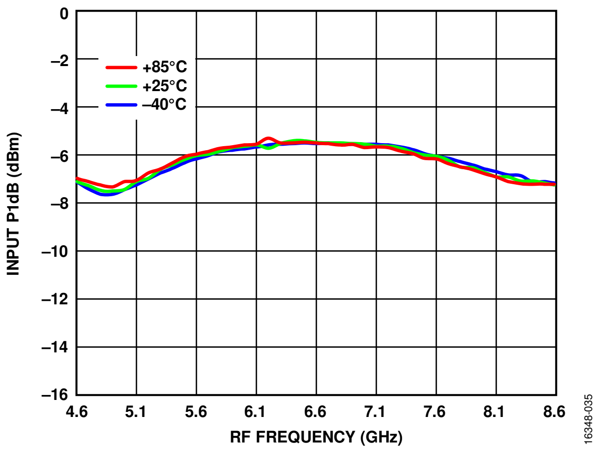

Figure 35. Input P1dB vs. RF Frequency over Temperatures, LO Power = 0 dBm

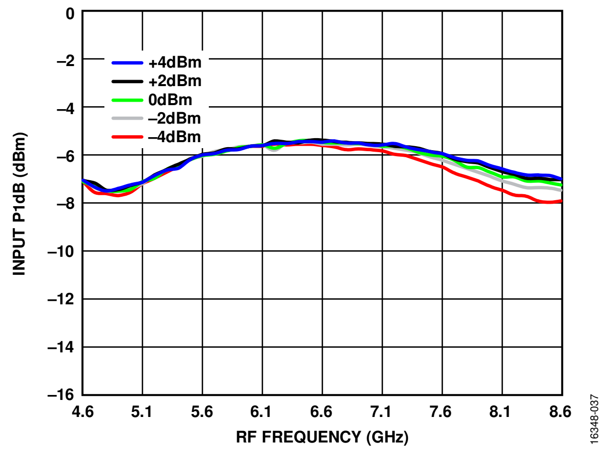

Figure 37. Input P1dB vs. RF Frequency over LO Powers, T_A = 25°C

UPPER SIDEBAND (LOW-SIDE LO)

IF = 150 MHz and RF input power = −20 dBm. Data de-embedded for RF trace loss, unless otherwise noted.

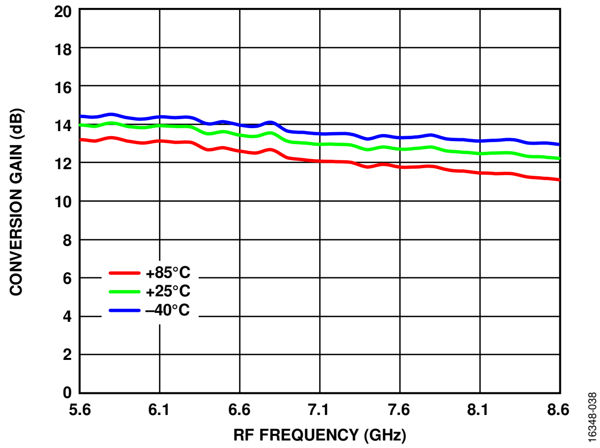

Figure 38. Conversion Gain vs. RF Frequency over Temperatures, LO Power = 0 dBm

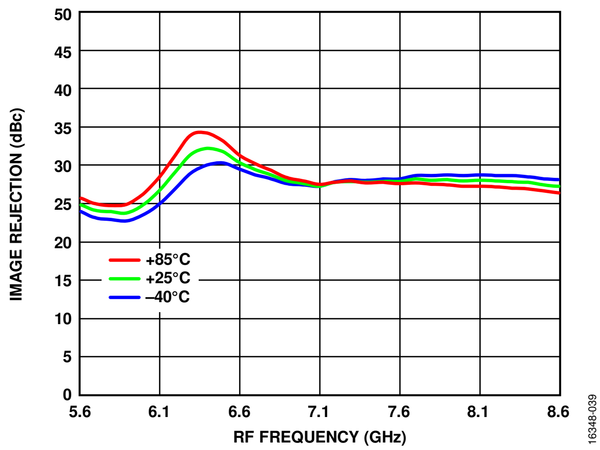

Figure 39. Image Rejection vs. RF Frequency over Temperatures, LO Power = 0 dBm

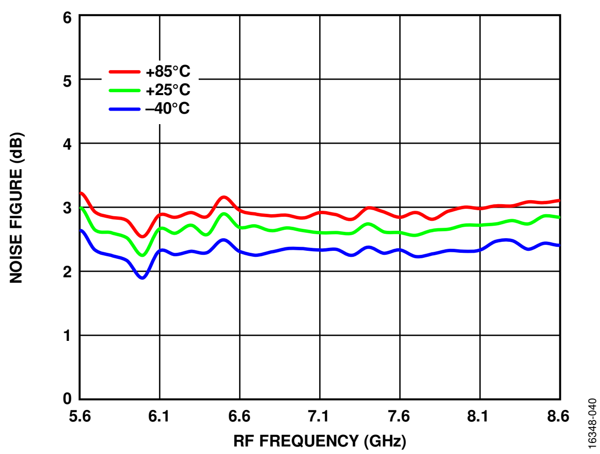

Figure 40. Noise Figure vs. RF Frequency over Temperatures, LO Power = 0 dBm

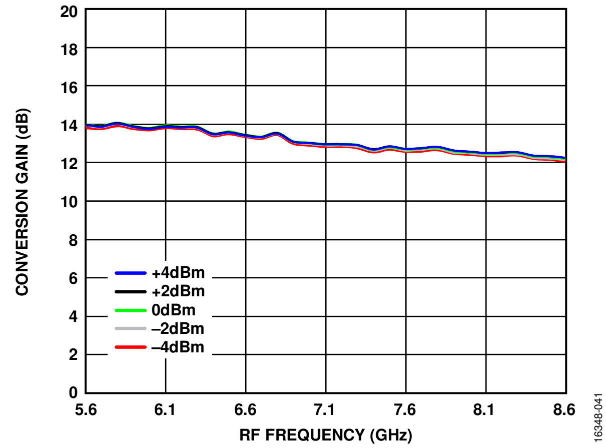

Figure 41. Conversion Gain vs. RF Frequency over LO Powers, T_A = 25°C

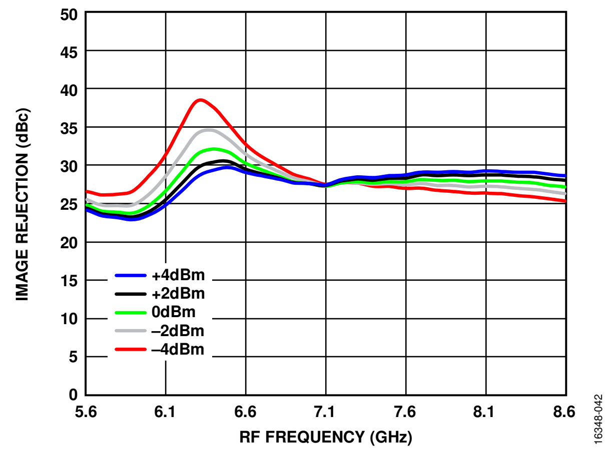

Figure 42. Image Rejection vs. RF Frequency over LO Powers, T_A = 25°C

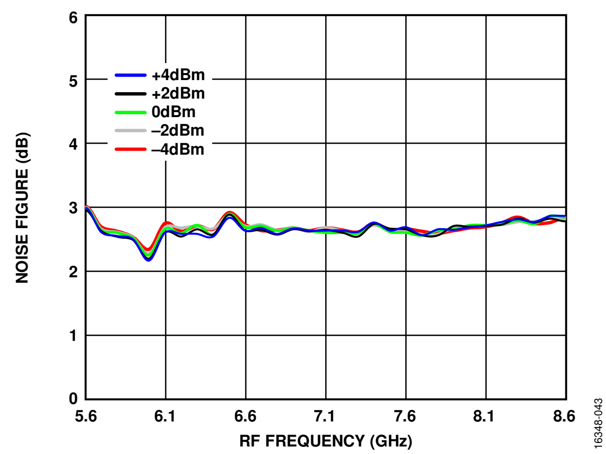

Figure 43. Noise Figure vs. RF Frequency over LO Powers, T_A = 25°C

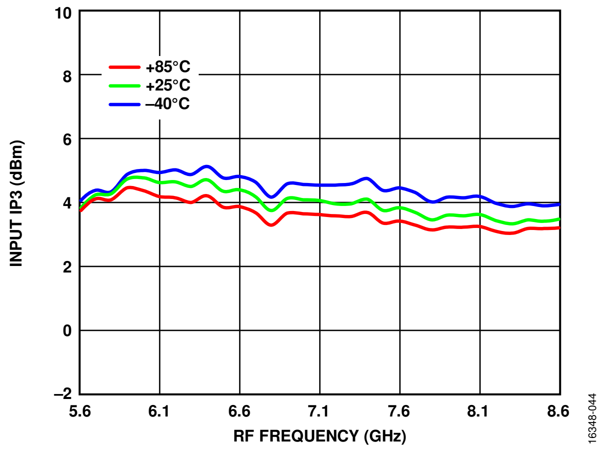

Figure 44. Input IP3 vs. RF Frequency over Temperatures, LO Power = 0 dBm

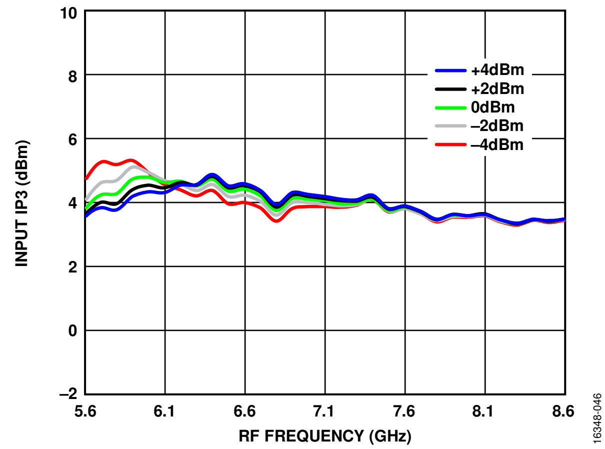

Figure 46. Input IP3 vs. RF Frequency over LO Powers, T_A = 25°C

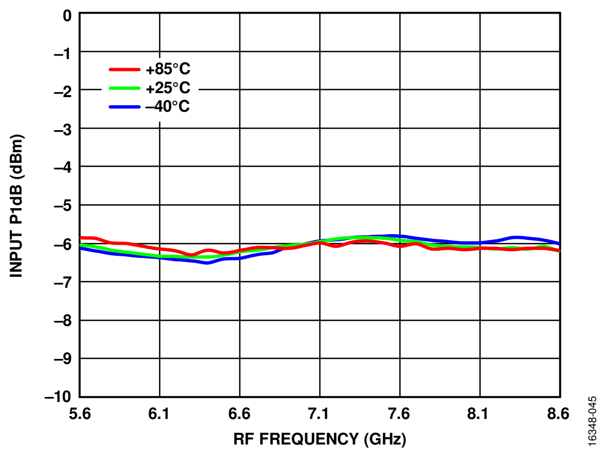

Figure 45. Input P1dB vs. RF Frequency over Temperatures, LO Power = 0 dBm

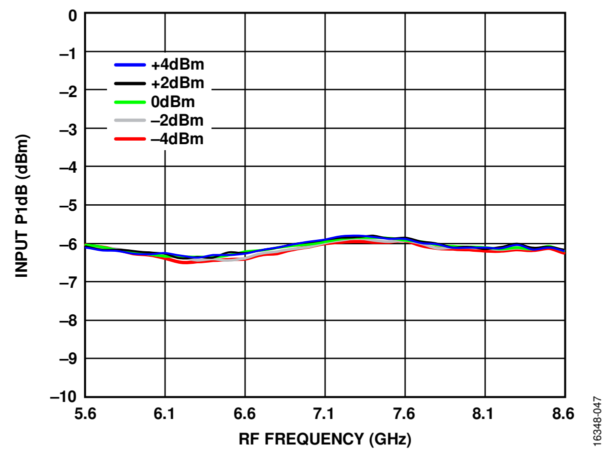

Figure 47. Input P1dB vs. RF Frequency over LO Powers, T_A = 25°C

IF = 1000 MHz and RF input power = −20 dBm. Data de-embedded for RF trace loss, unless otherwise noted.

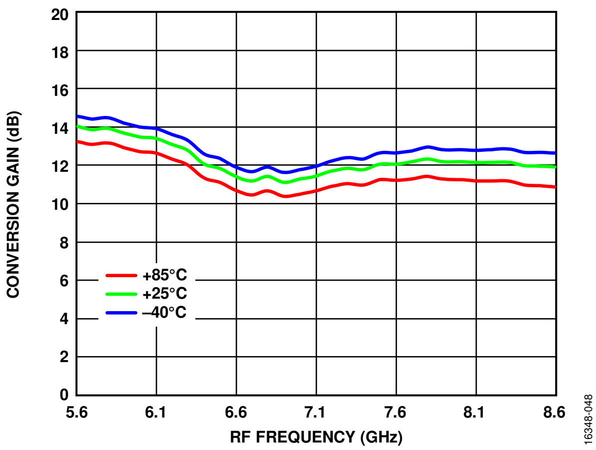

Figure 48. Conversion Gain vs. RF Frequency over Temperatures, LO Power = 0 dBm

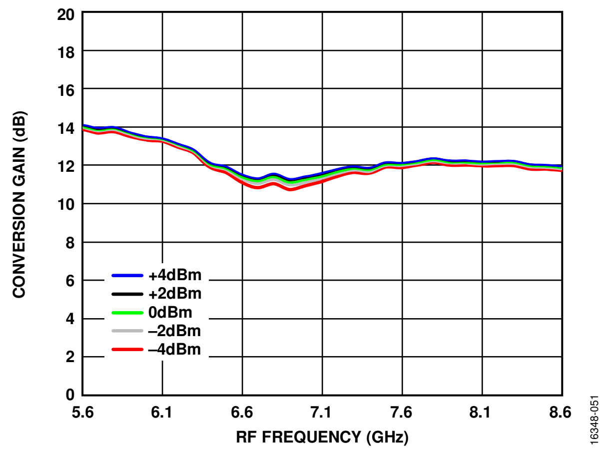

Figure 51. Conversion Gain vs. RF Frequency over LO Powers, T_A = 25°C

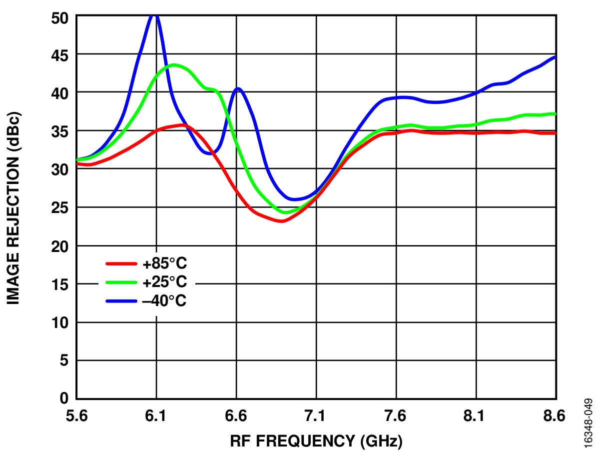

Figure 49. Image Rejection vs. RF Frequency over Temperatures, LO Power = 0 dBm

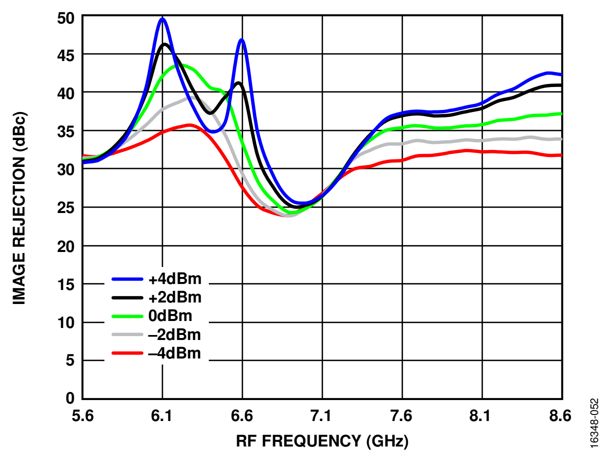

Figure 52. Image Rejection vs. RF Frequency over LO Powers, T_A = 25°C

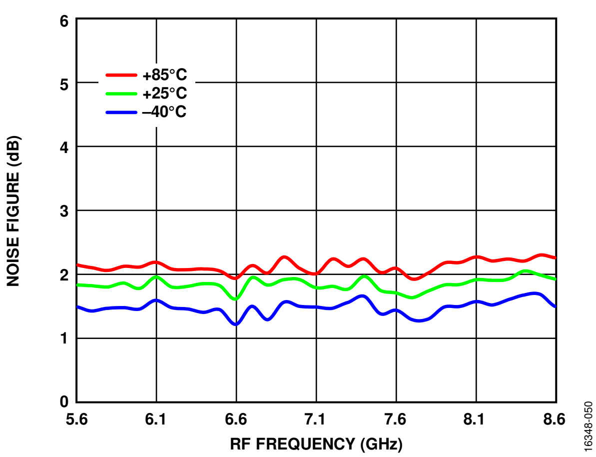

Figure 50. Noise Figure vs. RF Frequency over Temperatures, LO Power = 0 dBm

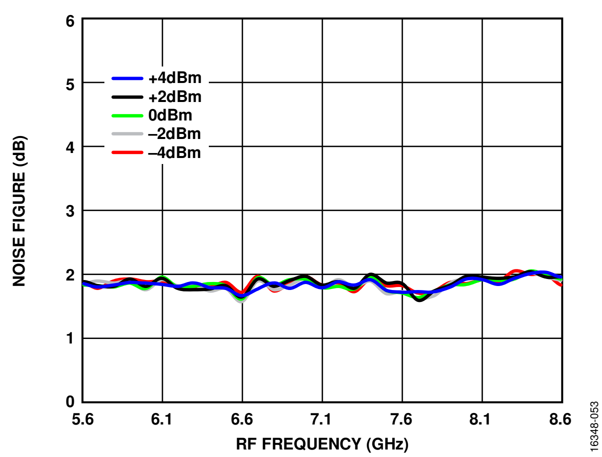

Figure 53. Noise Figure vs. RF Frequency over LO Powers, T_A = 25°C

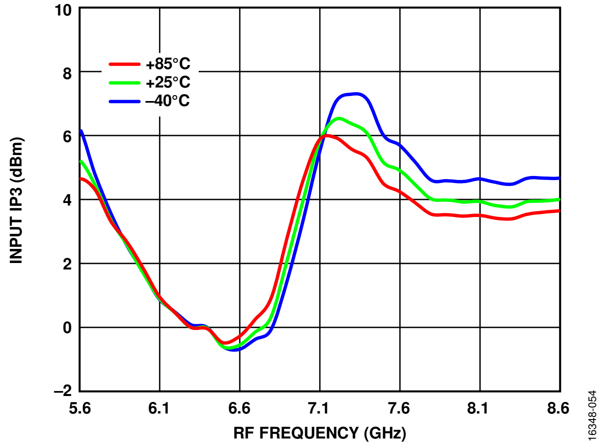

Figure 54. Input IP3 vs. RF Frequency over Temperatures, LO Power = 0 dBm

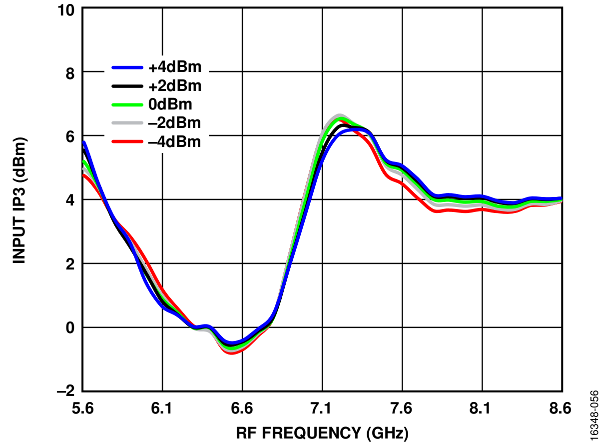

Figure 56. Input IP3 vs. RF Frequency over LO Powers, T_A = 25°C

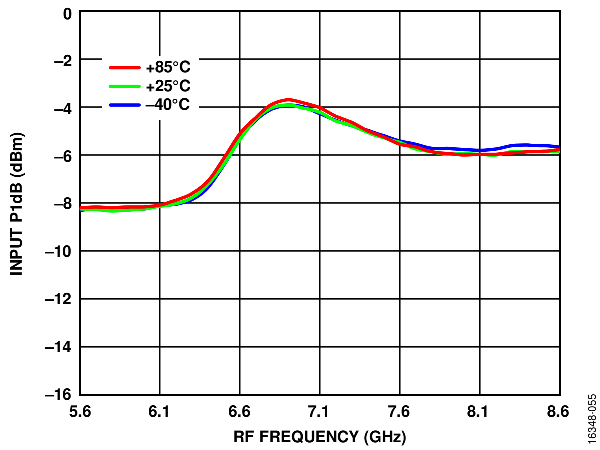

Figure 55. Input P1dB vs. RF Frequency over Temperatures, LO Power = 0 dBm

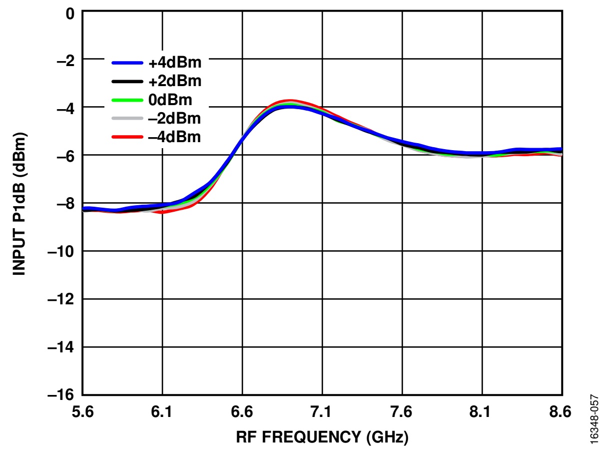

Figure 57. Input P1dB vs. RF Frequency over LO Powers, T_A = 25°C

IF = 3100 MHz and RF input power = −20 dBm. Data de-embedded for RF trace loss, unless otherwise noted.

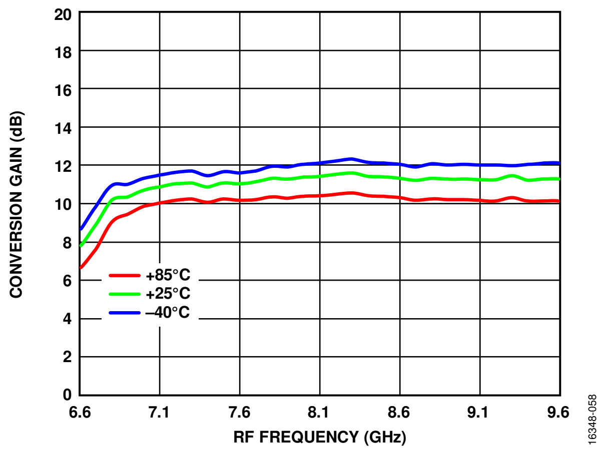

Figure 58. Conversion Gain vs. RF Frequency over Temperatures, LO Power = 0 dBm

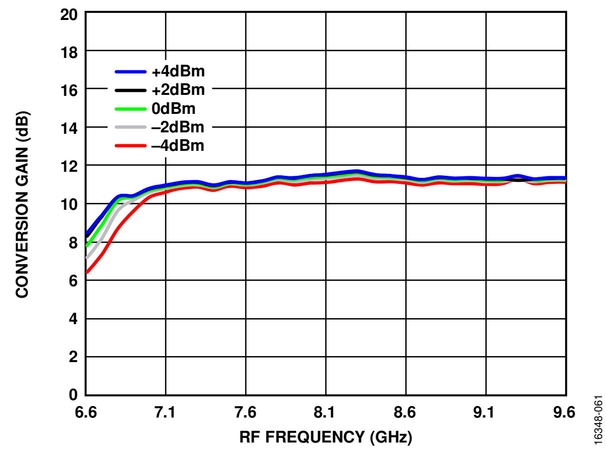

Figure 61. Conversion Gain vs. RF Frequency over LO Powers, T_A = 25°C

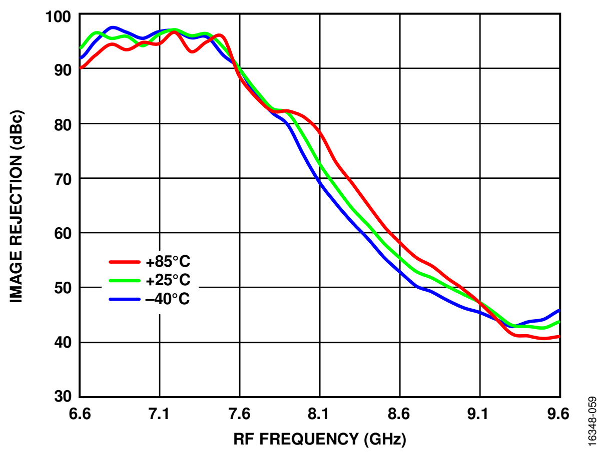

Figure 59. Image Rejection vs. RF Frequency over Temperatures, LO Power = 0 dBm

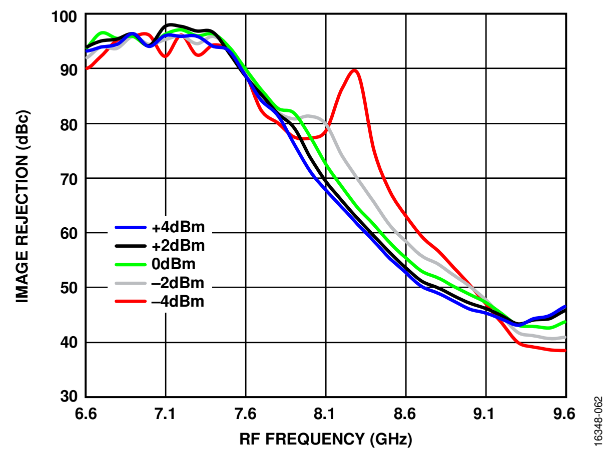

Figure 62. Image Rejection vs. RF Frequency over LO Powers, T_A = 25°C

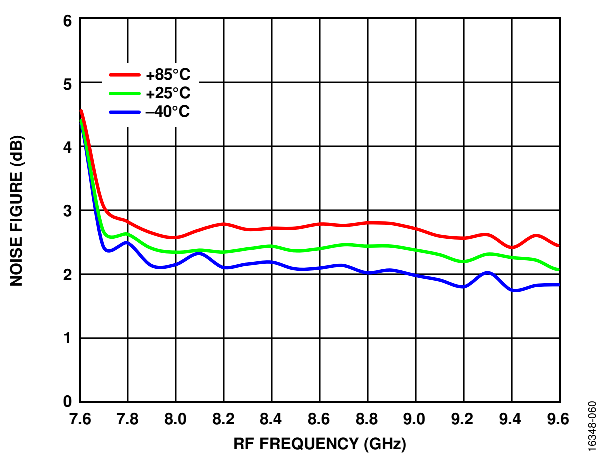

Figure 60. Noise Figure vs. RF Frequency over Temperatures, LO Power = 0 dBm

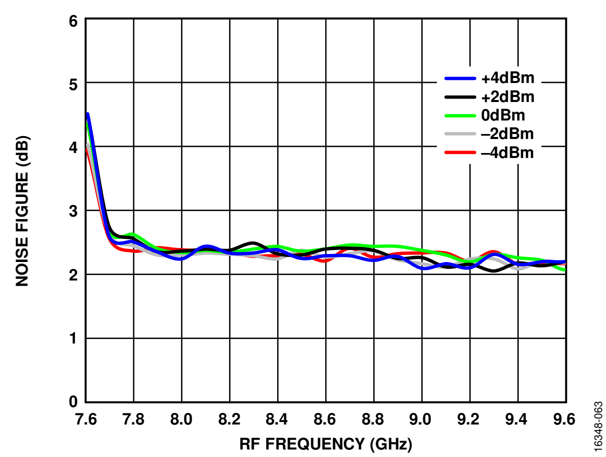

Figure 63. Noise Figure vs. RF Frequency over LO Powers, T_A = 25°C

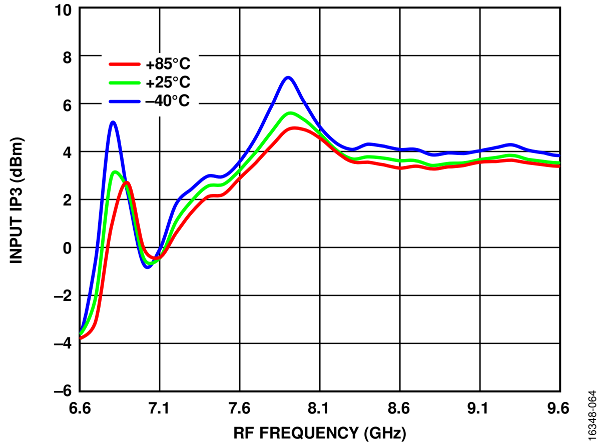

Figure 64. Input IP3 vs. RF Frequency over Temperatures, LO Power = 0 dBm

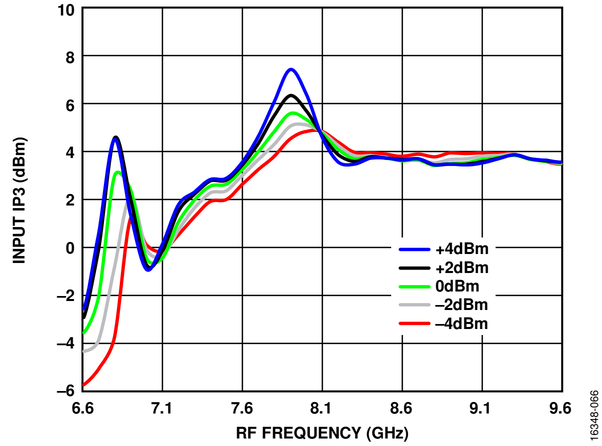

Figure 66. Input IP3 vs. RF Frequency over LO Powers, T_A = 25°C

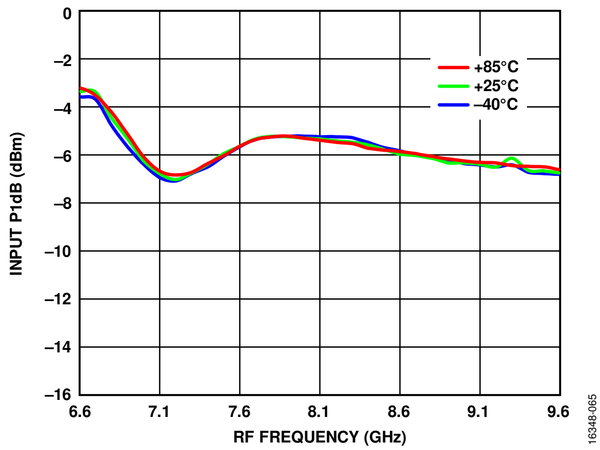

Figure 65. Input P1dB vs. RF Frequency over Temperatures, LO Power = 0 dBm

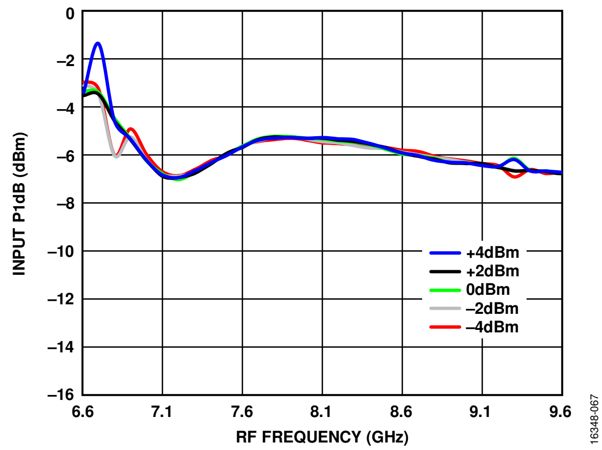

Figure 67. Input P1dB vs. RF Frequency over LO Powers, T_A = 25°C

ISOLATION AND RETURN LOSS

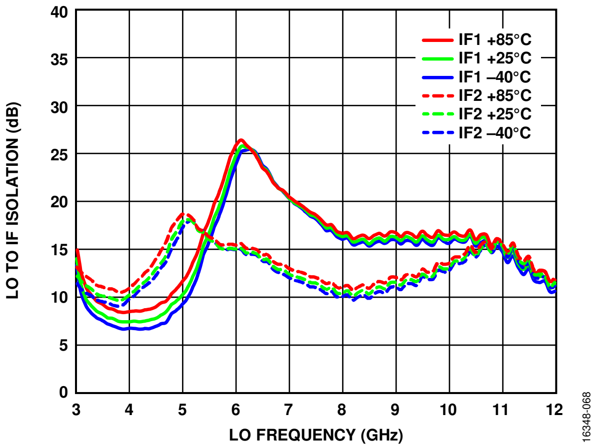

Figure 68. LO to IF Isolation vs. LO Frequency over Temperatures, LO Power = 0 dBm

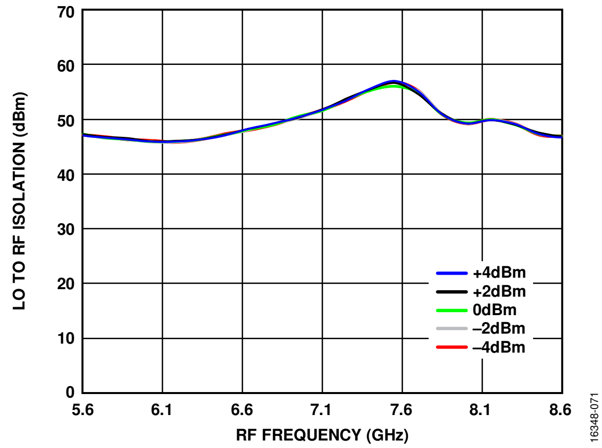

Figure 71. LO to RF Isolation vs. RF Frequency over LO Powers, T_A = 25°C

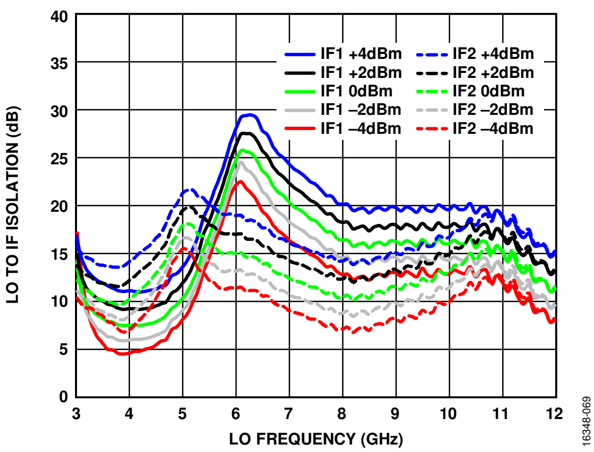

Figure 69. LO to IF Isolation vs. LO Frequency over LO Powers, T_A = 25°C

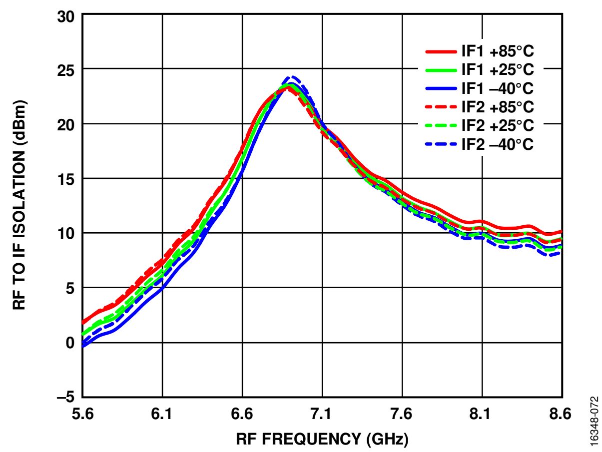

Figure 72. RF to IF Isolation vs. RF Frequency over Temperatures, LO Power = 0 dBm

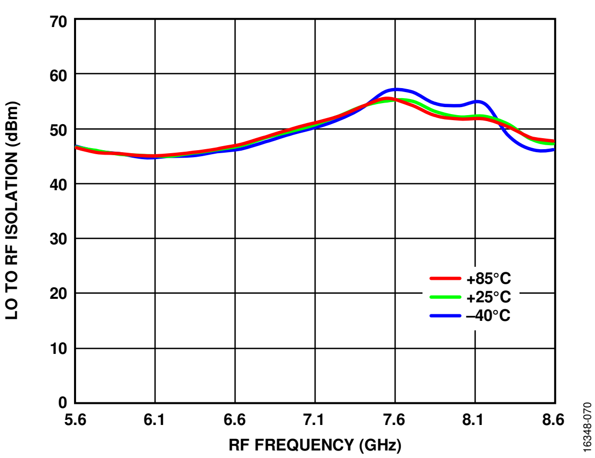

Figure 70. LO to RF Isolation vs. RF Frequency over Temperatures, LO Power = 0 dBm

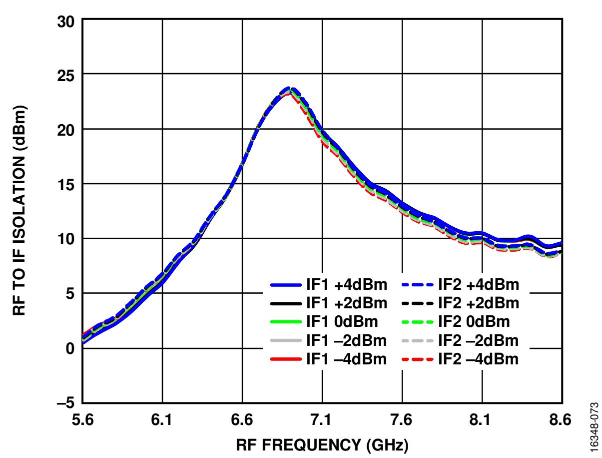

Figure 73. RF to IF Isolation vs. RF Frequency over LO Powers, T_A = 25°C

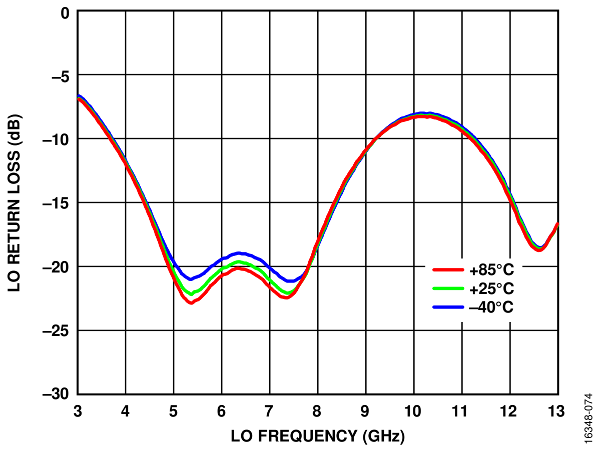

Figure 74. LO Return Loss vs. LO Frequency over Temperatures, LO Power = 0 dBm

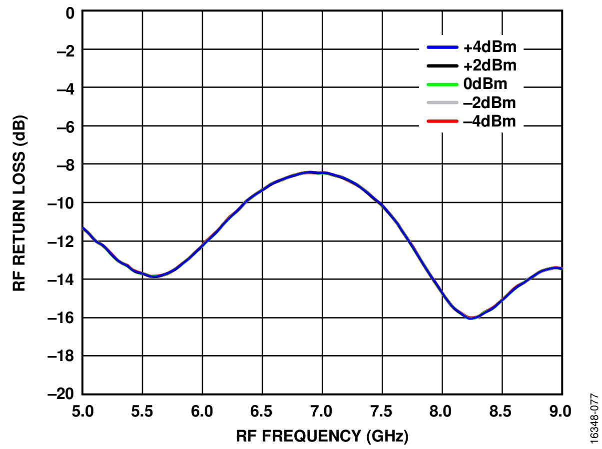

Figure 77. RF Return Loss vs. RF Frequency over LO Powers, LO Frequency = 7 GHz, T_A = 25°C

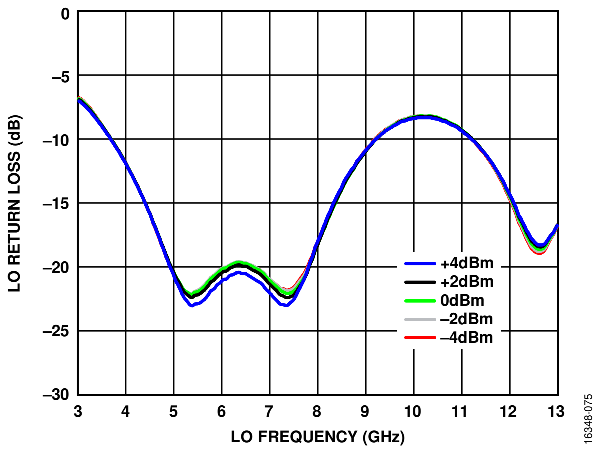

Figure 75. LO Return Loss vs. LO Frequency over LO Powers, T_A = 25°C

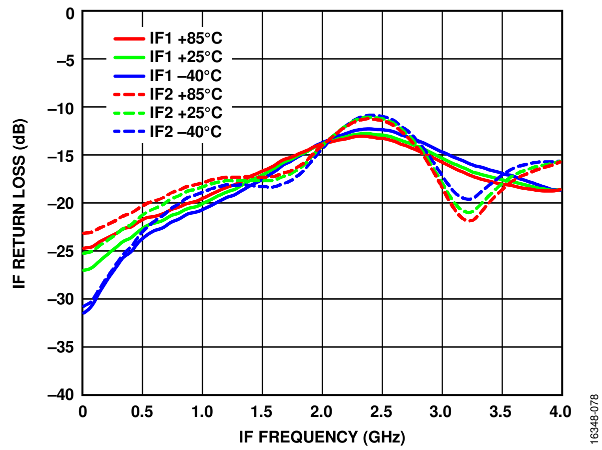

Figure 78. IF Return Loss vs. IF Frequency over Temperatures, LO Frequency = 7 GHz, LO Power = 0 dBm

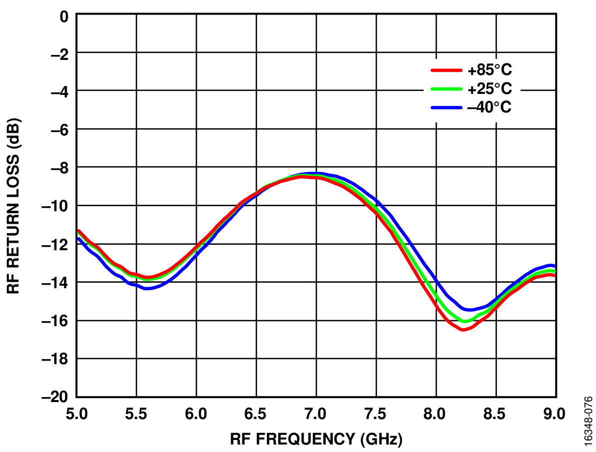

Figure 76. RF Return Loss vs. RF Frequency over Temperatures, LO Frequency = 7 GHz, LO Power = 0 dBm

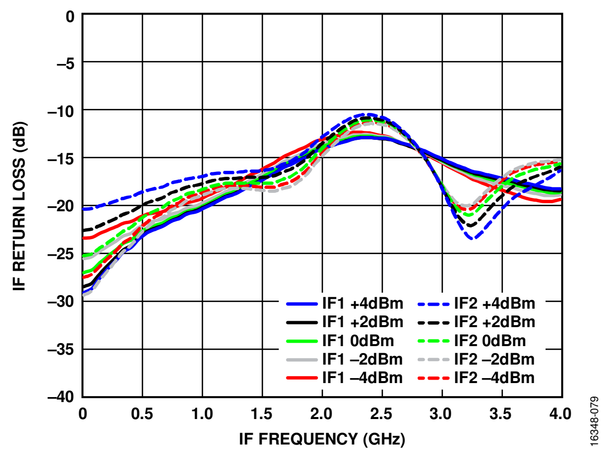

Figure 79. IF Return Loss vs. IF Frequency over LO Powers, LO Frequency = 7 GHz, T_A = 25°C

IF BANDWIDTH PERFORMANCE

Lower Sideband (High-Side LO)

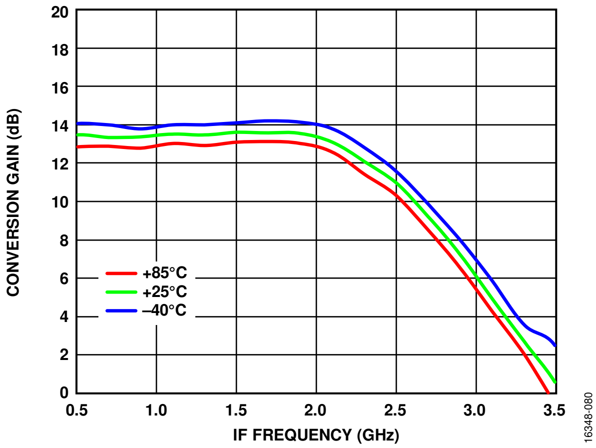

Figure 80. Conversion Gain vs. IF Frequency over Temperatures, LO Frequency = 7 GHz, LO Power = 0 dBm

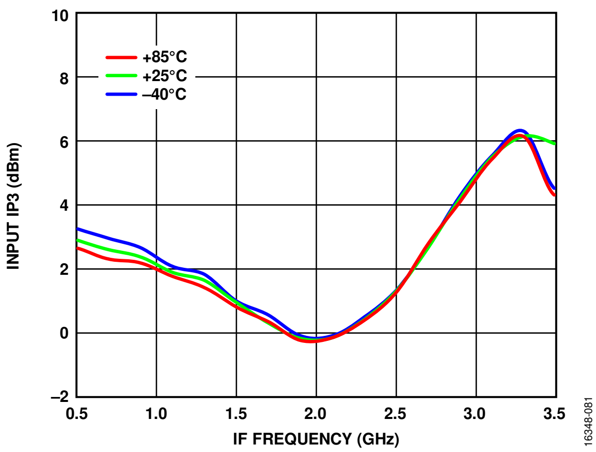

Figure 81. Input IP3 vs. IF Frequency over Temperatures, LO Frequency = 7 GHz, LO Power = 0 dBm

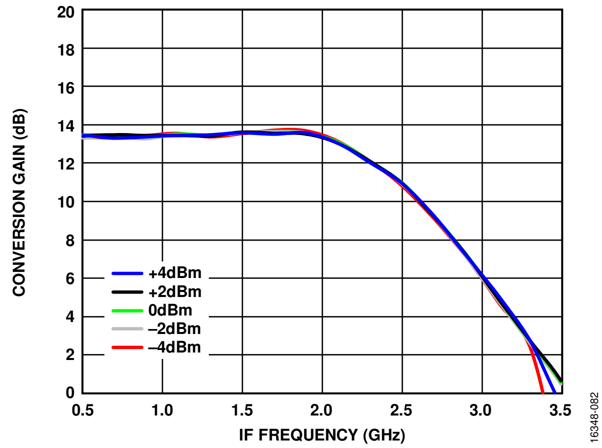

Figure 82. Conversion Gain vs. IF Frequency over LO Powers, LO Frequency = 7 GHz, T_A = 25°C

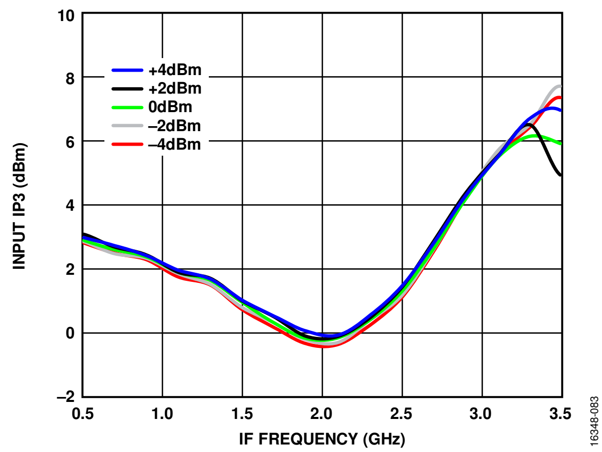

Figure 83. Input IP3 vs. IF Frequency over LO Powers, LO Frequency = 7 GHz, T_A = 25°C

Upper Sideband (Low-Side LO)

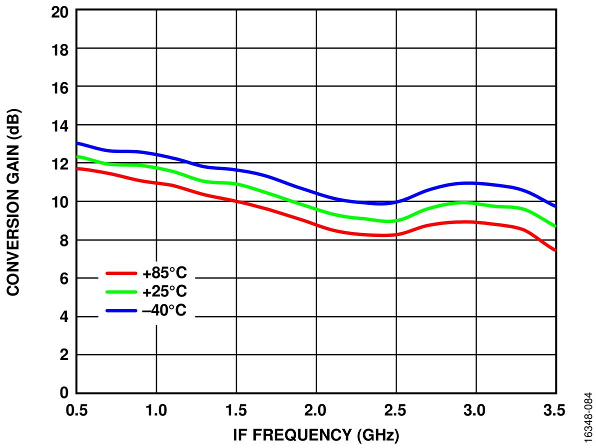

Figure 84. Conversion Gain vs. IF Frequency over Temperatures, LO Frequency = 7 GHz, LO Power = 0 dBm

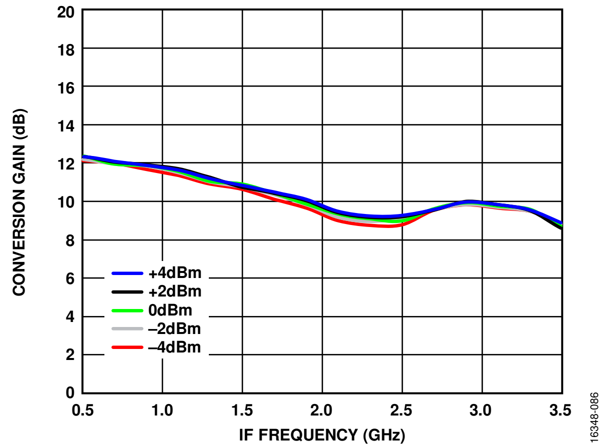

Figure 86. Conversion Gain vs. IF Frequency over LO Powers, LO Frequency = 7 GHz, T_A = 25°C

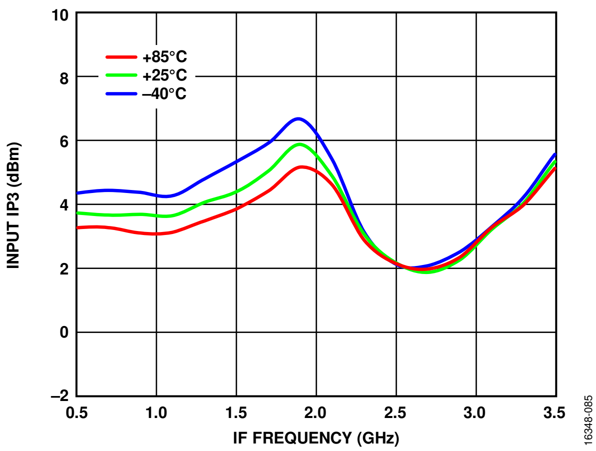

Figure 85. Input IP3 vs. IF Frequency over Temperatures, LO Frequency = 7 GHz, LO Power = 0 dBm

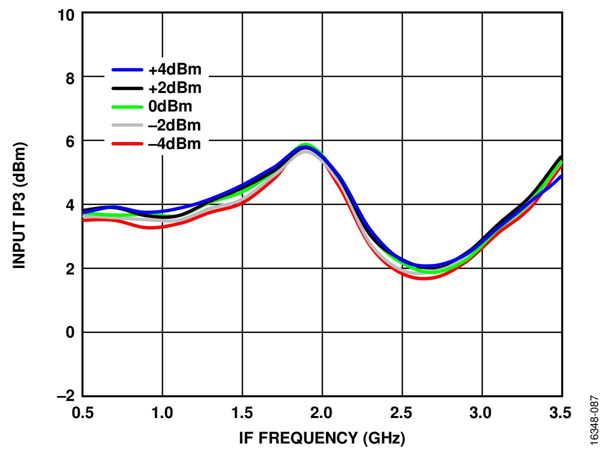

Figure 87. Input IP3 vs. IF Frequency over LO Powers, LO Frequency = 7 GHz, T_A = 25°C

AMPLITUDE AND PHASE IMBALANCE PERFORMANCE

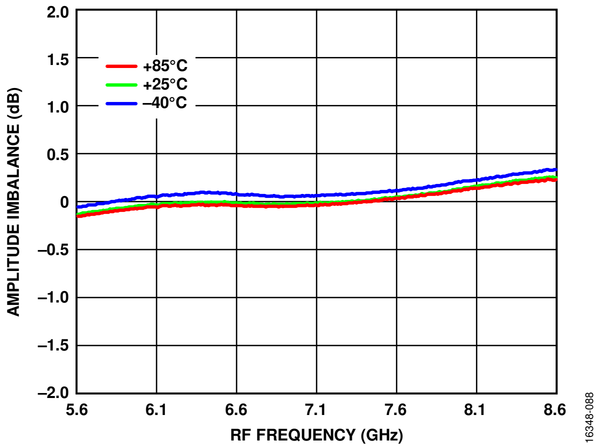

Figure 88. Amplitude Imbalance vs. RF Frequency over Temperatures, LO Power = 0 dBm, IF = 1000 MHz, Lower Sideband

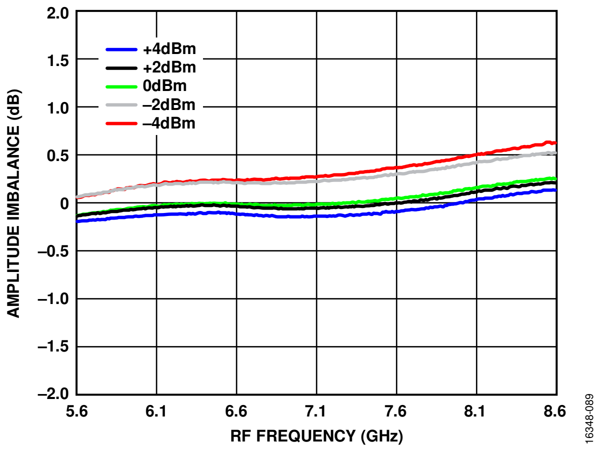

Figure 89. Amplitude Imbalance vs. RF Frequency over LO Powers, IF = 1000 MHz, T_A = 25°C, Lower Sideband

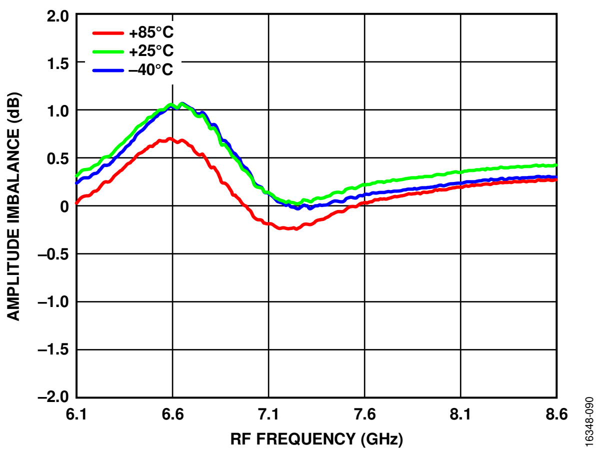

Figure 90. Amplitude Imbalance vs. RF Frequency over Temperatures, LO Power = 0 dBm, IF = 1000 MHz, Upper Sideband

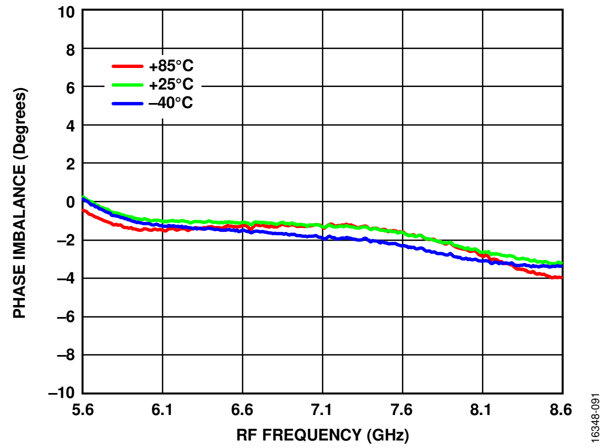

Figure 91. Phase Imbalance vs. RF Frequency over Temperatures, LO Power = 0 dBm, IF = 1000 MHz, Lower Sideband

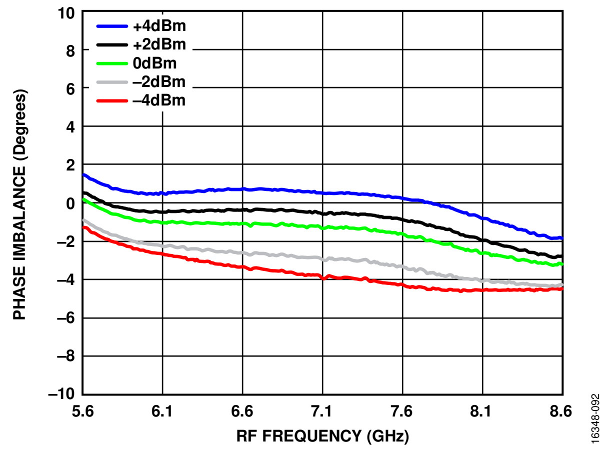

Figure 92. Phase Imbalance vs. RF Frequency over LO Powers, IF = 1000 MHz, T_A = 25°C, Lower Sideband

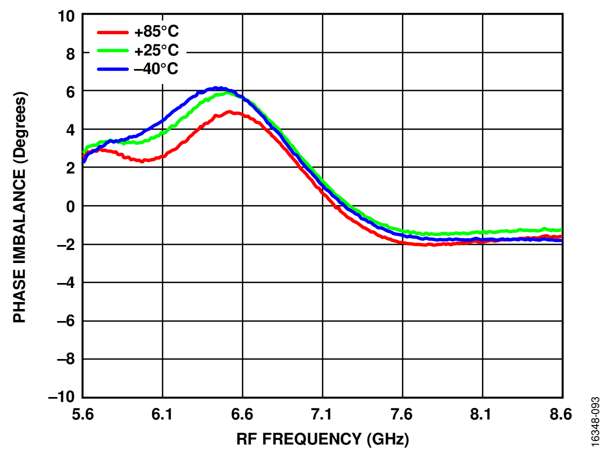

Figure 93. Phase Imbalance vs. RF Frequency over Temperatures, LO Power = 0 dBm, IF = 1000 MHz, Upper Sideband

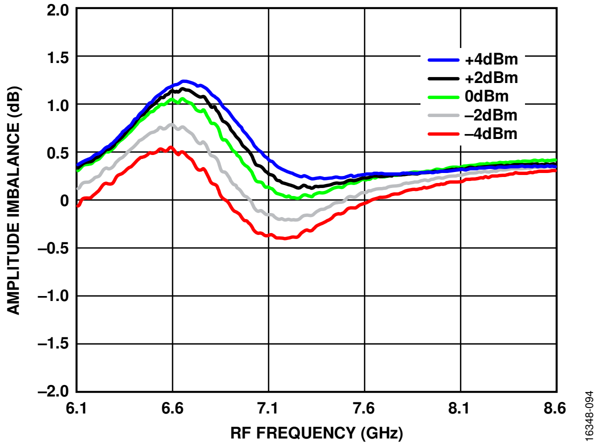

Figure 94. Amplitude Imbalance vs. RF Frequency over LO Powers, IF = 1000 MHz, T_A = 25°C, Upper Sideband

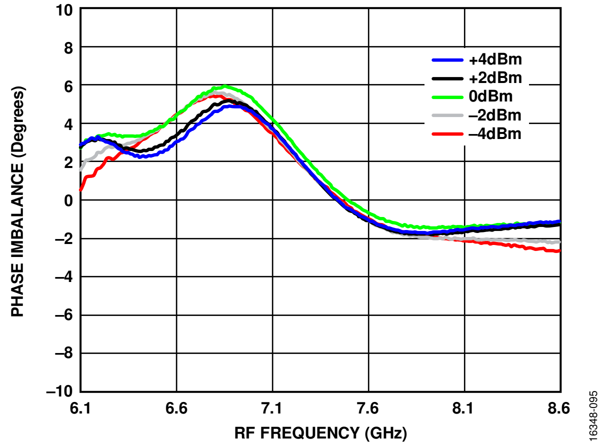

Figure 95. Phase Imbalance vs. RF Frequency over LO Powers, IF = 1000 MHz, T_A = 25°C, Upper Sideband

SPURIOUS PERFORMANCE

Mixer spurious products are measured in dBc from the RF output power level. Spur values are (M × RF) − (N × LO). N/A means not applicable.

M × N Spurious Outputs, IF = 150 MHz

RF = 5600 MHz, LO frequency = 5750 MHz at LO input power = 0 dBm, RF input power = −20 dBm.

		N × LO				
		0	1	2	3	4
M × RF	0	N/A	15	33	18	34
	1	17	0	30	37	43
	2	57	60	60	57	71
	3	70	78	59	59	68
	4	84	87	88	70	81

RF = 6100 MHz, LO frequency = 6250 MHz at LO input power = 0 dBm, IF input power = −20 dBm.

		N × LO				
		0	1	2	3	4
M × RF	0	N/A	18	26	27	29
	1	22	0	39	38	41
	2	58	72	68	68	73
	3	71	80	70	62	82
	4	83	87	88	77	81

RF = 8500 MHz, LO frequency = 8650 MHz at LO input power = 0 dBm, IF input power = −20 dBm.

		N × LO				
		0	1	2	3	4
M × RF	0	N/A	16	13	23	28
	1	28	0	46	53	59
	2	53	78	63	69	64
	3	79	82	85	68	86
	4	79	79	86	84	82

M × N Spurious Output, IF = 1000 MHz

RF = 5600 MHz, LO frequency = 6600 MHz at LO input power = 0 dBm, IF input power = −20 dBm.

		N × LO				
		0	1	2	3	4
M × RF	0	N/A	16	24	26	42
	1	17	0	47	43	50
	2	55	61	55	61	63
	3	75	88	61	76	86
	4	86	89	90	76	77

RF = 6100 MHz, LO frequency = 7100 MHz at LO input power = 0 dBm, IF input power = −20 dBm.

		N × LO				
		0	1	2	3	4
M × RF	0	N/A	17	14	21	32
	1	23	0	49	41	59
	2	57	54	54	68	68
	3	72	83	65	68	87
	4	82	89	91	83	77

RF = 8500 MHz, LO frequency = 9500 MHz at LO input power = 0 dBm, IF input power = −20 dBm.

		N × LO				
		0	1	2	3	4
M × RF	0	N/A	13	19	13	39
	1	28	0	39	44	57
	2	52	78	55	68	82
	3	78	81	88	76	84
	4	77	82	86	87	81

M × N Spurious Outputs, IF = 3100 MHz

RF = 5600 MHz, LO frequency = 8700 MHz at LO input power = 0 dBm, IF input power = −20 dBm.

		N × LO				
		0	**1**	**2**	**3**	**4**
M × RF	**0**	N/A	21	14	23	37
	1	14	0	32	43	52
	2	54	50	61	62	68
	3	74	81	59	83	77
	4	84	88	78	88	88

RF = 6100 MHz, LO frequency = 9200 MHz at LO input power = 0 dBm, IF input power = −20 dBm.

		N × LO				
		0	**1**	**2**	**3**	**4**
M × RF	**0**	N/A	16	19	14	29
	1	19	0	33	47	50
	2	55	56	59	56	65
	3	68	80	64	84	81
	4	81	86	86	86	88

RF = 8500 MHz, LO frequency = 11600 MHz at LO input power = 0 dBm, IF input power = −20 dBm.

		N × LO				
		0	**1**	**2**	**3**	**4**
M × RF	**0**	N/A	4	24	27	0
	1	27	0	28	65	75
	2	53	61	67	57	70
	3	80	85	84	86	82
	4	77	80	86	83	86

THEORY OF OPERATION

The HMC951A is a compact GaAs, MMIC, I/Q downconverter in a RoHS compliant package optimized for point to point and point to multipoint microwave radio applications operating in the 5.6 GHz to 8.6 GHz input RF frequency range. The HMC951A supports LO input frequencies of 4.5 GHz to 12.1 GHz and IF output frequencies of dc to 3.5 GHz.

The HMC951A uses an RF LNA amplifier followed by an I/Q double balanced mixer, where a driver amplifier drives the LO (see Figure 1). The combination of design, process, and packaging technology allows the functions of these subsystems to be integrated into a single die, using mature packaging and interconnection technologies to provide a high performance, low cost design with excellent electrical, mechanical, and thermal properties. In addition, the need for external components is minimized, optimizing cost and size.

LO DRIVER AMPLIFIER

The LO driver amplifier takes a single LO input and amplifies it to the desired LO signal level for the mixer to operate optimally. The LO driver amplifier is self biased, and it only requires a single dc bias voltage (VDLO) to operate. The bias current for the LO amplifier is 80 mA at 5 V typically. The LO drive range of −4 dBm to +4 dBm makes it compatible with Analog Devices, Inc., wideband synthesizer portfolio without the need for an external LO driver amplifier.

MIXER

The mixer is an I/Q double balanced mixer, and this mixer topology reduces the need for filtering the unwanted sideband. An external 90° hybrid is required to select the desired sideband of operation.

LNA

The LNA is self biased, and it requires only a single dc bias voltage (VDRF) to operate. The bias current for the LNA is 75 mA at 5 V typically.

The typical application circuit (see Figure 96) provided shows the necessary external components on the bias lines to eliminate any undesired stability problems for the RF amplifier and the LO amplifier.

The HMC951A is a much smaller alternative to hybrid style image reject converter assemblies, and it eliminates the need for wire bonding by allowing the use of surface-mount manufacturing assemblies.

The HMC951A downconverter comes in a compact, 4 mm × 4 mm, 24-lead LFCSP. The HMC951A operates over the −40°C to +85°C temperature range.

APPLICATIONS INFORMATION

TYPICAL APPLICATION CIRCUIT

Figure 96 shows the typical application circuit for the HMC951A. To select the appropriate sideband, an external 90° hybrid is required. For applications not requiring operation to dc, use an off-chip, dc blocking capacitor. For applications that require the LO signal at the output to be suppressed, use a bias tee or RF feed. Ensure that the source or sink current used for LO suppression is <3 mA for each IF port to prevent damage to the device. The common-mode voltage for each IF port is 0 V.

To select the lower sideband, connect the IF1 pin to the 90° port of the hybrid and the IF2 pin to the 0° port of the hybrid. To select the upper sideband, connect the IF1 pin to the 0° port of the hybrid and the IF2 pin to the 90° port of the hybrid.

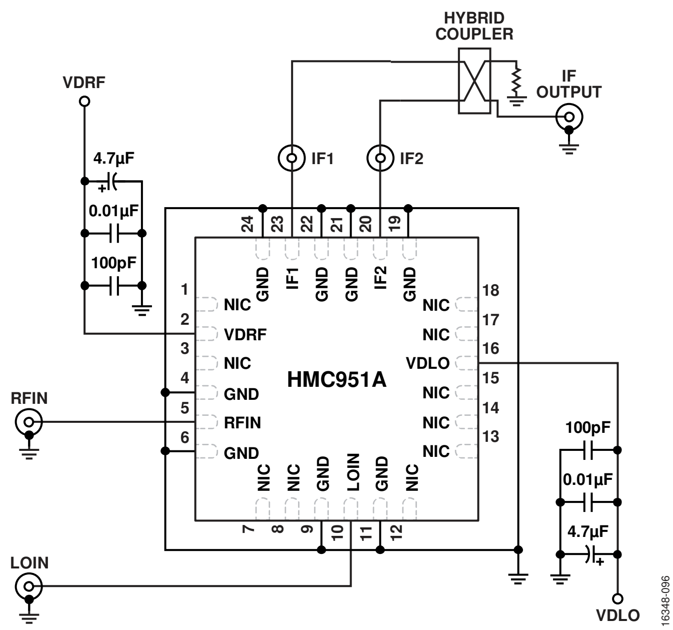

Figure 96. Typical Application Circuit

PERFORMANCE AT LOWER IF FREQUENCIES

The HMC951A can operate at low IF frequencies approaching dc. Figure 97 and Figure 98 show the conversion gain and image rejection performance at lower IF frequencies.

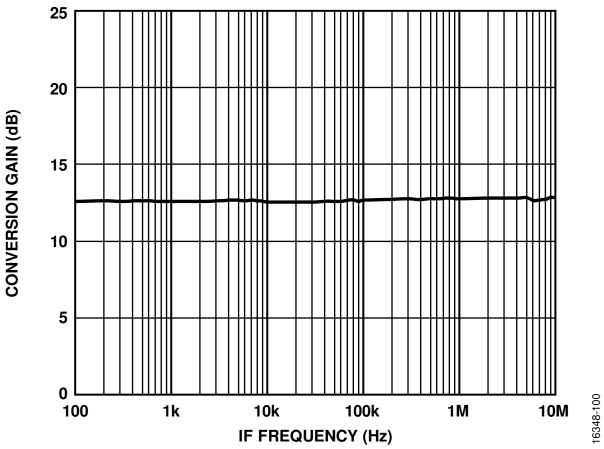

Figure 97. Conversion Gain vs. IF Frequency at Low IF Frequencies, LO = 7 GHz at 4 dBm, Upper Sideband (Low-Side LO)

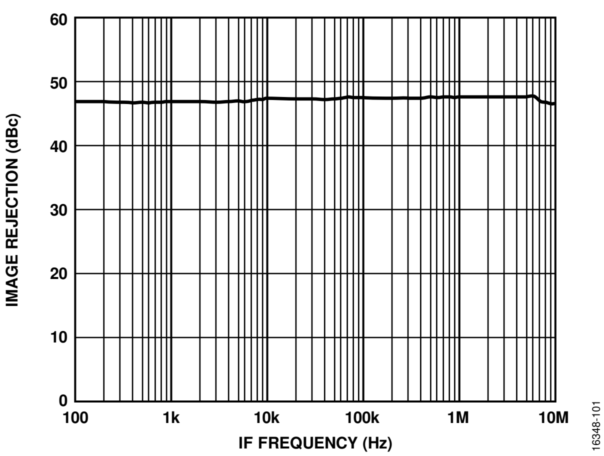

Figure 98. Image Rejection vs. IF Frequency at Low IF Frequencies, LO = 7 GHz at 4 dBm, Upper Sideband (Low-Side LO)

EVALUATION BOARD INFORMATION

The circuit board used in the application must use RF circuit design techniques. Signal lines must have 50 Ω impedance and connect the package ground leads and exposed pad directly to the ground plane similarly to that shown in Figure 99. Use a sufficient number of via holes to connect the top and bottom ground planes. The evaluation circuit board shown in Figure 100 is available from Analog Devices upon request.

EV1HMC951ALP4 Power-On Sequence

To power on the EV1HMC951ALP4, take the following steps:

1. Power up VDRF and VDLO with a 5 V supply.
2. Connect LOIN to the LO signal generator with an LO power of 0 dBm (typical).
3. Apply the RF signal.

EV1HMC951ALP4 Power-Off Sequence

To power off the EV1HMC951ALP4, take the following steps:

1. Turn off the LO and RF signals.
2. Set VDRF and VDLO to 0 V and then turn VDRF and VDLO off.

Layout

Solder the exposed pad on the underside of the HMC951A to a low thermal and electrical impedance ground plane. This pad is typically soldered to an exposed opening in the solder mask on the evaluation board. Connect these ground vias to all other ground layers on the evaluation board to maximize heat dissipation from the device package. Figure 99 shows the PCB land pattern footprint for the HMC951A evaluation board.

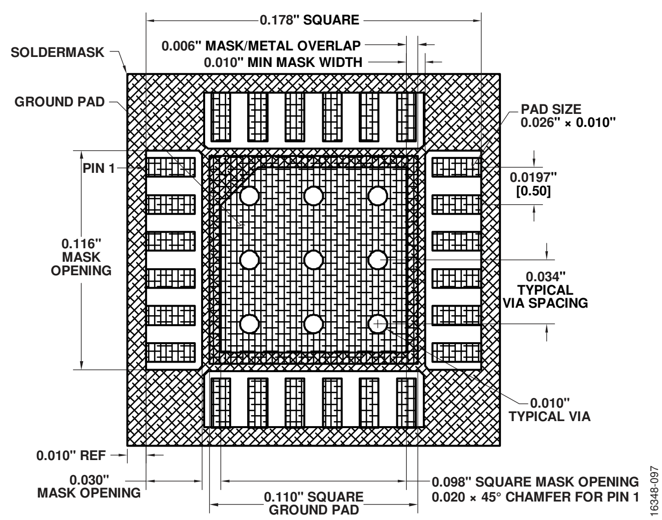

Figure 99. EV1HMC951ALP4 PCB Land Pattern Footprint

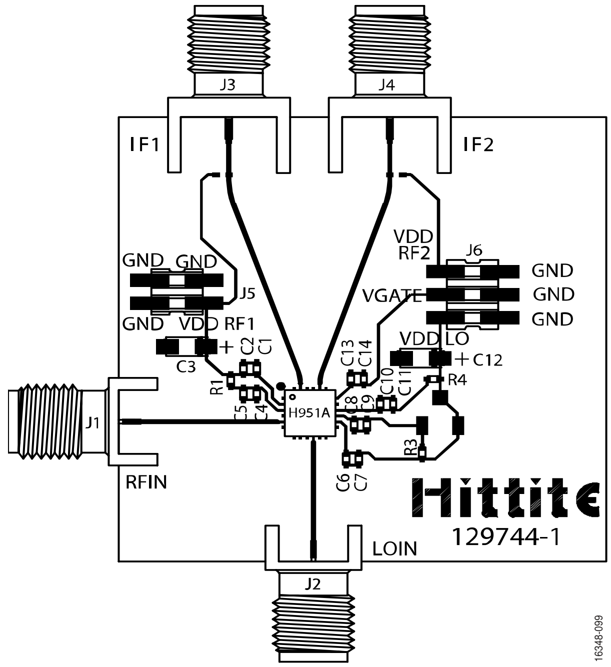

Figure 100. EV1HMC951ALP4 Evaluation Board Top Layer

Table 6. Bill of Materials for the EV1HMC951ALP4[1, 2] Evaluation Board PCB

Qty.	Reference Designator	Description	Manufacturer	Part Number
1	Not applicable	PCB, EV1HMC951ALP4; circuit board material: Rogers 4350	Analog Devices, Inc.	129744-1
2	J1, J2	SMA RF connectors, SRI	SRI Connector Gage Co.	25-146-1000-92
4	J3, J4	Johnson connectors, SRI	Johnson Components	142-0701-851
1	J5	Header connectors, 2 mm, four vertical positions, SMT	Molex	87759-0414
1	J6	Header connectors, 2 mm, four vertical positions, SMT	Molex	87759-0614
6	C1, C4, C6, C8, C10, C13	Ceramic capacitors, 100 pF, 5%, 50 V, C0G, 0402	Kemet	C0402C101J5GACTU
6	C2, C5, C7, C9, C11, C14	Ceramic capacitors, 0.01 µF, 50 V, 10%, X7R, 0603	Murata	RM155R71H102KA01D
2	C3, C12	Tantalum capacitors, 4.7 µF, 25 V, 10%, SMD, Case A	AVX Corp.	TAJA475M016R
1	H951A	Device under test, HM951A	Analog Devices, Inc.	HMC951A

[1] Reference this number when ordering the evaluation board PCB.
[2] This is a generic evaluation board. Some components or bias lines shown in Figure 100 are not used for the HMC951A.

OUTLINE DIMENSIONS

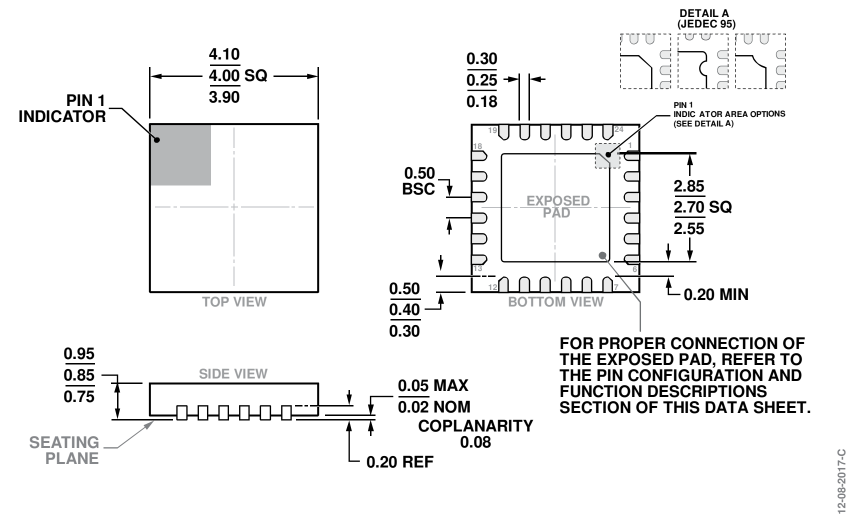

Figure 101. 24-Lead Lead Frame Chip Scale Package [LFCSP],
4 mm × 4 mm Body and 0.85 mm Package Height
(HCP-24-3)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Body Material	Lead Finish	Package Description	MSL Rating[2]	Package Option
HMC951ALP4E	−40°C to +85°C	Low Stress, Injected Molded Plastic	Ag	24-Lead LFCSP	MSL3	HCP-24-3
HMC951ALP4ETR	−40°C to +85°C	Low Stress, Injected Molded Plastic	Ag	24-Lead LFCSP	MSL3	HCP-24-3
EV1HMC951ALP4				Evaluation PCB Assembly		

[1] The HMC951ALP4E and the HMC951ALP4ETR are RoHS Compliant Parts.
[2] See the Absolute Maximum Ratings section.

D16348-0-4/18(A)