GAP-01

GENERAL-PURPOSE ANALOG SIGNAL PROCESSING SUBSYSTEM

Precision Monolithics Inc.

FEATURES

- **Low Offset Voltage** **3mV**
- **Low Zero-Scale Error** **4mV**
- **Low Droop Rate** **0.1mV/ms**
- **Wide Bandwidth** **400kHz**
- **Digitally Selected Signal Path**
- **Uncommitted Comparator On Chip**
- **Wide Application Versatility**
  - **Synchronous Demodulator**
  - **Absolute Value Amplifier**
  - **Two-Channel S/H Amplifier**
  - **Two-Channel Multiplexer With Gain**

ORDERING INFORMATION†

V_{OS} (mV)	V_{ZS} (mV)	MILITARY	HERMETIC INDUSTRIAL	PLASTIC COMMERCIAL
3	4	GAP01AX*	GAP01EX	GAP01EP
6	7	GAP01BX*	GAP01FX	GAP01FP

*For devices processed in total compliance to MIL-STD-883, add /883 after part number. Consult factory for 883 data sheet.

†All commercial and industrial temperature range parts are available with burn-in. For ordering information see 1986 Data Book, Section 2.

GENERAL DESCRIPTION

Designed as a general-purpose analog processing subsystem, the GAP-01 combines many commonly used system building blocks within a single integrated circuit.

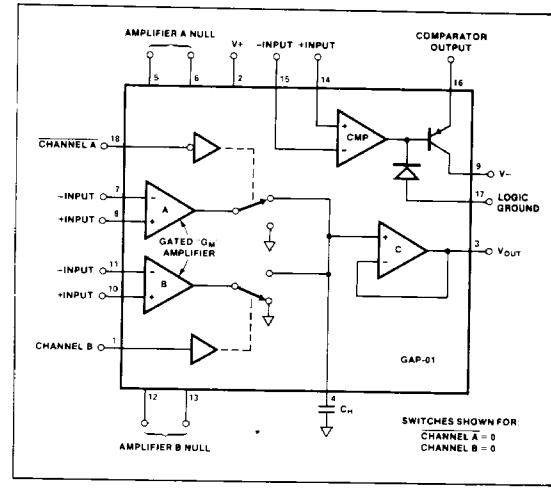
The basic circuit versatility stems from the GAP-01's architecture. The circuit features two differential input transconductance amplifiers, two low-glitch current mode switches, an output voltage buffer amplifier, and a precision comparator.

Both transconductance amplifier outputs are switched by current-mode switches into the voltage follower output buffer, thus providing two digitally selectable signal paths through the device. Gain through the two channels may be different in both sign and magnitude depending upon feedback selection. An external capacitor provides loop compensation and doubles as a hold or "memory" capacitor when the GAP-01 functions as a dual-channel sample/hold amplifier. Offset voltage and charge transfer errors are trimmed by using the "Zener-Zap" trim technique. The output buffer features a FET input stage to reduce droop rate error in S/H applications. A bias current cancellation circuit minimizes droop error at high ambient temperature.

The inclusion of a precision comparator on chip increases the GAP-01's versatility and cost effectiveness in data conversion applications. The output high voltage level is set by external resistors. This scheme maximizes noise immunity and permits interface to all standard logic families .

Several applications exploit the ability to select the signal path through the GAP-01. As a two-channel multiplexer or analog switch, the GAP-01 high input impedance offers advantages when switching high impedance signals. Gain through the "MUX" is also possible. The GAP-01 operates as a sample/hold amplifier in the hold mode when both transconductance amplifiers are unselected. With the on-board comparator, a two-channel successive approximation analog-to-digital conversion (ADC) system may be constructed. Combining a sign-magnitude, digital-to-analog (DAC) converter with the GAP-01 results in a four-quadrant multiplying DAC. The GAP-01 contains all the functional devices needed to perform synchronous demodulation or implement the absolute value function.

FUNCTIONAL DIAGRAM



CONTROL LOGIC

$\overline{\text{Ch A}}$	Ch B	OUTPUT to C
0	0	Channel A
0	1	Sum
1	0	Hold Last Input
1	1	Channel B

Manufactured under the following patent: 4,285,051.

ABSOLUTE MAXIMUM RATINGS (Note 2)

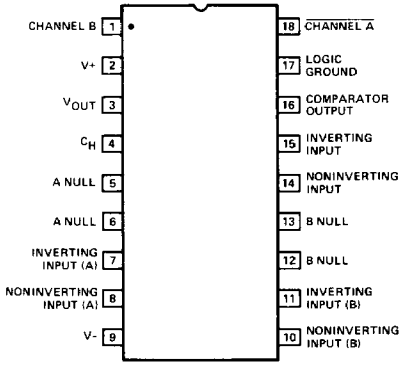
Supply Voltage ..... ±18V
Power Dissipation 500mW
Input Voltage ..... Equal to Supply Voltage
Logic and Logic Ground
Voltage ..... Equal to Supply Voltage
Output Short-Circuit Duration ..... Indefinite
Amplifier A or B Differential Input Voltage ..... ±24V
Comparator Differential Input Voltage ..... ±24V
Comparator Output Voltage... Equal to Positive Supply Voltage
Hold Capacitor Short-Circuit Duration ..... Indefinite
Storage Temperature ..... −65°C to +150°C
Lead Temperature (Soldering, 60 sec) ..... 300°C

Operating Temperature Range
GAP01AX, BX ..... −55°C to + 125°C
GAP01EX, FX ..... −25°C to +85°C
GAP01EP, FP ..... 0°C to +70°C
DICE Junction Temperature (T_j) ..... −65°C to +150°C

(NOTE 1)	MAXIMUM AMBIENT TEMPERATURE FOR RATING	DERATE ABOVE MAXIMUM AMBIENT TEMPERATURE
18-Pin DIP (X)	100°C	10mW/°C
18-Pin DIP (P)	50°C	10mW/°C

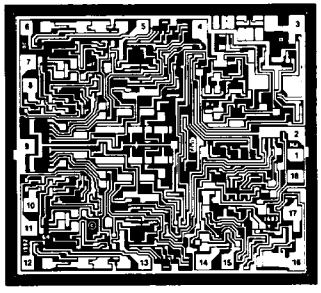
NOTES:
1. Maximum package power dissipation vs. ambient temperature.
2. Absolute ratings apply to both DICE and packaged parts, unless otherwise noted.

PIN CONNECTIONS



18-PIN HERMETIC DIP
(X-Suffix)
EPOXY DIP
(P-Suffix)

DICE CHARACTERISTICS



DIE SIZE 0.090 × 0.100 inch, 9,000 sq. mils
(2.286 × 2.54; 5.8 sq.mm)

1. CHANNEL (B)
2. V+
3. V_{OUT}
4. C_H
5. (A) NULL
6. (A) NULL
7. INVERTING INPUT (A)
8. NONINVERTING INPUT (A)
9. V−
10. NONINVERTING INPUT (B)
11. INVERTING INPUT (B)
12. (B) NULL
13. (B) NULL
14. COMPARATOR NONINVERTING INPUT
15. COMPARATOR INVERTING INPUT
16. COMPARATOR OUTPUT
17. LOGIC GND
18. CHANNEL (A)

For additional DICE information refer to 1986 Data Book, Section 2.

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $C_H = 1000pF$, $T_A = 25°C$.

PARAMETER	SYMBOL	CONDITIONS	GAP01A/E MIN	GAP01A/E TYP	GAP01A/E MAX	GAP01B/F MIN	GAP01B/F TYP	GAP01B/F MAX	UNITS
"g_m" AMPLIFIERS A, B									
Zero-Scale Error	V_{ZS}		—	2	4	—	3	7	mV
Input Offset Voltage	V_{OS}		—	2	3	—	3	6	mV
Input Bias Current	I_B		—	80	150	—	80	250	nA
Input Offset Current	I_{OS}		—	20	40	—	50	100	nA
Voltage Gain	A_V		18	25	—	10	25	—	V/mV
Open-Loop Bandwidth	BW	$A_V = 1$	—	0.4	—	—	0.4	—	MHz
Common-Mode Rejection Ratio	CMRR	$-10V \le V_{CM} \le +10V$	80	90	—	74	90	—	dB
Power Supply Rejection Ratio	PSRR	$\pm 9V \le V_S \le \pm 18V$	86	96	—	76	96	—	dB
Input Voltage Range	V_{CM}	(Note 2)	±11.5	±12	—	±11.5	±12	—	V
Slew Rate	SR		—	0.5	—	—	0.5	—	V/µs
Feedthrough Error		$\Delta V_{IN} = 20V$, CHA = 1, CHB = 0 (Note 2)	66	80	—	66	80	—	dB
Acquisition Time to 0.1% Accuracy	t_{aq}	20V Step, $A_{VCL} = +1$ (Note 2)	—	41	70	—	41	70	µs
Acquisition Time to 0.01% Accuracy	t_{aq}	20V Step, $A_{VCL} = +1$ (Note 2)	—	45	—	—	45	—	µs
COMPARATOR									
Input Offset Voltage	V_{OS}		—	0.5	1.5	—	1	3	mV
Input Bias Current	I_B		—	700	1000	—	700	1000	nA
Input Offset Current	I_{OS}		—	75	300	—	75	300	nA
Voltage Gain	A_V	2kΩ Pull-up Resistor to 5V (Note 2)	5	7.5	—	3.5	7	—	V/mV
Common-Mode Rejection Ratio	CMRR	$-10V \le V_{CM} \le +10V$	82	106	—	82	106	—	dB
Power Supply Rejection Ratio	PSRR	$\pm 9V \le V_S \le \pm 18V$	76	90	—	76	90	—	dB
Input Voltage Range	V_{CM}	(Note 2)	±11.5	±12.5	—	±11.5	±12.5	—	V
Low Output Voltage	V_{OL}	$I_{SINK} \le 5mA$, Logic GND = 0V	−0.2	0.15	0.4	−0.2	0.15	0.4	V
"OFF" Output Leakage Current	I_L	$V_{OUT} = 5V$	—	25	80	—	25	80	µA
Output Short-Circuit Current	I_{SC}	$V_{OUT} = 5V$	7	12	45	7	12	45	mA
Response Time	t_S	5mV Overdrive, (Note 3) 2kΩ Pull-up Resistor to 5V	—	150	—	—	150	—	ns
DIGITAL INPUTS-$\overline{CHA}$, CHB (Note 3)									
Logic "1" Input Voltage	V_H		2	—	—	2	—	—	V
Logic "0" Input Voltage	V_L		—	—	0.8	—	—	0.8	V
Logic "1" Input Current	I_{INH}	$V_H = 3.5V$	—	0.02	1	—	0.02	1	µA
Logic "0" Input Current	I_{INL}	$V_L = 0.4V$	—	1.6	10	—	2	10	µA
MISCELLANEOUS									
Droop Rate	V_{DR}	$T_j = +25°C$ (Note 1)	—	0.02	0.07	—	—	0.1	mV/ms
Output Voltage Swing: Amplifier C	V_{OP}	$R_L = 2.5k$	±11.5	±12.5	—	±11	±12	—	V
Short-Circuit Current: Amplifier C	I_{SC}		7	15	40	7	15	40	mA
Switch Aperture Time	t_{ap}		—	75	—	—	75	—	ns
Switch Switching Time	ts		—	50	—	—	50	—	ns
Slew Rate: Amplifier C	SR	$R_L = 2.5k$	—	2.5	—	—	2.5	—	V/µs
Power Supply Current	I_{SY}	No Load	—	5	7	—	6	9	mA

NOTES:

1. Due to limited production test times the droop current corresponds to junction temperature (T_j).
2. Guaranteed by design.
3. $\overline{\text{Channel A}}$ = "1", Channel B = "0".

ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $C_H = 1000pF$, $-55°C \le T_A \le 125°C$ for GAP01AX & BX; $-25°C \le T_A \le 85°C$ for GAP01EX & FX, and $0°C \le T_A \le 70°C$ for GAP01EP & FP.

PARAMETER	SYMBOL	CONDITIONS	GAP01A/E MIN	GAP01A/E TYP	GAP01A/E MAX	GAP01B/F MIN	GAP01B/F TYP	GAP01B/F MAX	UNITS
"g_m" AMPLIFIERS A, B									
Zero-Scale Error	V_{ZS}		—	4	7	—	6	12	mV
Input Offset Voltage	V_{OS}		—	3	6	—	5	10	mV
Average Input Offset Drift	TCV_{OS}	(Note 1)	—	−3	−6	—	−5	−6	µV/°C
Input Bias Current	I_B		—	160	250	—	160	500	nA
Input Offset Current	I_{OS}		—	30	100	—	30	150	nA
Voltage Gain	A_V		7.5	9	—	5	9	—	V/mV
Common-Mode Rejection Ratio	CMRR	$-10V \le V_{CM} \le +10V$	74	82	—	72	80	—	dB
Power Supply Rejection Ratio	PSRR	$\pm 9V \le V_S \le \pm 18V$	80	90	—	70	90	—	dB
Input Voltage Range	V_{CM}	(Note 1)	±11	±12	—	±10.5	±12	—	V
Slew Rate	SR		—	0.4	—	—	0.4	—	V/µs
Acquisition Time to 0.1% Accuracy	t_{aq}	20V Step, $A_{VCL} = +1$	—	60	—	—	60	—	µs
COMPARATOR									
Input Offset Voltage	V_{OS}		—	2	2.5	—	2	5	mV
Average Input Offset Drift	TCV_{OS}	(Note 1)	—	−4	−6	—	−4	−6	µV/°C
Input Bias Current	I_B		—	1000	2000	—	1100	2000	nA
Input Offset Current	I_{OS}		—	100	600	—	100	600	nA
Voltage Gain	A_V	2kΩ Pull-up Resistor to 5V, (Note 1)	4	6.5	—	2.5	6.5	—	V/mV
Common-Mode Rejection Ratio	CMRR	$-10V \le V_{CM} \le +10V$	80	100	—	80	92	—	dB
Power Supply Rejection Ratio	PSRR	$\pm 9V \le V_S \le \pm 18V$	72	82	—	72	86	—	dB
Input Voltage Range	V_{CM}	(Note 1)	±11	—	—	±11	—	—	V
Low Output Voltage	V_{OL}	$I_{SINK} \le 5mA$, Logic GND = 5V	−0.2	0.15	0.4	−0.2	0.15	0.4	V
"OFF" Output Leakage Current	I_L	$V_{OUT} = 5V$	—	25	100	—	25	160	µA
Output Short-Circuit Current	I_{SC}	$V_{OUT} = 5V$	6	10	45	6	10	45	mA
Response Time	t_s	5mV Overdrive, (Note 3) 2kΩ Pull-up Resistor to 5V	—	200	—	—	200	—	ns
DIGITAL INPUTS-$\overline{CHA}$, CHB (Note 3)									
Logic "1" Input Voltage	V_H		2	—	—	2	—	—	V
Logic "0" Input Voltage	V_L		—	—	0.8	—	—	0.8	V
Logic "1" Input Current	I_{INH}	$V_H = 3.5V$	—	0.02	1	—	0.02	1	µA
Logic "0" Input Current	I_{INL}	$V_L = 0.4V$	—	2.5	15	—	2.5	15	µA
MISCELLANEOUS									
Droop Rate	V_{DR}	T_j = Max. Operating Temp., (Note 2)	—	1	10	—	1	10	mV/ms
Output Voltage Swing: Amplifier C	V_{OP}	$R_L = 2.5k$	±11	±12	—	±10.5	±12	—	V
Short-Circuit Current: Amplifier C	I_{SC}		6	12	40	6	12	40	mA
Switch Aperture Time	t_{ap}		—	75	—	—	75	—	ns
Slew Rate: Amplifier C	SR	$R_L = 2.5k$	—	2	—	—	2	—	V/µs
Power Supply Current	I_{SY}	No Load	—	5.5	8	—	6.5	10	mA

NOTES: See next page.

WAFER TEST LIMITS at $V_S = \pm 15V$, $C_H = 1000pF$, $T_A = 25°C$.

PARAMETER	SYMBOL	CONDITIONS	GAP-01N LIMIT	UNITS
"g_m" AMPLIFIERS A, B				
Zero-Scale Error	V_{ZS}		7	mV MAX
Input Offset Voltage	V_{OS}		6	mV MAX
Input Bias Current	I_B		250	nA MAX
Input Offset Current	I_{OS}		100	nA MAX
Voltage Gain	A_V		10	V/mV MIN
Common-Mode Rejection Ratio	CMRR	$-10V \le V_{CM} \le +10V$	74	dB MIN
Power Supply Rejection Ratio	PSRR	$\pm 9V \le V_S \le \pm 18V$	76	dB MIN
Input Voltage Range	V_{CM}	(Note 1)	± 11.5	V MIN
Feedthrough Error		$\Delta V_{IN} = 20V$, $\overline{CHA} = 1$, CHB = 0 (Note 1)	66	dB MIN
COMPARATOR				
Input Offset Voltage	V_{OS}		3	mV MAX
Input Bias Current	I_B		1000	nA MAX
Input Offset Current	I_{OS}		300	nA MAX
Voltage Gain	A_V	2kΩ Pull-up Resistor to 5V (Note 1)	3.5	V/mV MIN
Common-Mode Rejection Ratio	CMRR	$-10V \le V_{CM} \le +10V$	82	dB MIN
Power Supply Rejection Ratio	PSRR	$\pm 9V \le V_S \le \pm 18V$	76	dB MIN
Input Voltage Range	V_{CM}	(Note 1)	± 11.5	V MIN
Low Output Voltage	V_{OL}	$I_{SINK} \le 5mA$, Logic GND = 5V	0.4 −0.2	V MAX V MIN
"OFF" Output Leakage Current	I_L	$V_{OUT} = 5V$	80	µA MAX
Output Short-Circuit Current	I_{SC}	$V_{OUT} = 5V$	45 7	mA MAX mA MIN
DIGITAL INPUTS-$\overline{CHA}$, CHB (Note 3)				
Logic "1" Input Voltage	V_H		2	V MIN
Logic "0" Input Voltage	V_L		0.8	V MAX
Logic "1" Input Current	I_{INH}	$V_H = 3.5V$	1	µA MAX
Logic "0" Input Current	I_{INL}	$V_L = 0.4V$	10	µA MAX
MISCELLANEOUS				
Droop Rate	V_{DR}	$T_j = 25°C$ (See Note 2) $T_A = 25°C$	0.1 0.20	mV/ms MAX mV/ms MAX
Output Voltage Swing: Amplifier C	V_{OP}	$R_L = 2.5k$	± 11	V MIN
Short-Circuit Current: Amplifier C	I_{SC}		40 7	mA MAX mA MIN
Power Supply Current	I_{SY}	No Load	9	mA MAX

NOTES:
1. Guaranteed by design.
2. Due to limited production test times the droop current corresponds to junction temperature (T_j). The droop current vs. time (after power-on) curve clarifies this point. Since most devices (in use) are on for more than 1 second, PMI specifies droop rate for ambient temperature (T_A) also. The warmed-up (T_A) droop current specification is correlated to the junction temperature (T_j) value. PMI has a droop current cancellation circuit which minimizes droop current at high temperatures.
3. $\overline{\text{Channel A}}$ = "1", Channel B = "0".

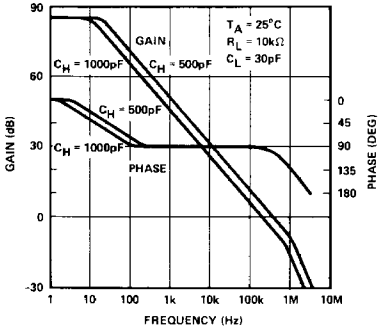
Electrical tests are performed at wafer probe to the limits shown. Due to variations in assembly methods and normal yield loss, yield after packaging is not guaranteed for standard product dice. Consult factory to negotiate specifications based on dice lot qualification through sample lot assembly and testing.

TYPICAL ELECTRICAL CHARACTERISTICS at $V_S = \pm 15V$, $C_H = 1000pF$, $T_A = 25°C$.

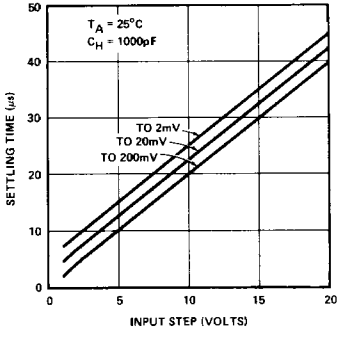
PARAMETER	SYMBOL	CONDITIONS	GAP-01N TYPICAL	UNITS
"g_m" AMPLIFIERS A, B				
Slew Rate	SR		0.5	V/μs
Acquisition Time to 0.1% Accuracy	t_{aq}	20V step, $A_{VCL} = 1$	41	μs
Acquisition Time to 0.01% Accuracy	t_{aq}	20V step, $A_{VCL} = 1$	45	μs
COMPARATOR				
Response Time	t_S	5mV Overdrive 2kΩ Pull-up Resistor to +5V	150	ns
MISCELLANEOUS				
Switch Aperture Time	t_{ap}		75	ns
Switching Time	t_S		50	ns
Slew Rate: Amplifier C	SR	$R_L = 2.5k\Omega$	2.5	V/μs

TYPICAL PERFORMANCE CHARACTERISTICS

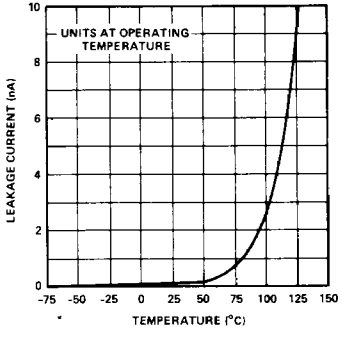
SMALL-SIGNAL OPEN-LOOP GAIN/PHASE vs FREQUENCY



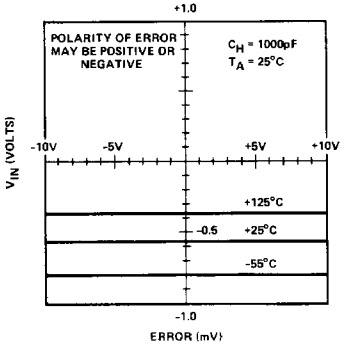
ACQUISITION TIME vs INPUT VOLTAGE STEP SIZE



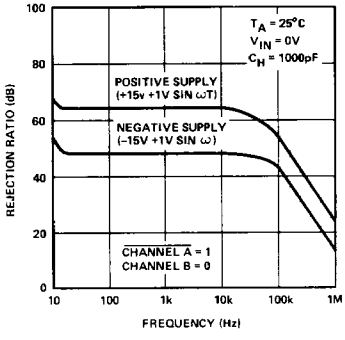
DROOP CURRENT vs TEMPERATURE



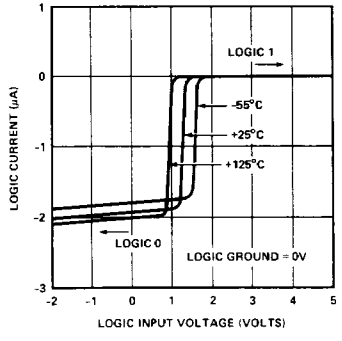
AMPLIFIER CHARGE INJECTION ERROR vs INPUT VOLTAGE AND TEMPERATURE



HOLD-MODE POWER SUPPLY REJECTION vs FREQUENCY

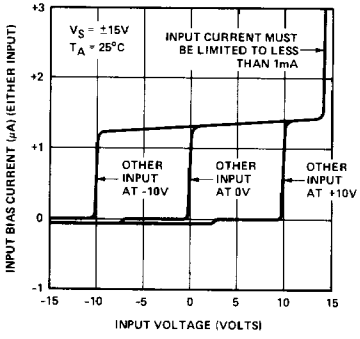


LOGIC INPUT CURRENT vs LOGIC INPUT VOLTAGE

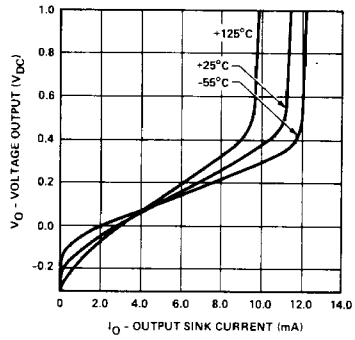


TYPICAL PERFORMANCE CHARACTERISTICS

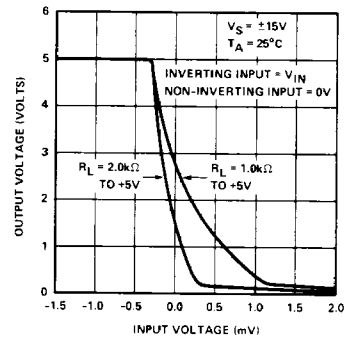
COMPARATOR INPUT BIAS CURRENT vs DIFFERENTIAL INPUT VOLTAGE



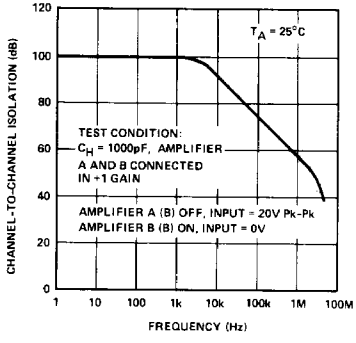
COMPARATOR OUTPUT VOLTAGE vs OUTPUT CURRENT AND TEMPERATURE



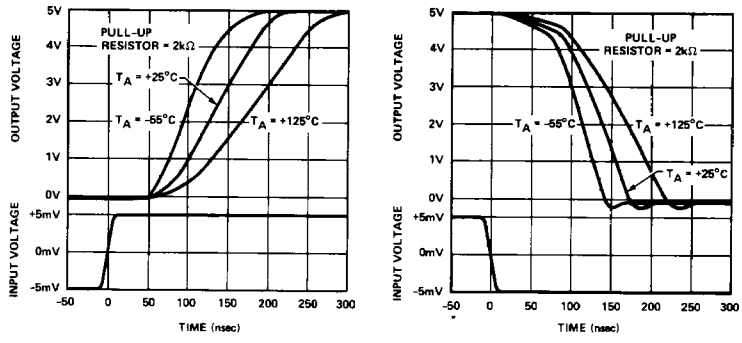
COMPARATOR TRANSFER CHARACTERISTIC



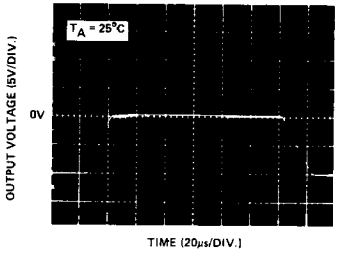
CHANNEL TO CHANNEL ISOLATION vs FREQUENCY



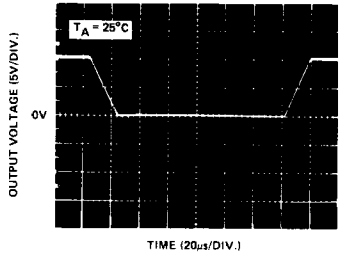
COMPARATOR RESPONSE TIME vs TEMPERATURE



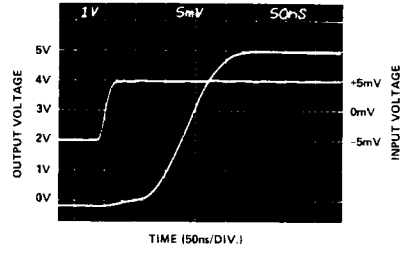
LARGE-SIGNAL INVERTING RESPONSE



LARGE-SIGNAL NONINVERTING RESPONSE

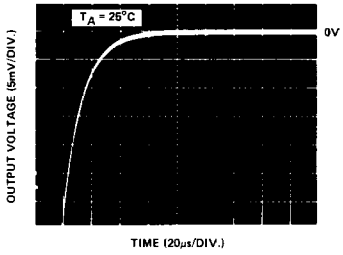


COMPARATOR OUTPUT RESPONSE TIME (2kΩ PULL-UP RESISTOR, T_A = 25° C)

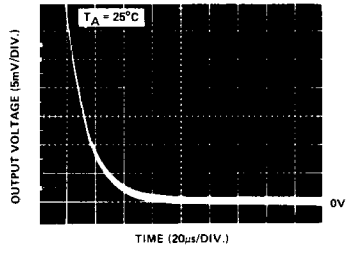


TYPICAL PERFORMANCE CHARACTERISTICS

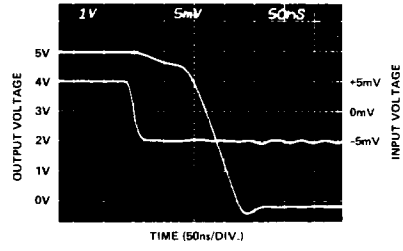
COMPARATOR SETTLING TIME FOR −10V TO 0V STEP INPUT



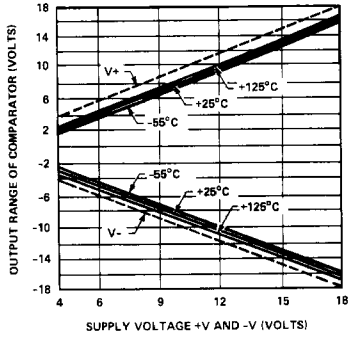
COMPARATOR SETTLING TIME FOR +10V TO 0V STEP INPUT



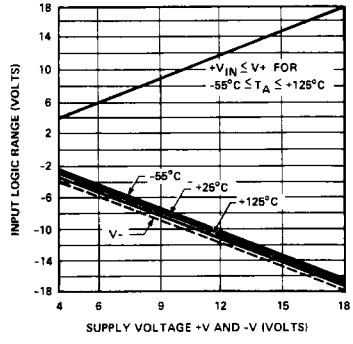
COMPARATOR OUTPUT RESPONSE TIME (2kΩ PULL-UP RESISTOR, T_A = 25° C)



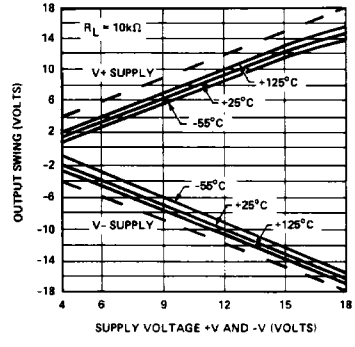
OUTPUT SWING OF COMPARATOR vs SUPPLY VOLTAGE



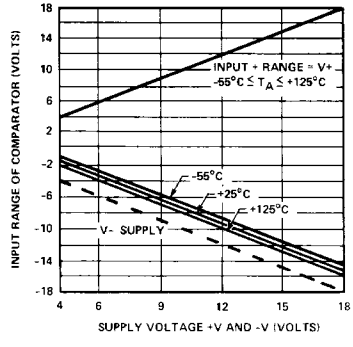
INPUT LOGIC RANGE vs SUPPLY VOLTAGE



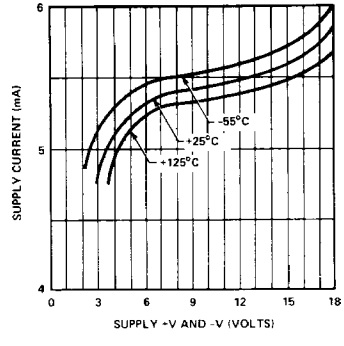
BUFFER OUTPUT VOLTAGE SWING vs SUPPLY VOLTAGE (DUAL SUPPLY OPERATION)



A AND B INPUT RANGE vs SUPPLY VOLTAGE

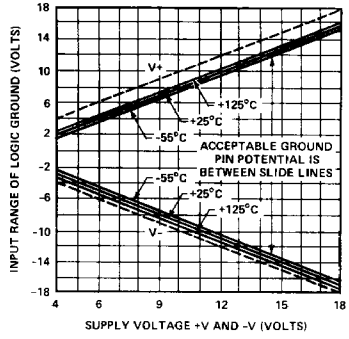


SUPPLY CURRENT vs SUPPLY VOLTAGE

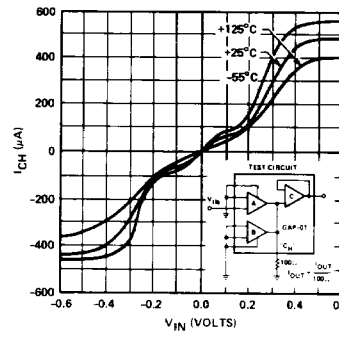


TYPICAL PERFORMANCE CHARACTERISTICS

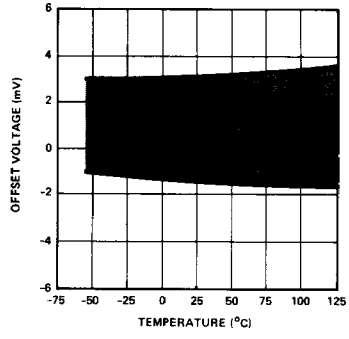
INPUT RANGE OF LOGIC GROUND vs SUPPLY VOLTAGE



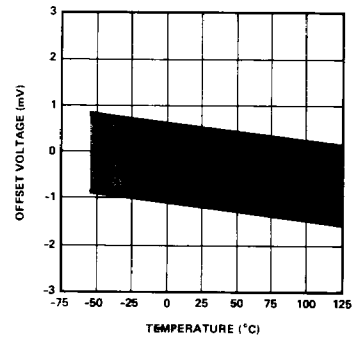
AMPLIFIER "A" OR "B" VOLTAGE TO CURRENT TRANSFER FUNCTION (V_{IN} vs I_{CH})



A AND B AMPLIFIERS OFFSET VOLTAGE vs TEMPERATURE

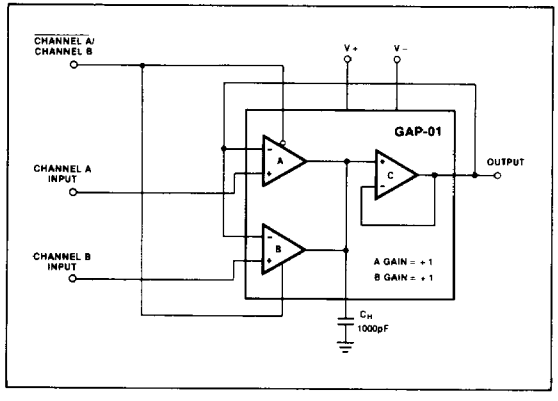


COMPARATOR OFFSET VOLTAGE vs TEMPERATURE

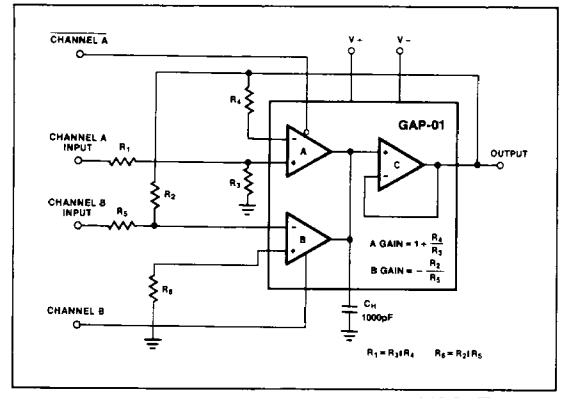


APPLICATION CIRCUITS

GAP-01 IN UNITY GAIN (+1) CONFIGURATION

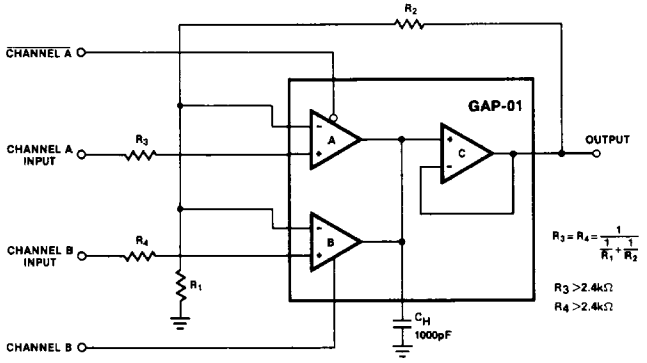


GAP-01 WITH POSITIVE AND NEGATIVE GAINS



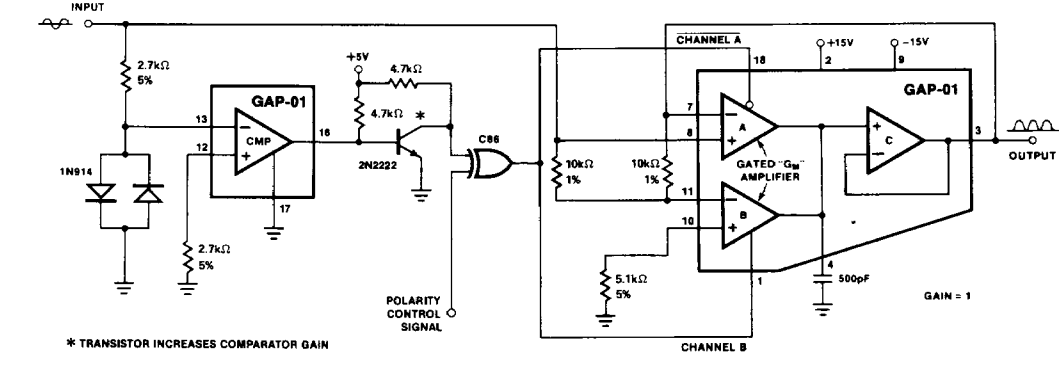
APPLICATION CIRCUITS

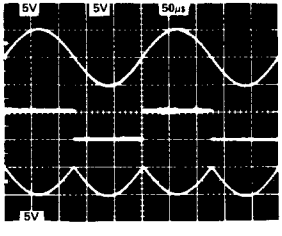
ALTERNATE GAIN CONFIGURATION



IF BOTH CHANNEL A AND CHANNEL B HAVE THE SAME POSITIVE VOLTAGE GAIN, A SINGLE VOLTAGE DIVIDER SETS THE GAIN FOR BOTH CHANNELS.

ABSOLUTE VALUE CIRCUIT WITH POLARITY PROGRAMMABLE OUTPUT

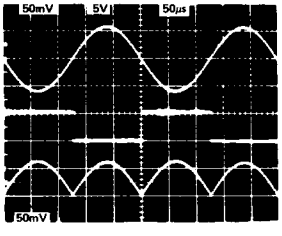




TRACE 1: INPUT SIGNAL

TRACE 2: $\overline{\text{CHANNEL A}}$/CHANNEL B CONTROL SIGNAL

TRACE 3: OUTPUT. POLARITY CONTROL SIGNAL = 0

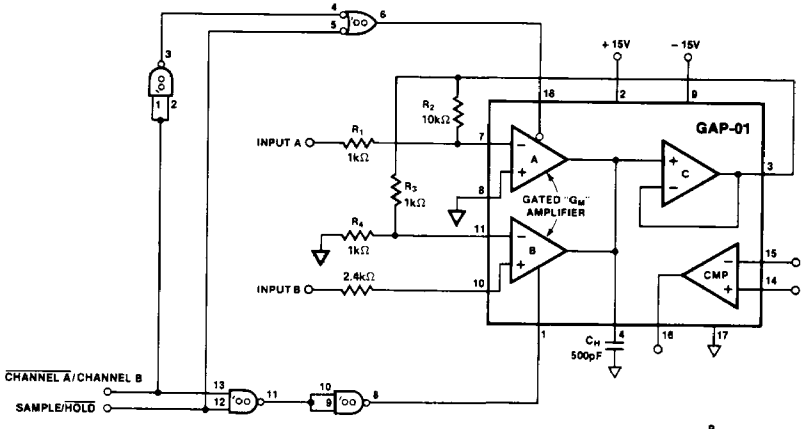


TRACE 1: INPUT SIGNAL

TRACE 2: $\overline{\text{CHANNEL A}}$/CHANNEL B CONTROL SIGNAL

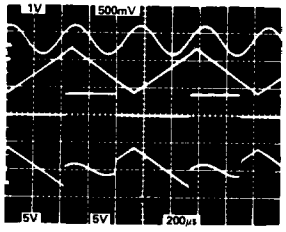
TRACE 3: OUTPUT. POLARITY CONTROL SIGNAL = 1

TWO-CHANNEL SAMPLE/HOLD AMPLIFIER



$$\text{CHANNEL A GAIN} = -\frac{R_2}{R_1} = -10$$

$$\text{CHANNEL B GAIN} = 1 + \frac{R_2}{R_1} = 2$$

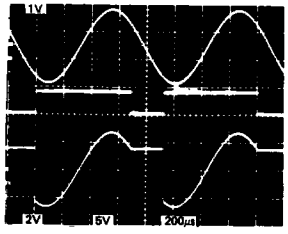


TRACE 1: INPUT SIGNAL B (1V/DIV.)

TRACE 2: INPUT SIGNAL A (0.5V/DIV.)

TRACE 3: $\overline{\text{CHANNEL A}}$/CHANNEL B CONTROL SIGNAL (5V/DIV.)

TRACE 4: OUTPUT WITH SAMPLE/$\overline{\text{HOLD}}$ = "1" (5V/DIV.)



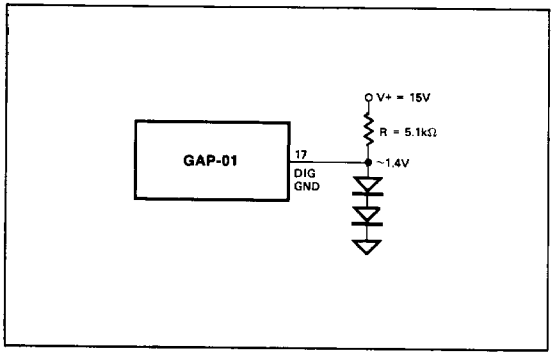
TRACE 1: INPUT SIGNAL B (1V/DIV.)

TRACE 2: SAMPLE/$\overline{\text{HOLD}}$ (5V/DIV.) CONTROL SIGNAL

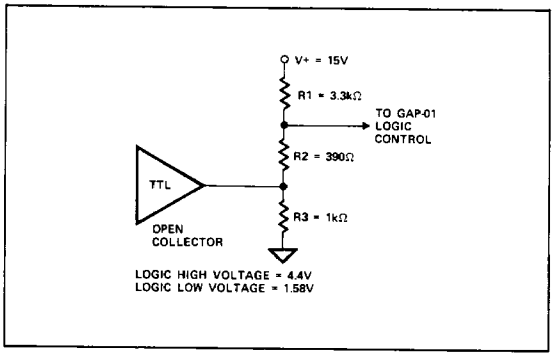
TRACE 3: OUTPUT SIGNAL (2V/DIV.) $\overline{\text{CHANNEL A}}$/CHANNEL B = "1"

APPLICATION CIRCUITS

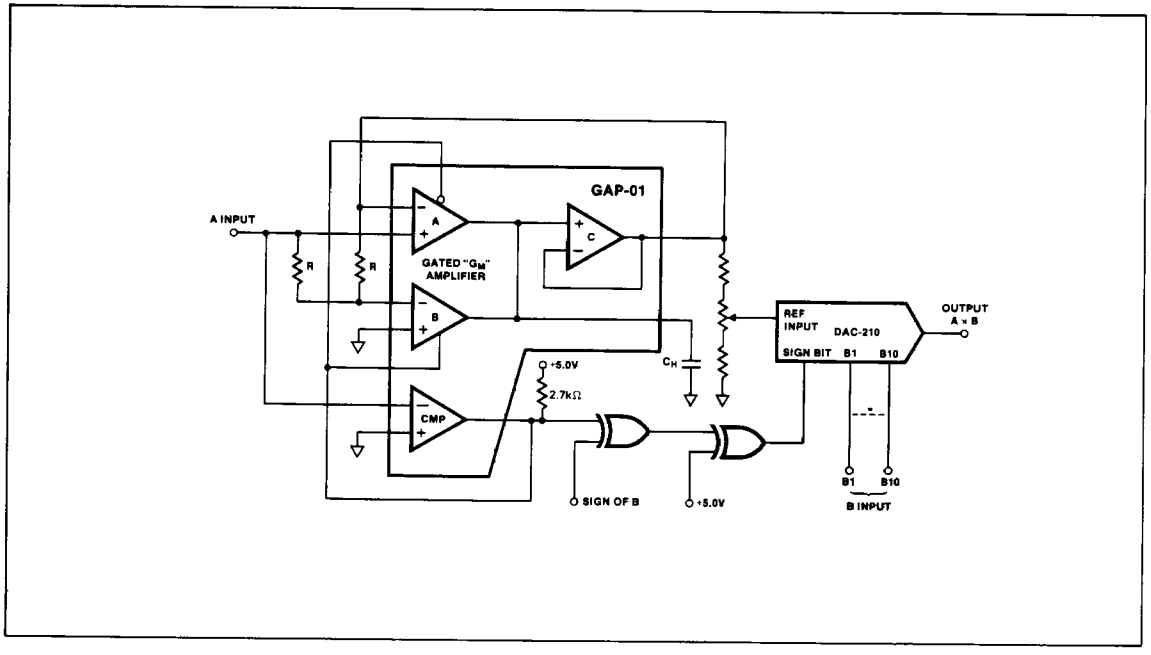
DIGITAL GROUND CONNECTION FOR SINGLE SUPPLY OPERATION



LOGIC LEVEL TRANSLATION FOR GAP-01 SINGLE SUPPLY OPERATION

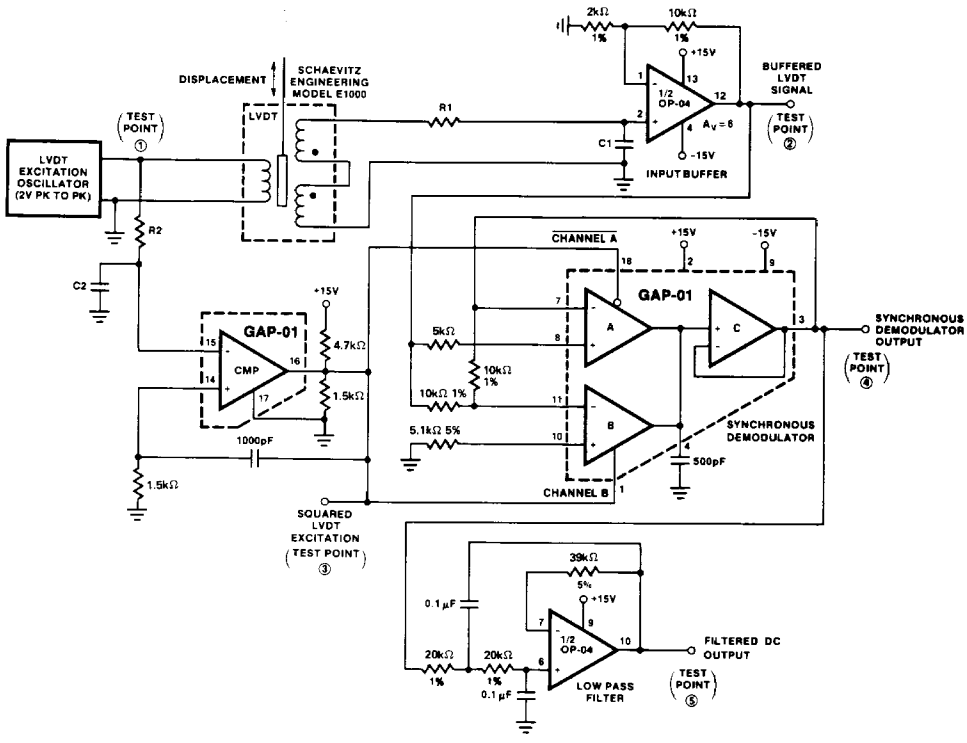


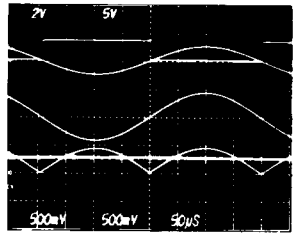
FOUR QUADRANT MULTIPLYING DAC



APPLICATION CIRCUITS

SYNCHRONOUS DEMODULATION OF LVDT SIGNAL





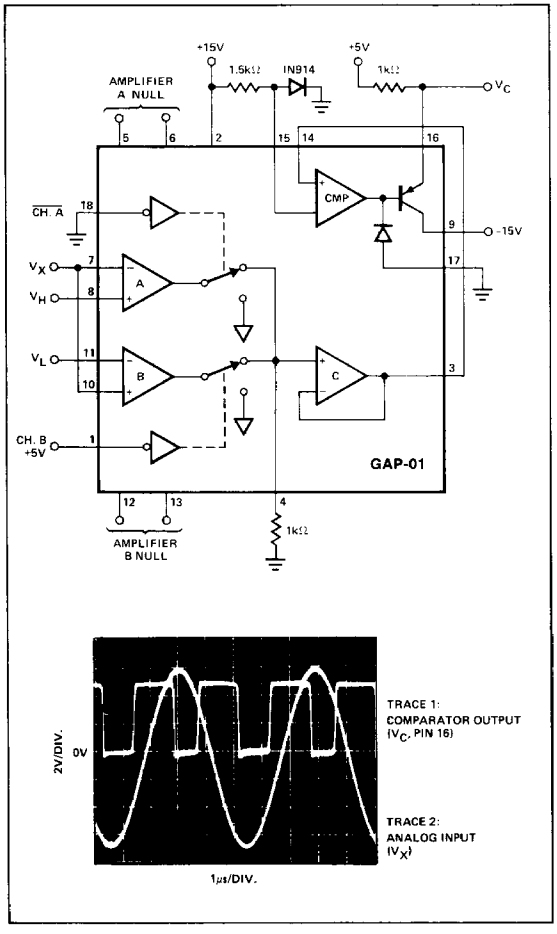
TRACE 1A: LVDT SINEWAVE EXCITATION (TEST POINT 1) –2V/DIV.
TRACE 1B: GAP-01 COMPARATOR OUTPUT (TEST POINT 3) –5V/DIV.

TRACE 2: BUFFERED LVDT OUTPUT AT GAP-01 INPUT (TEST POINT 2) 0.5V/DIV.

TRACE 3A: LVDT SIGNAL AFTER GAP-01 SYNCHRONOUS DEMODULATION (TEST POINT 4) –0.5V/DIV.
TRACE 3B: DC OUTPUT LEVEL INDICATING LVDT CORE POSITION (TEST POINT 5) 0.5V/DIV.

APPLICATION CIRCUITS

WINDOW COMPARATOR



APPLICATION INFORMATION

CAPACITOR RECOMMENDATIONS

The external capacitor (C_H) serves as the compensation capacitor and hold capacitor in sample/hold applications. Stable operation requires a minimum value of 500pF. Larger capacitors may be used to lower droop rate errors, but acquisition time will increase and bandwidth decrease.

The capacitor should have very high insulation resistance and low dielectric absorption. For temperatures below 85° C, a polystyrene capacitor is recommended, while a Teflon capacitor is recommended for high temperature environments.

COMPARATOR

The comparator output high level (V_{OH}) is set by external resistors. It's possible to optimize noise immunity while interfacing to all standard logic families — TTL, DTL, and CMOS. Figure 1 shows the comparator output with external level setting resistors. Table I gives typical R_1 and R_2 values for common circuit conditions.

With the comparator in the low state (V_{OL}), the output stage will be required to sink a current approximately equal to V_C/R_1.

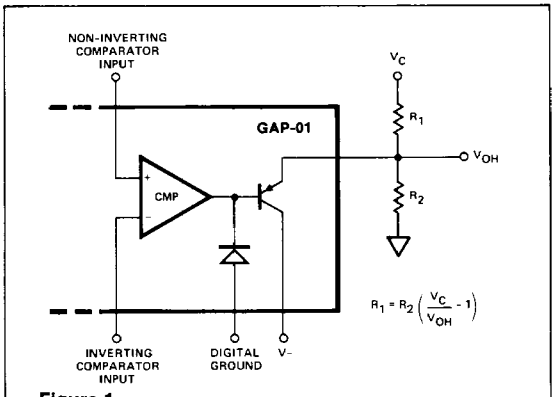


Figure 1

V_C	V_{OH}	R_1	R_2
5	3.5	2.7K	6.2K
5	5.0	2.7K	∞
15	3.5	4.7K	1.5K
15	5.0	4.7K	2.4K
15	7.5	7.5K	7.5K
15	10.0	7.5K	15K

$$R_1 \approx \frac{V_C}{I_{sink}}$$

$$R_2 \approx R_1\left(\frac{1}{\frac{V_C}{V_{OH}} - 1}\right)$$

Table I

The maximum comparator high output voltage (V_{OH}) should be constrained to: $V_{OH}\,(max) < V+ - 2V$

CAPACITOR GUARDING AND GROUND LAYOUT

Ground planes are recommended to minimize ground path resistance. Separate analog and digital grounds should be used. The two ground systems are tied together only at the

common system ground. This avoids digital currents returning to the system ground through the analog ground path.

The C_H terminal (Pin 4) is a high-impedance point. To minimize gain errors and maintain the GAP-01's inherently low droop rate, guarding Pin 4 as shown in Figure 2 is recommended.

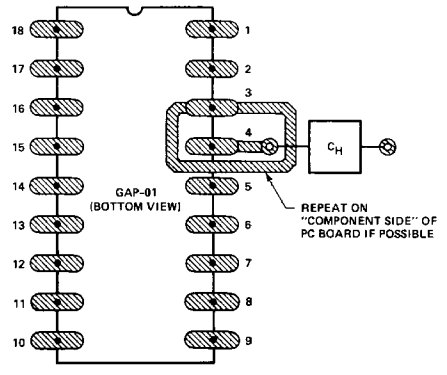


Figure 2

LOGIC CONTROL

The transconductance amplifier outputs are switched by the digital logic signals applied at $\overline{\text{Channel A}}$ and Channel B pins. Two signal paths through the GAP-01 are possible.

The logic threshold voltage is 1.4 volts when digital ground is at zero volts. Other threshold voltages (V_{TH}) may be selected by applying the formula:

$$V_{TH} \approx 1.4V + \text{Digital Ground Potential.}$$

Figure 3 shows the simplified logic control circuit. For proper operation, digital ground must always be at least 3.5V below the positive supply and 2.5V above the negative supply. The logic signals must always be at least 2.8V above the negative supply.

Operating the digital ground at other than zero volts does influence the comparator output low voltage. The V_{OL} level is referenced to digital ground and will follow any changes in digital ground potential:

$$V_{OL} \approx 0.2V + \text{Digital Ground Potential.}$$

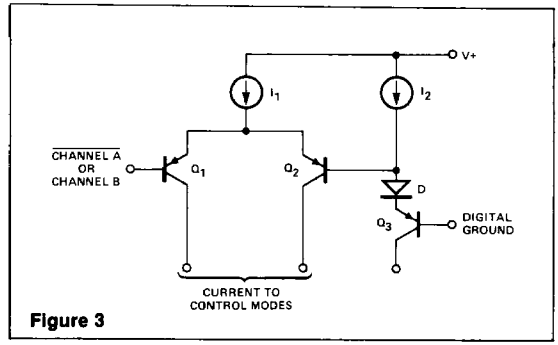


Figure 3

ZERO-SCALE ERROR ADJUSTMENT

For sample/hold applications the zero-scale error (V_{OS} plus charge injection error) can be adjusted to zero. With the input to each channel equal to zero, the GAP-01 is switched between the sample mode (either $\overline{\text{channel A}}$ or channel B active) and the hold mode ($\overline{\text{channel A}} = 1$, channel B = 0). The output is adjusted to read zero when the unit is in the hold mode.

The V_{ZS} trim circuit is identical to the V_{OS} trim circuit.

OFFSET VOLTAGE ERROR ADJUSTMENT Offset voltage through either $\overline{\text{channel A}}$ or channel B may be nulled with an external 100kΩ potentiometer as shown below.

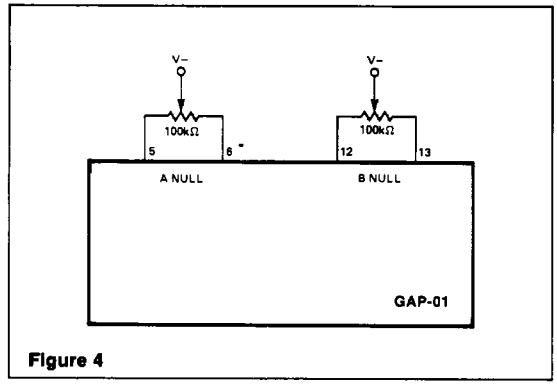


Figure 4