GV7605

Aviia™ Receiver

Key Features

- Serial digital video receiver for standard and high definition component video:
  - SD 525i and 625i
  - HD 720p 24, 25, 30, 50 and 60
  - HD 1080i 50, 60
  - HD 1080p 24, 25, 30, 50 and 60
- Supports 8-bit, 10-bit or 12-bit component digital video:
  - RGB or YCbCr 4:4:4 sampled
  - YCbCr 4:2:2 or 4:2:0 sampled
- Long reach cable performance when combined with the GV8501 cable equalizer
  - 140m typical HD performance over high quality 75Ω coaxial cable
- Serial digital loop-though output
- Integrated audio de-embedder for the extraction of up to 8 channels of 48kHz digital audio
- Supports IEC 13818-1 compliant transport streams over the Asynchronous Serial Interface (ASI)
- Automatic selection between SD/HD component video and ASI input data
- Ancillary (ANC) data detection and extraction
- User selectable processing features, including:
  - Timing Reference Signal (TRS) error detection and correction
  - ANC data checksum error detection and correction
  - Programmable ANC data detection
  - Line number and CRC error detection and correction
  - Illegal video code word re-mapping
- 4-wire Gennum Serial Peripheral Interface (GSPI) for external host command and control
- JTAG test interface
- 1.2V core and 3.3V analog voltage power supplies
- 1.8V or 3.3V selectable digital I/O power supply
- Small footprint 100-BGA (11mm x 11mm)
- Low power operation, typically 405mW
- Pb-free and RoHS compliant

Applications

- Digital Video Recorders (DVR)
- Video servers
- Video mixers and switchers
- Image capture devices
- Video framegrabbers
- Camcorders
- Video monitors & displays

Description

The GV7605 is a serial digital video receiver for standard and high definition component video, operating at 270Mb/s, 1.485Gb/s and 2.97Gb/s data rates. When combined with the GV8501 cable equalizer, the GV7605 is capable of receiving digital video over 75Ω coaxial cable at lengths up to 300m. This provides a complete receive solution for the transmission of both interlaced and progressive component digital video, up to 1920 x 1080, in coaxial cable-based video systems.

Using the GV7605 with the complete Aviia receiver reference design, it is possible to implement an all-digital, bi-directional multimedia interface over coax. This interface allows both DC power and a bi-directional, half-duplex, auxiliary data interface, up to 1Mb/s, to be carried over the same single, robust and cost effective coaxial cable as the high-speed serial digital video. The GV7605 also provides a re-timed serial digital output for video loop-through applications.

The GV7605 includes a broad range of user-selectable processing features, such as Timing Reference Signal (TRS) error detection and extraction, illegal code word re-mapping, and ancillary data packet extraction. The content of ancillary data packets, embedded by a Aviia transmitter, can be extracted and retrieved via the host interface. Device configuration and status reporting is

accomplished via the Gennum Serial Peripheral Interface (GSPI). Alternatively, many processing features and operational modes can be configured directly through external pin settings.

The device can output 8-bit, 10-bit and 12-bit video data, for RGB or YCbCr 4:4:4, and YCbCr 4:2:2 or 4:2:0. A configurable 20-bit wide parallel digital video output bus is provided, with associated pixel clock and timing signal outputs. The GV7605 supports ITU-R BT.656 SD formats, and HD formats conforming to ITU-R BT.709 and BT.1120-6 for 1125-line formats, and SMPTE 296M for 750-line formats. The device may also be configured to output CEA-861 timing.

The GV7605 audio de-embedding function allows the up to 8 channels of serial digital audio within the ancillary data space of the video data stream to be extracted. The audio output signal formats supported by the device include AES/EBU for professional applications, S/PDIF, and I^2S. 16-bit, 20-bit and 24-bit audio formats are supported at 48kHz synchronous-to-video for SD video formats and 48kHz synchronous or asynchronous for HD formats. Additional audio processing features include: individual channel extraction, audio group selection, group replacement, channel swapping and audio channel status extraction.

The GV7605 supports an Asynchronous Serial Interface (ASI) 270Mb/s input, carrying compressed audio and video transport streams, conforming to IEC 13818-1. Transport stream data is output from the device at a synchronous 27MHz clock rate. The device will automatically deserialize and 8b/10b decode the data.

Packaged in a space saving 100-BGA, the GV7605 is ideal for designs where high-density component placement is required. Typically requiring only 405mW power, the device can be used as a high bandwidth alternative to analog composite or component video interfaces, providing a high quality, all-digital, long reach video receive solution.

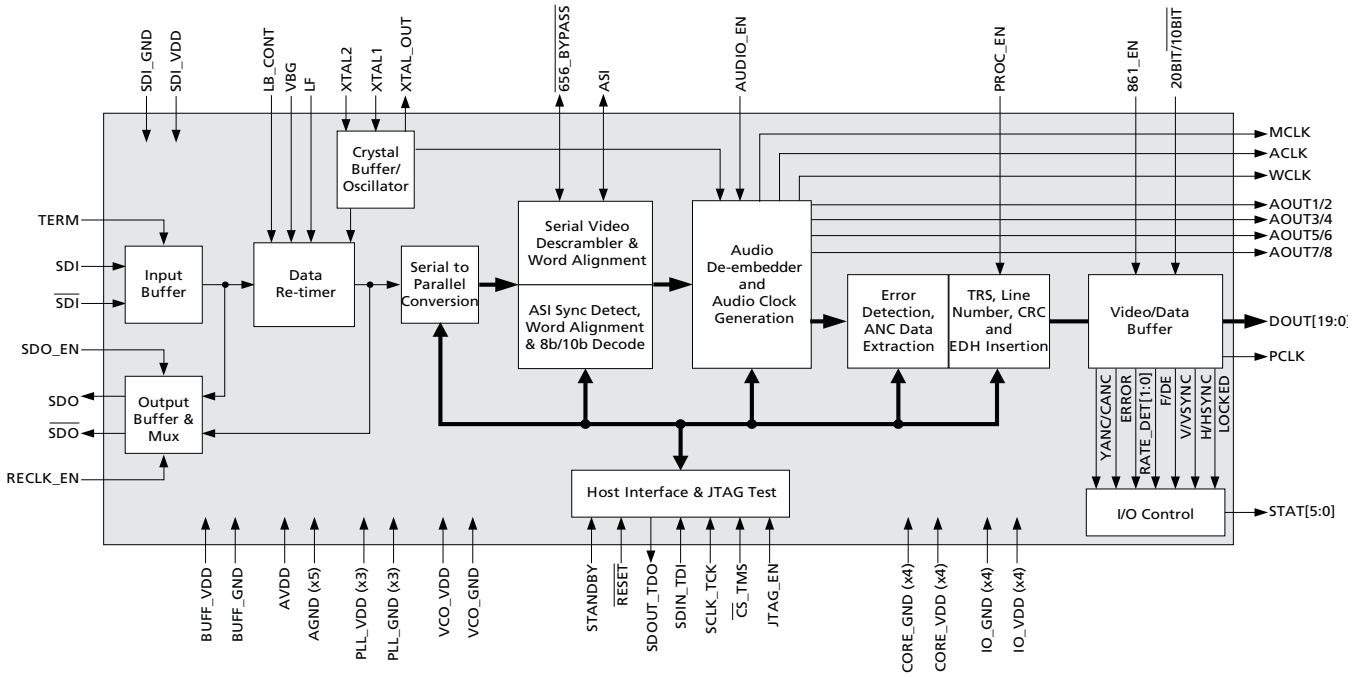


Figure A: GV7605 Functional Block Diagram

Revision History

Version	ECR	Date	Changes and / or Modifications
8	019059	April 2014	Updated Figure 6-1: GV7605 Package Dimensions
7	153582	February 2010	Added analog input absolute maximum ratings to Table 2-1: Absolute Maximum Ratings. Updated device latency values in Table 2-4: AC Electrical Characteristics.
6	152574	September 2009	Updates.
5	152158	June 2009	Modified Section 4.11.1.1, Section 4.12, Section 4.17.4, Section 4.19, and Table 4-34. Added Figure 4-64. Changed 6.3 Marking Diagram.
4	151834	May 2009	Re-ordered the DOUT[19:10] & DOUT[9:0] in Table 1-1 to reflect the pin names. Changed Figure 4-41.
3	151652	April 2009	Changed 4.16.8 Ancillary Data Extraction and its registers.
2	151552	March 2009	Changed DOUT[18_10] and DOUT[9:0] pin descriptions.
1	151322	February 2009	Changed block diagram. Changed $\overline{656}$_BYPASS pin description. Changed/Added H:V:F Timing diagrams. Added GSPI timing delays values. Added Index.
0	150966	December 2008	New document.

Contents

List of Tables

List of Figures

1. Pin Out

1.1 Pin Assignment

	1	2	3	4	5	6	7	8	9	10
A	VBG	LF	LB_ CONT	VCO_ VDD	STAT0	STAT1	IO_ VDD	PCLK	DOUT18	DOUT17
B	AVDD	PLL_ VDD	RSV	VCO_ GND	STAT2	STAT3	IO_ GND	DOUT19	DOUT16	DOUT15
C	SDI	AGND	PLL_ VDD	PLL_ VDD	STAT4	STAT5	$\overline{\text{RESET}}$	DOUT12	DOUT14	DOUT13
D	$\overline{\text{SDI}}$	AGND	AGND	PLL_ GND	CORE_ GND	CORE_ VDD	RSV	JTAG _EN	IO_ GND	IO_ VDD
E	SDI_ VDD	SDI_ GND	AGND	PLL_ GND	CORE_ GND	CORE_ VDD	SDOUT _TDO	SDIN _TDI	DOUT10	DOUT11
F	TERM	RSV	AGND	PLL_ GND	CORE_ GND	CORE_ VDD	$\overline{\text{CS}}$_ TMS	SCLK _TCK	DOUT8	DOUT9
G	RSV	RSV	RECLK _EN	RSV	CORE_ GND	CORE_ VDD	$\overline{656}$_ $\overline{\text{BYPASS}}$	ASI	IO_ GND	IO_ VDD
H	BUFF _VDD	BUFF _GND	AUDIO _EN	WCLK	861_EN	XTAL _OUT	20BIT/ $\overline{\text{10BIT}}$	PROC _EN	DOUT6	DOUT7
J	SDO	SDO _EN	AOUT 1/2	ACLK	AOUT 5/6	XTAL2	IO_ GND	DOUT1	DOUT4	DOUT5
K	$\overline{\text{SDO}}$	STAND BY	AOUT 3/4	MCLK	AOUT 7/8	XTAL1	IO_ VDD	DOUT0	DOUT2	DOUT3

1.2 Pin Descriptions

Table 1-1: Pin Descriptions

Pin Number	Name	Type	Description
A1	VBG	Analog Input	Band Gap voltage filter connection.
A2	LF	Analog Input	Loop Filter component connection.
A3	LB_CONT	Analog Input	Connection for loop bandwidth control resistor.
A4	VCO_VDD	Input Power	POWER pin for the VCO. Connect to 1.2V DC analog through an RC filter (see 5. References & Relevant Standards). VCO_VDD is nominally 0.7V (Do not connect directly to 0.7V).

Table 1-1: Pin Descriptions (Continued)

<table>
<tr><th>Pin Number</th><th>Name</th><th>Type</th><th>Description</th></tr>
<tr><td>A5, A6, B5, B6, C5, C6</td><td>STAT[0:5]</td><td>Output</td><td>MULTI-FUNCTIONAL OUTPUT PORT.
Signal levels are LVCMOS/LVTTL compatible.
Each of the STAT[5:0] pins can be configured individually to output one of the following signals:
Signal — Default
H/HSYNC — STAT0
V/VSYNC — STAT1
F/DE — STAT2
LOCKED — STAT3
Y/1ANC — STAT4
C/2ANC — –
DATA_ERROR — STAT5
VIDEO_ERROR — –
AUDIO_ERROR — –
EDH_DETECTED — –
CARRIER_DETECT — –
RATE_DET0 — –
RATE_DET1 — –</td></tr>
<tr><td>A7, D10, G10, K7</td><td>IO_VDD</td><td>Input Power</td><td>POWER connection for digital I/O. Connect to 3.3V or 1.8V DC digital.</td></tr>
<tr><td>A8</td><td>PCLK</td><td>Output</td><td>PARALLEL DATA BUS CLOCK
Signal levels are LVCMOS/LVTTL compatible.
Full HD 10-bit or 20-bit mode — PCLK @ 148.5 or 148.5/1.001MHz
HD 10-bit mode — PCLK @ 148.5 or 148.5/1.001MHz
HD 20-bit mode — PCLK @ 74.25 or 74.25/1.001MHz
SD 10-bit mode — PCLK @ 27MHz
SD 20-bit mode — PCLK @ 13.5MHz</td></tr>
</table>

Table 1-1: Pin Descriptions (Continued)

Pin Number	Name	Type	Description	
B8, A9, A10, B9, B10,C9, C10, C8, E10, E9	DOUT[19:10]	Output	PARALLEL DATA BUS Signal levels are LVCMOS/LVTTL compatible.	
			20-bit mode 20BIT/$\overline{10BIT}$ = HIGH	Video mode ($\overline{656\_BYPASS}$ = HIGH and ASI = LOW): Luma data output for SD and HD data rates; Data Stream 1 for Full HD at 148.5MHz ASI mode ($\overline{656\_BYPASS}$ = LOW and ASI = HIGH): Not defined Data-Through mode ($\overline{656\_BYPASS}$ = LOW and ASI = LOW): Data output
			10-bit mode 20BIT/$\overline{10BIT}$ = LOW	Video mode ($\overline{656\_BYPASS}$ = HIGH and ASI = LOW): Multiplexed Luma/Chroma data output for SD and HD data rates; Multiplexed Data Stream 1/2 for Full HD at 148.5MHz ASI mode ($\overline{656\_BYPASS}$ = LOW and ASI = HIGH): 8b/10b decoded transport stream data Data-Through mode ($\overline{656\_BYPASS}$ = LOW and ASI = LOW): Data output
			Video mode ($\overline{656\_BYPASS}$ = HIGH and ASI = LOW)	Luma data output for SD and HD data rates; Data Stream 1 for Full HD at 148.5MHz (20-bit mode)
			ASI mode ($\overline{656\_BYPASS}$ = LOW and ASI = HIGH)	Transport stream output
			Data-Through mode ($\overline{656\_BYPASS}$ = LOW and ASI = LOW)	Data output
B1	AVDD	Input Power	POWER pin for analog circuitry. Connect to 3.3V DC analog.	
B2, C3, C4	PLL_VDD	Input Power	POWER pins for the Reclocker PLL. Connect to 1.2V DC analog.	
B3, F2, G1, G2, G4	RSV		These pins must be left unconnected.	
B4	VCO_GND	Input Power	GND pin for the VCO. Connect to analog GND.	
B7, D9, G9, J7	IO_GND	Input Power	GND connection for digital I/O. Connect to digital GND.	
C1, D1	SDI, $\overline{SDI}$	Analog Input	Serial Digital Differential Input.	

Table 1-1: Pin Descriptions (Continued)

Pin Number	Name	Type	Description
C2, D2, D3, E3, F3	AGND	Input Power	GND pins for sensitive analog circuitry. Connect to analog GND.
C7	$\overline{\text{RESET}}$	Input	CONTROL SIGNAL INPUT Signal levels are LVCMOS/LVTTL compatible. Used to reset the internal operating conditions to default settings and to reset the JTAG sequence. Normal mode (JTAG_EN = LOW): When LOW, all functional blocks are set to default conditions and all digital output signals become high impedance. When HIGH, normal operation of the device resumes. JTAG test mode (JTAG_EN = HIGH): When LOW, all functional blocks are set to default and the JTAG test sequence is reset. When HIGH, normal operation of the JTAG test sequence resumes.
D4, E4, F4	PLL_GND	Input Power	GND pins for the Reclocker PLL. Connect to analog GND.
D5, E5, F5, G5	CORE_GND	Input Power	GND connection for device core. Connect to digital GND.
D6, E6, F6, G6	CORE_VDD	Input Power	POWER connection for device core. Connect to 1.2V DC digital.
D7	RSV	Input	Connect to core ground.
D8	JTAG_EN	Input	CONTROL SIGNAL INPUT Signal levels are LVCMOS/LVTTL compatible. Used to select JTAG test mode or host interface mode. When JTAG_EN is HIGH, the host interface port is configured for JTAG test. When JTAG_EN is LOW, normal operation of the host interface port resumes.
E1	SDI_VDD	Input Power	POWER pin for SDI buffer. Connect to 3.3V DC analog.
E2	SDI_GND	Input Power	GND pin for SDI buffer. Connect to analog GND.
E7	SDOUT_TDO	Output	COMMUNICATION SIGNAL OUTPUT Signal levels are LVCMOS/LVTTL compatible. GSPI serial data output/test data out. In JTAG mode (JTAG_EN = HIGH), this pin is used to shift test results from the device. In host interface mode, this pin is used to read status and configuration data from the device.

Table 1-1: Pin Descriptions (Continued)

Pin Number	Name	Type	Description	
E8	SDIN_TDI	Input	COMMUNICATION SIGNAL INPUT Signal levels are LVCMOS/LVTTL compatible. GSPI serial data in/test data in. In JTAG mode (JTAG_EN = HIGH), this pin is used to shift test data into the device. In host interface mode, this pin is used to write address and configuration data words into the device.	
F1	TERM	Analog Input	Decoupling for internal SDI termination resistors.	
F7	$\overline{CS}$_TMS	Input	COMMUNICATION SIGNAL INPUT Signal levels are LVCMOS/LVTTL compatible. Chip select / test mode start. In JTAG mode (JTAG_EN = HIGH), this pin is Test Mode Start, used to control the operation of the JTAG test. In host interface mode (JTAG_EN = LOW), this pin operates as the host interface chip select and is active LOW.	
F8	SCLK_TCK	Input	COMMUNICATION SIGNAL INPUT Signal levels are LVCMOS/LVTTL compatible. Serial data clock signal. In JTAG mode (JTAG_EN = HIGH), this pin is the JTAG clock. In host interface mode (JTAG_EN = LOW), this pin is the host interface serial bit clock. All JTAG/host interface addresses and data are shifted into/out of the device synchronously with this clock.	
F10, F9, H10, H9, J10, J9, K10, K9, J8, K8	DOUT[9:0]	Output	PARALLEL DATA BUS Signal levels are LVCMOS/LVTTL compatible.	
			20-bit mode 20BIT/$\overline{10BIT}$ = HIGH	Video mode ($\overline{656\_BYPASS}$ = HIGH and ASI = LOW): Chroma data output for SD and HD data rates; Data Stream 2 for Full HD at 148.5MHz ASI mode ($\overline{656\_BYPASS}$ = LOW and ASI = HIGH): Not defined Data-Through mode ($\overline{656\_BYPASS}$ = LOW and ASI = LOW): Data output
			10-bit mode 20BIT/$\overline{10BIT}$ = LOW	Forced LOW
G3	RECLK_EN	Input	CONTROL SIGNAL INPUT Signal levels are LVCMOS/LVTTL compatible. When this pin is LOW, the serial digital output is the buffered version of the input serial data. When this pin is HIGH, the serial digital output is the reclocked version of the input serial data.	

Table 1-1: Pin Descriptions (Continued)

Pin Number	Name	Type	Description
G7	$\overline{656\_BYPASS}$	Input/Output	CONTROL SIGNAL INPUT/OUTPUT Signal levels are LVCMOS/LVTTL compatible. Indicates the presence or valid video data. When the AUTO/$\overline{MAN}$ bit in the host interface register is HIGH (Default), this pin is an OUTPUT. $\overline{656\_BYPASS}$ is HIGH when the device locks to a ITU-R BT.656 or BT.1120 compliant input. $\overline{656\_BYPASS}$ is LOW under all other conditions. When the AUTO/$\overline{MAN}$ bit in the host interface register is LOW, this pin is an INPUT. No video data descrambling takes place, and none of the video processing features of the device are available when $\overline{656\_BYPASS}$ is set LOW. When $\overline{656\_BYPASS}$ is set HIGH, the device carries out descrambling and video processing. When $\overline{656\_BYPASS}$ and ASI are both set LOW, the device operates in Data-Through mode.
G8	ASI	Input/Output	CONTROL SIGNAL INPUT Signal Levels are LVCMOS/LVTTL compatible. Used to enable/disable ASI data extraction in manual mode. When the AUTO/$\overline{MAN}$ bit in the host interface is LOW, this pin is an input, and when the ASI pin is set HIGH the device carries out ASI data extraction and processing. The $\overline{656\_BYPASS}$ pin must be set LOW. When $\overline{656\_BYPASS}$ and ASI are both set LOW, the device operates in Data-Through mode. When the AUTO/$\overline{MAN}$ bit in the host interface is HIGH (Default), ASI input is not supported.
H1	BUFF_VDD	Input Power	POWER pin for the serial digital output 50Ω buffer. Connect to 3.3V DC analog.
H2	BUFF_GND	Input Power	GND pin for the cable driver buffer. Connect to analog GND.
H3	AUDIO_EN	Input	CONTROL SIGNAL INPUT Signal levels are LVCMOS/LVTTL compatible. Enables or disables audio extraction.
H4	WCLK	Output	48kHz word clock for Audio.
H5	861_EN	Input	CONTROL SIGNAL INPUT Signal levels are LVCMOS/LVTTL compatible. Used to select CEA-861 timing mode. When 861_EN is HIGH, the device outputs CEA-861 timing signals (HSYNC/VSYNC/DE) instead of H:V:F digital timing signals.
H6	XTAL_OUT	Digital Output	Buffered 27MHz crystal output. Can be used to cascade the crystal signal.

Table 1-1: Pin Descriptions (Continued)

Pin Number	Name	Type	Description
H7	20BIT/$\overline{10BIT}$	Input	CONTROL SIGNAL INPUT Levels are LVCMOS/LVTTL compatible. Used to select the output bus width. HIGH = 20-bit LOW = 10-bit
H8	PROC_EN	Input	CONTROL SIGNAL INPUT Levels are LVCMOS/LVTTL compatible. Used to enable or disable audio and video processing features. When PROC_EN is HIGH, the audio and video processing features of the device are enabled. When PROC_EN is LOW, the processing features of the device are disabled, and the device is in a low-latency operating mode.
J1, K1	SDO, $\overline{SDO}$	Output	Serial Data Output Signal. 50Ω CML buffer for interfacing to an external cable driver. Serial digital output signal operating at 2.97Gb/s, 2.97/1.001Gb/s, 1.485Gb/s, 1.485/1.001Gb/s and 270Mb/s.
J2	SDO_EN	Input	CONTROL SIGNAL INPUT Signal levels are LVCMOS/LVTTL compatible. Used to enable/disable the serial digital output stage. When SDO_EN is LOW, the serial digital output signals, SDO and $\overline{SDO}$, are both pulled HIGH. When SDO_EN is HIGH, the serial digital output signals, SDO and $\overline{SDO}$, are enabled.
J3	AOUT1/2	Output	Serial Audio Output; Channels 1 and 2.
J4	ACLK	Output	64fs sample clock for audio.
J5	AOUT5/6	Output	Serial Audio Output; Channels 5 and 6.
J6, K6	XTAL2, XTAL1	Analog Input	Input connection for 27MHz crystal.
K2	STANDBY	Input	CONTROL SIGNAL INPUT Signal levels are LVCMOS/LVTTL compatible. When this pin is set HIGH, the device is placed in a power-saving mode. No data processing occurs, and the digital I/Os are powered down. In this mode, the serial digital output signals, SDO and $\overline{SDO}$, are both pulled HIGH.
K3	AOUT3/4	Output	Serial Audio Output; Channels 3 and 4.
K4	MCLK	Output	Oversampled master clock for audio (128fs, 256fs, 512fs selectable).
K5	AOUT7/8	Output	Serial Audio Output; Channels 7 and 8.

2. Electrical Characteristics

2.1 Absolute Maximum Ratings

Table 2-1: Absolute Maximum Ratings

Parameter	Value/Units
Supply Voltage, Digital Core (CORE_VDD)	-0.3V to +1.5V
Supply Voltage, Digital I/O (IO_VDD)	-0.3V to +4.0V
Supply Voltage, Analog 1.2V (PD_VDD, VCO_VDD)	-0.3V to +1.5V
Supply Voltage, Analog 3.3V (SDI_VDD, BUFF_VDD, AVDD)	-0.3V to +4.0V
Input Voltage Range (SDI, $\overline{SDI}$, TERM, LB_CONT)	-0.3V to (SDI_VDD + 0.3)V
Input Voltage Range (VBG)	-0.3V to (AVDD + 0.3)V
Input Voltage Range (LF)	-0.3V to (PLL_VDD + 0.3)V
Input Voltage Range (digital inputs)	-2.0V to +5.25V
Ambient Operating Temperature (T_A)	$-40°C \leq T_A \leq 95°C$
Storage Temperature (T_{STG})	$-40°C \leq T_{STG} \leq 125°C$
Peak Reflow Temperature (JEDEC J-STD-020C)	260°C
ESD Sensitivity, HBM (JESD22-A114)	2kV

Note:

1. Absolute Maximum Ratings are those values beyond which damage may occur. Functional operation under these conditions or at any other condition beyond those indicated in the AC/DC Electrical Characteristics sections is not implied.

2.2 Recommended Operating Conditions

Table 2-2: Recommended Operating Conditions

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Notes
Operating Temperature Range, Ambient	T_A	–	-20	–	85	°C	–
Supply Voltage, Digital Core	CORE_VDD	–	1.14	1.2	1.26	V	–
Supply Voltage, Digital I/O	IO_VDD	1.8V mode	1.71	1.8	1.89	V	–
		3.3V mode	3.13	3.3	3.47	V	–
Supply Voltage, PLL	PLL_VDD	–	1.14	1.2	1.26	V	–

Table 2-2: Recommended Operating Conditions (Continued)

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Notes
Supply Voltage, VCO	VCO_VDD	–	–	0.7	–	V	1
Supply Voltage, Analog	AVDD	–	3.13	3.3	3.47	V	2
Supply Voltage, Serial Digital Input	SDI_VDD	–	3.13	3.3	3.47	V	2
Supply Voltage, CD Buffer	BUFF_VDD	–	3.13	3.3	3.47	V	2

Notes:

1. This is 0.7V rather than 1.2V because there is a voltage drop across an external 105Ω resistor.
2. The 3.3V supplies must track the 3.3V supply of an external EQ and external CD.

2.3 DC Electrical Characteristics

Table 2-3: DC Electrical Characteristics

Guaranteed over recommended operating conditions unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Notes
System							
+1.2V Supply Current	I_{1V2}	10-bit Full HD	–	220	265	mA	–
		20-bit Full HD	–	215	265	mA	–
		10/20-bit HD	–	175	215	mA	–
		10/20-bit SD	–	145	180	mA	–
		ASI	–	135	165	mA	–
+1.8V Supply Current	I_{1V8}	10-bit Full HD	–	32	34	mA	–
		20-bit Full HD	–	32	34	mA	–
		10/20-bit HD	–	20	21	mA	–
		10/20-bit SD	–	6	7	mA	–
		ASI	–	6	7	mA	–
+3.3V Supply Current	I_{3V3}	10-bit Full HD	–	95	105	mA	–
		20-bit Full HD	–	95	105	mA	–
		10/20-bit HD	–	65	75	mA	–
		10/20-bit SD	–	35	45	mA	–
		ASI	–	35	45	mA	–

Table 2-3: DC Electrical Characteristics (Continued)

Guaranteed over recommended operating conditions unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Notes
Total Device Power (IO_VDD = 1.8V)	P_{1D8}	10-bit Full HD	–	380	470	mW	–
		20-bit Full HD	–	350	435	mW	–
		10/20-bit HD	–	300	360	mW	–
		10/20-bit SD	–	235	305	mW	–
		ASI	–	235	305	mW	–
		Reset	–	200	–	mW	–
		Standby	–	16	44	mW	–
Total Device Power (IO_VDD = 3.3V)	P_{3D3}	10-bit Full HD	–	580	700	mW	–
		20-bit Full HD	–	580	695	mW	–
		10/20-bit HD	–	430	530	mW	–
		10/20-bit SD	–	290	370	mW	–
		ASI	–	290	370	mW	–
		Reset	–	220	–	mW	–
		Standby	–	16	44	mW	–
Digital I/O							
Input Logic LOW	V_{IL}	3.3V or 1.8V operation	IO_VDD + 0.3	–	0.3 x IO_VDD	V	–
Input Logic HIGH	V_{IH}	3.3V or 1.8V operation	0.7 x IO_VDD	–	IO_GND - 0.3	V	–
Output Logic LOW	V_{OL}	I_{OL} = 5mA, 1.8V operation	–	–	0.2	V	–
		I_{OL} = 8mA, 3.3V operation	–	–	0.4	V	–
Output Logic HIGH	V_{OH}	I_{OH} = 5mA, 1.8V operation	1.4	–	–	V	–
		I_{OH} = 8mA, 3.3V operation	2.4	–	–	V	–
Output Drive Strength	–	–	–	–	–	–	1
Serial Input							
Serial Input Common Mode Voltage	–	75Ω load	–	(SDI_VDD) x 5 / 6	–	V	–
Serial Output							
Serial Output Common Mode Voltage	–	50Ω load	BUFF_VDD - (0.6 / 2)	BUFF_VDD - (0.45 / 2)	BUFF_VDD - (0.35 / 2)	V	–

Note:

1. The output drive strength of the digital outputs can be programmed through the host interface. Please see Table 4-34: Video Core Configuration and Status Registers, register 06Dh for details.

2.4 AC Electrical Characteristics

Table 2-4: AC Electrical Characteristics

Guaranteed over recommended operating conditions unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Notes
System							
Reset Pulse Width	t_{reset}	–	1	–	–	ms	–
Device Latency							
Full HD (Audio Enabled)	–	PCLK = 148.5MHz	79	–	83	PCLK	1
HD (Audio Enabled)	–	PCLK = 74.25MHz	79	–	83	PCLK	1
SD (Audio Enabled)	–	PCLK = 27MHz	50	–	59	PCLK	1
Full HD (Audio Disabled)	–	PCLK = 148.5MHz	44	–	48	PCLK	2
HD (Audio Disabled)	–	PCLK = 74.25MHz	44	–	48	PCLK	2
SD (Audio Disabled)	–	PCLK = 27MHz	44	–	53	PCLK	2
ASI Mode	–	PCLK = 27MHz	12	–	16	PCLK	3
Parallel Output							
Parallel Clock Frequency	f_{PCLK}	–	13.5	–	148.5	MHz	–
Parallel Clock Duty Cycle	DC_{PCLK}	–	40	–	60	%	–

Table 2-4: AC Electrical Characteristics (Continued)

Guaranteed over recommended operating conditions unless otherwise noted.

Parameter	Symbol	Conditions		Min	Typ	Max	Units	Notes
Output Data Hold Time (1.8V)	t_{oh}	Full HD 10-bit	SPI	1.5	–	–	ns	4
			Audio Outputs	1.5	–	–	ns	4
			Video Data Bus	0.4	–	–	ns	4
			STAT Pins	0.45	–	–	ns	4
		Full HD 20-bit	Video Data Bus	1.0	–	–	ns	4
			STAT Pins	1.0	–	–	ns	4
		HD 10-bit	Video Data Bus	1.0	–	–	ns	4
			STAT Pins	1.0	–	–	ns	4
		HD 20-bit	Video Data Bus	1.0	–	–	ns	4
			STAT Pins	1.0	–	–	ns	4
		SD 10-bit	Video Data Bus	19.4	–	–	ns	4
			STAT Pins	19.4	–	–	ns	4
		SD 20-bit	Video Data Bus	38.0	–	–	ns	4
			STAT Pins	38.0	–	–	ns	4

Table 2-4: AC Electrical Characteristics (Continued)

Guaranteed over recommended operating conditions unless otherwise noted.

Parameter	Symbol	Conditions		Min	Typ	Max	Units	Notes
Output Data Hold Time (3.3V)	t_{oh}	Full HD 10-bit	SPI	1.5	–	–	ns	5
			Audio Outputs	1.5	–	–	ns	5
			Video Data Bus	0.45	–	–	ns	5
			STAT Pins	0.45	–	–	ns	5
		Full HD 20-bit	Video Data Bus	1.0	–	–	ns	5
			STAT Pins	1.0	–	–	ns	5
		HD 10-bit	Video Data Bus	1.0	–	–	ns	5
			STAT Pins	1.0	–	–	ns	5
		HD 20-bit	Video Data Bus	1.0	–	–	ns	5
			STAT Pins	1.0	–	–	ns	5
		SD 10-bit	Video Data Bus	19.4	–	–	ns	5
			STAT Pins	19.4	–	–	ns	5
		SD 20-bit	Video Data Bus	38.0	–	–	ns	5
			STAT Pins	38.0	–	–	ns	5

Table 2-4: AC Electrical Characteristics (Continued)

Guaranteed over recommended operating conditions unless otherwise noted.

Parameter	Symbol	Conditions		Min	Typ	Max	Units	Notes
Output Data Delay Time (1.8V)	t_{od}	Full HD 10-bit	SPI	–	–	14.0	ns	6
			Audio Outputs	–	–	7.0	ns	6
			Video Data Bus	–	–	1.8	ns	6
			STAT Pins	–	–	2.5	ns	6
		Full HD 20-bit	Video Data Bus	–	–	3.7	ns	6
			STAT Pins	–	–	4.4	ns	6
		HD 10-bit	Video Data Bus	–	–	3.7	ns	6
			STAT Pins	–	–	4.4	ns	6
		HD 20-bit	Video Data Bus	–	–	3.7	ns	6
			STAT Pins	–	–	4.4	ns	6
		SD 10-bit	Video Data Bus	–	–	22.2	ns	6
			STAT Pins	–	–	22.2	ns	6
		SD 20-bit	Video Data Bus	–	–	41.0	ns	6
			STAT Pins	–	–	41.0	ns	6

Table 2-4: AC Electrical Characteristics (Continued)

Guaranteed over recommended operating conditions unless otherwise noted.

Parameter	Symbol	Conditions		Min	Typ	Max	Units	Notes
Output Data Delay Time (3.3V)	t_{od}	Full HD 10-bit	SPI	–	–	14.0	ns	7
			Audio Outputs	–	–	7.0	ns	7
			Video Data Bus	–	–	1.9	ns	7
			STAT Pins	–	–	2.2	ns	7
		Full HD 20-bit	Video Data Bus	–	–	3.7	ns	7
			STAT Pins	–	–	4.1	ns	7
		HD 10-bit	Video Data Bus	–	–	3.7	ns	7
			STAT Pins	–	–	4.1	ns	7
		HD 20-bit	Video Data Bus	–	–	3.7	ns	7
			STAT Pins	–	–	4.1	ns	7
		SD 10-bit	Video Data Bus	–	–	22.2	ns	7
			STAT Pins	–	–	22.2	ns	7
		SD 20-bit	Video Data Bus	–	–	41.0	ns	7
			STAT Pins	–	–	41.0	ns	7

Table 2-4: AC Electrical Characteristics (Continued)

Guaranteed over recommended operating conditions unless otherwise noted.

Parameter	Symbol	Conditions		Min	Typ	Max	Units	Notes
Output Data Rise/Fall Time (1.8V)	t_r/t_f	Full HD 10-bit 6pF load	Video Data Bus	0.4	–	–	ns	4
			STAT Pins	0.3	–	–	ns	4
			Audio Outputs	0.6	–	–	ns	4
		All other modes 6pF load	Video Data Bus	0.4	–	–	ns	4
			STAT Pins	0.4	–	–	ns	4
			Audio Outputs	0.6	–	–	ns	4
		Full HD 10-bit 15pF load	Video Data Bus	–	–	1.5	ns	6
			STAT Pins	–	–	1.1	ns	6
			Audio Outputs	–	–	2.3	ns	6
		All other modes 15pF load	Video Data Bus	–	–	1.5	ns	6
			STAT Pins	–	–	1.4	ns	6
			Audio Outputs	–	–	2.3	ns	6
Output Data Rise/Fall Time (3.3V)	t_r/t_f	Full HD 10-bit 6pF load	Video Data Bus	0.5	–	–	ns	5
			STAT Pins	0.4	–	–	ns	5
			Audio Outputs	0.6	–	–	ns	5
		All other modes 6pF load	Video Data Bus	0.5	–	–	ns	5
			STAT Pins	0.4	–	–	ns	5
			Audio Outputs	0.6	–	–	ns	5

Table 2-4: AC Electrical Characteristics (Continued)

Guaranteed over recommended operating conditions unless otherwise noted.

Parameter	Symbol	Conditions		Min	Typ	Max	Units	Notes
Output Data Rise/Fall Time (3.3V)	t_r/t_f	Full HD 10-bit 15pF load	Video Data Bus	–	–	1.6	ns	7
			STAT Pins	–	–	1.5	ns	7
			Audio Outputs	–	–	2.2	ns	7
		All other modes 15pF load	Video Data Bus	–	–	1.6	ns	7
			STAT Pins	–	–	1.4	ns	7
			Audio Outputs	–	–	2.2	ns	7
Serial Digital Input								
Serial Input Data Rate	DR_{SDI}	–		0.27	–	2.97	Gb/s	–
Serial Input Swing	ΔV_{SDI}	Differential with 100Ω load		500	800	1100	mVp-p	–
Serial Input Jitter Tolerance	IJT	Nominal loop bandwidth	Square wave mod.	0.7	0.8	–	UI	–
Serial Digital Output								
Serial Output Data Rate	DR_{SDO}	–		0.27	–	2.97	Gb/s	–
Serial Output Swing	ΔV_{SDO}	Differential with 100Ω load		350	–	600	mVp-p	–
Serial Output Rise Time 20% ~ 80%	tr_{SDO}	–		–	–	180	ps	–
Serial Output Fall Time 20% ~ 80%	tf_{SDO}	–		–	–	180	ps	–
Serial Output Intrinsic Jitter	t_{OJ}	Full HD colour bar signal		–	–	100	ps	–
		HD colour bar signal		–	–	100	ps	–
		SD colour bar signal		–	–	400	ps	–
Serial Output Duty Cycle Distortion	DCD_{SDD}	Full HD		–	10	–	ps	–
		HD		–	10	–	ps	–
		SD		–	20	–	ps	–
Synchronous lock time	–	–		–	–	25	µs	–
Asynchronous lock time	–	–		100	–	825	µs	–

Table 2-4: AC Electrical Characteristics (Continued)

Guaranteed over recommended operating conditions unless otherwise noted.

Parameter	Symbol	Conditions	Min	Typ	Max	Units	Notes
Lock time from standby de-asserted	–	–	–	–	10	ms	–
Lock time from power-up	–	–	–	–	100	ms	–
	–	After 20 minutes at -20°C	–	325		ms	–
GSPI							
GSPI Input Clock Frequency	f_{SCLK}	50% levels 3.3V or 1.8V operation	–	–	60	MHz	8
GSPI Input Clock Duty Cycle	DC_{SCLK}		40	50	60	%	8
GSPI Input Data Setup Time	–		1.5	–	–	ns	8
GSPI Input Data Hold Time	–		1.5	–	–	ns	8
GSPI Output Data Hold Time	–	–	1.5	–	–	ns	8
$\overline{CS}$ low before SCLK rising edge	t_0	50% levels 3.3V or 1.8V operation	1.5	–	–	ns	8
Time between end of command word (or data in Auto-Increment mode) and the first SCLK of the following data word - write cycle	t_4	50% levels 3.3V or 1.8V operation	37.1	–	–	ns	8
Time between end of command word (or data in Auto-Increment mode) and the first SCLK of the following data word - read cycle	t_5	50% levels 3.3V or 1.8V operation	148.4	–	–	ns	8
$\overline{CS}$ high after SCLK rising edge	t_7	50% levels 3.3V or 1.8V operation	37.1	–	–	ns	8

Notes:

1. $\overline{656\_BYPASS}$ = 1, PROC_EN = 1, AUDIO_EN = 1, ASI = 0
2. $\overline{656\_BYPASS}$ = 1, PROC_EN = 1, AUDIO_EN = 0, ASI = 0
3. ASI = 1
4. 1.89V and 0°C.
5. 3.47V and 0°C.
6. 1.71V and 125°C
7. 3.13V and 125°C
8. For GSPI timing parameters, refer to Figure 4-62 and Figure 4-63 in Section 4.18.3, as appropriate.

3. Input/Output Circuits

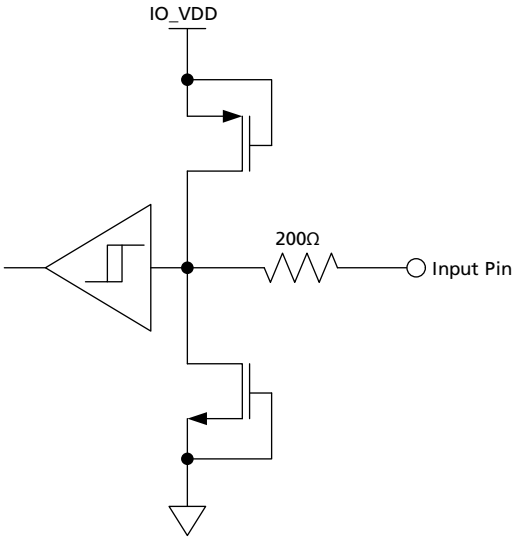


Figure 3-1: Digital Input Pin with Schmitt Trigger (20BIT/$\overline{10BIT}$, AUDIO_EN, $\overline{CS}$_TMS, PROC_EN, JTAG_EN, RECLK_EN, $\overline{RESET}$, SCLK_TCK, SDIN_TDI, SDO_EN, STANDBY, 861_EN)

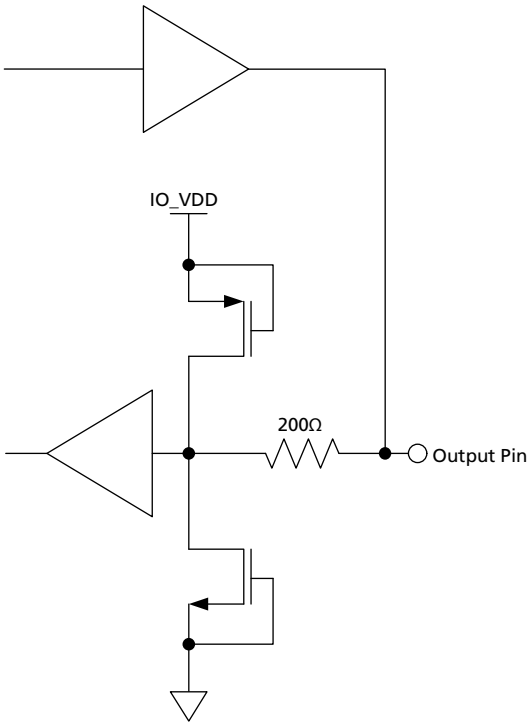


Figure 3-2: Bidirectional Digital Input/Output Pin - Configured to Output unless in $\overline{Reset}$ Mode. (ACLK, MCLK, AOUT1/2, AOUT3/4, AOUT5/6, AOUT7/8, ASI, $\overline{656\_BYPASS}$, WCLK)

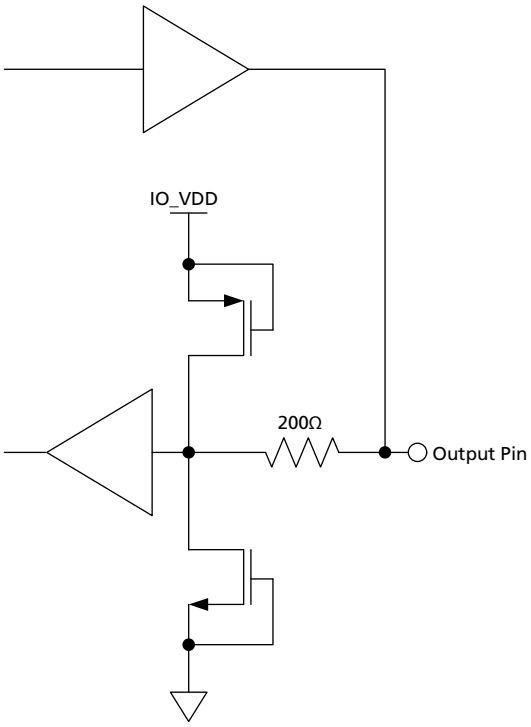


Figure 3-3: Bidirectional Digital Input/Output Pin with programmable drive strength.

These pins in Figure 3-3 are configured to output unless in Reset Mode; in which case they are high-impedance. The drive strength can be set by writing to address 06Dh in the host interface register. (DOUT0, DOUT1, DOUT2, DOUT3, DOUT4, DOUT5, DOUT6, DOUT7, DOUT8, DOUT9, SDOUT_TDO, STAT0, STAT1, STAT2, STAT3, STAT4, STAT5, XTAL_OUT, DOUT10, DOUT11, DOUT12, DOUT13, DOUT14, DOUT15, DOUT16, DOUT17, DOUT18, DOUT19, PCLK)

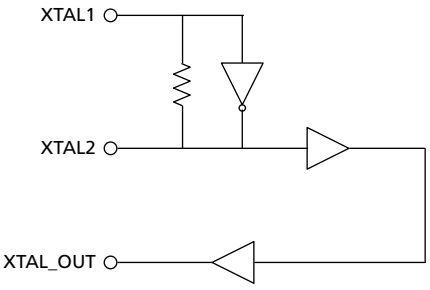


Figure 3-4: XTAL1/XTAL2/XTAL_OUT

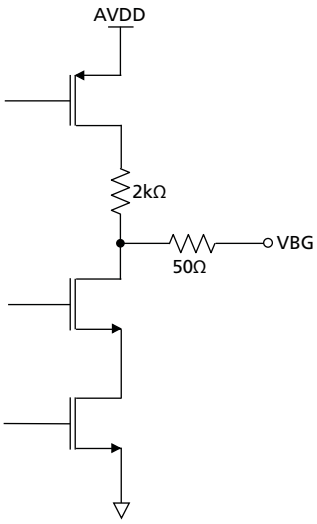


Figure 3-5: VBG

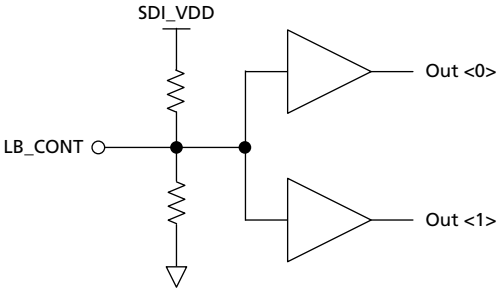


Figure 3-6: LB_CONT

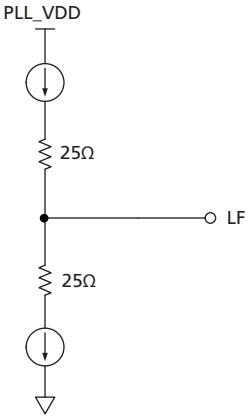


Figure 3-7: Loop Filter (LF)

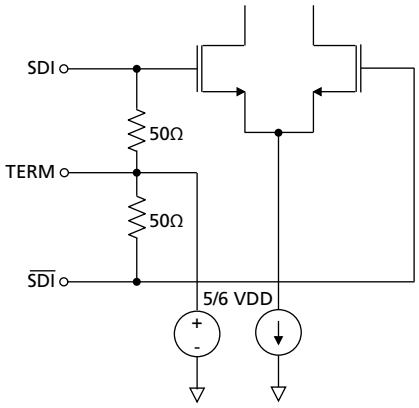


Figure 3-8: SDI/$\overline{\text{SDI}}$ and TERM

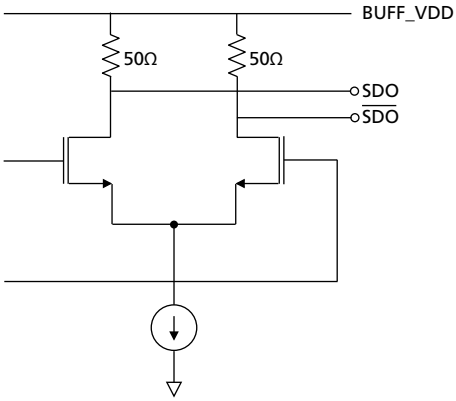


Figure 3-9: SDO/$\overline{\text{SDO}}$

4. Detailed Description

4.1 Functional Overview

The GV7605 is a multi-rate, multi-standard Aviia receiver with an integrated audio de-embedder. When used in conjunction with Semtech's GV8501, a complete Aviia receive solution that supports full bandwidth 1080p video at 50/60Hz can be realized.

The GV7605 includes an integrated reclocker, serial data loop through output, robust serial-to-parallel conversion and additional processing functions such as audio extraction, ancillary data extraction, and ASI decoding.

The device supports four distinct modes of operation that can be set through external device pins or by programming internal registers through the host interface; Video mode, Data-Through mode, ASI mode and Standby mode.

In Video mode, all video processing features, ancillary data extraction, and audio de-embedding features are enabled by default.

In ASI mode, the GV7605 carries out 8b/10b decoding and outputs IEC 13818-1 compliant stream data.

In Data-Through mode, the device operates as a simple serial to parallel converter. No additional processing features are enabled.

Standby mode is the low power consumption mode of the device. In this mode, the internal reclocker unlocks, and the internal configuration registers are not accessible through the host interface.

The GV7605 includes a JTAG interface for boundary scan testing.

4.2 Serial Digital Input

The GV7605 can accept serial digital inputs compliant with ITU-R BT.656, and BT.1120. The serial digital input buffer features 50Ω input termination and may be DC-coupled to Semtech's GV8501 cable equalizer.

4.3 Serial Digital Output

The GV7605 contains a 100Ω differential serial output buffer which can be configured to output either a retimed or a buffered version of the serial digital input. The SDO and $\overline{\text{SDO}}$ outputs of this buffer can interface directly to GV8500 cable driver.

When the RECLK_EN pin is set HIGH, the serial digital output is the re-timed version of the serial input.

When the RECLK_EN pin is set LOW, the serial digital output is simply the buffered version of the serial input, bypassing the internal reclocker.

The output may be disabled by setting the SDO_EN pin LOW. The output is also disabled when STANDBY pin is asserted HIGH. When disabled, both SDO and $\overline{\text{SDO}}$ pins go to VDD and remain static.

The SDO output is muted when RECLK_EN pin is set HIGH and the PLL is unlocked (LOCKED pin is LOW). When muted, the output is held static in 0 or 1.

Table 4-1: Serial Digital Output

SDO_EN	RECLK_EN	SDO/$\overline{\text{SDO}}$
0	X	Disabled
1	1	Re-timed
1	0	Buffered (not re-timed)

Note: The serial digital output is muted when the GV7605 is unlocked.

4.4 Serial Digital Reclocker

The GV7605 includes both a PLL stage and a sampling stage.

The PLL is comprised of two distinct loops:

- A coarse frequency acquisition loop sets the centre frequency of the integrated Voltage Controlled Oscillator (VCO) using an external 27MHz reference clock
- A fine frequency and phase locked loop aligns the VCO's phase and frequency to the input serial digital stream

The frequency lock loop results in very fast lock time.

The sampling stage re-times the serial digital input with the locked VCO clock. This generates a clean serial digital stream, which may be output on the SDO/$\overline{\text{SDO}}$ output pins and converted to parallel data for further processing.

4.4.1 Reclocker PLL Loop Bandwidth

The fine frequency and phase lock loop in the GV7605 reclocker is non-linear. The PLL loop bandwidth scales with the jitter amplitude of the input data stream; automatically reduces bandwidth in response to higher jitter. This allows the PLL to reject more of the jitter in the input data stream and produce a very clean reclocked output.

The loop bandwidth of the GV7605 PLL is defined with 0.2UI input jitter. The bandwidth is controlled through the LB_CONT pin of the device. Under nominal conditions, with the LB_CONT pin floating and 0.2UI input jitter applied, the loop bandwidth is set to 1/1000 of the frequency of the input data stream. Connecting the LB_CONT pin to 3.3V reduces the bandwidth to half of the nominal setting. Connecting the LB_CONT pin to GND increases the bandwidth to double the nominal setting. Table 4-2 below summarizes this information.

Table 4-2: PLL Loop Bandwidth

Input Data Rate	LB_CONT Pin Connection	Loop Bandwidth (MHz)[1]
SD	3.3V	0.135
	Floating	0.27
	0V	0.54
HD	3.3V	0.75
	Floating	1.5
	0V	3.0
Full HD	3.3V	1.5
	Floating	3.0
	0V	6.0

[1]Measured with 0.2UI input jitter applied

4.5 External Crystal/Reference Clock

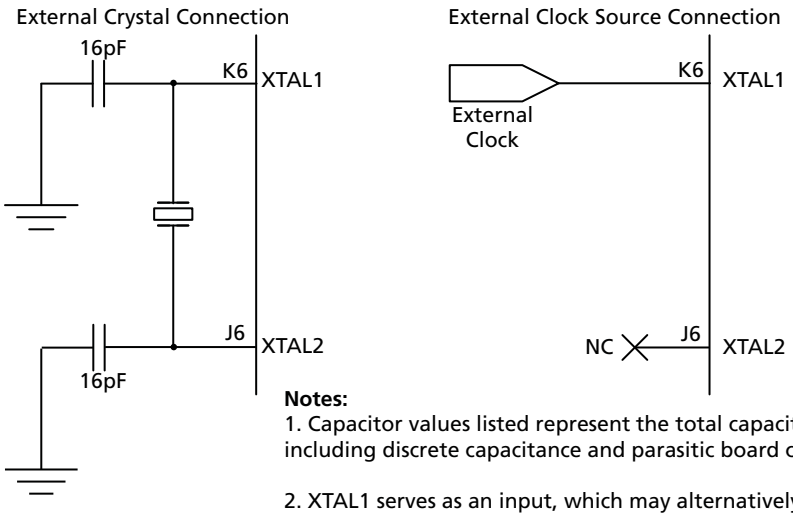
The GV7605 requires an external 27MHz reference clock for correct operation. This reference clock is generated by connecting a crystal to the XTAL1 and XTAL2 pins of the device.

Alternately, a 27MHz external clock source can be connected to the XTAL1 pin of the device, as shown in Figure 4-1.

The frequency variation of the crystal including aging, supply and temperature variation, should be less than +/-100ppm.

The equivalent series resistance (or motional resistance) should be a maximum of 50Ω.

The external crystal is used in the frequency acquisition process. It has no impact on the output jitter performance of the part when the part is locked to incoming data. Because of this, the only key parameter is the frequency variation of the crystal that is stated above.



Notes:
1. Capacitor values listed represent the total capacitance, including discrete capacitance and parasitic board capacitance.

2. XTAL1 serves as an input, which may alternatively accept a 27MHz clock source.

Figure 4-1: 27MHz Clock Sources

Table 4-3: Input Clock Requirements

Parameter	Min	Typ	Max	Units	Notes
XTAL1 Low Level Input Voltage (V_{il})	–	–	20% of VDD_IO	V	1
XTAL1 High Level Input Voltage (V_{ih})	80% of VDDIO	–	–	V	1
XTAL1 Input Slew Rate	2	–	–	V/ns	1
XTAL1 to XOUT Prop. Delay (High to Low)	1.3	1.5	2.3	ns	1
XTAL1 to XOUT Prop. Delay (Low to High)	1.3	1.6	2.3	ns	1

1. Valid when the cell is used to buffer an external clock source which is connected to the XTAL1 pin, then nothing should be connected to the XTAL2 pin.

4.6 Lock Detect

The LOCKED output signal is available by default on the STAT3 output pin, but may be programmed to be output through any one of the six programmable multi-functional pins of the device; STAT[5:0].

The LOCKED output signal sets HIGH by the Lock Detect block under the following conditions:

Table 4-4: Lock Detect Conditions

Mode of Operation	Mode Setting	Condition for Locked
Data-Through Mode	$\overline{656\_BYPASS}$ = LOW ASI = LOW	Reclocker PLL is locked.
Video Mode	$\overline{656\_BYPASS}$ = HIGH ASI = LOW	Reclocker PLL is locked 2 consecutive TRS words in 2 lines are detected.
ASI Mode	$\overline{656\_BYPASS}$ = LOW ASI = HIGH AUTO/$\overline{MAN}$ = LOW	Reclocker PLL is locked 32 consecutive ASI words with no errors are detected within a 128-word window.

All other combinations result in the LOCKED signal being LOW.

Note: In Standby mode, the reclocker PLL unlocks. However, the LOCKED signal retains whatever status it previously held. So, if before Standby assertion, the LOCKED signal is HIGH, then during standby, it remains HIGH regardless of the status of the PLL.

4.6.1 Asynchronous Lock

The lock detection algorithm is a continuous process, beginning at device power-up or after a system reset. It continues until the device is powered down or held in reset.

The device first determines if a valid serial digital input signal has been presented to the device. If no valid serial data stream has been detected, the serial data into the device is considered invalid, and the LOCKED signal is LOW.

Once a valid input signal has been detected, the asynchronous lock algorithm enters a "hunt" phase, in which the device attempts to detect the presence of either TRS words or ASI sync words.

By default, the device powers up in auto mode (the AUTO/$\overline{MAN}$ bit in the host interface is set HIGH). In this mode, the device operating frequency toggles between Full HD, HD and SD rates as it attempts to lock to the incoming data rate. The PCLK output continues to operate, and the frequency may switch between 148.5MHz, 74.25MHz, 27MHz and 13.5MHz.

When the device is operating in manual mode (AUTO/$\overline{MAN}$ bit in the host interface is LOW), the operating frequency needs to be set through the host interface using the RATE_DET[1:0] bits. In this mode, the asynchronous lock algorithm does not toggle the operating rate of the device and attempts to lock within a single standard. Lock is achieved within three lines of the selected standard.

4.6.2 Signal Interruption

The device tolerates a signal interruption of up to 10µs as long as no TRS words are deleted by this interruption.

4.7 Video Functionality

4.7.1 Standard Definition Video Output Formats

ITU-R BT.656 (formally CCIR-656) defines an 8-bit or 10-bit parallel interface for transmitting 4:2:2 YCbCr digital video. To reduce the number of wires required for the interface, timing codes are embedded in the video stream to provide information traditionally transmitted by dedicated HSYNC, VSYNC, and BLANK signals. Ancillary digital data such as audio and closed captioning may be transmitted during blanking intervals (see Figure 4-2 and Figure 4-4). Figure 4-3 shows the multiplexed 10-bit 4:2:2 YCbCr data for 525 line video at 60Hz. Figure 4-5 shows the multiplexed 10-bit 4:2:2 YCbCr data for 625 line video at 50Hz. The start of active video and the end of active video are marked by the SAV and EAV codes, respectively. The values of these codes are reserved for this purpose and should not occur elsewhere in the video raster. F, V, H timing information is stored in the 10-bit XYZ word as follows:

- Bit 8 - (F-bit) 0 for field one; and 1 for field two
- Bit 7 - (V-bit) 1 in vertical blanking interval; and 0 during active video lines
- Bit 6 - (H-bit) 1 indicates the EAV sequence; and 0 indicates the SAV sequence

The two LSB's of the XYZ word are set to zero for compatibility with 8-bit systems.

Table 4-5: 525/60Hz Format

Line Number	F	V	H (EAV)	H (SAV)
1-3	1	1	1	0
4-20	0	1	1	0
21-263	0	0	1	0
264-265	0	1	1	0
266-282	1	1	1	0
283-525	1	0	1	0

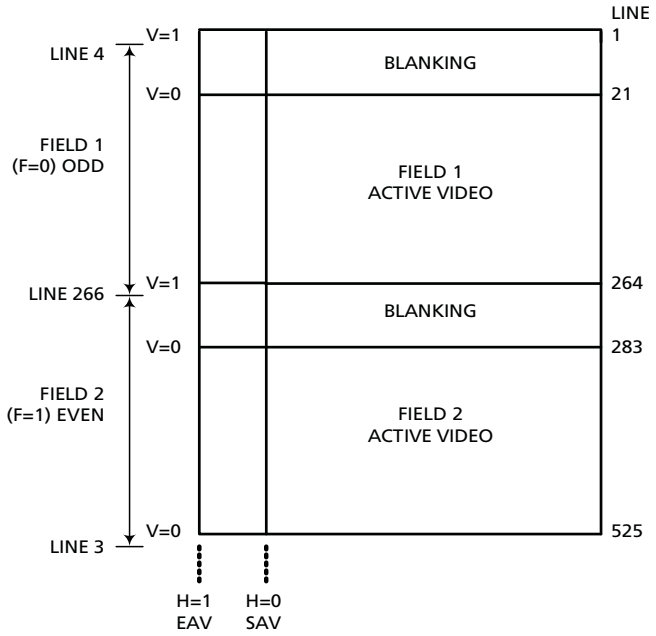


Figure 4-2: Data transmitting with blanking, 525/60Hz

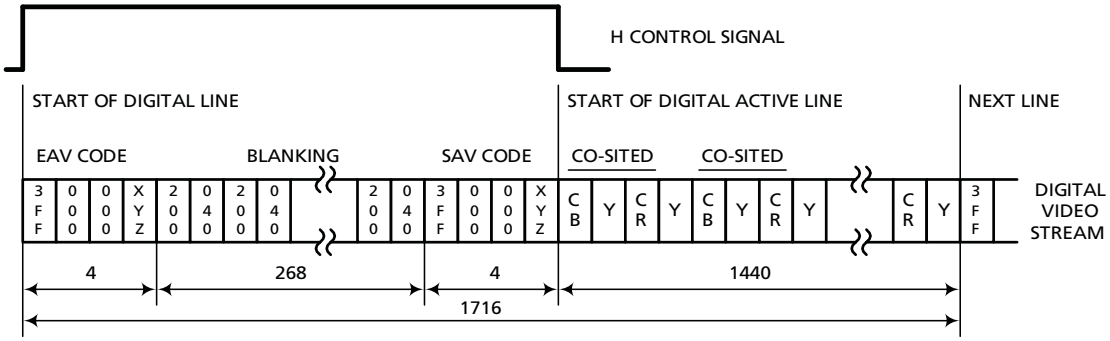


Figure 4-3: Multiplexing 10-bit 4:2:2 YCbCr data for 525 lines at 60Hz

Table 4-6: 625/50Hz Format

Line Number	F	V	H (EAV)	H (SAV)
1-22	0	1	1	0
23-310	0	0	1	0
311-312	0	1	1	0
313-335	1	1	1	0
336-623	1	0	1	0
624-625	1	1	1	0

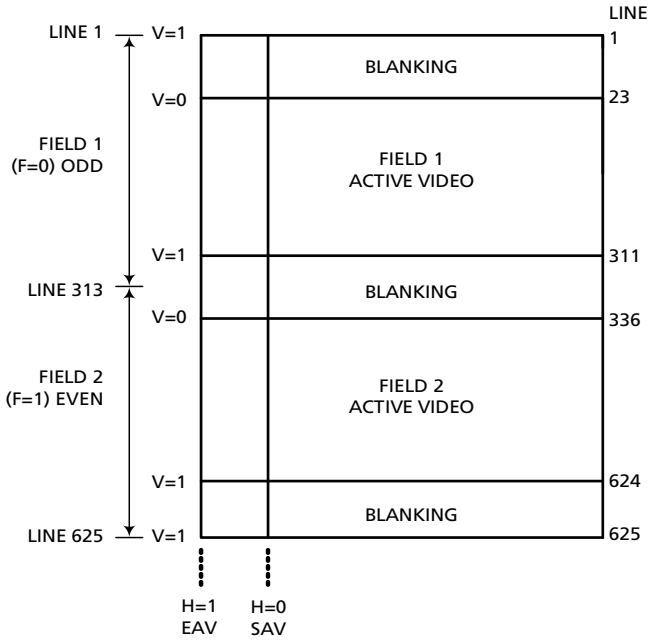


Figure 4-4: Data transmitting with blanking, 625/50Hz

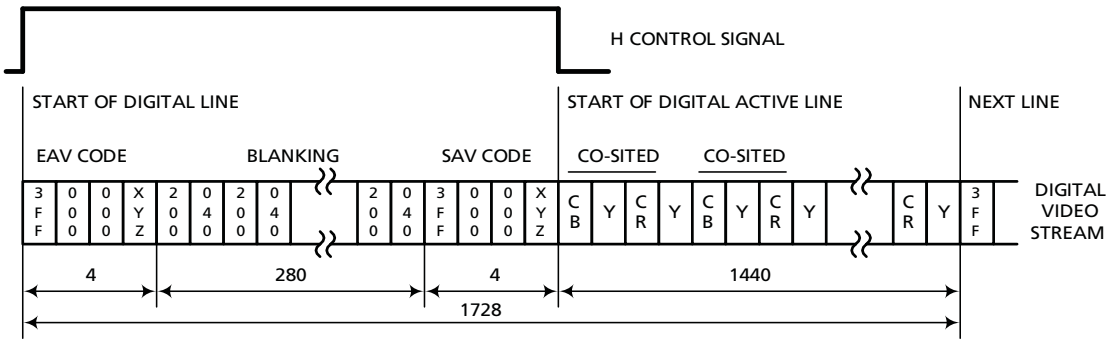


Figure 4-5: Multiplexing 10-bit 4:2:2 YCbCr data for 625 lines at 50Hz

4.7.2 High Definition Video Output Formats

ITU-R BT.1120 describes the serial and parallel format for 1080-line interlaced and progressive digital video. As with ITU-R BT.656, the field/frame blanking period (V), the line blanking period (H), and the field identification (F), are embedded as digital timing codes (TRS) within the video. After deserialization, a single 10-bit bus carrying the C'_B, Y', C'_R, Y', etc. data pattern is demultiplexed into two 10-bit buses. This 20-bit parallel data interface carries 10 bits of Luma data (Y') and 10 bits of colour difference data (C'_B, C'_R), operating at a clock of 74.25MHz or 74.25/1.001 MHz.

The following figures show horizontal and vertical timing for 1080-line interlaced systems.

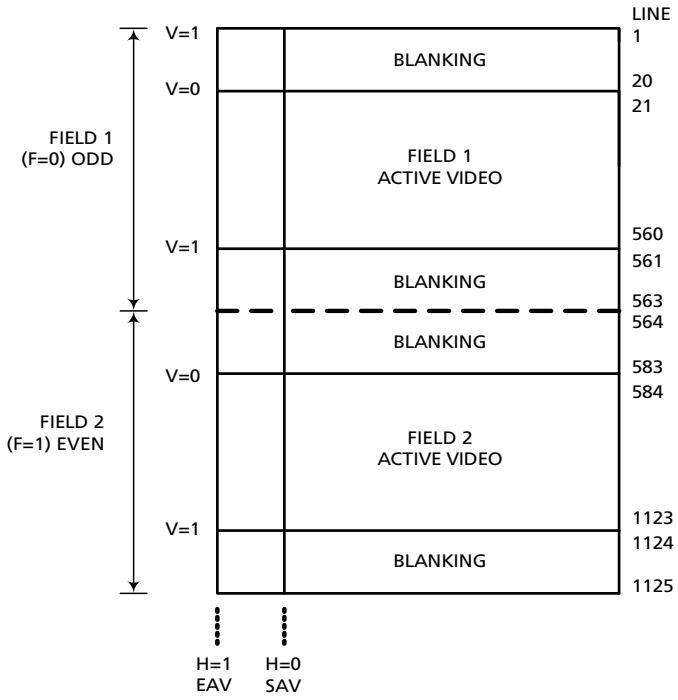


Figure 4-6: Field Timing Relationship for 1080-line Interlaced Systems

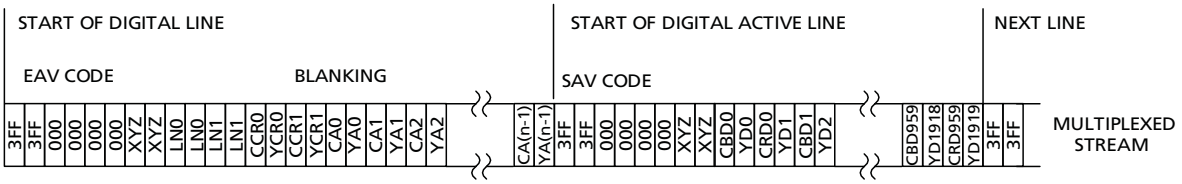


Figure 4-7: Multiplexed Luma and Chroma Over One Video Line - 1080i

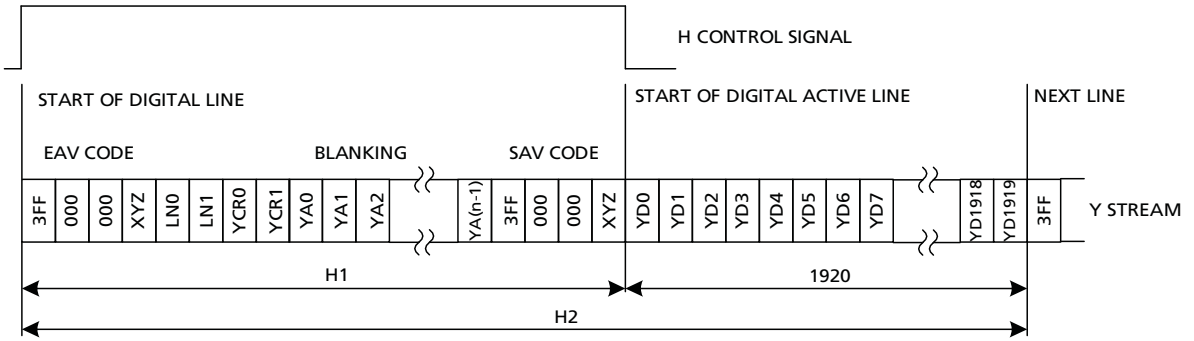


Figure 4-8: Luma Stream Over One Video Line - 1080i

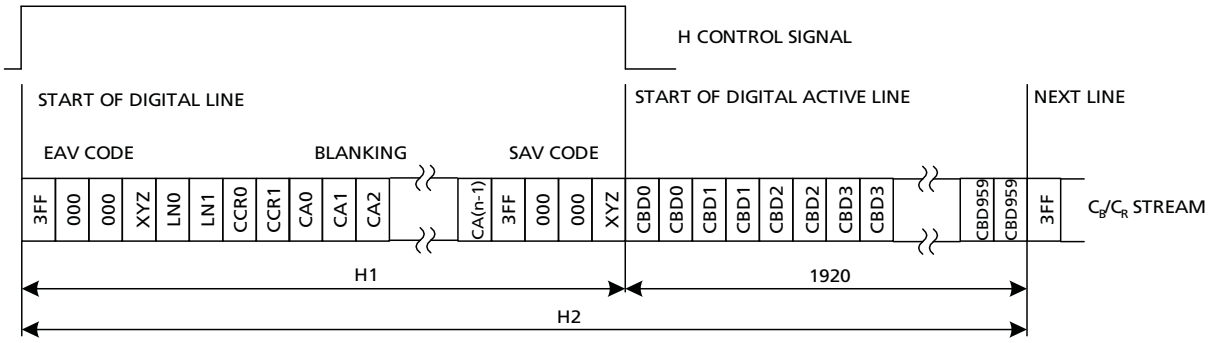


Figure 4-9: Chroma Stream Over One Video Line - 1080i

Table 4-7: 1080-line Interlaced Horizontal Timing

Interlaced	60 or 60/1.001 Hz	50Hz
H1	280	720
H2	2200	2640

4.7.2.1 High Definition 1080p Output Formats

ITU-R BT.1120 also includes progressive scan formats with 1080 active lines, with $Y'C'_BC'_R$ 4:2:2 sampling at pixel rates of 74.25MHz or 74.25/1.001 MHz. The following diagrams show horizontal and vertical timing for 1080-line progressive systems.

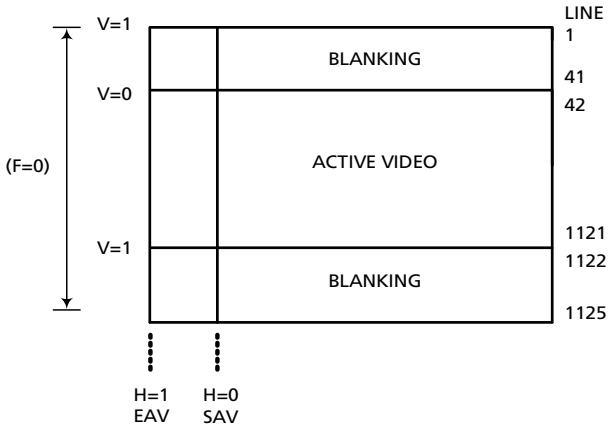


Figure 4-10: Frame Timing Relationship For 1080-line Progressive Systems

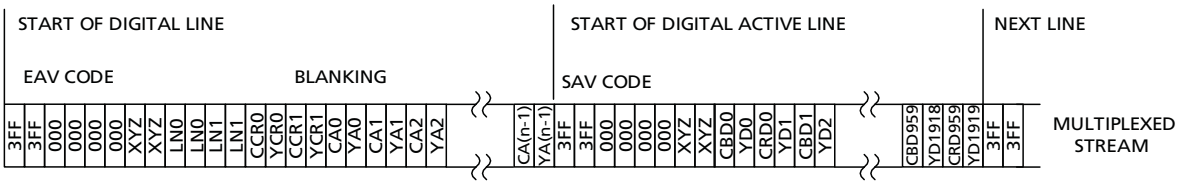


Figure 4-11: Multiplexed Luma and Chroma Over One Video Line - 1080p

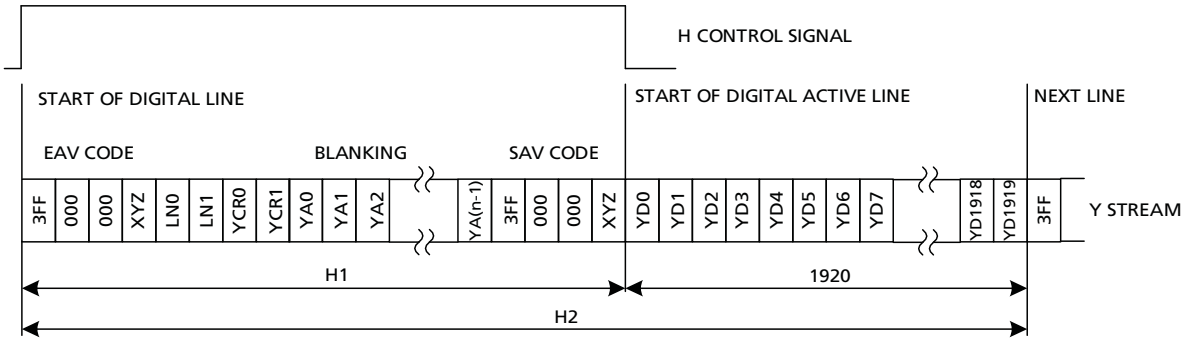


Figure 4-12: Luma Stream Over One Video Line - 1080p

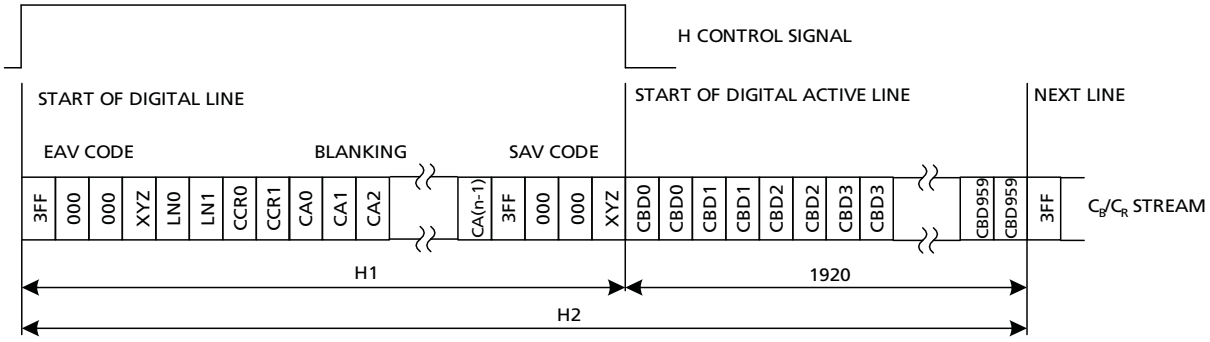


Figure 4-13: Chroma Stream Over One Video Line - 1080p

Table 4-8: 1080-line Progressive Horizontal Timing

Progressive	30 or 30/1.001 Hz	25Hz	24 or 24/1.001 Hz
H1	280	720	830
H2	2200	2640	2750

4.7.2.2 High Definition 720p Output Formats

The Society of Motion Picture and Television Engineers (SMPTE) defines the standard for progressive scan 720-line HD image formats. SMPTE ST 296-2001 specifies the representation for 720p digital $Y'C'_BC'_R$ 4:2:2 signals at pixel rates of 74.25MHz or 74.25/1.001 MHz.

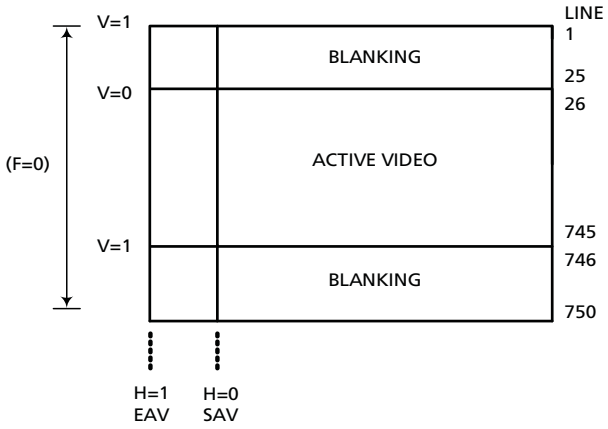


Figure 4-14: 720p Digital Vertical Timing

The frame rate determines the horizontal timing, which is shown in Table 4-9.

Table 4-9: 720p Horizontal Timing

Frame Rate	H = 1 Sample Number	H = 0 Sample Number
24 or 24/1.001	1283	4124
25	1283	3959
30 or 30/1.001	1283	3299
50	1283	1979
60 or 60/1.001	1283	1649

4.7.2.3 Full HD Output Formats

High definition formats that require the Aviia serial data rate to operate at 2.97Gb/s are defined as Full HD formats. These formats are generally 1080-line based, operating at 50 or 60Hz progressive frame rate. However, the sampling structure and bit-depth of HD formats may also increase the payload rate at the digital input of the GV7605. There are also 720-line Full HD formats with 4:4:4 sampling.

The GV7605 can support the progressive scan Full HD formats shown in Table 4-10.

Table 4-10: Full HD 1080-line and 720-line Progressive Image Formats

Active Image Format	Total Pixels x Lines	Sampling Structure	Pixel Depth	Frame Rate (Hz)
1920 x 1080	2640 x 1125	4:2:2 (Y'C'BC'R)	8 or 10-bit	50
	2200 x 1125			60 or 60/1.001
	2750 x 1125	4:4:4 (R'G'B' or Y'C'$_B$C'$_R$)	8 or 10-bit	24 or 24/1.001
	2640 x 1125			25
	2200 x 1125			30 or 30/1.001
	2750 x 1125	4:4:4 (R'G'B' or Y'C'$_B$C'$_R$)	12-bit	24 or 24/1.001
	2640 x 1125			25
	2200 x 1125			30 or 30/1.001
	2750 x 1125	4:2:2 (Y'C'$_B$C'$_R$)	12-bit	24 or 24/1.001
	2640 x 1125			25
	2200 x 1125			30 or 30/1.001
1280 x 720	4125 x 750	4:4:4 (R'G'B' or Y'C'$_B$C'$_R$)	8 or 10-bit	24 or 24/1.001
	3960 x 750			25
	3300 x 750			30 or 30/1.001
	1980 x 750			50
	1650 x 750			60 or 60/1.001

Full HD formats must be output to the GV7605 using a 20-bit input bus format at a clock rate of 148.5 MHz. The 20-bit output format consists of two 10-bit data streams, Data Stream 1 (DS1) and Data Stream 2 (DS2). The following diagrams show how the Full HD image formats should be multiplexed into DS1 and DS2, at the output of the GV7605.

The GV7605 also supports a 10-bit DDR output mode, where DS1 and DS2 are word multiplexed.

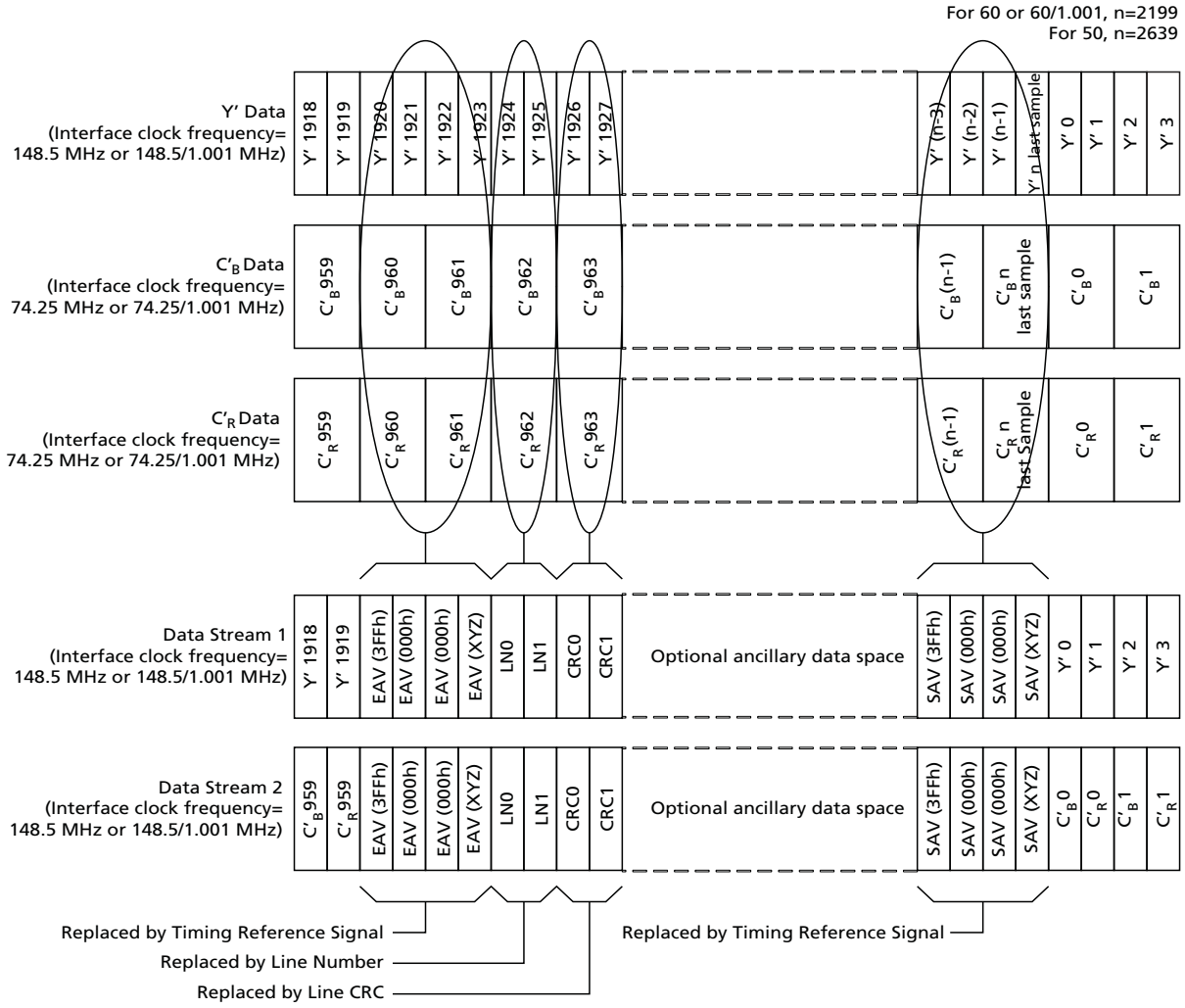


Figure 4-15: Aviia 20-bit Mapping Structure for 1920 x 1080 50/60Hz Progressive 4:2:0 & 4:2:2 (Y'C'$_B$C'$_R$) 8/10-bit Signals

Table 4-11: 1080p Y'C'$_B$C'$_R$ 4:2:0 & 4:2:2 10-bit Bit Structure Mapping

Data Stream	Bit Number									
	9	8	7	6	5	4	3	2	1	0
DS1	Y'[9:0]									
DS2	C'$_B$C'$_R$[9:0]									

Note: For 8-bit systems, the data should be justified to the most significant bit (Y'9 and C'$_B$C'$_R$9), with the two least significant bits (Y'[1:0] and C'$_B$C'$_R$[1:0]) set to zero.

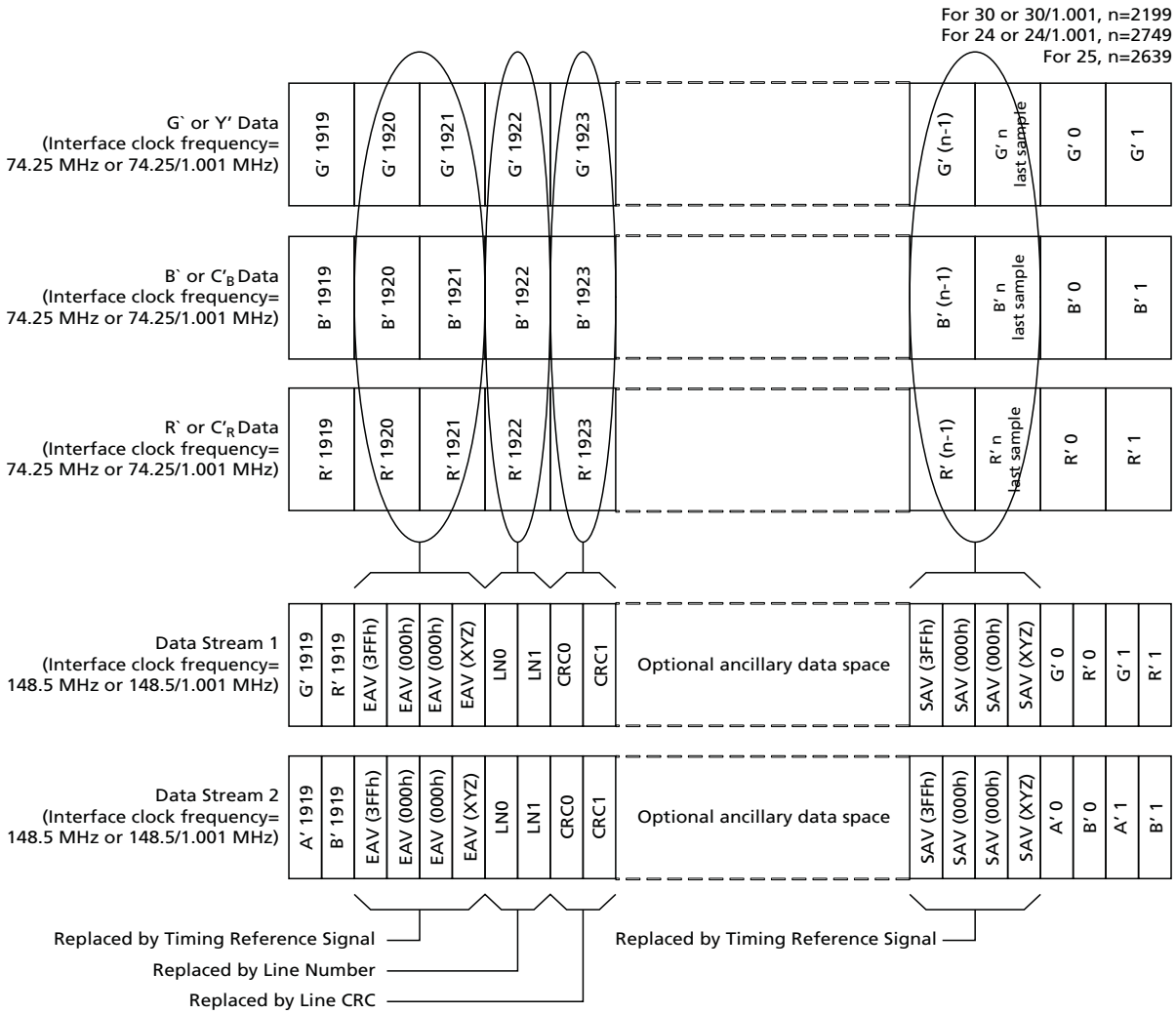


Figure 4-16: Aviia 20-bit Mapping Structure for 1920 x 1080 24/25/30Hz Progressive 4:4:4 (R'G'B') 8/10-bit Signals

Table 4-12: 1080p R'G'B' or Y'C'$_B$C'$_R$ 4:4:4 10-bit Bit Structure Mapping

Data Stream	Bit Number									
	9	8	7	6	5	4	3	2	1	0
DS1 First Word	G'[9:0] or Y'[9:0]									
DS1 Second Word	R'[9:0] or C'$_R$[9:0]									
DS2 First Word	A'[9:0]									
DS2 Second Word	B'[9:0] or C'$_B$[9:0]									

Note 1: The 10-bit 'A' data in Figure 4-16 is used to pad DS2 and should be set to the value 040h.

Note 2: For 8-bit systems, the data should be justified to the most significant bit (R'/C'$_R$9, G'/Y'9 and B'/C'$_B$9), with the two least significant bits (R'/C'$_R$[1:0], G'/Y'[1:0] and B'/C'$_B$[1:0]) set to zero.

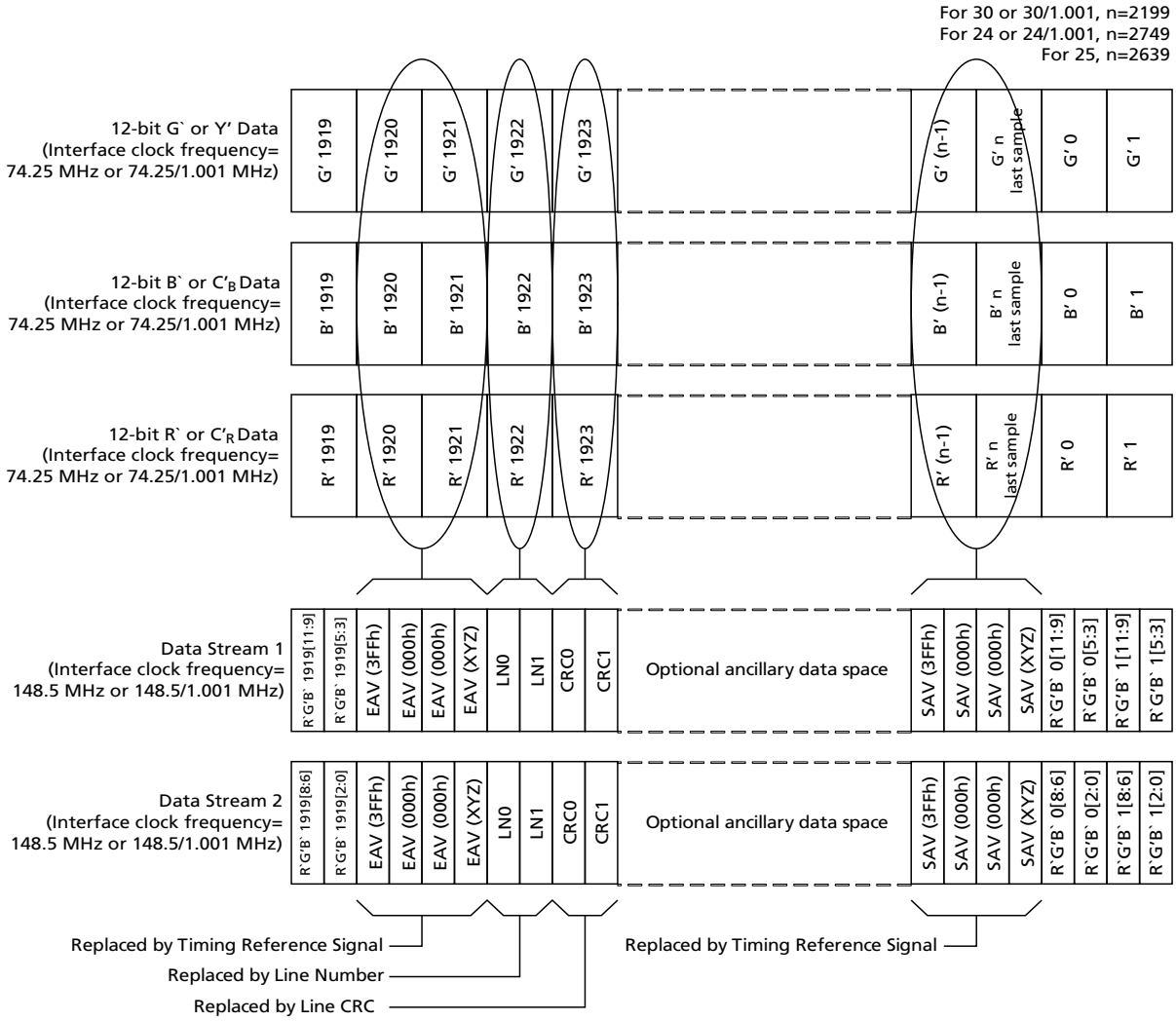


Figure 4-17: Aviia 20-bit Mapping Structure for 1920 x 1080 24/25/30Hz Progressive 4:4:4 (R'G'B' or Y'C'$_B$C'$_R$) 12-bit Signals

Table 4-13: 1080p R'G'B' or Y'C'$_B$C'$_R$ 4:4:4 12-bit Bit Structure Mapping

Data Stream	Bit Number									
	9	8	7	6	5	4	3	2	1	0
DS1 First Word	$\overline{B8}$	R'[11:9] or C'$_R$[11:9]			G'[11:9] or Y'[11:9]			B'[11:9] or C'$_B$[11:9]		
DS1 Second Word	$\overline{B8}$	R'[5:3] or C'$_R$[5:3]			G'[5:3] or Y'[5:3]			B'[5:3] or C'$_B$[5:3]		
DS2 First Word	$\overline{B8}$	R'[8:6] or C'$_R$[8:6]			G'[8:6] or Y'[8:6]			B'[8:6] or C'$_B$[8:6]		
DS2 Second Word	$\overline{B8}$	R'[2:0] or C'$_R$[2:0]			G'[2:0] or Y'[2:0]			B'[2:0] or C'$_B$[2:0]		

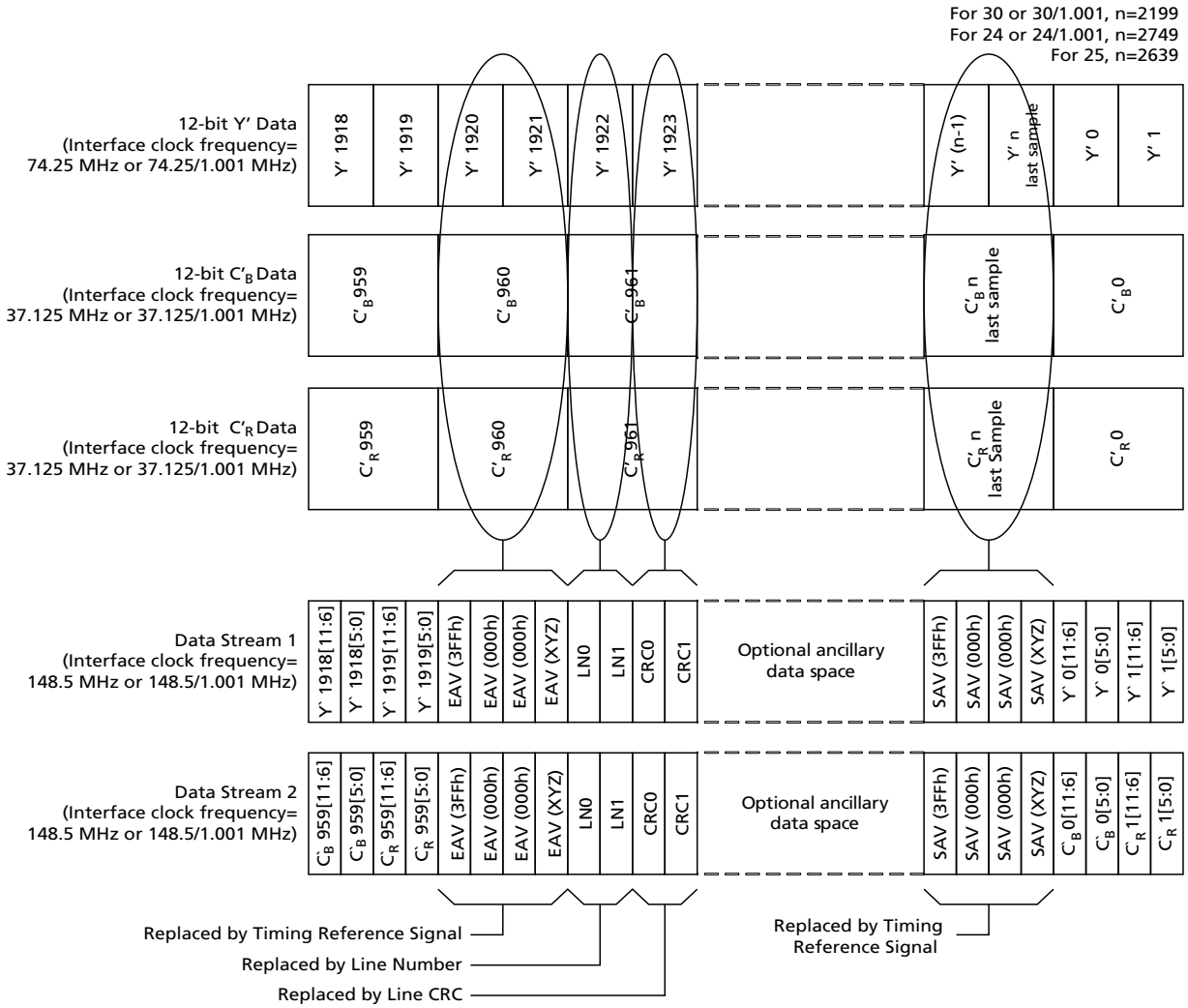


Figure 4-18: Aviia 20-bit Mapping Structure for 1920 x 1080 24/25/30Hz Progressive 4:2:2 (Y'C'$_B$C'$_R$) 12-bit Signals

Table 4-14: 1080p Y'C'$_B$C'$_R$ 4:2:2 12-bit Bit Structure Mapping

Data Stream	Bit Number									
	9	8	7	6	5	4	3	2	1	0
DS1 First Word	1	0	0	0	Y'[11:6]					
DS1 Second Word	1	0	0	0	Y'[5:0]					
DS2 First Word	1	0	0	0	C'$_B$[11:6]					
DS2 Second Word	1	0	0	0	C'$_B$[5:0]					
DS2 Third Word	1	0	0	0	C'$_R$[11:6]					
DS2 Fourth Word	1	0	0	0	C'$_R$[5:0]					

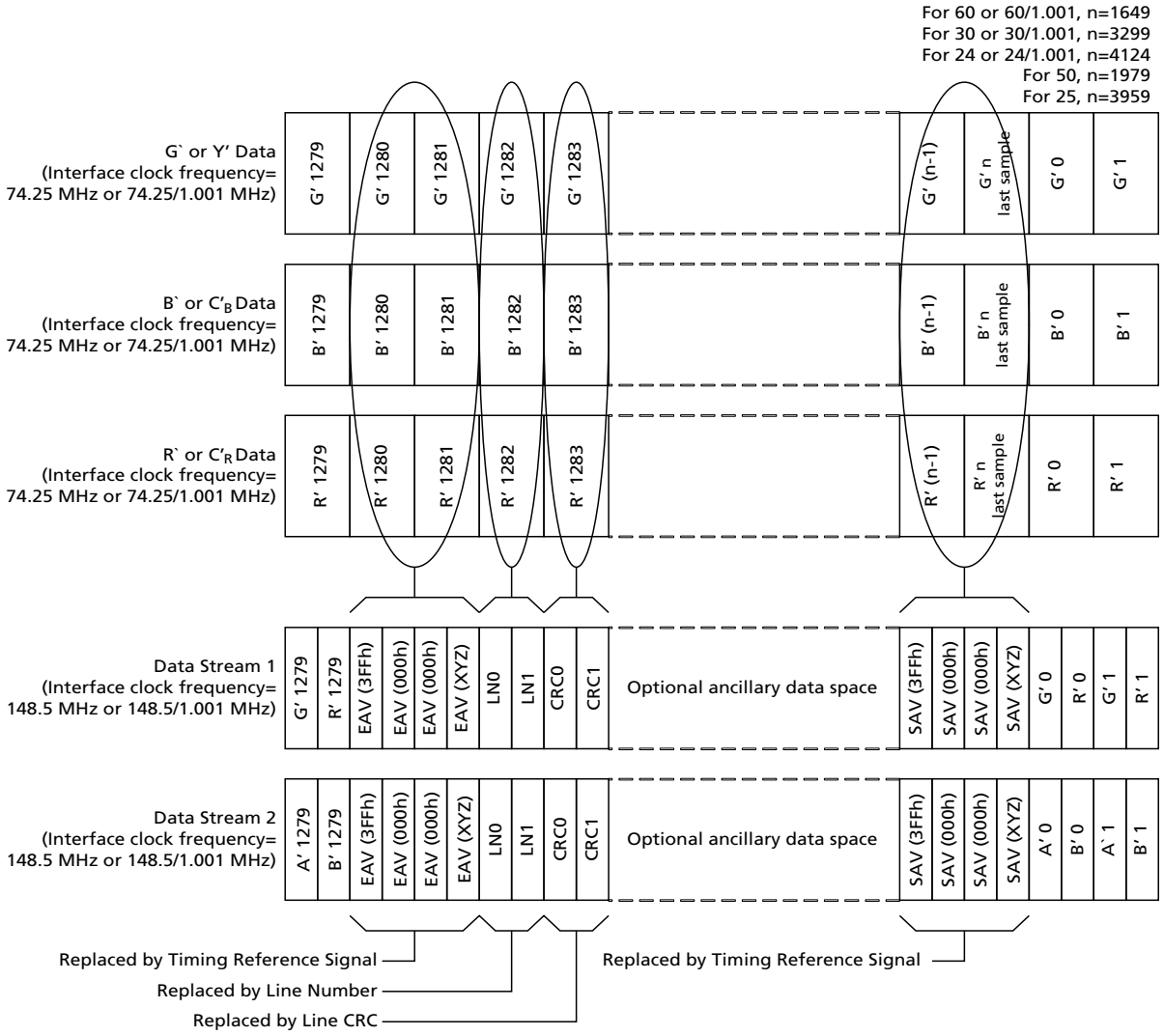


Figure 4-19: Aviia 20-bit Mapping Structure for 1280 x 720 24/25/30/25/60Hz Progressive 4:4:4 (R'G'B' or Y'C'$_B$C'$_R$) 8/10-bit Signals

Table 4-15: 720p R'G'B' or Y'C'$_B$C'$_R$ 4:4:4 10-bit Bit Structure Mapping

Data Stream	Bit Number									
	9	8	7	6	5	4	3	2	1	0
DS1 First Word	G'[9:0] or Y'[9:0]									
DS1 Second Word	R'[9:0] or C'$_R$[9:0]									
DS2 First Word	A'[9:0]									
DS2 Second Word	B'[9:0] or C'$_B$[9:0]									

Note 1: The 10-bit 'A' data in Figure 4-19 is used to pad DS2 and should be set to the value 040h.

Note 2: For 8-bit systems, the data should be justified to the most significant bit (R'/C'$_R$9, G'/Y'9 and B'/C'$_B$9), with the two least significant bits (R'/C'$_R$[1:0], G'/Y'[1:0] and B'/C'$_B$[1:0]) set to zero.

4.7.3 Descrambling and Word Alignment

The GV7605 performs NRZI to NRZ decoding and data descrambling according to ITU-R BT.656 and BT.1120, and word aligns the data to TRS sync words.

When operating in manual mode (AUTO/$\overline{\text{MAN}}$ = LOW), the device only carries out video decoding, descrambling and word alignment when the $\overline{\text{656\_BYPASS}}$ pin is set HIGH and the ASI pin is set LOW.

When operating in Auto mode (AUTO/$\overline{\text{MAN}}$ = HIGH), the GV7605 carries out descrambling and word alignment to enable the detection of TRS sync words. When two consecutive valid TRS words (SAV and EAV), with the same bit alignment have been detected, the device word-aligns the data to the TRS ID words.

TRS ID word detection is a continuous process. The device remains in video mode until TRS ID words fail to be detected.

Note: Both 8-bit and 10-bit TRS headers are identified by the device.

4.8 Parallel Video Data Outputs DOUT[19:0] and DOUT[9:0]

The parallel data outputs are aligned to the rising edge of the PCLK.

4.8.1 Parallel Data Bus Buffers

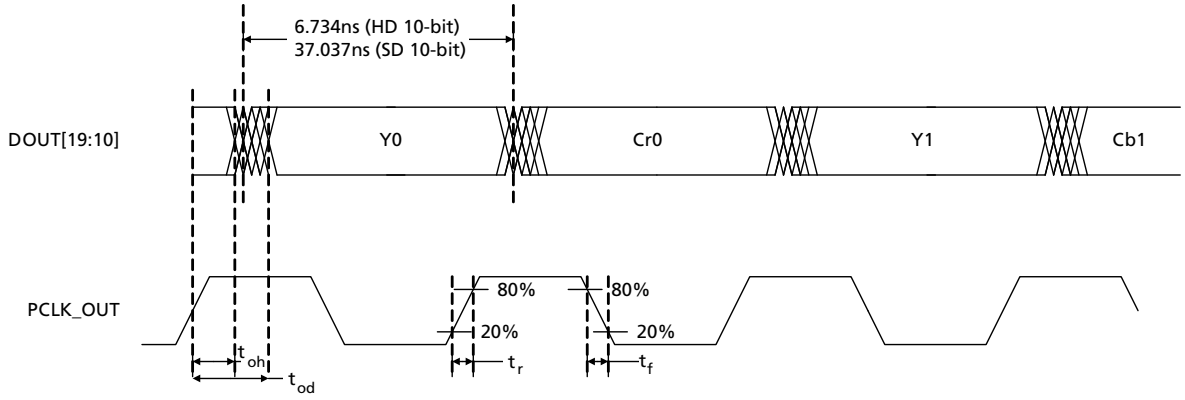
The parallel data bus, status signal outputs and control signal input pins are all connected to high-impedance buffers.

The device supports 1.8 or 3.3V (LVTTL and LVCMOS levels) supplied at the IO_VDD and IO_GND pins.

All output buffers (including the PCLK output) are set to high-impedance in Reset mode ($\overline{RESET}$ = LOW).

I/O Timing Specs:

10-bit SDR Mode:



10-bit HD Mode

	3.3V						1.8V					
	t_{oh}	$\frac{t_r}{t_f}$ (min)	Cload	t_{od}	$\frac{t_r}{t_f}$ (max)	Cload	t_{oh}	$\frac{t_r}{t_f}$ (min)	Cload	t_{od}	$\frac{t_r}{t_f}$ (max)	Cload
dbus	1.000ns	0.400ns	6pF	3.700ns	1.400ns	15pF	1.000ns	0.400ns	6pF	3.700ns	1.400ns	15pF
stat	1.000ns	0.500ns		4.100ns	1.600ns		1.000ns	0.400ns		4.400ns	1.500ns	

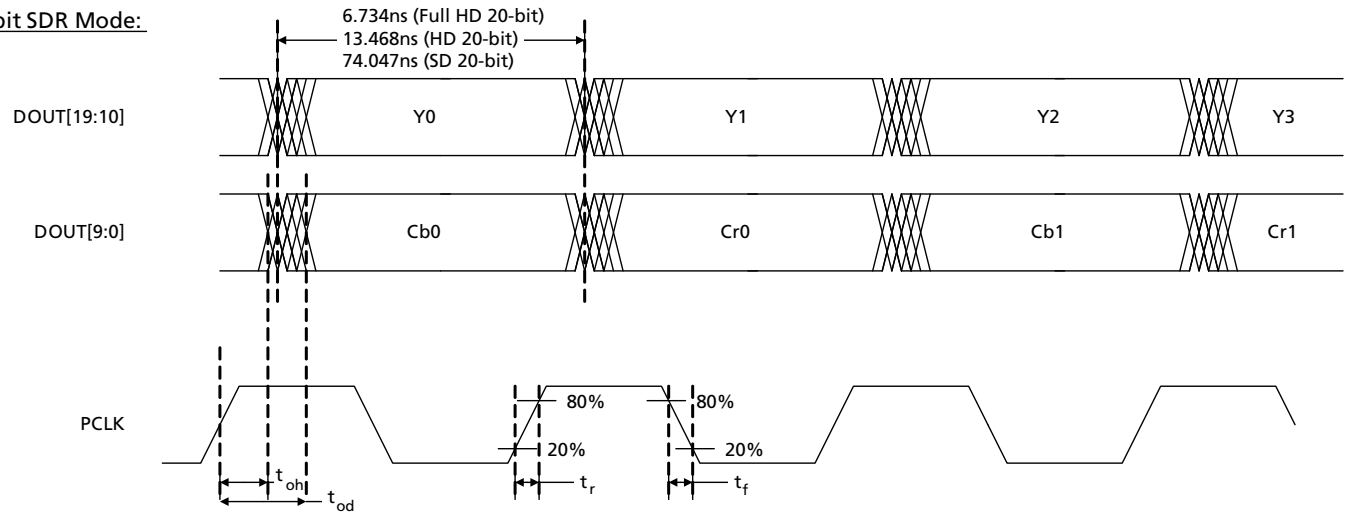
10-bit SD Mode

	3.3V						1.8V					
	t_{oh}	$\frac{t_r}{t_f}$ (min)	Cload	t_{od}	$\frac{t_r}{t_f}$ (max)	Cload	t_{oh}	$\frac{t_r}{t_f}$ (min)	Cload	t_{od}	$\frac{t_r}{t_f}$ (max)	Cload
dbus	19.400ns	0.400ns	6pF	22.200ns	1.400ns	15pF	19.400ns	0.400ns	6pF	22.200ns	1.400ns	15pF
stat	19.400ns	0.500ns		22.200ns	1.600ns		19.400ns	0.400ns		22.200ns	1.500ns	

Figure 4-20: PCLK to Data and Control Signal Output Timing - SDR Mode 1

I/O Timing Specs:

20-bit SDR Mode:



20-bit HD Mode

	3.3V						1.8V					
	t_{oh}	$\frac{t_r}{t_f}$ (min)	Cload	t_{od}	$\frac{t_r}{t_f}$ (max)	Cload	t_{oh}	$\frac{t_r}{t_f}$ (min)	Cload	t_{od}	$\frac{t_r}{t_f}$ (max)	Cload
dbus	1.000ns	0.400ns	6pF	3.700ns	1.400ns	15pF	1.000ns	0.400ns	6pF	3.700ns	1.400ns	15pF
stat	1.000ns	0.500ns		4.100ns	1.600ns		1.000ns	0.400ns		4.400ns	1.500ns	

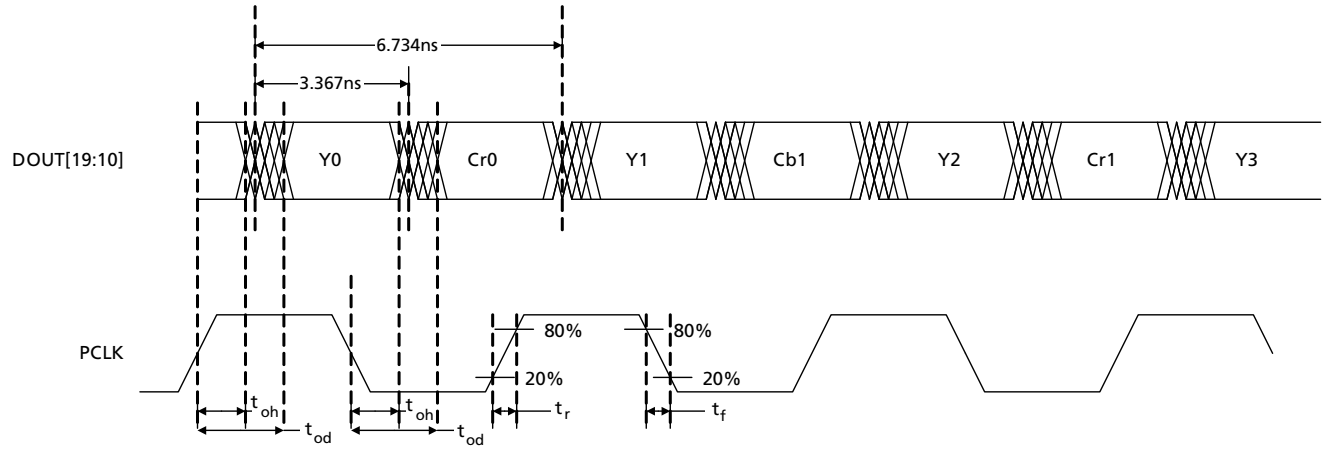
20-bit SD Mode

	3.3V						1.8V					
	t_{oh}	$\frac{t_r}{t_f}$ (min)	Cload	t_{od}	$\frac{t_r}{t_f}$ (max)	Cload	t_{oh}	$\frac{t_r}{t_f}$ (min)	Cload	t_{od}	$\frac{t_r}{t_f}$ (max)	Cload
dbus	38.000ns	0.400ns	6pF	41.000ns	1.400ns	15pF	38.000ns	0.400ns	6pF	41.000ns	1.400ns	15pF
stat	38.000ns	0.500ns		41.000ns	1.600ns		38.000ns	0.400ns		41.000ns	1.500ns	

Figure 4-21: PCLK to Data and Control Signal Output Timing - SDR Mode 2

I/O Timing Specs:

DDR Mode:



10-bit Full HD Mode

	3.3V						1.8V					
	t_{oh}	$\frac{t_r}{t_f}$ (min)	Cload	t_{od}	$\frac{t_r}{t_f}$ (max)	Cload	t_{oh}	$\frac{t_r}{t_f}$ (min)	Cload	t_{od}	$\frac{t_r}{t_f}$ (max)	Cload
dbus	0.450ns	0.400ns	6pF	1.900ns	1.500ns	15pF	0.400ns	0.300ns	6pF	1.800ns	1.100ns	15pF
stat	0.450ns	0.500ns		2.200ns	1.600ns		0.450ns	0.400ns		2.500ns	1.500ns	

Figure 4-22: PCLK to Data and Control Signal Output Timing - DDR Mode

Table 4-16: GV7605 Output Video Data Format Selections

Output Data Format	Pin/Register Bit Settings					DOUT[9:0]	DOUT[19:10]
	20BIT /10BIT	RATE_ SEL0	RATE_ SEL1	656_ BYPASS	ASI		
20-bit demultiplexed HD format	HIGH	LOW	LOW	HIGH	LOW	Chroma	Luma
20-bit data output HD format	HIGH	LOW	LOW	LOW	LOW	DATA	DATA
20-bit demultiplexed SD format	HIGH	HIGH	X	HIGH	LOW	Chroma	Luma
20-bit data output SD format	HIGH	HIGH	X	LOW	LOW	DATA	DATA
10-bit multiplexed Full HD DDR format	LOW	LOW	HIGH	HIGH	LOW	Driven LOW	DS1 / DS2
10-bit multiplexed HD format	LOW	LOW	LOW	HIGH	LOW	Driven LOW	Luma / Chroma

Table 4-16: GV7605 Output Video Data Format Selections (Continued)

Output Data Format	Pin/Register Bit Settings					DOUT[9:0]	DOUT[19:10]
	20BIT /$\overline{10BIT}$	RATE_ SEL0	RATE_ SEL1	$\overline{656}$_ $\overline{BYPASS}$	ASI		
10-bit data output HD format	LOW	LOW	LOW	LOW	LOW	Driven LOW	DATA
10-bit multiplexed SD format	LOW	HIGH	X	HIGH	LOW	Driven LOW	Luma / Chroma
10-bit data output SD format	LOW	HIGH	X	LOW	LOW	Driven LOW	DATA
20-bit demultiplexed Full HD format	HIGH	LOW	HIGH	HIGH	LOW	DS2	DS1
Transport stream	LOW	HIGH	X	–	HIGH	DOUT19 = WORD_ERR DOUT18 = SYNC_OUT DOUT17 = H_OUT DOUT16 = G_OUT DOUT15 = F_OUT DOUT14 = E_OUT DOUT13 = D_OUT DOUT12 = C_OUT DOUT11 = B_OUT DOUT10 = A_OUT	

4.8.2 Parallel Output in Video Mode

When the device is operating in video mode ($\overline{656\_BYPASS}$ = HIGH and ASI = LOW), data is output in either Multiplexed or Demultiplexed form depending on the setting of the 20BIT/$\overline{10BIT}$ pin.

When operating in 20-bit mode (20BIT/$\overline{10BIT}$ = HIGH), the output data is demultiplexed Luma and Chroma data for SD and HD data rates, and DS1 and DS2 for the Full HD data.

When operating in 10-bit mode (20BIT/$\overline{10BIT}$ = LOW), the output data is multiplexed Luma and Chroma data for SD and HD data rates, and multiplexed DS1 and DS2 for the Full HD data. In this mode, the data is presented on the DOUT[19:10] pins, with DOUT[9:0] being forced LOW.

4.8.3 Parallel Output in ASI Mode

In ASI mode, the 20BIT/$\overline{10BIT}$ pin must be set LOW to configure the output parallel bus for 10-bit operation.

ASI mode is enabled when the AUTO/$\overline{MAN}$ bit is LOW, $\overline{656\_BYPASS}$ pin is LOW and the ASI pin is HIGH.

The extracted 8-bit transport stream data is presented on DOUT[17:10] such that DOUT[17:10] = HOUT ~ AOUT, where AOUT is the least significant bit of the decoded transport stream data.

In addition, the DOUT19 and DOUT18 pins are configured as ASI status signals WORDERR and SYNCOUT respectively.

SYNCOUT is HIGH whenever a K28.5 sync character is output from the device.

WORDERR is HIGH whenever the device has detected a running disparity error or illegal code word.

4.8.4 Parallel Output In Data-Through Mode

This mode is enabled when the $\overline{656\_BYPASS}$ and ASI pins are LOW.

In this mode, data is passed to the output bus without any decoding, descrambling or word-alignment.

The output data width (10-bit or 20-bit) is controlled by the setting of the 20BIT/$\overline{10BIT}$ pin.

4.8.5 Parallel Output Clock (PCLK)

The frequency of the PCLK output signal of the GV7605 is determined by the output data format. Table 4-17 lists the output signal formats according to the data format selected in Manual mode (AUTO/$\overline{MAN}$ bit in the host interface is set LOW), or detected in Auto mode (AUTO/$\overline{MAN}$ bit in the host interface is set HIGH).

Table 4-17: GV7605 PCLK Output Rates

Output Data Format	Pin/Control Bit Settings					PCLK Rate
	20BIT/$\overline{10BIT}$	RATE_DET0	RATE_DET1	$\overline{656\_BYPASS}$	ASI	
20-bit demultiplexed HD format	HIGH	LOW	LOW	HIGH	LOW	74.25 or 74.25/1.001MHz
20-bit data output HD format	HIGH	LOW	LOW	LOW	LOW	74.25 or 74.25/1.001MHz
20-bit demultiplexed SD format	HIGH	HIGH	X	HIGH	LOW	13.5MHz
20-bit data output SD format	HIGH	HIGH	X	LOW	LOW	13.5MHz
20-bit demultiplexed Full HD format	HIGH	LOW	HIGH	HIGH	LOW	148.5 or 148.5/1.001MHz
10-bit multiplexed Full HD DDR format	LOW	LOW	HIGH	HIGH	LOW	148.5 or 148.5/1.001MHz

Table 4-17: GV7605 PCLK Output Rates (Continued)

Output Data Format	Pin/Control Bit Settings					PCLK Rate
	20BIT/$\overline{10BIT}$	RATE_DET0	RATE_DET1	$\overline{656\_BYPASS}$	ASI	
10-bit multiplexed HD format	LOW	LOW	LOW	HIGH	LOW	148.5 or 148.5/1.001MHz
10-bit data output HD format	LOW	LOW	LOW	LOW	LOW	148.5 or 148.5/1.001MHz
10-bit multiplexed SD format	LOW	HIGH	X	HIGH	LOW	27MHz
10-bit data output SD format	LOW	HIGH	X	LOW	LOW	27MHz
10-bit transport stream output	LOW	HIGH	X	LOW	HIGH	27MHz

4.8.6 DDR Parallel Clock Timing

The GV7605 has the ability to transmit 10-bit parallel video data with a DDR (Dual Data Rate) pixel clock over a single-ended interface. DDR Mode can be enabled when the input data rate is 2.97Gb/s. In this case, the 10-bit parallel data rate is 297Mb/s, and the frequency of the DDR clock is 148.5MHz (10-bit output in Full HD mode).

The DDR pixel clock avoids the need to operate a high-drive pixel clock at 297MHz. This reduces power consumption, clock drive strength, and noise generation, and precludes from generating excessive EMI had PCLK on the board have to run at 297MHz. It also enables easier board routing and avoids the need to use the higher-speed I/Os on FPGAs, which may require more expensive speed grades.

Figure 4-23 shows how the DDR interface operates. The pixel clock is transmitted at half the data rate, and the interleaved data is sampled at the receiver on both clock edges.

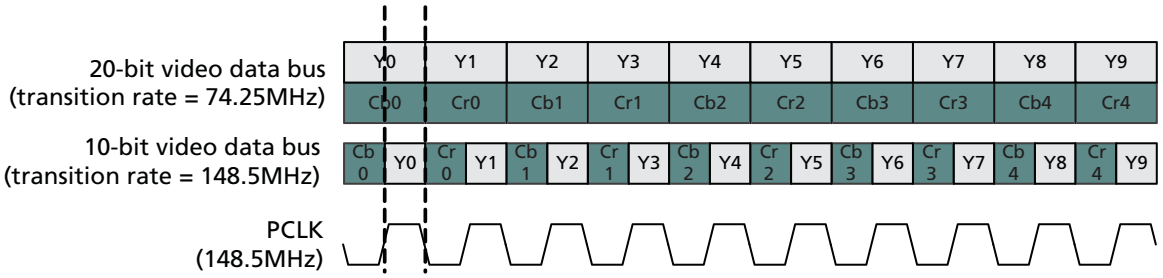


Figure 4-23: DDR Video Interface

The GV7605 has the ability to shift the Setup/Hold window on the receive interface, by using an on-chip delay line to shift the phase of PCLK with respect to the data bus.

The timing of the PCLK output, relative to the data, can be adjusted through the host interface registers. Address 06Ch contains the delay line controls:

Bit[5] (DEL_LINE_CLK_SEL) is a coarse delay adjustment that selects between the default (nominal) PCLK phase and a quadrature phase, for a 90° phase shift.

Bits[4:0] (DEL_LINE_OFFSET) comprise a fine delay adjustment to shift the PCLK in 40ps increments (typical conditions). The maximum fine delay adjustment is approximately 1.2ns under nominal conditions.

An example delay adjustment over min/typ/max conditions is illustrated in Figure 4-24. The target delay is 0.84 ns under typical conditions (approximately 45° PCLK phase shift), and requires a control word setting of 0x0014 for address 0x006C.

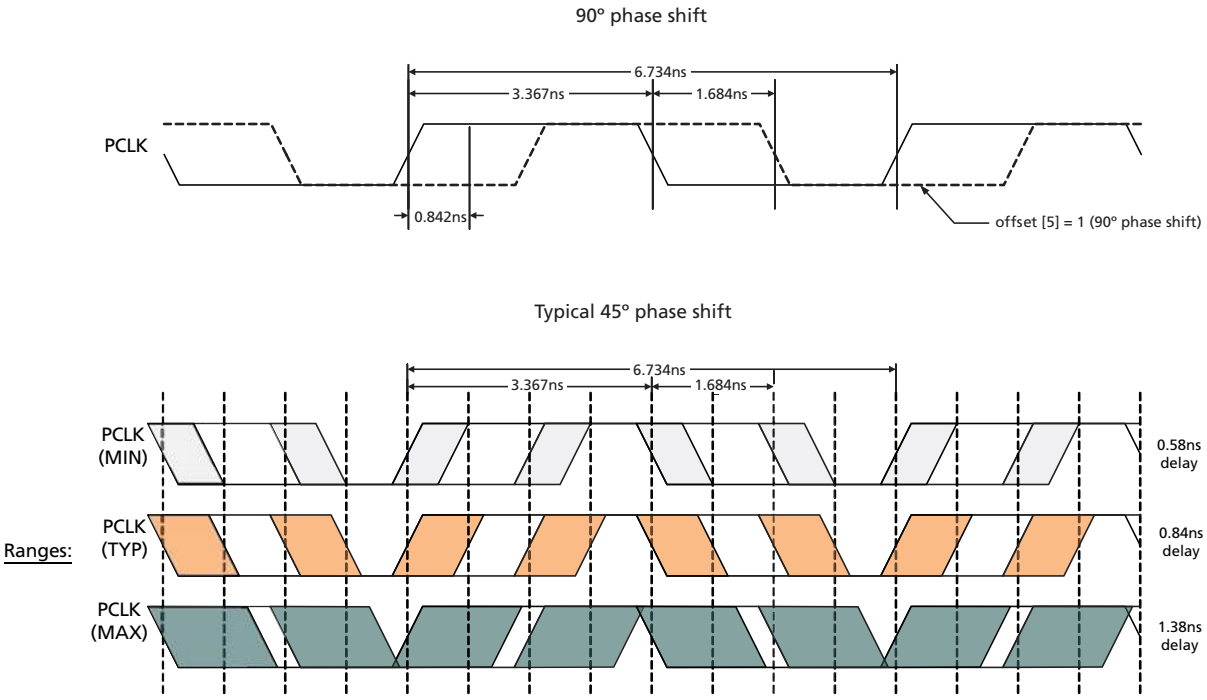


Figure 4-24: Delay Adjustment Ranges

4.9 Timing Signal Generator

The GV7605 has an internal timing signal generator which is used to generate digital FVH timing reference signals, to detect and correct certain error conditions and automatic video standard detection.

The timing signal generator is only operational in video mode ($\overline{656\_BYPASS}$ = HIGH).

The timing signal generator consists of a number of counters and comparators operating at video pixel and video line rates. These counters maintain information about the total line length, active line length, total number of lines per field/frame and total active lines per field/frame for the received video standard.

The timing signal generator 'learns' the video standard by timing the horizontal and vertical reference information contained in the TRS IDs of the received video data (specifically, the XYZ word). It therefore takes one video frame to obtain full synchronization to the received video standard.

Note: Both 8-bit and 10-bit TRS words are identified by the device. Once synchronization has been achieved, the timing signal generator continues to monitor the received TRS timing information to maintain synchronization.

The timing signal generator re-synchronizes all pixel and line based counters on every received TRS ID.

4.10 Programmable Multi-function Outputs

The GV7605 has 6 multi-function output pins, STAT[5:0], which are programmable via the host interface to output one of the following signals:

Table 4-18: Output Signals Available on Programmable Multi-Function Pins

Status Signal	Selection Code	Default Output Pin
H/HSYNC (according to 861_EN Pin) Section 4.11	0000	STAT 0
V/VSYNC (according to 861_EN Pin) Section 4.11	0001	STAT 1
F/DE (according to 861_EN Pin) Section 4.11	0010	STAT 2
LOCKED Section 4.6	0011	STAT 3
Y/1ANC Section 4.15	0100	STAT 4
C/2ANC Section 4.15	0101	–
$\overline{\text{DATA\_ERROR}}$ Section 4.14	0110	STAT 5
$\overline{\text{VIDEO\_ERROR}}$	0111	–
$\overline{\text{AUDIO\_ERROR}}$	1000	–
EDH_DETECTED	1001	–
CARRIER_DETECT	1010	–
RATE_DET0	1011	–
RATE_DET1	1100	–

Each of the STAT[5:0] pins are configurable individually using the register bits in the host interface; STAT[5:0]_CONFIG (008h/009h).

4.11 H:V:F Timing Signal Generation

The GV7605 extracts critical timing parameters from the received TRS words.

Horizontal blanking (H), Vertical blanking (V), and Field odd/even (F) timing are output on the STAT[2:0] pins by default.

Using the H_CONFIG bit in the host interface, the H signal timing can be selected as one of the following:

1. Active line blanking (H_CONFIG = LOW) - the H output is HIGH for the horizontal blanking period, including the EAV TRS words.
2. TRS based blanking (H_CONFIG = HIGH) - the H output is set HIGH for the entire horizontal blanking period as indicated by the H bit in the received TRS signals.

The timing of these signals is shown in Figure 4-25, Figure 4-26, Figure 4-27, Figure 4-28 and Figure 4-29.

Note: Both 8-bit and 10-bit TRS words are identified by the device.

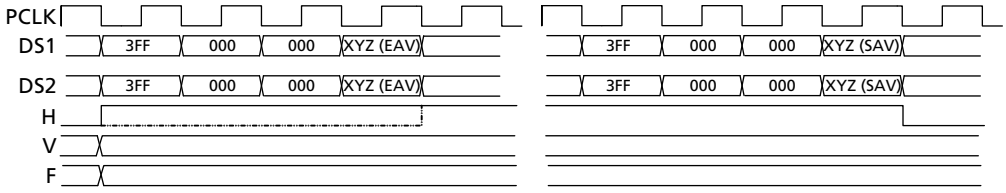


Figure 4-25: H:V:F Output Timing - Full HD 20-bit Output Mode

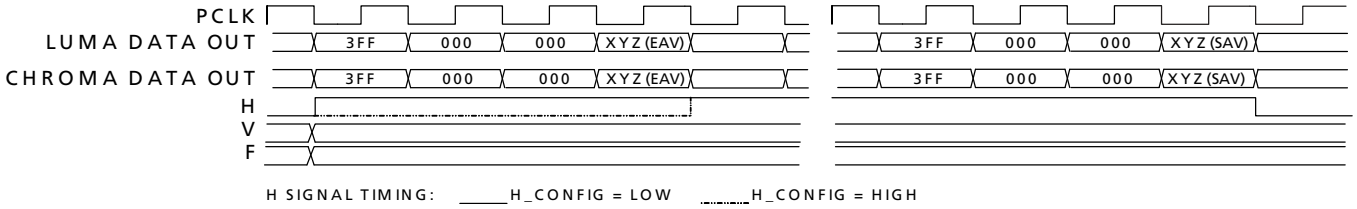


Figure 4-26: H:V:F Output Timing - HD 20-bit Output Mode

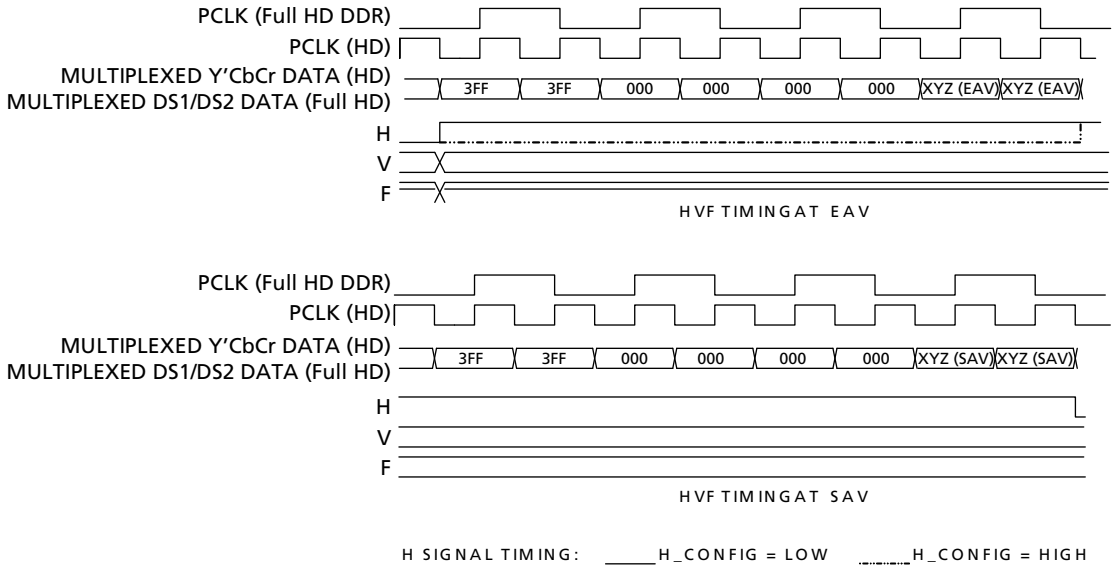


Figure 4-27: H:V:F Output Timing - HD & Full HD 10-bit Output Mode

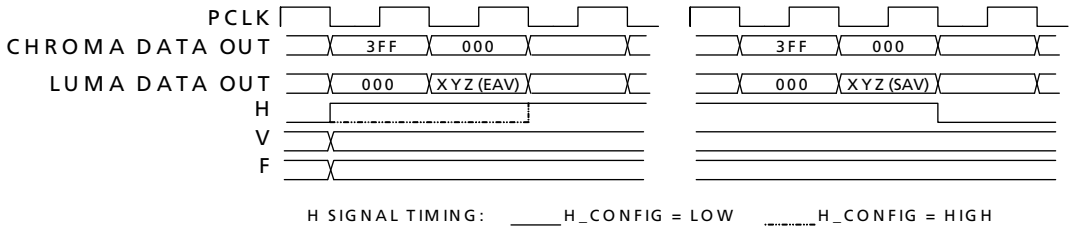


Figure 4-28: H:V:F Output Timing - SD 20-bit Output Mode

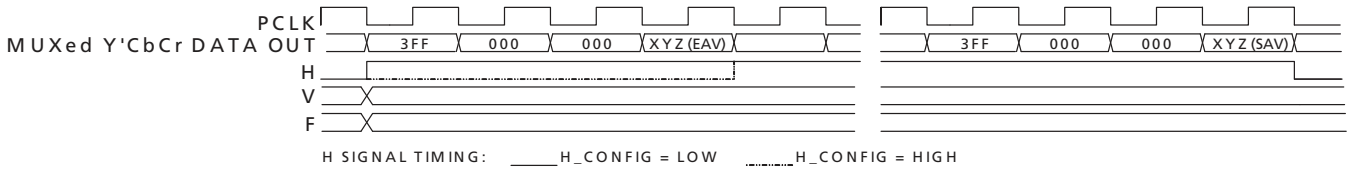


Figure 4-29: H:V:F Output Timing - SD 10-bit Output Mode

4.11.1 CEA-861 Timing Generation

The GV7605 is capable of generating CEA 861 timing instead of HVF timing for all of the supported video formats.

This mode is selected when the 861_EN pin is HIGH.

Horizontal sync (HSYNC), Vertical sync (VSYNC), and Data Enable (DE) timing are output on the STAT[2:0] pins by default.

Table 4-19 shows the CEA-861 formats supported by the GV7605:

Table 4-19: Supported CEA-861 Formats

Format	CEA-861 Format	VD_STD[5:0]
720(1440) x 480i @ 59.94/60Hz	6 & 7	16h, 17h, 19h, 1Bh
720(1440) x 576i @ 50Hz	21 & 22	18h, 1Ah
1280 x 720p @ 59.94/60Hz	4	20h, 00h
1280 x 720p @ 50Hz	19	24h, 04h
1920 x 1080i @ 59.94/60Hz	5	2Ah, 0Ah
1920 x 1080i @ 50Hz	20	2Ch, 0Ch
1920 x 1080p @ 29.97/30Hz	34[1]	2Bh, 0Bh
1920 x 1080p @ 25Hz	33[2]	2Dh, 0Dh
1920 x 1080p @ 23.98/24Hz	32	30h, 10h
1920 x 1080p @ 59.94/60Hz	16[1]	2Bh
1920 x 1080p @ 50Hz	31[2]	2Dh

Notes:

1,2: Timing is identical for the corresponding formats.

4.11.1.1 Vertical Timing

When CEA-861 timing is selected, the device outputs standards compliant CEA-861 timing signals as shown in the figures below.

The digital representation of 525 video, commonly referred to as D1, contains 487 lines of active video. However, the CEA-861 standard is defined as 525 video having 480 active lines. When the TRS_861 host interface bit is set LOW, the DE output signal will be set HIGH for 480 lines. When the TRS_861 bit is set HIGH, the DE signal will be set HIGH for 487 lines.

The timing of these signals is shown in the CEA-861 specifications. For information, they are included in the following diagrams. These diagrams may not be comprehensive.

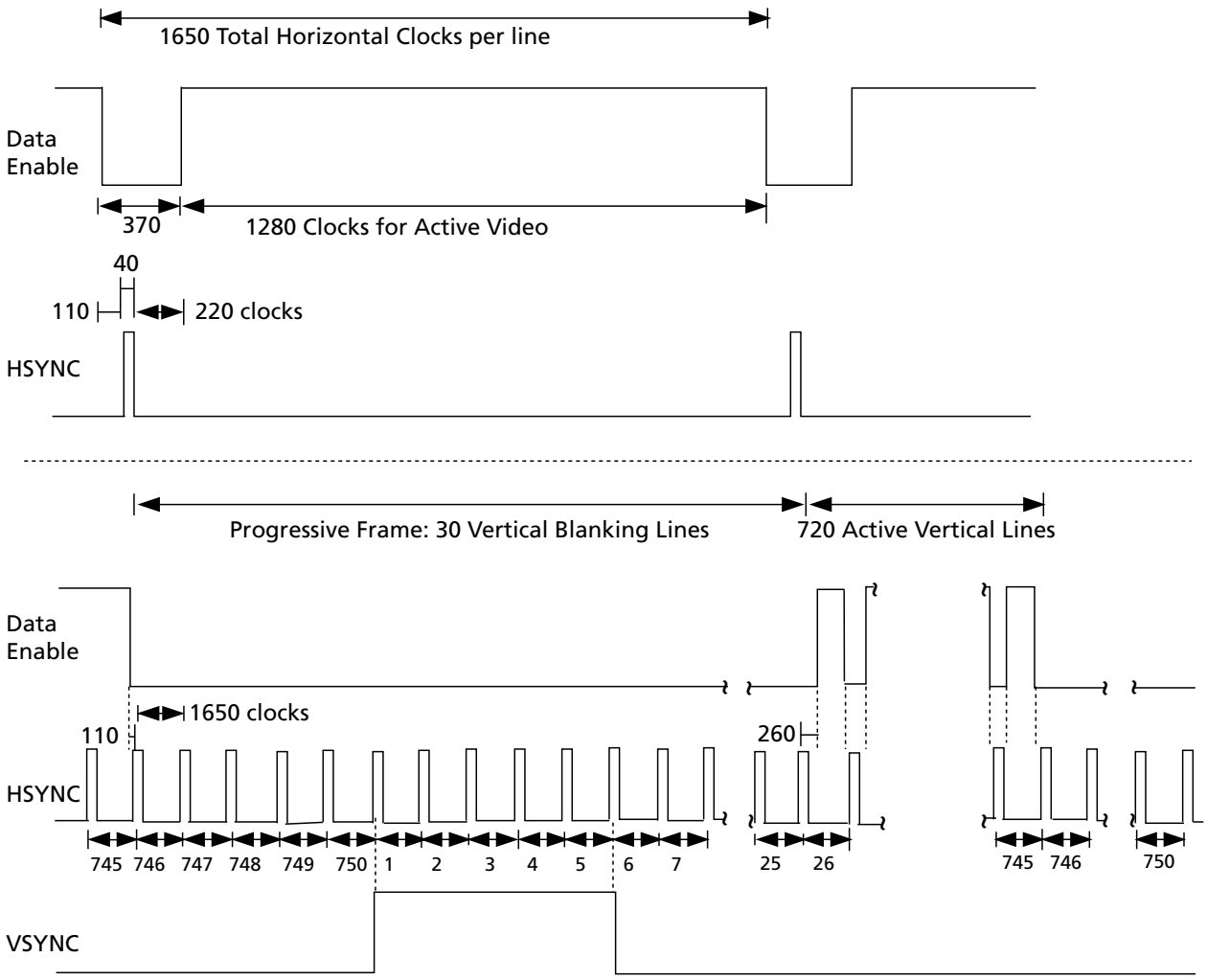


Figure 4-30: H:V:DE Output Timing 1280 x 720p @ 59.94/60 (Format 4)

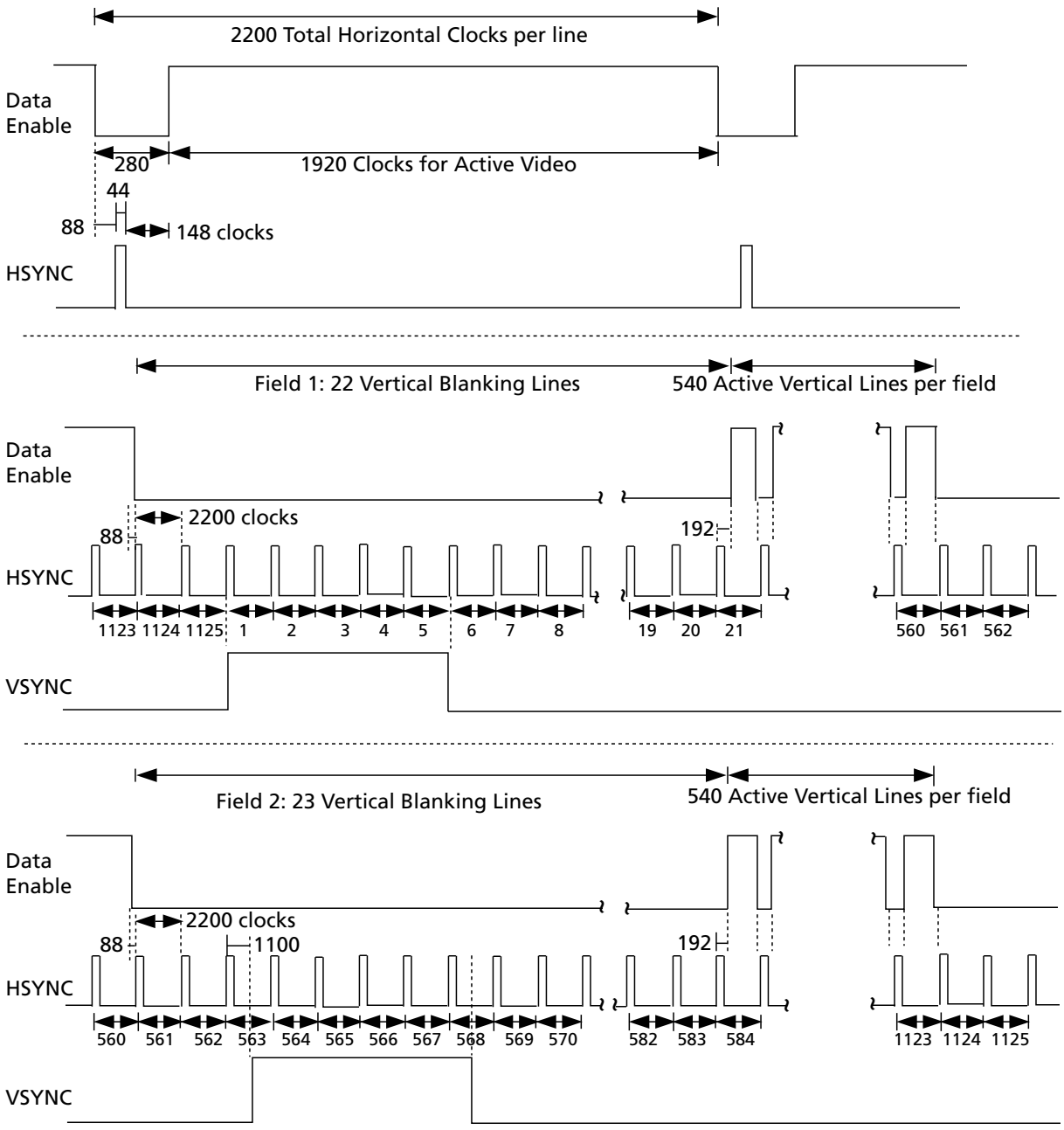


Figure 4-31: H:V:DE Output Timing 1920 x 1080i @ 59.94/60 (Format 5)

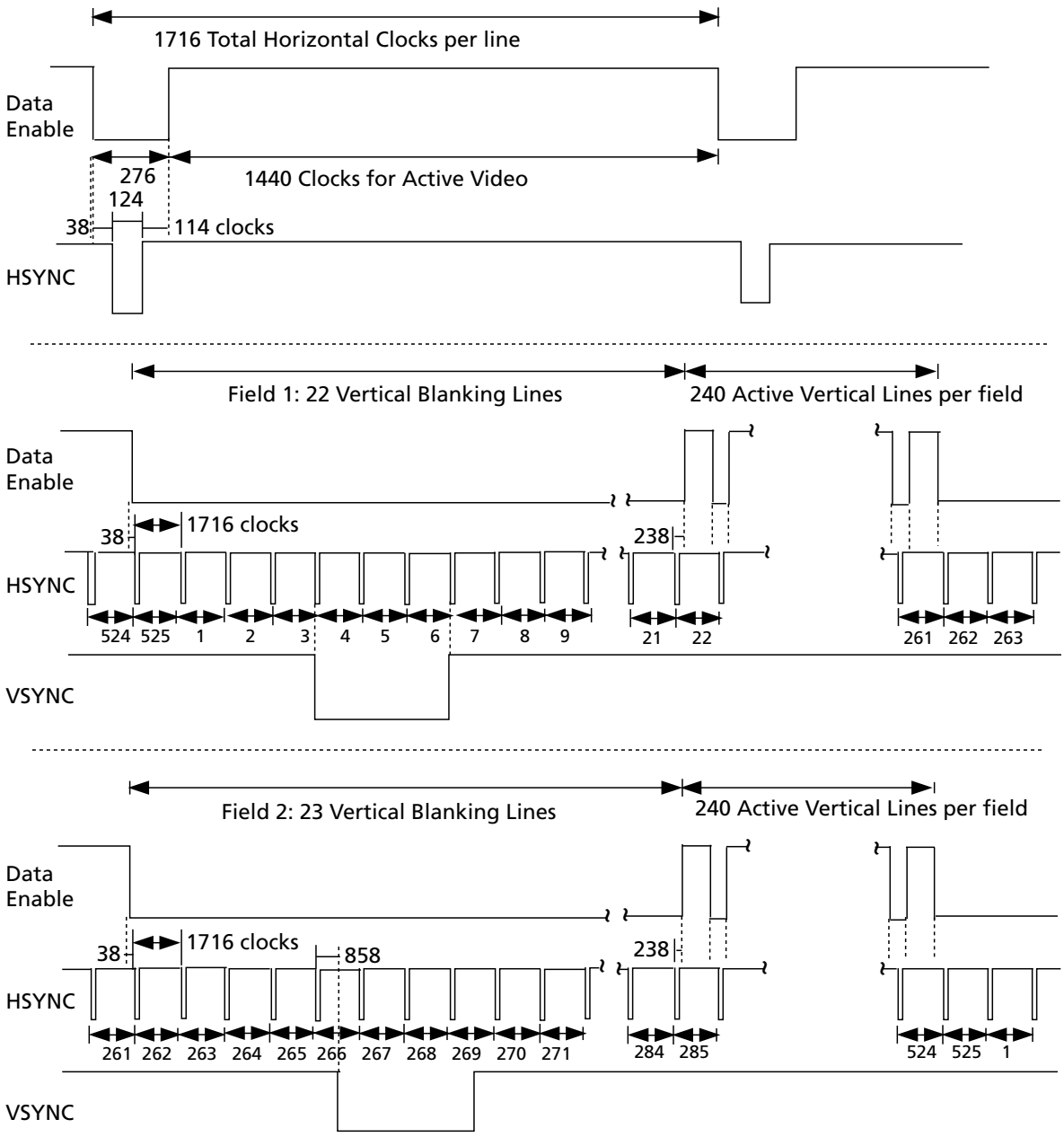


Figure 4-32: H:V:DE Output Timing 720 (1440) x 480i @ 59.94/60 (Format 6 & 7)

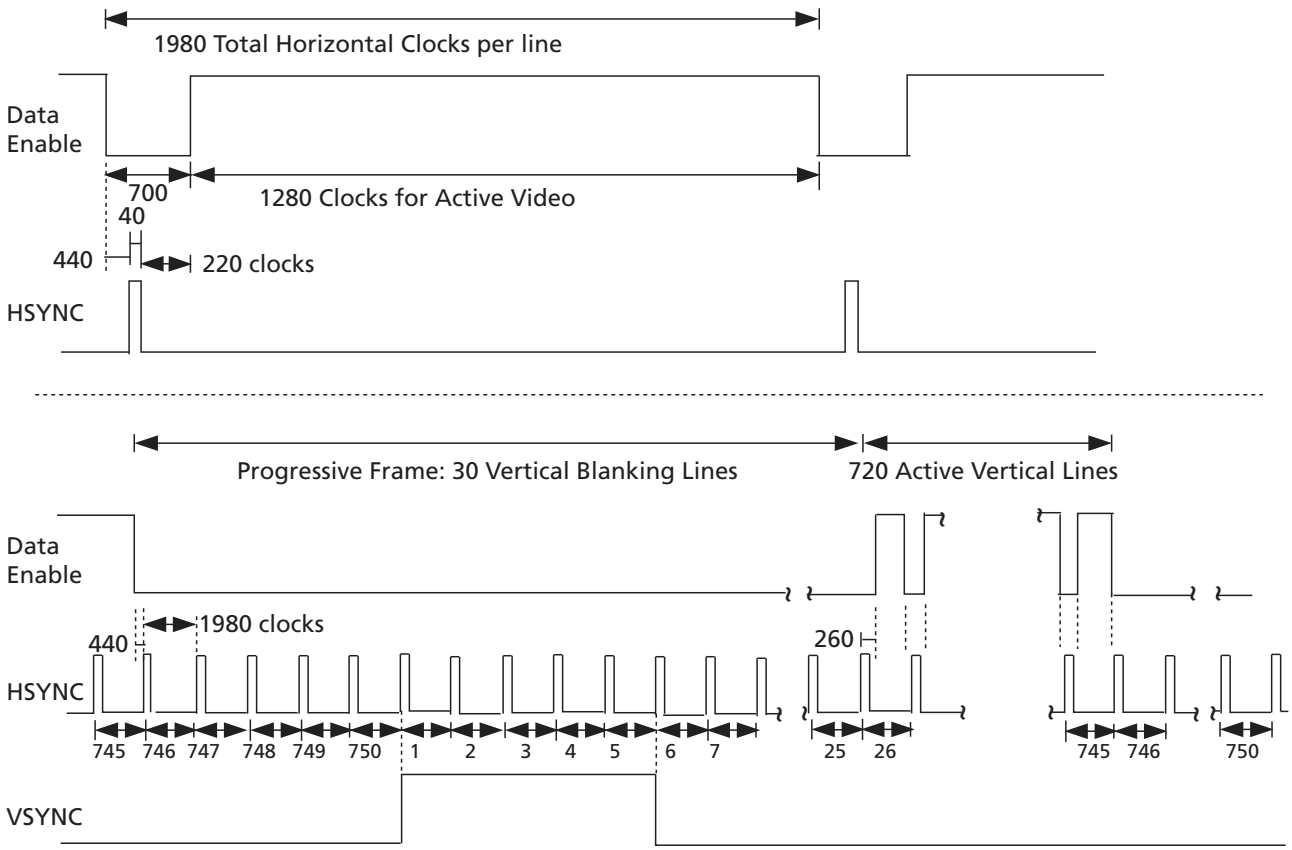


Figure 4-33: H:V:DE Output Timing 1280 x 720p @ 50 (Format 19)

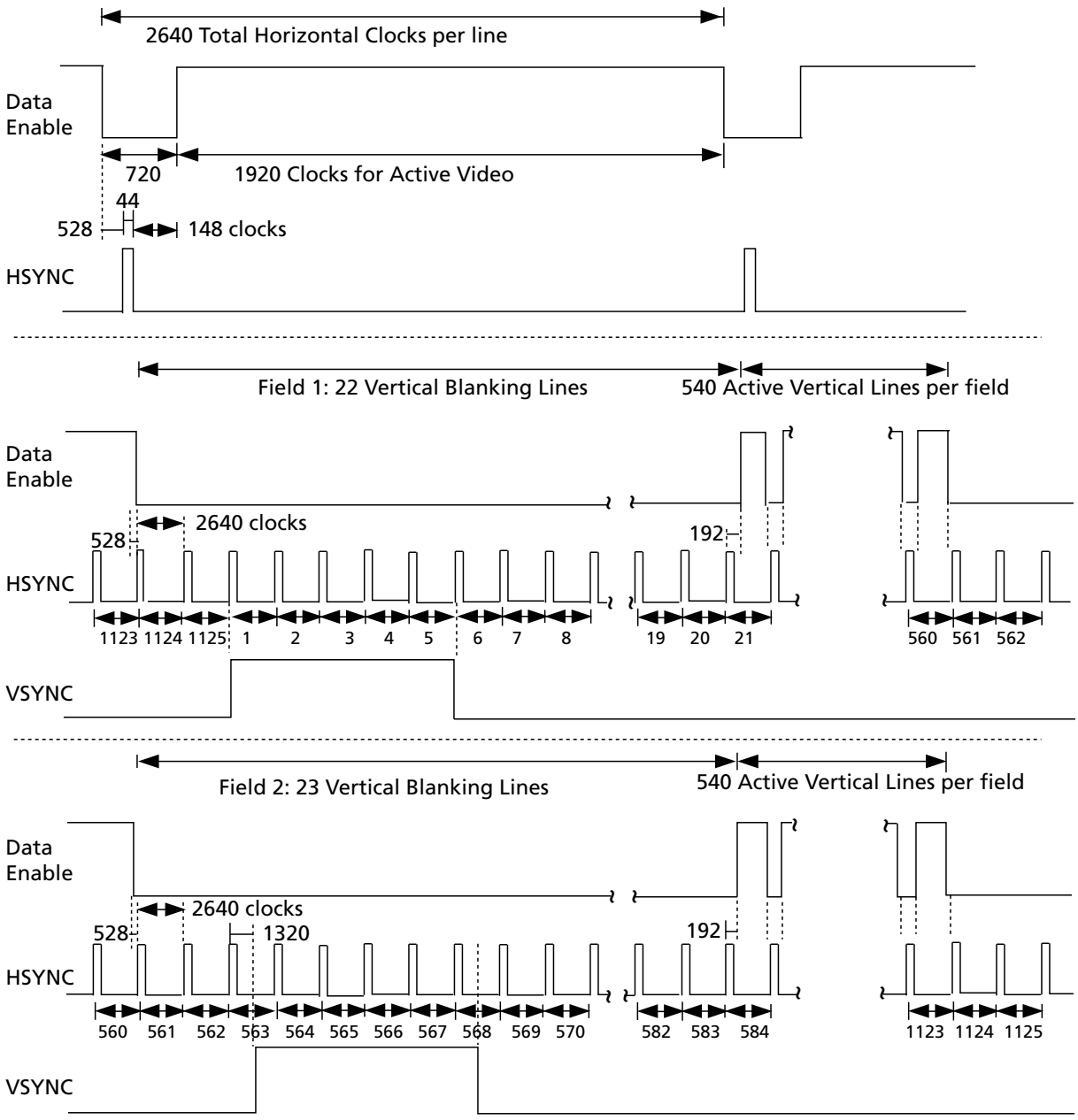


Figure 4-34: H:V:DE Output Timing 1920 x 1080i @ 50 (Format 20)

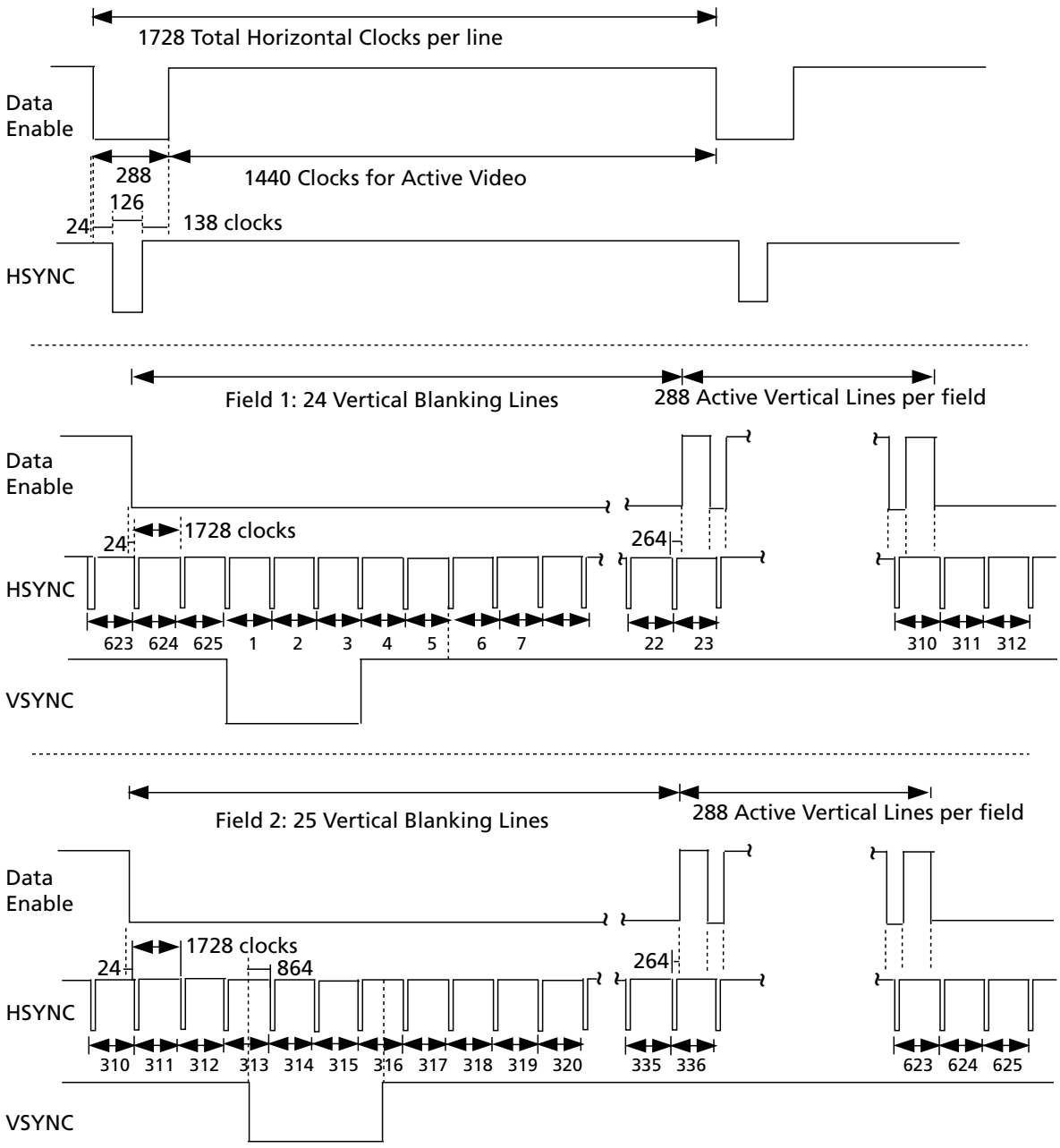


Figure 4-35: H:V:DE Output Timing 720 (1440) x 576 @ 50 (Format 21 & 22)

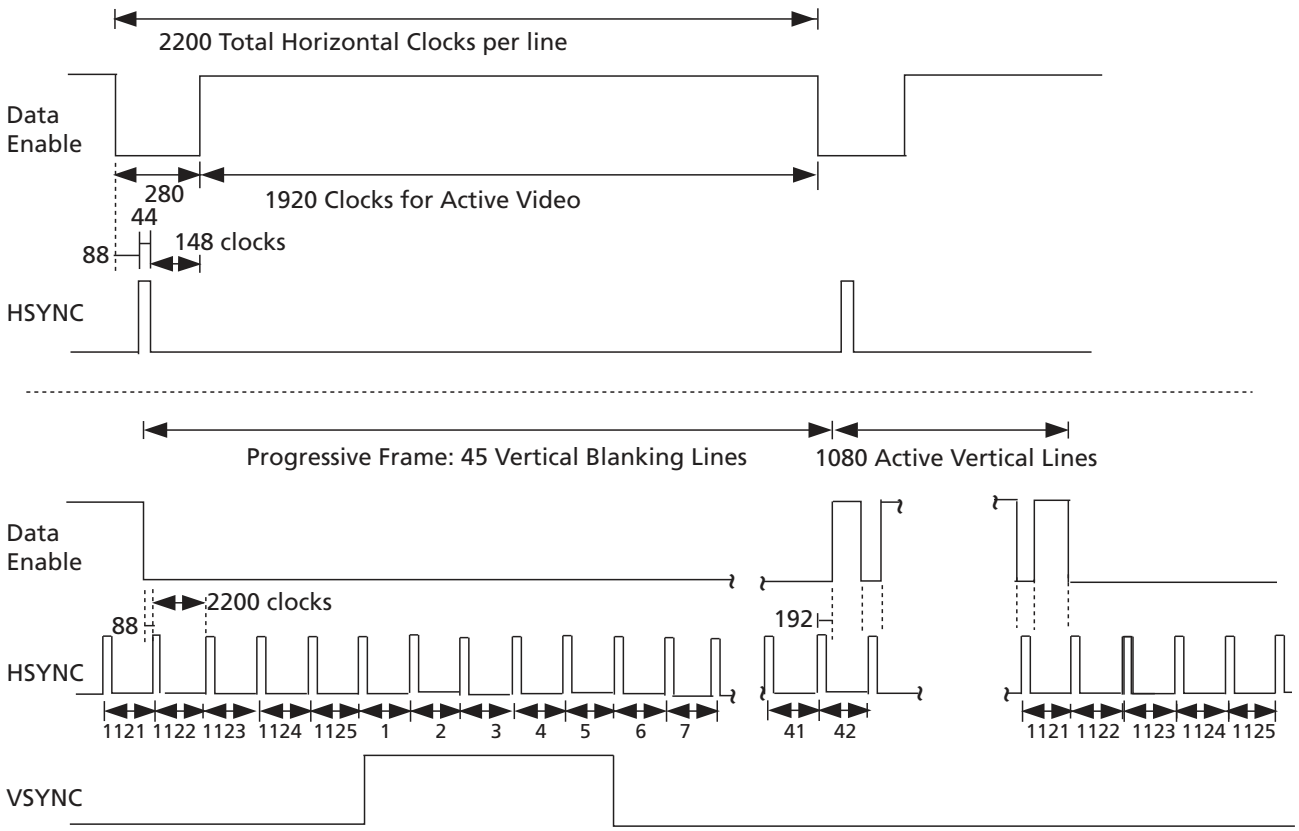


Figure 4-36: H:V:DE Output Timing 1920 x 1080p @ 59.94/60 (Format 16)

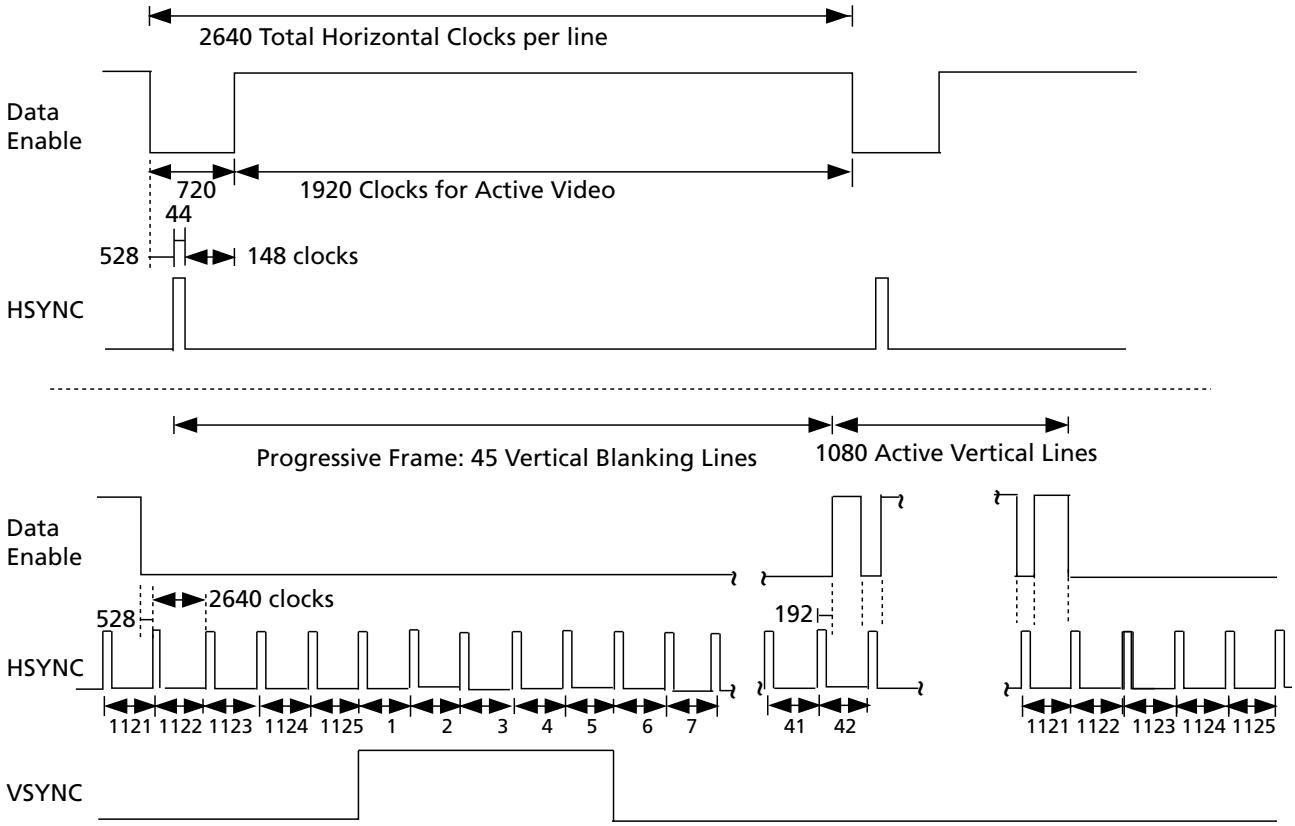


Figure 4-37: H:V:DE Output Timing 1920 x 1080p @ 50 (Format 31)

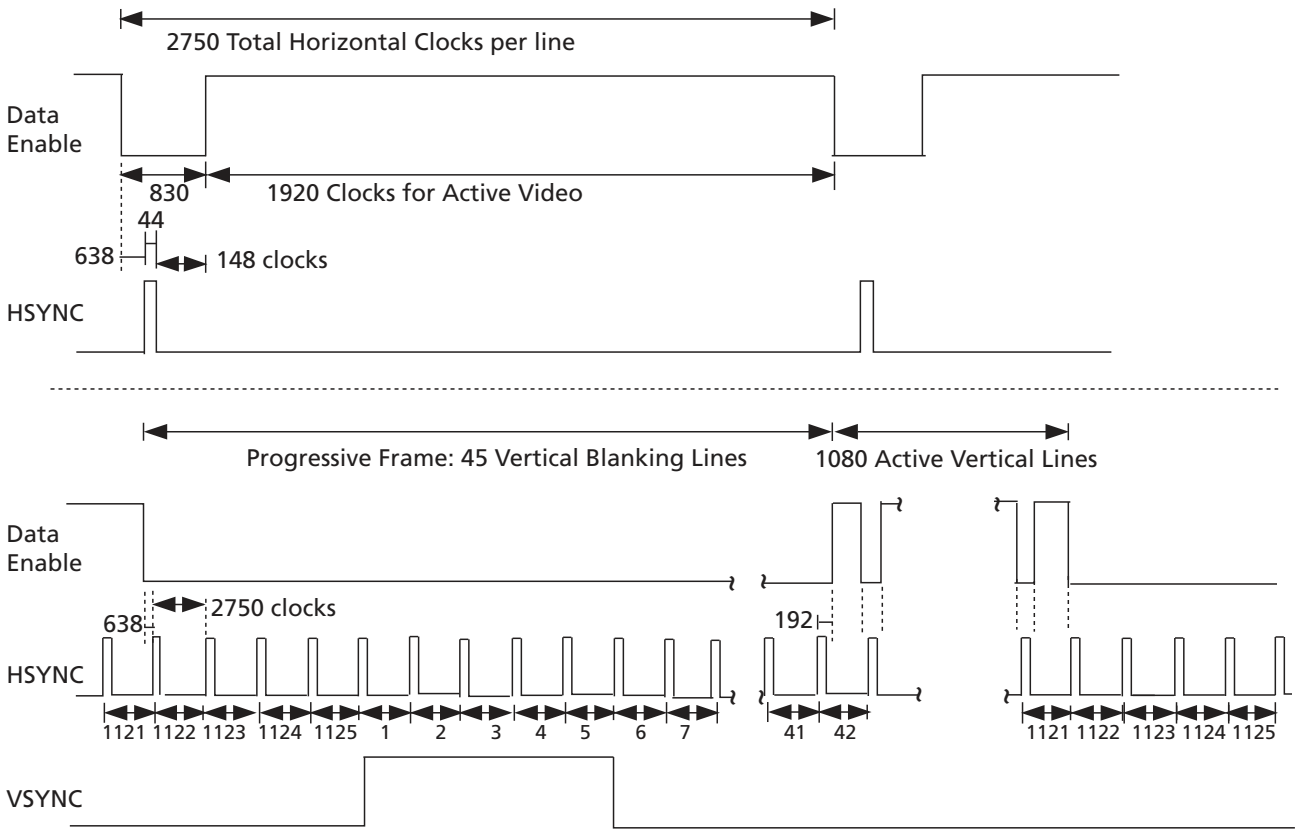


Figure 4-38: H:V:DE Output Timing 1920 x 1080p @ 23.94/24 (Format 32)

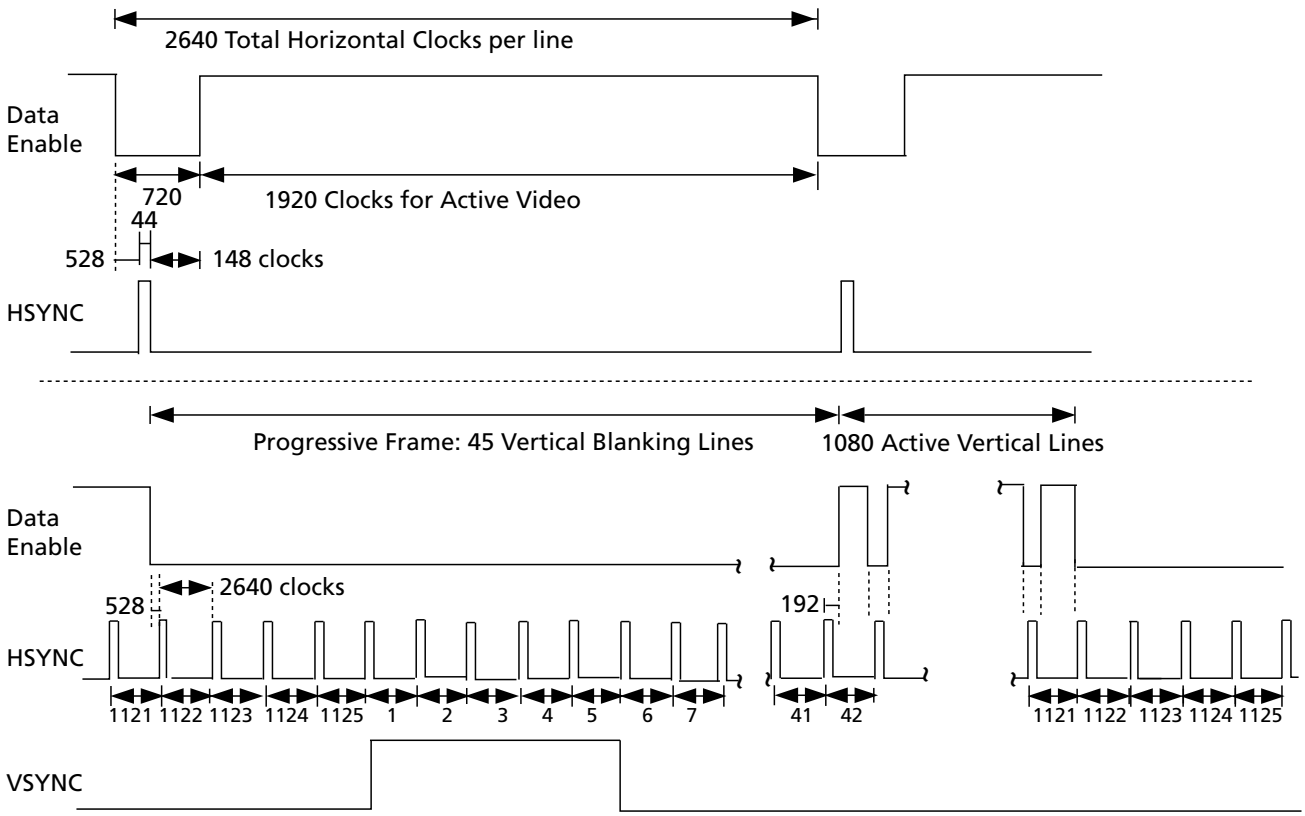


Figure 4-39: H:V:DE Output Timing 1920 x 1080p @ 25 (Format 33)

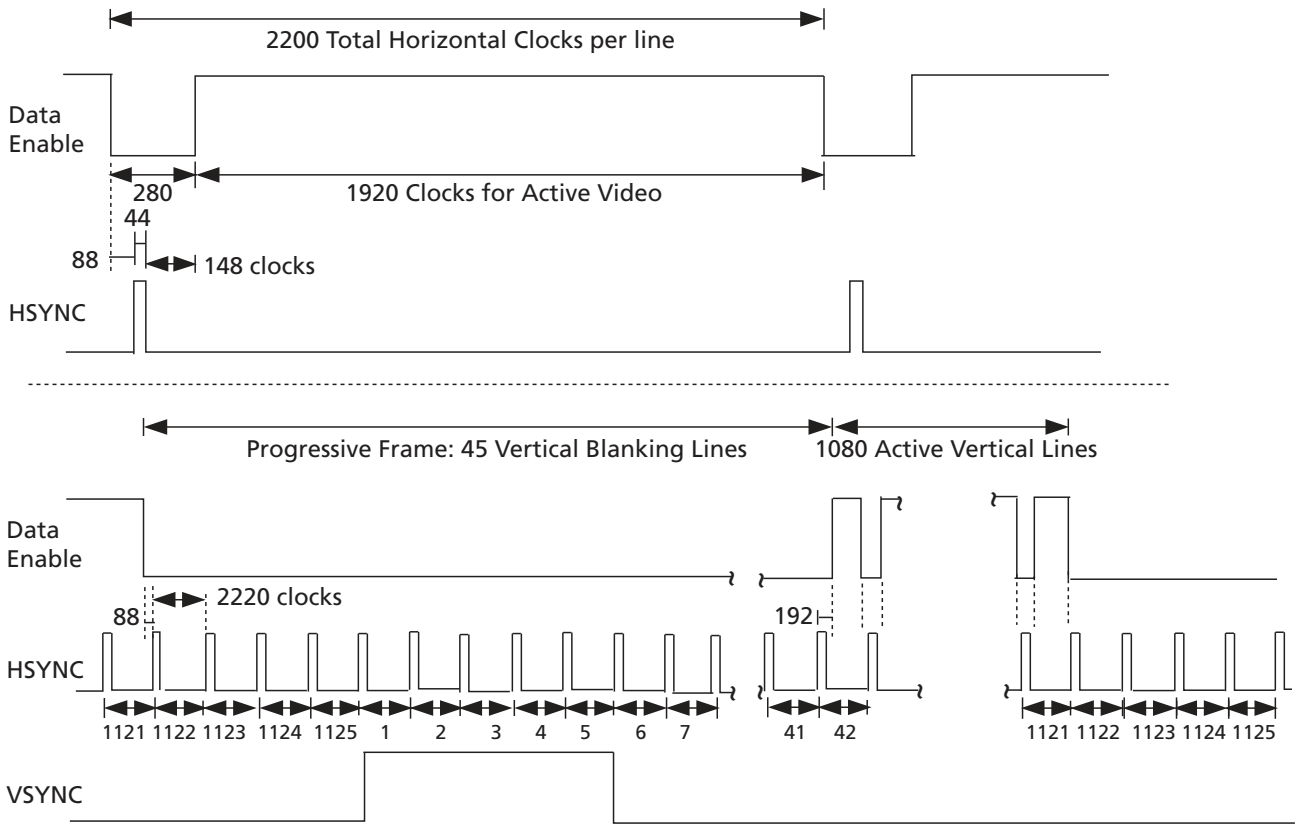


Figure 4-40: H:V:DE Output Timing 1920 x 1080p @ 29.97/30 (Format 34)

4.12 Automatic Video Standards Detection

Using the timing extracted from the received TRS signals, the GV7605 is able to identify the received video standard.

For inputs operating at 2.97Gb/s, the GV7605 measures the timing parameters of one of the two identical data streams. The Rate Selection/Indication bits and the VD_STD code may be used in combination to determine the video standard.

The total samples per line, active samples per line, total lines per field/frame and active lines per field/frame are all measured.

Four registers are provided to allow the system to read the video standard information from the device.

The raster structure registers also contain three status bits: STD_LOCK, INT/$\overline{\text{PROG}}$ and M. The STD_LOCK bit is set HIGH whenever the timing signal generator is fully synchronized to the incoming standard, and detects it as one of the supported formats. The INT/$\overline{\text{PROG}}$ bit is set HIGH if the detected video standard is interlaced and LOW if the detected video standard is progressive. M is set HIGH if the clock frequency includes the "1000/1001" factor denoting a 23.98, 29.97 or 59.94Hz frame rate.

The video standard code is reported in the VD_STD bits of the host interface register. Table 4-20 describes the 5-bit codes for the recognized video standards.

Table 4-20: Supported Video Standard Codes

Active Video Area	RATE_DET[1] $\overline{HD}$/Full HD	RATE_DET[0] SD/$\overline{HD}$	Lines per Field	Active Lines per Field	Words per Active Line	Words per Line	VD_STD [5:0]
1920x1080/60 (1:1)	1	0	1125	1080	1920	2200	2Bh
1920x1080/50 (1:1)	1	0	1125	1080	1920	2640	2Dh
1920x1080/60 (2:1)	1	0	1125	1080	3840	4400	2Ah
1920x1080/50 (2:1)	1	0	1250	1080	3840	5280	2Ch
1280x720/60 (1:1)	1	0	750	720	2560	3300	20h
1280x720/50 (1:1)	1	0	750	720	2560	3960	24h
1920x1080/30 (1:1)	1	0	1125	1080	3840	4400	2Bh
1920x1080/25 (1:1)	1	0	1125	1080	3840	5280	2Dh
1280x720/25 (1:1)	1	0	750	720	2560	7920	26h
1920x1080/24 (1:1)	1	0	1125	1080	3840	5500	30h
1280x720/24 (1:1)	1	0	750	720	2560	8250	28h
1920x1035/60 (2:1)	0	0	1125	1035	1920	2200	15h
1920x1080/50 (2:1)	0	0	1250	1080	1920	2376	14h
1920x1080/60 (2:1)	0	0	1125	1080	1920	2200	0Ah
1920x1080/50 (2:1)	0	0	1250	1080	1920	2640	0Ch
1920x1080/30 (1:1)	0	0	1125	1080	1920	2200	0Bh
1920x1080/25 (1:1)	0	0	1125	1080	1920	2640	0Dh
1920x1080/24 (1:1)	0	0	1125	1080	1920	2750	10h
1920x1080/25 (1:1) –	0	0	1125	1080	2304	2640	0Eh
1920x1080/24 (1:1) –	0	0	1125	1080	2400	2750	12h
1280x720/30 (1:1)	0	0	750	720	1280	3300	02h
1280x720/30 (1:1) – EM	0	0	750	720	2880	3300	03h
1280x720/50 (1:1)	0	0	750	720	1280	1980	04h
1280x720/50 (1:1) – EM	0	0	750	720	1728	1980	05h
1280x720/25 (1:1)	0	0	750	720	1280	3960	06h
1280x720/25 (1:1) – EM	0	0	750	720	3456	3960	07h
1280x720/24 (1:1)	0	0	750	720	1280	4125	08h
1280x720/24 (1:1) – EM	0	0	750	720	3600	4125	09h
1280x720/60 (1:1)	0	0	750	720	1280	1650	00h

Table 4-20: Supported Video Standard Codes (Continued)

Active Video Area	RATE_DET[1] HD/Full HD	RATE_DET[0] SD/HD	Lines per Field	Active Lines per Field	Words per Active Line	Words per Line	VD_STD [5:0]
1280x720/60 (1:1) – EM	0	0	750	720	1440	1650	01h
1440x487/60 (2:1)	x	1	525	244 or 243	1440	1716	16h
1440x507/60	x	1	525	254 or 253	1440	1716	17h
525-line 487 generic	x	1	525	–	–	1716	19h
525-line 507 generic	x	1	525	–	–	1716	1Bh
1440x576/50 (2:1) Or dual link progressive)	x	1	625	–	1440	1728	18h
625-line generic	x	1	625	–	–	1728	1Ah

Note: Other values of VD_STD[5:0] not listed in Table 4-20 may be reported in the host interface (0Fh, 11h, 13h, 1Dh, 1Eh, 3Ch). These values denote "unknown video format". The device will lock to the unknown format and output valid data. It is the responsibility of the user to determine any unknown video formats.

By default (after power up or after systems reset), the four RASTER_STRUCTURE, VD_STD, STD_LOCK and INT/$\overline{\text{PROG}}$ bits are set to zero. These registers are also cleared when the $\overline{\text{656\_BYPASS}}$ pin is LOW.

4.13 EDH Detection

The Error Detection and Handling (EDH) concept is based on making Cyclic Redundancy Check (CRC) calculations for each field of component digital video prior to transmission over a serial digital interface, such as Aviia. Separate CRC values are calculated for the entire video field, including blanking, and the active picture region. The calculated CRC values, along with status flags, are sent with the video data over the Aviia link.

The Aviia receiver also performs the same CRC calculations and compares the values to those sent across the link. If the CRC values are not identical to the transmitted values, an error can be indicated by the receive equipment. This allows the onset of errors, systematic of faulty or poor cable and connectors, to be detected and flagged.

EDH is fully defined by a recommended practice, RP 165, from the Society of Motion Pictures and Television Engineers (SMPTE). RP 165 defines the CRC calculation ranges, error status flag handling, and format and position of the EDH packet to be embedded in the video.

The GV7605 can be configured to automatically detect EDH packets, re-calculate CRC values and compare them with the values in the received EDH packets. Status flags are also extracted and can be accessed via the host interface.

4.13.1 EDH Packet Detection

The GV7605 determines if EDH packets are present in the incoming video data and asserts the EDH_DETECT status flag.

EDH_DETECT is set HIGH when EDH packets have been detected and remains HIGH until EDH packets are no longer present. It is set LOW at the end of the vertical blanking (falling edge of V) if an EDH packet has not been detected during vertical blanking.

EDH_DETECT can be programmed to be output on the multi-function output port pins. The EDH_DETECT bit is also available in the host interface.

4.13.2 EDH Flag Detection

The EDH flags for ancillary data, active picture, and full field areas are extracted from the detected EDH packets and placed in the EDH_FLAG_IN register.

When the EDH_FLAG_UPDATE_MASK bit in the host interface is set HIGH, the GV7605 updates the Ancillary Data, Full Field, and Active Picture EDH flags according to SMPTE RP165. The updated EDH flags are available in the EDH_FLAG_OUT register. The EDH packet output from the device contains these updated flags.

One set of flags is provided for both fields 1 and 2. The field 1 flag data is overwritten by the field 2 flag data.

When EDH packets are not detected, the UES flags in the EDH_FLAG_OUT register are set HIGH to signify that the received signal does not support Error Detection and Handling. In addition, the EDH_DETECT bit is set LOW. These flags are set regardless of the setting of the EDH_FLAG_UPDATE_MASK bit.

EDH_FLAG_OUT and EDH_FLAG_IN may be read via the host interface at any time during the received frame except on the lines defined in SMPTE RP165, when these flags are updated.

The GV7605 indicates the CRC validity for both active picture and full field CRCs. The AP_CRC_V bit in the host interface indicates the active picture CRC validity, and the FF_CRC_V bit indicates the full field CRC validity. When EDH_DETECT = LOW, these bits are cleared.

The EDH_FLAG_OUT and EDH_FLAG_IN register values remain set until overwritten by the decoded flags in the next received EDH packet. When an EDH packet is not detected during vertical blanking, the flag registers are cleared at the end of the vertical blanking period.

4.14 Video Signal Error Detection & Indication

The GV7605 includes a number of video signal error detection functions. These are provided to enhance operation of the device when operating in video mode ($\overline{656\_BYPASS}$ = HIGH). These features are not available in the other operating modes of the device (i.e. when $\overline{656\_BYPASS}$ = LOW).

Signal errors that can be detected include:

1. TRS errors.
2. HD line based CRC errors.
3. EDH errors.
4. HD line number errors.

The device maintains an ERROR_STAT register. Each error condition has a specific flag in the ERROR_STAT register, which is set HIGH whenever an error condition is detected.

An ERROR_MASK register is also provided, allowing the user to select which error conditions to be reported. Each bit of the ERROR_MASK register corresponds to a unique error type.

Separate SD_AUDIO_ERROR_MASK and HD_AUDIO_ERROR_MASK registers for SD and HD audio are also provided, allowing select error conditions to be reported. Each bit of each ERROR_MASK register corresponds to a unique error type.

By default (at power up or after system reset), all bits of the ERROR_MASK registers are zero, enabling all errors to be reported. Individual error detection may be disabled by setting the corresponding bit HIGH in the mask registers.

Error conditions are indicated by a $\overline{\text{VIDEO\_ERROR}}$ signal and an $\overline{\text{AUDIO\_ERROR}}$ signal, which are available for output on the multifunction I/O output pins. The two signals are also combined into a summary $\overline{\text{DATA\_ERROR}}$ signal, which is also available on the multifunction I/O pins. These signals are normally HIGH, but are set LOW by the device when an error condition has been detected.

These signals are a logical 'NOR' of the appropriate error status flags stored in the ERROR_STATUS register, which are gated by the bit settings in the ERROR_MASK registers. When an error status bit is HIGH and the corresponding error mask bit is LOW, the corresponding $\overline{\text{DATA\_ERROR}}$ signal is set LOW by the device.

The ERROR_STATUS registers, and correspondingly the $\overline{\text{DATA\_ERROR}}$, $\overline{\text{VIDEO\_ERROR}}$, and $\overline{\text{AUDIO\_ERROR}}$ signals, are cleared at the start of the next video field or when read via the host interface, which ever condition occurs first.

All bits of the ERROR_STATUS registers are also cleared under any of the following conditions:

1. LOCKED signal = LOW.
2. $\overline{\text{656\_BYPASS}}$ = LOW.
3. When a change in video standard has been detected.
4. $\overline{\text{RESET}}$ = LOW

Table 4-21 shows the VIDEO_ERROR_STATUS register and VIDEO_ERROR_MASK bits.

Note: Since the error indication registers are cleared once per field, if an external host micro is polling the error registers periodically, an error flag may be missed if it is intermittent, and the polling frequency is less than the field rate.

Table 4-21: Video Error Status Register and Error Disable Mask Bits

Video Error Stat Register	Video Error Mask Register
SAV_ERR (02h, 03h)	SAV_ERR_MASK (037h, 038h)
EAV_ERR (02h, 03h)	EAV_ERR_MASK (037h, 038h)
YCRC_ERR (02h, 03h)	YCRC_ERR_MASK (037h, 038h)
CCRC_ERR (02h, 03h)	CCRC_ERR_MASK (037h, 038h)
LNUM_ERR (02h, 03h)	LNUM_ERR_MASK (037h, 038h)
YCS_ERR (02h, 03h)	YCS_ERR_MASK (037h, 038h)
CCS_ERR (02h, 03h)	CCS_ERR_MASK (037h, 038h)
AP_CRC_ERR (02h)	AP_CRC_ERR_MASK (037h)
FF_CRC_ERR (02h)	FF_CRC_ERR_MASK (037h)

Note: See Section 4.17 for Audio Error Status.

4.14.1 TRS Error Detection

TRS error flags are generated by the GV7605 under the following two conditions:

1. A phase shift in received TRS timing is observed.
2. The received TRS Hamming codes are incorrect.

Both SAV and EAV TRS words are checked for timing and data integrity errors.

For HD mode, only the Y channel TRS codes are checked for errors.

ForFull HD signals, only DS1 TRS codes are checked for errors.

Both 8-bit and 10-bit TRS code words are checked for errors.

The SAV_ERR bit of the ERROR_STAT register is set HIGH when an SAV TRS error is detected.

The EAV_ERR bit of the ERROR_STAT register is set HIGH when an EAV TRS error is detected.

4.14.2 Line Based CRC Error Detection

The GV7605 calculates line based CRCs for HD video signals. CRC calculations are done for each 10-bit channel (Y and C, DS1 and DS2).

These calculated CRC values are compared with the received CRC values.

If a mismatch in the calculated and received CRC values is detected for the Y channel data, the YCRC_ERR bit in the ERROR_STAT register is set HIGH.

If a mismatch in the calculated and received CRC values is detected for the C channel data, the CCRC_ERR bit in the ERROR_STAT register is set HIGH.

Y or C CRC errors are also generated if CRC values are not received.

Line based CRC errors are only generated when the device is operating in HD mode.

Note: By default, 8-bit to 10-bit TRS remapping is enabled. If an 8-bit input is used, the HD CRC check is based on the 10-bit remapped value, not the 8-bit value, so the CRC Error Flag is incorrectly asserted and should be ignored. If 8-bit to 10-bit remapping is enabled, then CRC correction and insertion should be enabled by setting the CRC_INS_MASK bit in the PROC_DISABLE register LOW. This ensures that the CRC values are updated.

4.14.3 EDH CRC Error Detection

The GV7605 also calculates Full Field (FF) and Active Picture (AP) CRC's according to SMPTE RP165 in support of Error Detection and Handling packets in SD signals.

These calculated CRC values are compared with the received CRC values.

Error flags for AP and FF CRC errors are provided and are shared between the field 1 and field 2 error conditions.

The AP_CRC_ERR bit in the VIDEO_ERROR_STATUS register is set HIGH when an Active Picture CRC mismatch has been detected in field 1 or 2.

The FF_CRC_ERR bit in the VIDEO_ERROR_STATUS register is set HIGH when a Full Field CRC mismatch has been detected in field 1 or 2.

EDH CRC errors are only indicated when the device is operating in SD mode and when the device has correctly received EDH packets.

4.14.4 HD Line Number Error Detection

If a mismatch in the calculated and received line numbers is detected, the LNUM_ERR bit in the VIDEO_ERROR_STATUS register is set HIGH.

4.15 Ancillary Data Detection & Indication

The horizontal and vertical blanking regions of a digital video signal may be used to carry ancillary data packets. The payload of the ancillary data packet can be used to carry user-defined or proprietary data, which can be sent between an Aviia transmitter and receiver.

The ancillary data packet must be formatted according to Figure 4-41. The packet must always begin with the Ancillary Data Flag (ADF), defined as the following 10-bit word sequence: 000h, 3FFh, 3FFh.

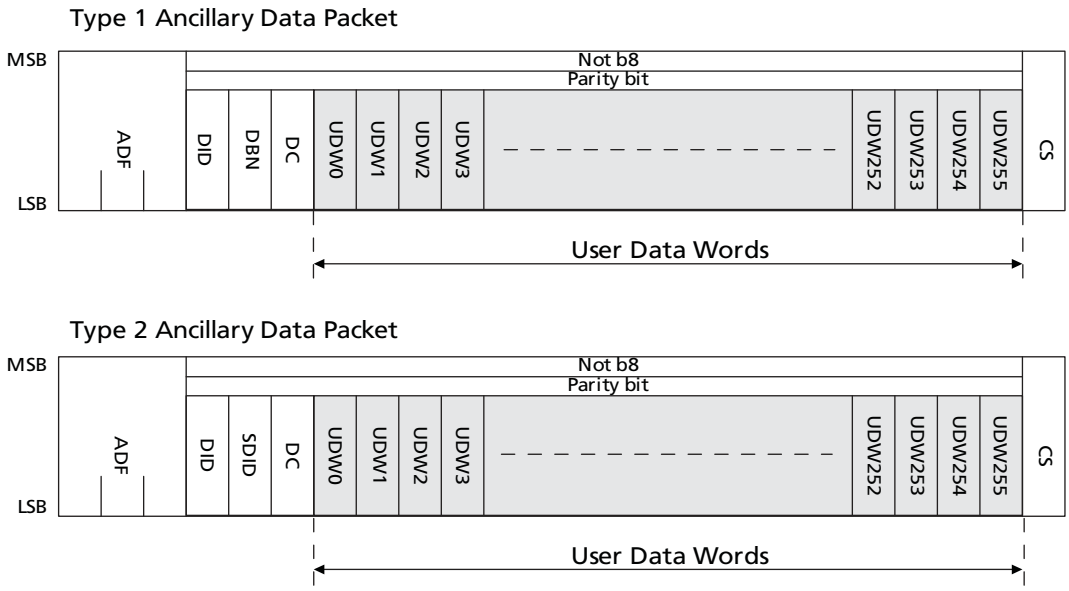


Figure 4-41: Ancillary Data Packets

The next data word is the 8-bit Data ID (DID), used to define the contents of the packet. For example, a unique DID can be used to denote alarm data, with another DID to denote status data. After the DID, there are two possible options, as shown in Figure 4-41.

A Type 1 packet defines an 8-bit Data Block Number (DBN) sequence, used to distinguish successive packets with the same DID. The DBN simply increments with each packet of the same DID, between 0 and 255.

For a Type 2 packet, an 8-bit Secondary Data ID (SDID) word is defined, which can be used to denote variants of payloads with the same DID. For example, packets with a DID to denote error data may distinguish different error types using unique SDID's.

After the DBN or SDID, the next data work is the 8-bit Data Count (DC). This word must be set to the number of user data words (UDW) that follow the DC, and must not exceed 255 (maximum payload size).

The final word of the ancillary data packet is the 9-bit Checksum (CS). The CS value must be equal to the nine least significant bits of the sum of the nine least significant bits of the DID, the DBN or the SDID, the DC and all user data words (UDW) in the packet.

The GV7605 detects ancillary data in both the vertical and horizontal ancillary data spaces. Status signal outputs Y/1ANC and C/2ANC are provided to indicate the position of ancillary data in the output data streams. These signals may be programmed for output on the multi-function I/O port pins (STAT[5:0]).

The GV7605 indicates the presence of all types of ancillary data by simply detecting the 000h, 3FFh, 3FFh (00h, FFh, FFh for 8-bit video) ancillary data preamble.

Note: Both 8 and 10-bit ancillary data preambles are detected by the device.

By default (at power up or after system reset) the GV7605 indicates all types of ancillary data. Up to 5 types of ancillary data can be specifically programmed for recognition.

For HD video signals, ancillary data may be placed in both the Y and Cb/Cr video data streams separately. For SD video signals, the ancillary data is multiplexed and combined into the YCbCr data space.

For Full HD signals, ancillary data may be placed in either or both of the data streams. Both data streams are examined for ancillary data.

When operating in HD mode, the Y/1ANC signal is HIGH whenever ancillary data is detected in the Luma data stream, and C/2ANC is HIGH whenever ancillary data is detected in the Chroma data stream. The signals are asserted HIGH at the start of the ancillary data preamble, and remain HIGH until after the ancillary data checksum.

When detecting ancillary data in Full HD data, the Y/1ANC status output is HIGH whenever DS1 ancillary data is detected and the C/2ANC status output is HIGH whenever DS2 ancillary data is detected.

When operating in SD mode, the Y/1ANC and C/2ANC signals depend on the output data format. For 20-bit demultiplexed data, the Y/1ANC and C/2ANC signals operate independently to indicate the first and last ancillary Data Word position in the Luma and/or Chroma data streams. For 10-bit multiplexed data, the Y/1ANC signal is HIGH whenever ancillary data is detected, and the C/2ANC signal is always LOW.

When operating in Full HD mode, the Y/1ANC and C/2ANC flags are both zero if 10-bit multiplexed output format is selected.

These status signal outputs are synchronous with PCLK and may be used as clock-enables for external logic, or as write-enables for an external FIFO or other memory devices.

The operation of the Y/1ANC and C/2ANC signals is shown in Figure 4-42, Figure 4-43, Figure 4-44 and Figure 4-45.

Note: When I/O processing is disabled, the Y/1ANC and C/2ANC flags may toggle, but they are invalid and should be ignored.

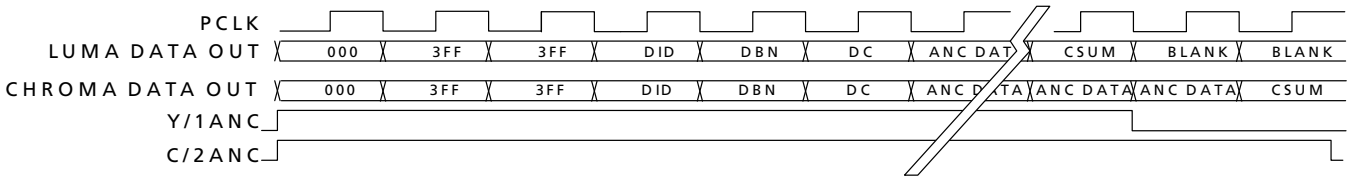


Figure 4-42: Y/1ANC and C/2ANC Signal Timing - HD 20-bit

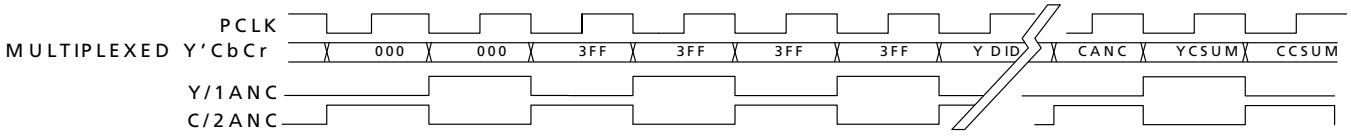


Figure 4-43: Y/1ANC and C/2ANC Signal Timing - HD 10-bit

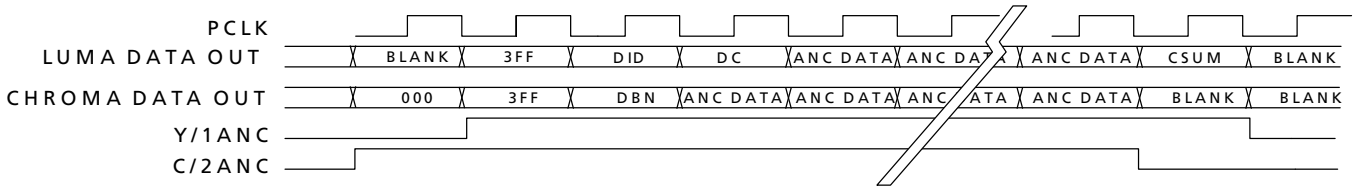


Figure 4-44: Y/1ANC and C/2ANC Signal Timing - SD 20-bit

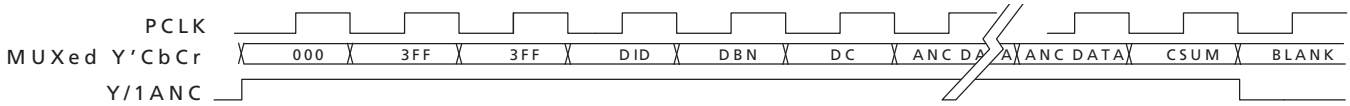


Figure 4-45: Y/1ANC and C/2ANC Signal Timing - SD 10-bit

4.15.1 Programmable Ancillary Data Detection

As described above in Section 4.15, the GV7605 detects and indicates all ancillary data types by default.

It is possible to program which ancillary data types are to be detected and indicated. Up to 5 different ancillary data types may be programmed for detection by the GV7605 in the ANC_TYPE_DS1 registers for SD and HD data.

When so programmed, the GV7605 only indicates the presence of the specified ancillary data types, ignoring all other ancillary data. For each data type to be detected, the user must program the DID and/or SDID of that ancillary data type. In the case where no DID or SDID values are programmed, the GV7605 indicates the presence of all ancillary data. In the case where one or more, DID and/or SDID values have been programmed, then only those matching data types are detected and indicated.

The timing of the Y/1ANC and C/2ANC signals in this case is as shown in Figure 4-42, Figure 4-43, Figure 4-44 and Figure 4-45.

The GV7605 compares the received DID and/or SDID with the programmed values. If a match is found, ancillary data is indicated.

For any DID or SDID value set to zero, no comparison or match is made. For example, if the DID is programmed and the SDID is not programmed, the GV7605 only detects a match to the DID value.

If both DID and SDID values are non-zero, then the received ancillary data type must match both the DID and SDID before Y/1ANC and/or C/2ANC is set HIGH.

4.15.2 Ancillary Data Checksum Error

The GV7605 calculates checksums for all received ancillary data.

These calculated checksums are compared with the received ancillary data checksum words.

If a mismatch in the calculated and received checksums is detected, then a checksum error is indicated.

When operating in HD mode, the device makes comparisons on both the Y and C channels separately. If an error condition in the Y channel is detected, the YCS_ERR bit in the VIDEO_ERROR_STATUS register is set HIGH. If an error condition in the C channel is detected, the CCS_ERR bit in the VIDEO_ERROR_STATUS register is set HIGH.

When operating in Full HD mode, the device makes comparisons on both the Y (DS1) and C (DS2) channels separately. If an error condition in the Y channel is detected, the YCS_ERR bit in the VIDEO_ERROR_STATUS register is set HIGH. If an error condition in the C channel is detected, the CCS_ERR bit in the VIDEO_ERROR_STATUS register is set HIGH.

When operating in SD mode, only the YCS_ERR bit is set HIGH when checksum errors are detected.

4.15.2.1 Programmable Ancillary Data Checksum Calculation

As described above, the GV7605 calculates and compares checksum values for all ancillary data types by default. It is possible to program which ancillary data types are checked as described in Section 4.15.1.

When so programmed, the GV7605 only checks ancillary data checksums for the specified data types, ignoring all other ancillary data.

The YCS_ERR and/or CCS_ERR bits in the VIDEO_ERROR_STATUS register are only set HIGH if an error condition is detected for the programmed ancillary data types.

4.16 Video Error Correction

In addition to error detection and indication, the GV7605 can also correct errors, inserting corrected code words, checksums and CRC values into the data stream.

The following processing can be performed by the GV7605:

1. TRS error correction and insertion.
2. HD line based CRC correction and insertion.
3. EDH CRC error correction and insertion.
4. HD line number error correction and insertion.
5. Illegal code re-mapping.
6. Ancillary data checksum error correction and insertion.

All of the above features are only available in video mode ($\overline{656\_BYPASS}$ = HIGH).

To enable these features, the PROC_EN pin must be set HIGH, and the individual feature must be enabled via bits in the PROC_DISABLE register.

The PROC_DISABLE register contains one bit for each processing feature allowing each one to be enabled/disabled individually.

By default (at power up or after system reset), all of the PROC_DISABLE register bits are LOW, enabling all of the processing features.

To disable an individual processing feature, set the corresponding PROC_DISABLE bit HIGH in the PROC_DISABLE register.

Table 4-22: PROC_DISABLE Register Bits

Processing Feature	PROC_DISABLE Register Bit
TRS error correction and insertion	TRS_INS
Y and C line based CRC error correction	CRC_INS
Y and C line number error correction	LNUM_INS
Ancillary data check sum correction	ANC_CHECKSUM_INSERTION
EDH CRC error correction	EDH_CRC_INS
Illegal code re-mapping	ILLEGAL_WORD_REMAP
H timing signal configuration	H_CONFIG
Update EDH Flags	EDH_FLAG_UPDATE
Audio Data Extraction	AUDIO_SEL
Ancillary Data Extraction	ANC_DATA_EXT
Audio Extraction	AUD_EXT

4.16.1 TRS Correction & Insertion

When TRS Error Correction and Insertion is enabled, the GV7605 generates and overwrites TRS code words as required.

TRS Word Generation and Insertion is performed using the timing generated by the Timing Signal Generator, providing an element of noise immunity over using just the received TRS information.

This feature is enabled when the PROC_EN pin is HIGH and the TRS_INS bit in the PROC_DISABLE register is set LOW.

Note: Inserted TRS code words will always be 10-bit compliant, irrespective of the bit depth of the incoming video stream.

4.16.2 Line Based CRC Correction & Insertion

When CRC Error Correction and Insertion is enabled, the GV7605 generates and inserts line based CRC words into both the Y and C channels of the data stream.

Line based CRC word generation and insertion only occur in HD mode, and is enabled in when the PROC_EN pin is HIGH and the CRC_INS bit in the PROC_DISABLE register is set LOW.

4.16.3 Line Number Error Correction & Insertion

When Line Number Error Correction and Insertion is enabled, the GV7605 calculates and inserts line numbers into the output data stream. Re-calculated line numbers are inserted into both the Y and C channels.

Line number generation is in accordance with the relevant HD or Full HD video standard as determined by the Automatic Standards Detection block.

This feature is enabled when the device is operating in HD mode, the PROC_EN pin is HIGH and the LNUM_INS bit in the PROC_DISABLE register is set LOW.

4.16.4 Ancillary Data Checksum Error Correction & Insertion

When ancillary data Checksum Error Correction and Insertion is enabled, the GV7605 generates and inserts ancillary data checksums for all ancillary data words by default.

Where user specified ancillary data has been programmed (see Section 4.15.1), only the checksums for the programmed ancillary data are corrected.

This feature is enabled when the PROC_EN pin is HIGH and the ANC_CSUM_INS bit in the PROC_DISABLE register is set LOW.

4.16.5 EDH CRC Correction & Insertion

When EDH CRC Error Correction and Insertion is enabled, the GV7605 generates and overwrites full field and active picture CRC check-words.

Additionally, the device sets the active picture and full field CRC 'V' bits HIGH in the EDH packet. The AP_CRC_V and FF_CRC_V register bits only report the received EDH validity flags.

EDH FF and AP CRC's are only inserted when the device is operating in SD mode, and if the EDH data packet is detected in the received video data.

Although the GV7605 modifies and inserts EDH CRC's and EDH packet checksums, EDH error flags are only updated when the EDH_FLAG_UPDATE bit is LOW.

This feature is enabled in SD mode, when the PROC_EN pin is HIGH and the EDH_CRC_INS bit in the PROC_DISABLE register is set LOW.

4.16.6 Illegal Word Remapping

All words within the active picture (outside the horizontal and vertical blanking periods), between the values of 3FCh and 3FFh are re-mapped to 3FBh. All words within the active picture area between the values of 000h and 003h are remapped to 004h.

This feature is enabled when the PROC_EN pin is HIGH and the ILLEGAL_WORD_REMAP bit in the PROC_DISABLE register is set LOW.

4.16.7 TRS and Ancillary Data Preamble Remapping

8-bit TRS and ancillary data preambles are re-mapped to 10-bit values. 8-bit to 10-bit mapping of TRS headers is only supported if the TRS values are 3FC 000 000. Other values such as 3FD, 3FE, 001, and 003 are not supported. This feature is enabled by default, and cannot be disabled via the PROC_DISABLE register.

4.16.8 Ancillary Data Extraction

Ancillary data may be extracted externally from the GV7605 output stream using the Y/1ANC and C/2ANC signals, and external logic.

As an alternative, the GV7605 includes a memory block, which extracts ancillary data using read access via the host interface to ease system implementation. The memory block stores up to 2048 x 16 bit words of ancillary data in two separate 1024 word memory banks. Data is accessed from both memory banks using the same host interface addresses, 800h to BFFh (see Table 4-37: Ancillary Data Extraction Memory Access Registers).

The device writes the contents of ANC packets into memory, starting with the first Ancillary Data Flag (ADF), followed by up to 1024 words.

All Data Identification (DID), Secondary Data Identification (SDID), Data Count (DC), user data, and checksum words are written into the device memory.

The device detects ancillary data packet DID's placed anywhere in the video data stream, including the active picture area.

In HD and full HD modes, ancillary data from the Y channel or DS1 is placed in the Least Significant Word (LSW) of the memory, allocated to the lower 8 bits of each memory address.

Ancillary data from the C channel or DS2 is placed in the Most Significant Word (MSW) (upper 8 bits) of each memory address.

In SD mode, ancillary data is placed in the LSW of the memory. The MSW is set to zero.

If the ANC_TYPE registers are all set to zero, the device extracts all types of ancillary data. If programmable ancillary data extraction is required, then up to five types of ancillary data to be extracted can be programmed in the ANC_TYPE registers (see Section 4.15.1).

Additionally, the lines from which the packets are to be extracted can be programmed into the ANC_LINEA[10:0] and ANC_LINEB[10:0] registers, allowing ancillary data from a maximum of two lines per frame to be extracted. If only one line number register is programmed (with the other set to zero), ancillary data packets are extracted from one line per frame only. When both registers are set to zero, the device extracts packets from all lines.

To start Ancillary Data Extraction, the ANC_DATA_EXT_MASK bit of the host interface must be set LOW. Ancillary Data Packet Extraction begins in the following frame (see Figure 4-46: Ancillary Data Extraction - Step A).

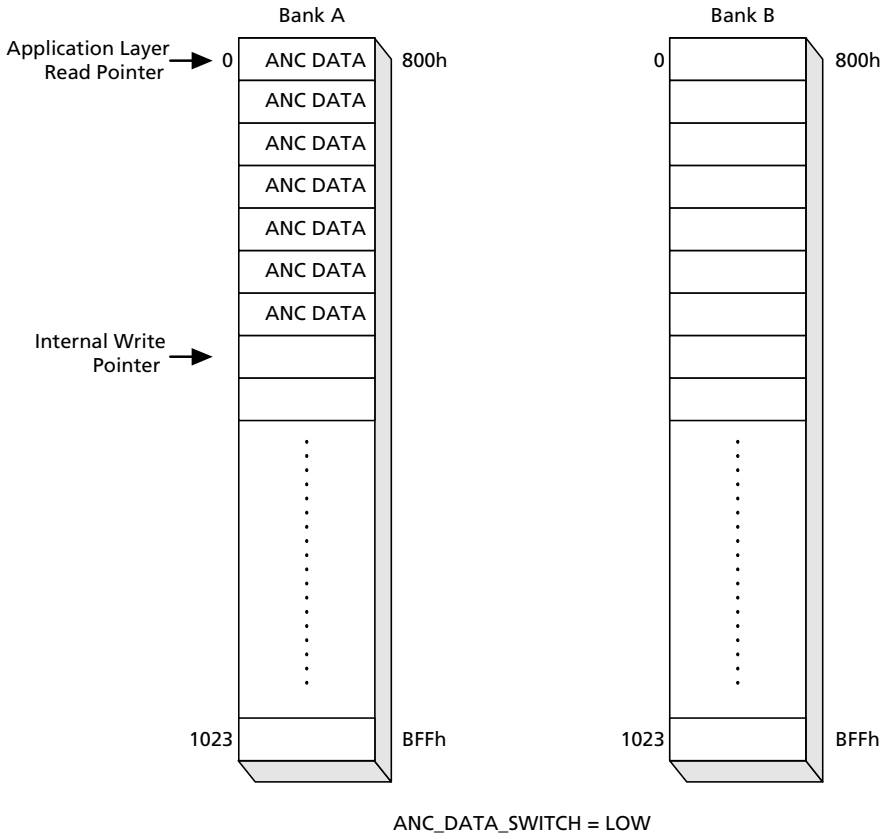


Figure 4-46: Ancillary Data Extraction - Step A

Ancillary data is written into Bank A until full. The Y/1ANC and C/2ANC output flags can be used to determine the length of the ancillary data extracted and when to begin reading the extracted data from memory.

While the ANC_DATA_EXT_MASK bit is set LOW, the ANC_DATA_SWITCH bit can be set HIGH during or after reading the extracted data. New data is then written into Bank B (up to 1024 x 16-bit words), at the same host interface addresses (see Figure 4-47: Ancillary Data Extraction - Step B).

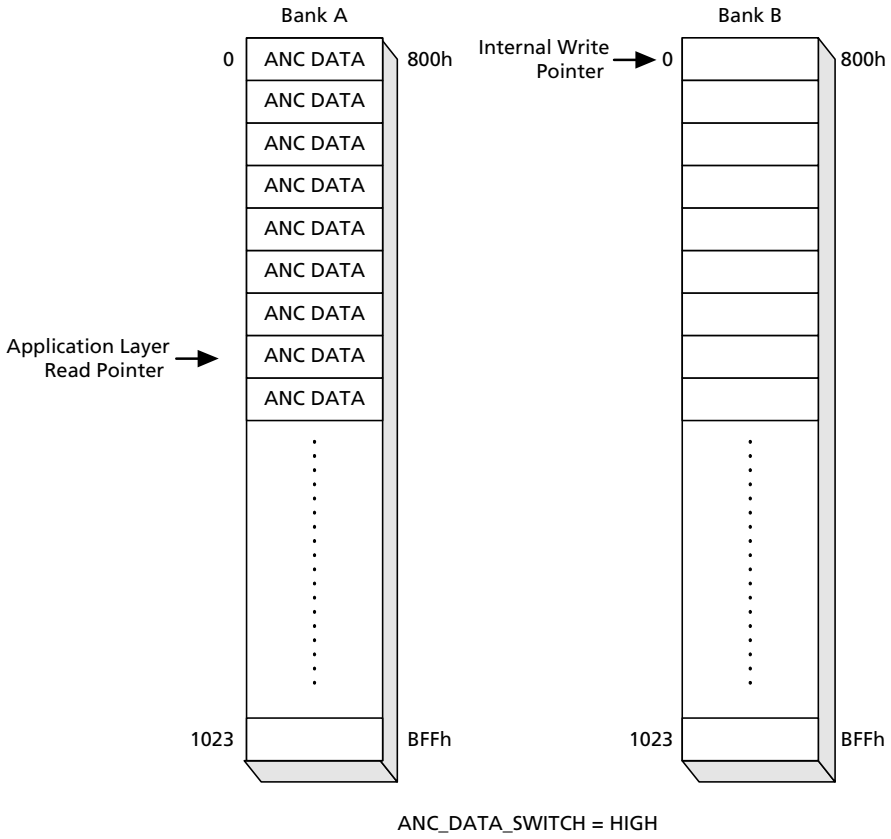


Figure 4-47: Ancillary Data Extraction - Step B

To read the new data, toggle the ANC_DATA_SWITCH bit LOW. The old data in Bank A is cleared to zero and extraction continues in Bank B (see Figure 4-48: Ancillary Data Extraction - Step C).

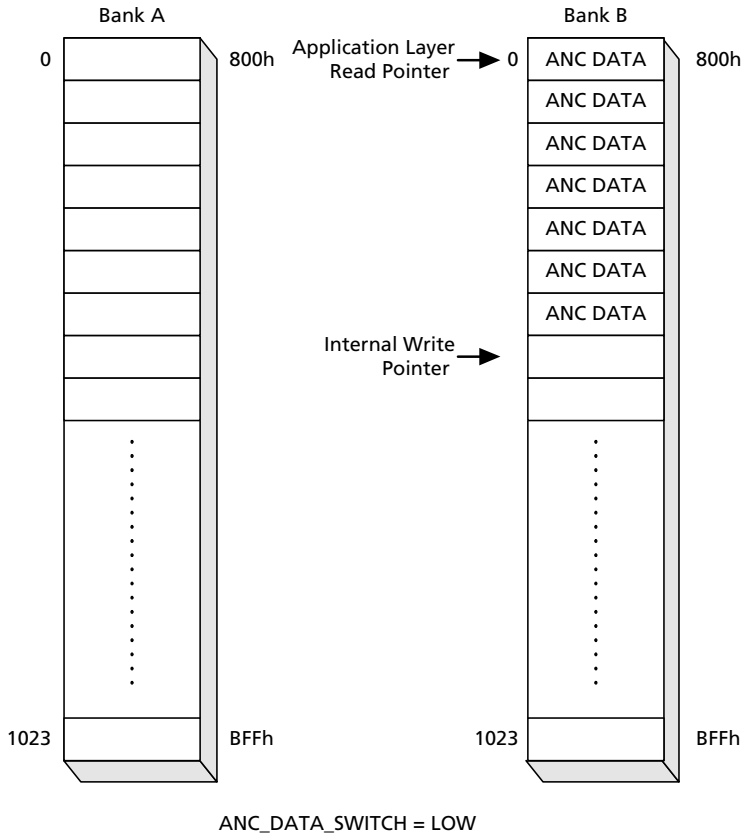


Figure 4-48: Ancillary Data Extraction - Step C

If the ANC_DATA_SWITCH bit is not toggled, extracted data is written into Bank B until full. To continue extraction in Bank A, the ANC_DATA_SWITCH bit must be toggled HIGH (see Figure 4-49: Ancillary Data Extraction - Step D).

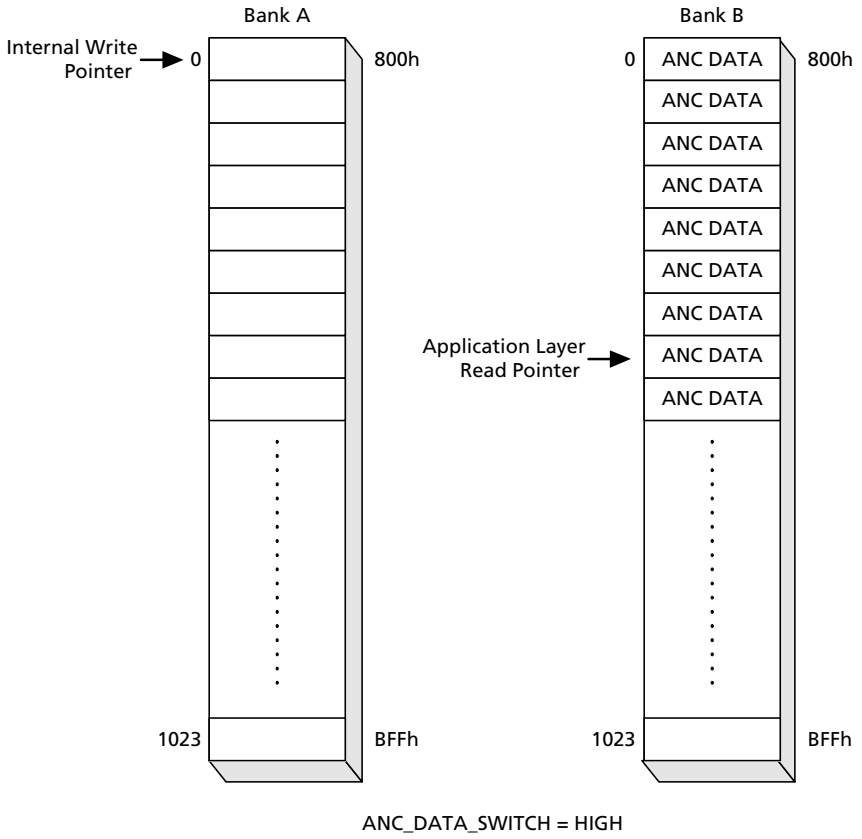


Figure 4-49: Ancillary Data Extraction - Step D

Toggling the ANC_DATA_SWITCH bit LOW returns the process to step A (Figure 4-46).

Note: Toggling the ANC_DATA_SWITCH must occur at a time when no extraction is taking place, i.e. when the both the Y/1ANC and C/2ANC signals are LOW.

To turn extraction off, the ANC_DATA_EXT_MASK bit must be set HIGH.

In HD mode, the device can detect ancillary data packets in the Luma video data only, Chroma video data only, or both. By default (at power-up or after a system reset) the device extracts ancillary data packets from the Luma channel only.

In Full HD mode, the device can detect ancillary data packets in Luma video (DS1) only, Chroma video (DS2) only, or both. By default (at power-up or after a system reset) the device extracts ancillary data packets from DS1 only.

To extract packets from the Chroma/DS2 channel only, the HD_ANC_C/2 bit of the host interface must be set HIGH. To extract packets from both Luma/DS1 and Chroma/DS2 video data, the HD_ANC_Y/1_C/2 bit must be set HIGH (the setting of the HD_ANC_C/2 bit is ignored).

The default setting of both the HD_ANC_C/2 and HD_ANC_Y/1_C/2 is LOW. The setting of these bits is ignored when the device is configured for SD video standards.

Ancillary data packet extraction and deletion is disabled when the PROC_EN pin is set LOW.

After extraction, the ancillary data may be deleted from the video stream by setting the ANC_DATA_DELETE bit of the host interface HIGH. When set HIGH, all existing ancillary data is removed and replaced with blanking values. If any of the ANC_TYPE registers are programmed with a DID and/or DID and SDID, only the ancillary data packets with the matching ID's are deleted from the video stream.

Note1: After the ancillary data determined by the ANC_TYPE registers has been deleted, other existing ancillary data may not be contiguous. The device does not concatenate the remaining ancillary data.

Note2: Reading extracted ancillary data from the host interface must be performed while there is a valid video signal present at the serial input and the device is locked (LOCKED signal is HIGH).

4.17 Audio De-embedder

The GV7605 includes an integrated audio de-embedder which is enabled by default in video mode. It can be disabled by setting the AUDIO_EN pin LOW, or by setting the host interface AUD_EXT_MASK bit to HIGH, or by keeping PROC_EN pin LOW. In non-video modes, the audio de-embedder is not active.

Up to eight channels of audio may be extracted from the received serial digital video stream. The output signal formats supported by the device include AES/EBU or S/PDIF, I^2S (default) and industry standard serial digital formats.

16, 20 and 24-bit audio bit depths are supported for 48kHz synchronous audio for SD. 16, 20 and 24-bit, 48kHz, synchronous or asynchronous audio bit depths are supported for HD mode.

Additional audio processing features include audio mute on loss of lock, de-embed and delete, group selection, audio output re-mapping, ECC error detection and correction (HD mode only), and audio channel status extraction.

4.17.1 Serial Audio Data I/O Signals

The Serial Audio Data I/O pins are listed in Table 4-23: Serial Audio Pin Descriptions.

Table 4-23: Serial Audio Pin Descriptions

Pin Name	Description
AUDIO_EN	Enable Input for Audio Processing
AOUT1/2	Serial Audio Output; Channels 1 and 2
AOUT3/4	Serial Audio Output; Channels 3 and 4
AOUT5/6	Serial Audio Output; Channels 5 and 6
AOUT7/8	Serial Audio Output; Channels 7 and 8
ACLK	64fs clock

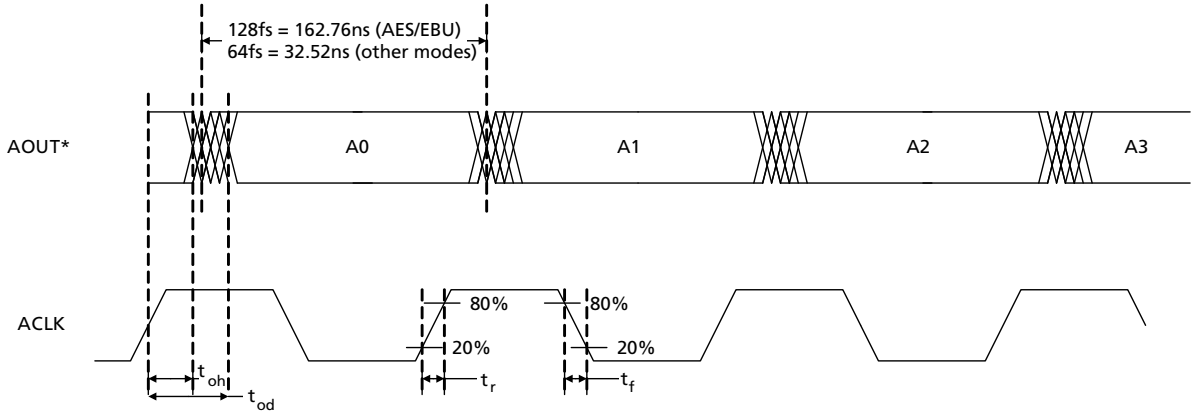
Table 4-23: Serial Audio Pin Descriptions (Continued)

Pin Name	Description
WCLK	Word clock
MCLK	Audio Master Clock, selectable 128fs, 256fs, or 512fs

The timing of the serial audio output signals, the WCLK output signal, and the ACLK output signal is as shown in Figure 4-50: ACLK to Data and WCLK Signal Output Timing.

Audio I/O Timing Specs:

Audio Outputs:



Audio Outputs

	3.3V						1.8V					
	t_{oh}	$\frac{t_r}{t_f}$ (min)	Cload	t_{od}	$\frac{t_r}{t_f}$ (max)	Cload	t_{oh}	$\frac{t_r}{t_f}$ (min)	Cload	t_{od}	$\frac{t_r}{t_f}$ (max)	Cload
AOUT	1.500ns	0.600ns	6pF	7.000ns	2.200ns	15pF	1.500ns	0.600ns	6pF	7.000ns	2.300ns	15pF

Figure 4-50: ACLK to Data and WCLK Signal Output Timing

When AUDIO_EN is set HIGH, audio extraction is enabled and the audio output signals are extracted from the video data stream. When set LOW, the serial audio outputs, ACLK and WCLK outputs are set LOW.

In addition, all functional logic associated with audio extraction is disabled to reduce power consumption.

4.17.2 Serial Audio Data Format Support

The GV7605 supports the following serial audio data formats:

- I^2S (default)
- AES/EBU or S/PDIF
- Serial Audio Left Justified, MSB First
- Serial Audio Left Justified, LSB First
- Serial Audio Right Justified, MSB First
- Serial Audio Right Justified, LSB First (this mode is not supported in SD)

By default (at power up or after system reset) I^2S is selected. The other data formats are selectable via the host interface using the AMA/AMB[1:0] bits.

Table 4-24: Audio Output Formats

AMA/AMB[1:0]	Audio Output Format
00	AES/EBU or S/PDIF audio output
01	Serial audio output: Left Justified; MSB first
10	Serial audio output: Right Justified; MSB first
11	I^2S (Default)

The serial audio output formats may use LSB first according to the settings of the control bits LSB_FIRSTA, LSB_FIRSTB, LSB_FIRSTC, and LSB_FIRSTD. When in I^2S mode, these control bits must all be set LOW (default).

When I^2S format is desired, both groups must be set to I^2S (i.e. AMA = AMB = 11). This is because they share the same WCLK.

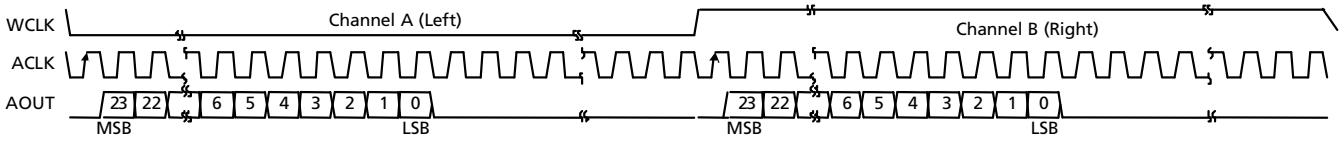


Figure 4-51: I^2S Audio Output Format

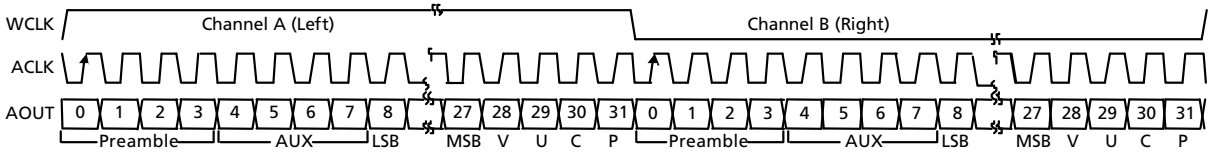


Figure 4-52: AES/EBU or S/PDIF Audio Output Format

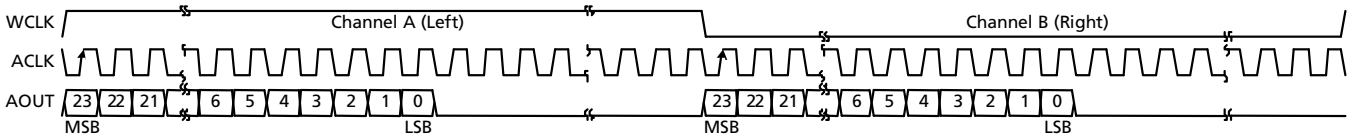


Figure 4-53: Serial Audio, Left Justified, MSB First

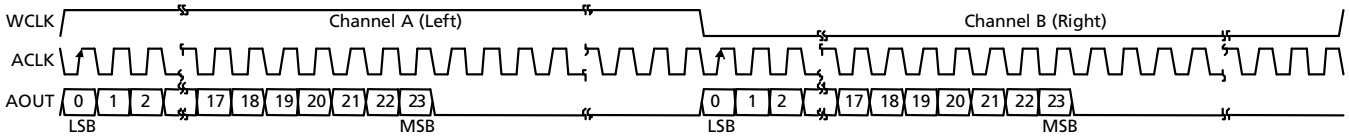


Figure 4-54: Serial Audio, Left Justified, LSB First

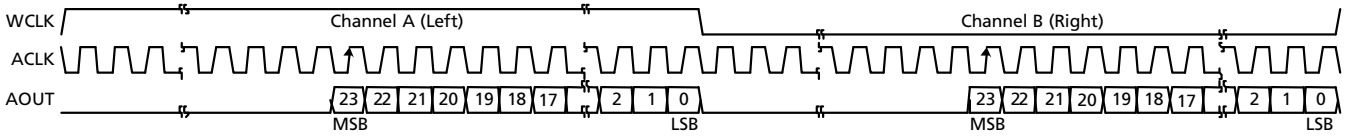


Figure 4-55: Serial Audio, Right Justified, MSB First

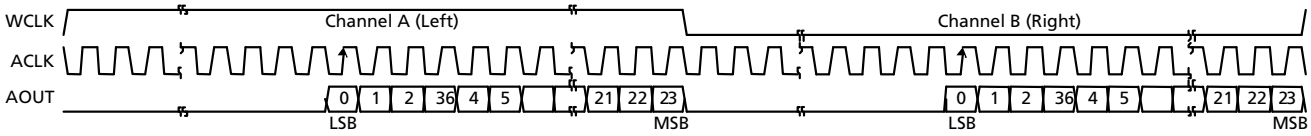


Figure 4-56: Serial Audio, Right Justified, LSB First

4.17.2.1 AES/EBU or S/PDIF Mode

In AES/EBU or S/PDIF output mode, the audio de-embedder uses a 128fs (6.144MHz audio bit clock) clock as shown in Figure 4-57.

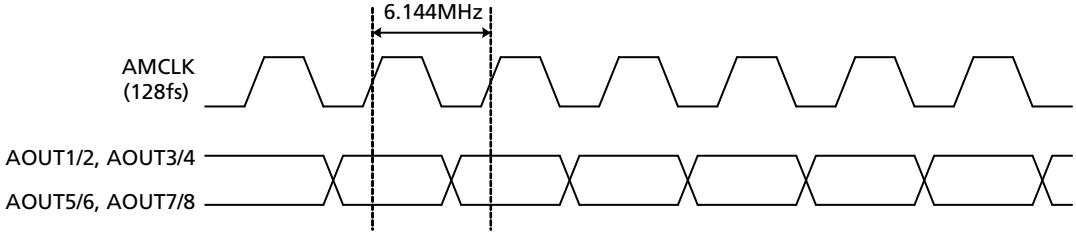


Figure 4-57: AES/EBU or S/PDIF Audio Output to Bit Clock Timing

4.17.2.2 Audio Data Packet Extraction Block

The audio de-embedder looks for audio data packets on every line of the incoming video.

The audio data must be embedded by Aviia compliant transmitter, such as the GV7600.

For Full HD formats, the audio data words must be embedded only in DS2.

The Audio Group Detect registers are set HIGH when audio data packets with a corresponding group DID are detected in the input video stream. The host interface reports the individual audio groups detected.

Table 4-25: Audio Data Packet Detect Register

Name	Description	Default
ADPG4_DET	Audio Group Four Data Packet Detection (1: Detected)	0
ADPG3_DET	Audio Group Three Data Packet Detection (1: Detected)	0
ADPG2_DET	Audio Group Two Data Packet Detection (1: Detected)	0
ADPG1_DET	Audio Group One Data Packet Detection (1: Detected)	0

When an audio data packet with a DID set in IDA[1:0] and IDB[1:0] is detected, the audio sample information is extracted and written into the audio FIFO.

The embedded audio group selected by IDA[1:0] is described henceforth in this document as Group A or Primary Group. The embedded audio group selected by IDB[1:0] is described henceforth in this document as Group B or Secondary Group.

Due to the large size of the horizontal ancillary data space in 720p/24, 720p/25 and 720p/30 video standards, the maximum number of ancillary data words the audio de-embedder can process is limited to 1024 when receiving these standards.

4.17.2.3 Audio Control Packets

Audio control packers carry additional information about the embedded audio sample data, such as audio sample rate, audio validity, audio synchronization, and audio-to-video timing relationship (delay). For both SD and HD formats, an Aviia transmitter, such as the GV7600, embeds audio control packets, formatted according to the following Society of Motion Pictures and Television Engineers (SMPTE) standards: SMPTE ST 272-2004 for SD video and SMPTE ST 299-2004 for HD video formats.

The GV7605 automatically detects the presence of audio control packets in the video stream. When audio control packets for audio Group A are detected, the CTRA_DET bit of the host interface is set HIGH. When audio control packets for audio Group B are detected, the CTRB_DET bit of the host interface is set HIGH.

The audio control packet data is accessible via the host interface.

Note: In SD, the control packet host interface registers are updated with new control packet values, after the CTRA_DET/CTRB_DET flags are cleared. In HD, the update happens automatically.

4.17.2.4 Setting Packet DID

Table 4-26 below, shows the 2-bit host interface setting for the audio group DID's.

For 24-bit audio support in SD mode, extended audio packets for Group A must have the same group DID set in IDA[1:0] of the host interface. Extended audio packets for Group B must have the same group DID set in IDB[1:0] of the host interface.

The audio de-embedder automatically detects the presence of extended audio packets. When detected, the audio output format is set to 24-bit audio sample word length.

The audio de-embedder defaults to audio Groups One and Two, where Group A is extracted from packets with audio Group One DID, and Group B from packets with audio Group Two DID.

Table 4-26: Audio Group DID Host Interface Settings

Audio Group	SD Data DID	SD Extended DID	HD Data DID	SD Control DID	HD Control DID	Host Interface Register Setting (2-bit)
1	2FFh	1FEh	2E7h	1EFh	1E3h	00b
2	1FDh	2FCh	1E6h	2EEh	2E2h	01b
3	1FBh	2FAh	1E5h	2EDh	2E1h	10b
4	2F9h	1F8h	2E4h	1ECh	1E0h	11b

Table 4-27: Audio Data and Control Packet DID Setting Register

Name	Description	Default
IDA[1-0]	Group A Audio data and control packet DID setting	00b
IDB[1-0]	Group B Audio data and control packet DID setting	01b

4.17.2.5 Audio Packet Delete Block

To delete all ancillary data with a group DID shown in Table 4-26, the ALL_DEL bit in the host interface must be set HIGH.

4.17.2.6 ECC Error Detection & Correction Block (HD Mode Only)

For HD video formats, the embedded audio sample data is protected for bit errors using error correction codes (ECC). The error correction codes are carried in the same packet as the audio sample data, to allow error detection and correction at the Aviia receiver.

The GV7605 performs BCH(31,25) forward error detection and correction. The error correction for all embedded audio data packets is activated when the host interface ECC_OFF bit is set LOW (default LOW). The audio de-embedder corrects any errors in both the audio output and the embedded packet.

When a one-bit error is detected in a bit array of the ECC protected region of the audio data packet with audio group DID set in IDA[1:0], the ECCA_ERROR flag is set HIGH. When a one-bit error is detected in the ECC protected region of the audio data packet with audio group DID set in IDB[1:0], the ECCB_ERROR flag is set HIGH.

Figure 4-58 shows examples of error correction and detection. Up to 8 bits in error can be corrected, providing each bit error is in a different bit array (shown below). When there are two or more bits in error in the same 24-bit array, the errors are detected, but not corrected.

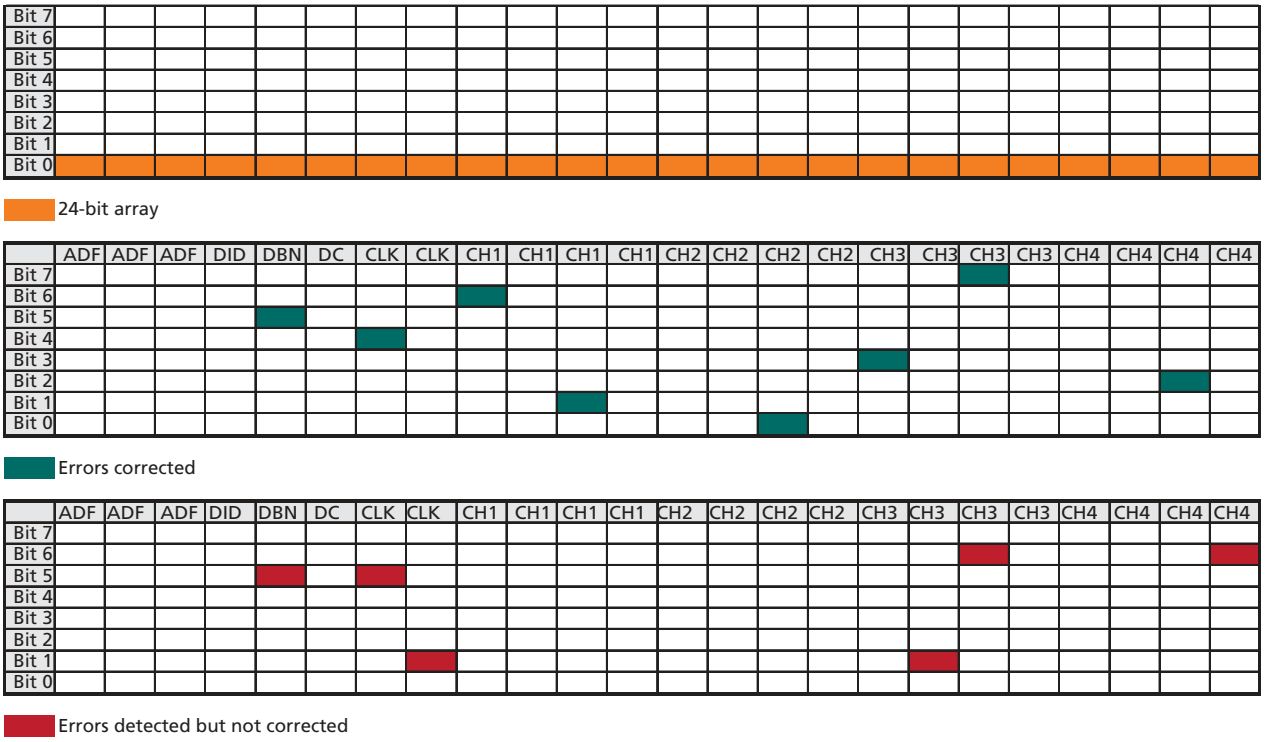


Figure 4-58: ECC 24-bit Array and Examples

4.17.3 Audio Processing

4.17.3.1 Audio Clock Generation

For SD and HD audio, a single set of audio frequencies is generated for all audio channels, using a Direct Digital Period Synthesizer (DDPS) to minimize jitter.

In HD modes, the input control for the DDPS is derived from the two embedded audio clock phase words in the audio data packet corresponding to Group A. The audio clock phase information used is taken from the first embedded audio packet in the HANC space.

The audio de-embedder also includes a Flywheel block to overcome any inconsistencies in the embedded audio clock phase information.

4.17.3.2 Audio Crosspoint Block

The Audio Crosspoint is used for audio output channel re-mapping. This feature allows any of the selected audio channels in Group A or Group B to be output on any of the eight output channels. The default setting is for one to one mapping, where AOUT1/2 is extracted from Group A CH1 and CH2, AOUT3/4 is extracted from Group A CH3 and CH4, and so on.

Note: If audio samples from embedded audio packets with the group set in IDA[1:0] are to be paired with samples from the group set in IDB[1:0], all of the channels must have been derived from the same Word Clock and must be synchronous.

The output channel is set in the OPn_SRC[2:0] host interface registers. Table 4-28 lists the 3-bit address for audio channel mapping.

Table 4-28: Audio Channel Mapping Codes

Audio Output Channel	3-bit Host Interface Source Address
1	000
2	001
3	010
4	011
5	100
6	101
7	110
8	111

4.17.3.3 Serial Audio Output Word Length

The audio output, in serial modes, has a selectable 24, 20 or 16-bit sample word length. The ASWL[1:0] host interface register is used to configure the audio output sample word length. Figure 4-29 shows the host interface 2-bit code for setting the audio sample word length. When the presence of extended audio packets is detected in SD mode, the GV7605 defaults to 24-bit audio sample word length.

Table 4-29: Audio Sample Word Lengths

ASWL[1:0]	Audio Sample Word Length (SD)	Audio Sample Word Length (HD)
00	24-bit	24-bit
01	20-bit	20-bit
10	16-bit	16-bit
11	Auto 24/20-bit (Default)	Reserved (Default)

Note: By default, at power-up, the word length is set to 12 bits. The desired word length should be programmed through the host interface.

4.17.3.4 Audio Channel Status

The GV7605 detects the AES/EBU or S/PDIF Audio Channel Status (ACS) block information for each of the selected channel pairs.

ACS data detection is indicated by corresponding ACS_DET flag bits in the host interface. The flag is cleared by writing to the same location.

4.17.3.4.1 Audio Channel Status Read

ACS data is available separately for each of the channels in a stereo pair. The GV7605 defaults to reading the first channel of each pair. There are 184 bits in each ACS packet, which are written to twelve 16-bit right-justified registers in the host interface.

The ACS_USE_SECOND bit (default LOW) selects the second channel in each audio pair when set HIGH.

Once all of the ACS data for a channel has been acquired, the corresponding ACS_DET bit is set, and acquisition stops. The ACS data is overwritten with new data when the ACS_DET bit is cleared in the system.

4.17.3.4.2 Audio Channel Status Regeneration

When the ACS_REGEN bit in the host interface is set HIGH, the audio de-embedder embeds the 24 bytes of the Audio Channel Status information programmed in the ACSR[183:0] registers into the 'C' bit of the AES/EBU or S/PDIF outputs. The same Audio Channel Status information is used for all output channels.

In order to apply ACSR data;

- Set the ACS_REGEN bit to logic HIGH
- Write the desired ACSR data to the ACSR registers
- Set the ACS_APPLY bit to HIGH

At the next status boundary, the device outputs the contents of the ACSR registers as ACS data. This event may occur at a different time for each of the output channels. While waiting for the status boundary, the device sets the appropriate ACS_APPLY_WAIT[A:D] flag.

Table 4-30 shows the host interface default settings for the Audio Channel Status block. The audio de-embedder automatically generates the CRC word.

Table 4-30: Audio Channel Status Information Registers

Name	Description	Default
ACSR[7-0]	Audio channel status block byte 0 set. Used when ACS_REGEN is set HIGH	85h
ACSR[15-8]	Audio channel status block byte 1 set. Used when ACS_REGEN is set HIGH	08h
ACSR[23-16]	Audio channel status block byte 2 set. Used when ACS_REGEN is set HIGH	28h (SD) 2Ch (HD)
ACSR[31-24]: ACSR[183-176]	Audio channel status block data for bytes 3 to 22. Used when ACS_REGEN is set HIGH	00h
ACS_REGEN	Audio channel status regenerate	0
ACS_APPLY	Apply new ACSR data	0

Table 4-30: Audio Channel Status Information Registers (Continued)

Name	Description	Default
ACS_APPLY_WAIT[A:D]	Waiting to apply new ACSR data	0
ACS[7-0]: ACS[183-176]	Audio channel status block data for bytes 0 to 22	00h: 00h

Table 4-31: Audio Channel Status Block for Regenerate Mode Default Settings

Name	Byte	Bit	Default	Mode
PRO	0	0	1b	Professional use of channel status block
Emphasis	0	2-4	100b	100b None. Rec. manual override disabled
Sample Frequency	0	6-7	01b	48kHz. Manual override or auto disabled
Channel Mode	1	0-3	0001b	Two channels. Manual override disabled
AUX	2	0-2	000b	SD Modes: Maximum audio word length is 20 bits
			001b	HD Mode: Maximum audio word length is 24 bits
Source Word Length	2	3-5	101b	Maximum word length (based on AUX setting). 24-bit for HD Modes; 20-bit for SD Modes
All other bits set to zero				

4.17.3.5 Audio Mute

When the MUTE bits in the host interface are set HIGH, the audio outputs are muted (all audio sample bits are set to zero). To set all the audio output channels to mute, set the host interface MUTE_ALL bit HIGH.

Table 4-32: Audio Mute Control Bits

Name	Description	Default
MUTE_ALL	Ch1-8 audio mute enable (1: Enabled)	0
MUTE8	Ch8 audio mute enable (1: Enabled)	0
MUTE7	Ch7 audio mute enable (1: Enabled)	0
MUTE6	Ch6 audio mute enable (1: Enabled)	0
MUTE5	Ch5 audio mute enable (1: Enabled)	0
MUTE4	Ch4 audio mute enable (1: Enabled)	0
MUTE3	Ch3 audio mute enable (1: Enabled)	0

Table 4-32: Audio Mute Control Bits (Continued)

Name	Description	Default
MUTE2	Ch2 audio mute enable (1: Enabled)	0
MUTE1	Ch1 audio mute enable (1: Enabled)	0

4.17.3.5.1 Mute On Loss Of Lock

When the GV7605 loses lock (LOCKED signal is LOW), the device sets all audio outputs LOW (no audio formatting is performed). The ACLK, WCLK and MCLK outputs are also forced LOW.

4.17.4 Error Reporting

4.17.4.1 Data Block Number Error

When the 1-255 count sequence in the Data Block Number (DBN) word of Group A audio data packets is discontinuous, the DBNA_ERR bit in the host interface is set HIGH. When the 1-255 count sequence in the DBN word of Group B audio data packets is discontinuous, the DBNB_ERR bit is set HIGH. The DBNx_ERR flags are in register 401h for SD, and register 201h for HD.

The DBNA_ERR and DBNB_ERR flags also have associated error interrupt mask register flags for configuration of error reporting in the Receiver. The interrupt mask flags for SD are in register 407h, and register 207h for HD. The DBNA_ERR and DBNB_ERR flags remains set until cleared by writing to these locations.

4.17.4.2 ECC Error

The GV7605 monitors the ECC error status of the two selected audio groups, as described in Section 4.17.2.6 on page 95.

The ECC[N]_ERROR flags also have an associated error interrupt mask register flag for configuration of error reporting. The ECC[N]_ERROR flags remain set until read via the host interface. The ECC error flags are in register 203h with associated error mask flags in register 207h.

4.18 Gennum Serial Peripheral Interface

The GSPI, or Gennum Serial Peripheral Interface, is a 4-wire interface provided to allow the system to access additional status and control information through configuration registers in the GV7605.

The GSPI is comprised of a Serial Data Input signal (SDIN), Serial Data Output signal (SDOUT), an active low Chip Select ($\overline{CS}$), and a Burst Clock (SCLK).

Because these pins are shared with the JTAG interface port, an additional control signal pin JTAG_EN is provided.

When JTAG_EN is LOW, the GSPI interface is enabled. When JTAG_EN is HIGH, the JTAG interface is enabled.

When operating in GSPI mode, the SCLK, SDIN, and $\overline{CS}$ signals must be provided by the system. The SDOUT pin is a non-clocked loop-through of SDIN and may be connected to the SDIN of another device, allowing multiple devices to be connected to the GSPI chain. See Section 4.18.2 for details. The interface is illustrated in the Figure 4-59.

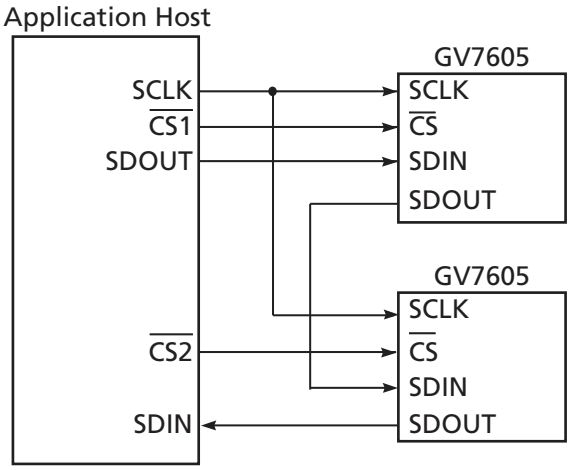


Figure 4-59: GSPI Application Interface Connection

All read or write access to the GV7605 is initiated and terminated by the system host processor. Each access always begins with a Command/Address Word, followed by a data write to, or data read from, the GV7605.

4.18.1 Command Word Description

The Command Word consists of a 16-bit word transmitted MSB first and contains a read/write bit, an Auto-Increment bit and a 12-bit address.

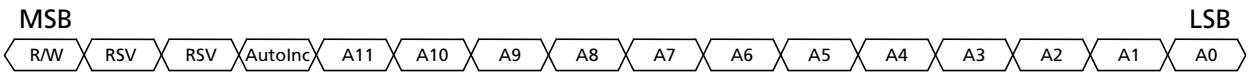


Figure 4-60: Command Word Format

Command Words are clocked into the GV7605 on the rising edge of the Serial Clock SCLK, which operates in a burst fashion. The chip select ($\overline{CS}$) signal must be set low a minimum of 1.5ns (t0 in Figure 4-62) before the first clock edge to ensure proper operation.

When the Auto-Increment bit is set LOW, each Command Word must be followed by only one Data Word to ensure proper operation.

If the Auto-Increment bit is set HIGH, the following Data Word is written into the address specified in the Command Word, and subsequent Data Words is written into incremental addresses from the first Data Word. This facilitates multiple address writes without sending a Command Word for each Data Word.

4.18.2 Data Read or Write Access

During a read sequence (Command Word R/W bit set HIGH) serial data is transmitted or received MSB first, synchronous with the rising edge of the serial clock SCLK. The Chip Select ($\overline{CS}$) signal must be set low a minimum of 1.5ns (t_0 in Figure 4-62) before the first clock edge to ensure proper operation. The first bit (MSB) of the Serial Output (SDOUT) is available (t_5 in Figure 4-63) following the last falling SCLK edge of the read Command Word, the remaining bits are clocked out on the negative edges of SCLK.

Note: When several devices are connected to the GSPI chain, only one $\overline{CS}$ may be asserted during a read sequence.

During a write sequence (Command Word R/W bit set LOW), a wait state of 37.1ns (t_4 in Figure 4-62) is required between the Command Word and the following Data Word. This wait state must also be maintained between successive Command Word/Data Word write sequences. When Auto Increment mode is selected (AutoInc = 1), the wait state must be maintained between successive Data Words after the initial Command Word/Data Word sequence.

During the write sequence, all Command and following Data Words input at the SDIN pin are output at the SDOUT pin unchanged. When several devices are connected to the GSPI chain, data can be written simultaneously to all the devices which have $\overline{CS}$ set LOW.

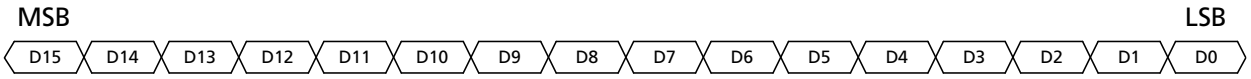


Figure 4-61: Data Word Format

4.18.3 GSPI Timing

Write and Read Mode timing for the GSPI interface;

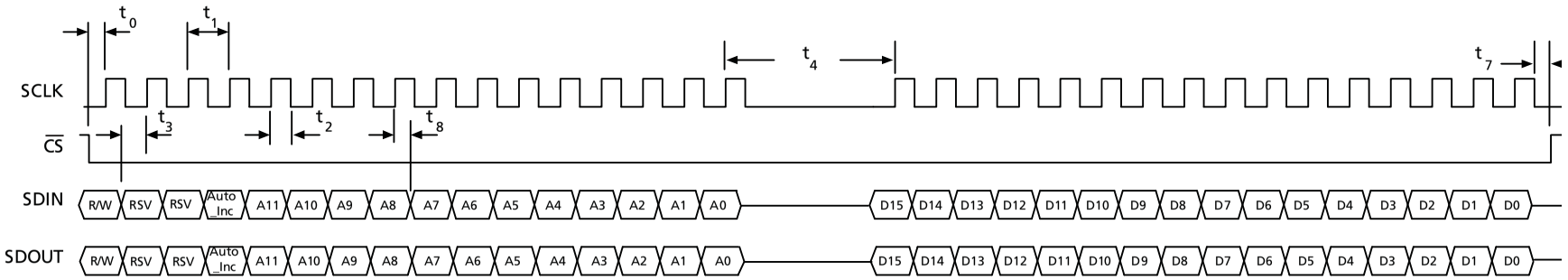


Figure 4-62: Write Mode

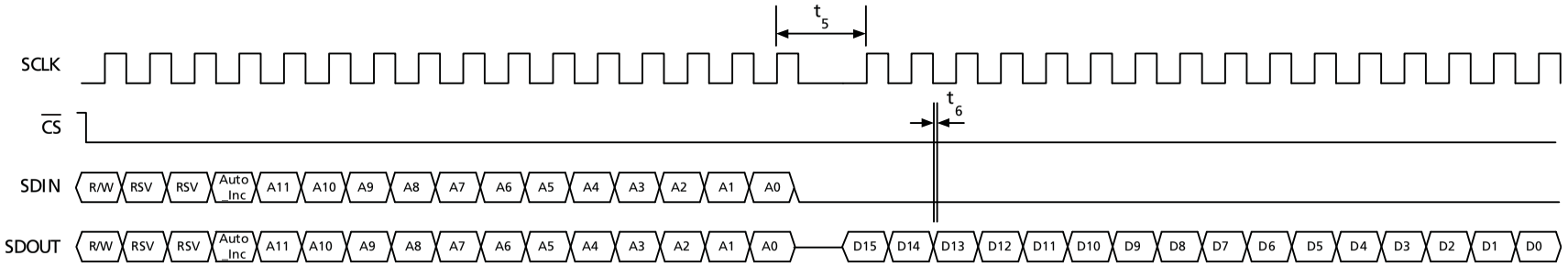


Figure 4-63: Read Mode

4.18.3.1 GSPI Timing Delays

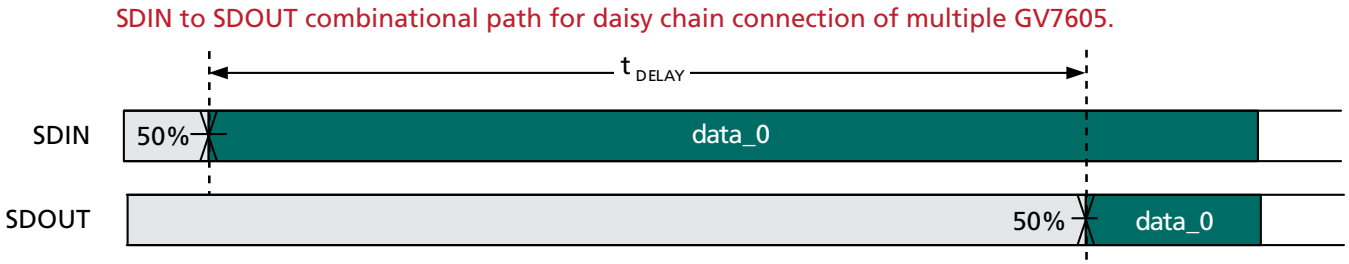


Figure 4-64: GV7605 GSPI Timing Delays

Table 4-33: GV7605 GSPI Electrical Characteristics

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Input data delay time	t_{DELAY}	50% levels; 1.8V operation	–	–	13.1	ns
Input data delay time	t_{DELAY}	50% levels; 3.3V operation	–	–	9.7	ns

4.19 Host Interface Register Maps

Note: The GV7605 only accepts write/read commands to/from the Audio Register Maps when the audio de-embedder is locked to the incoming video data rate. The Video Register Map is always active, whether valid serial input data is present or not.

Note: ROCW denotes register bits which are Read Only, but which must be cleared by writing a one to the same bit location (Read Only Clear on Write).

4.19.1 Video Core Registers

Table 4-34: Video Core Configuration and Status Registers

Address	Register Name	Bit	Description	R/W	Default
	RSVD	15	Reserved.	R	0
	TRS_WORD_REMAP _DISABLE_MASK	14	Disables 8-bit TRS word remapping.	R/W	0
	RSVD	13	Reserved.	R/W	0
	EDH_FLAG_UPDATE _MASK	12	Disables updating of EDH error flags.	R/W	0
	EDH_CRC_INS_MASK	11	Disables EDH_CRC error correction and insertion.	R/W	0
	H_CONFIG	10	Selects the H blanking indication: HIGH = TRS based blanking - the H output is set HIGH for the entire horizontal blanking period as indicated by the H bit in the received TRS signals. LOW = Active line blanking - the H output is HIGH for all the horizontal blanking period, including the EAV and SAV TRS words. This signal is only valid when 861_EN is set to '0' (via pin or host interface).	R/W	0
000h	ANC_DATA_EXT_MASK	9	Disables ancillary data extraction.	R/W	0
	AUD_EXT_MASK	8	Disables audio extraction block.	R/W	0
	861_EN_PIN_DISABLE	7	Disable 861_EN pin control when set to '1', and use TIMING_861 bit instead.	R/W	0
	TIMING_861	6	Selects the output timing reference format: HIGH = CEA-861 timing output. LOW = Digital FVH timing output.	R/W	0
	RSVD	5	Reserved.	R/W	0
	ILLEGAL_WORD_REMAP _MASK	4	Disables illegal word remapping.	R/W	0
	ANC_CHECKSUM _INSERTION_MASK	3	Disables insertion of ancillary data checksums.	R/W	0
	CRC_INS_MASK	2	Disables insertion of HD CRC words.	R/W	0
	LNUM_INS_MASK	1	Disables insertion of line numbers.	R/W	0
	TRS_INS_MASK	0	Disables insertion of TRS words.	R/W	0
001h	RSVD	15-0	Reserved.	R/W	256

Table 4-34: Video Core Configuration and Status Registers (Continued)

Address	Register Name	Bit	Description	R/W	Default
002h	RSVD	15-11	Reserved.	ROCW	0
	VD_STD_ERR	10	Video Standard Error indication.	ROCW	0
	FF_CRC_ERR	9	EDH Full Frame CRC error indication.	ROCW	0
	AP_CRC_ERR	8	EDH Active Picture CRC error indication.	ROCW	0
	RSVD	7	Reserved.	ROCW	0
	CCS_ERR	6	Chroma ancillary data checksum error indication.	ROCW	0
	YCS_ERR	5	Luma ancillary data checksum error indication.	ROCW	0
	CCRC_ERR	4	Chroma CRC error indication.	ROCW	0
	YCRC_ERR	3	Luma CRC error indication.	ROCW	0
	LNUM_ERR	2	Line number error indication.	ROCW	0
	SAV_ERR	1	SAV error indication.	ROCW	0
	EAV_ERR	0	EAV error indication.	ROCW	0
003h	RSVD	15-0	Reserved.	ROCW	0
004h	EDH_DETECT	15	Embedded EDH packet detected.	R	0
	ANC_UES_IN	14	Ancillary data – unknown error status flag.	R	0
	ANC_IDA_IN	13	Ancillary data – internal error detected already flag.	R	0
	ANC_IDH_IN	12	Ancillary data – internal error detected here flag	R	0
	ANC_EDA_IN	11	Ancillary data – error detected already flag.	R	0
	ANC_EDH_IN	10	Ancillary data – error detected here flag.	R	0
	FF_UES_IN	9	EDH Full Field – unknown error status flag.	R	0
	FF_IDA_IN	8	EDH Full Field – internal error detected already flag.	R	0
	FF_IDH_IN	7	EDH Full Field – internal error detected here flag.	R	0
	FF_EDA_IN	6	EDH Full Field – error detected already flag.	R	0
	FF_EDH_IN	5	EDH Full Field – error detected here flag.	R	0
	AP_UES_IN	4	EDH Active Picture – unknown error status flag.	R	0
	AP_IDA_IN	3	EDH Active Picture – internal error detected already flag.	R	0
	AP_IDH_IN	2	EDH Active Picture – internal error detected here flag.	R	0
	AP_EDA_IN	1	EDH Active Picture – error detected already flag.	R	0
	AP_EDH_IN	0	EDH Active Picture – error detected here flag.	R	0

Table 4-34: Video Core Configuration and Status Registers (Continued)

Address	Register Name	Bit	Description	R/W	Default
005h	RSVD	15	Reserved.	R	0
	ANC_UES	14	Ancillary data – Unknown Error Status flag.	R	1
	ANC_IDA	13	Ancillary data – Internal error Detected Already flag.	R	0
	ANC_IDH	12	Ancillary data – Internal error Detected Here flag.	R	0
	ANC_EDA	11	Ancillary data – Error Detected Already flag.	R	0
	ANC_EDH	10	Ancillary data – Error Detected Here flag.	R	0
	FF_UES	9	EDH Full Field – Unknown Error Status flag.	R	1
	FF_IDA	8	EDH Full Field – Internal error Detected Already flag.	R	0
	FF_IDH	7	EDH Full Field – Internal error Detected Here flag.	R	0
	FF_EDA	6	EDH Full Field – Error Detected Already flag.	R	0
	FF_EDH	5	EDH Full Field – Error Detected Here flag.	R	0
	AP_UES	4	EDH Active Picture – Unknown Error Status flag.	R	1
	AP_IDA	3	EDH Active Picture – Internal error Detected Already flag.	R	0
	AP_IDH	2	EDH Active Picture – Internal error Detected Here flag.	R	0
	AP_EDA	1	EDH Active Picture – Error Detected Already flag.	R	0
	AP_EDH	0	EDH Active Picture – Error Detected Here flag.	R	0
006h	FF_CRC_V	15	EDH Full Field CRC Validity bit.	R	0
	AP_CRC_V	14	EDH Active Picture CRC Validity bit.	R	0
	VD_STD	13-8	Detected Video Standard.	R	29
	RSVD	7-0	Reserved.	R	255
007h	RSVD	15-0	Reserved.	R	0

Table 4-34: Video Core Configuration and Status Registers (Continued)

Address	Register Name	Bit	Description	R/W	Default
008h	RSVD	15	Reserved.	RW	0
	STAT2_CONFIG	14-10	Configure STAT2 output pin: 00000 = H Blanking when 861_EN = 0; HSYNC when 861_EN = 1 00001 = V Blanking when 861_EN = 0; VSYNC when 861_EN = 1 00010 = F bit when 861_EN = 0; Data Enable (DE) when 861_EN = 1 00011 = LOCKED 00100 = Y/1ANC: ANC indication (SD), Luma ANC indication (HD), DS1 ANC data indication (Full HD) 00101 = C/2ANC: Chroma ANC indication (HD) or DS2 ANC data indication (Full HD) 00110 = Data Error 00111 = Video Error 01000 = Audio Error 01001 = EDH Detected 01010 = Carrier Detect 01011 = RATE_DET0 01100 = RATE_DET1 01101 to 11111 = Reserved	RW	2
	STAT1_CONFIG	9-5	Configure STAT1 output pin. (Refer to above for decoding)	RW	1
	STAT0_CONFIG	4-0	Configure STAT0 output pin. (Refer to above for decoding)	RW	0
009h	RSVD	15	Reserved.	RW	0
	STAT5_CONFIG	14-10	Configure STAT5 output pin. (Refer to above for decoding)	RW	6
	STAT4_CONFIG	9-5	Configure STAT4 output pin. (Refer to above for decoding)	RW	4
	STAT3_CONFIG	4-0	Configure STAT3 output pin. (Refer to above for decoding)	RW	3

Table 4-34: Video Core Configuration and Status Registers (Continued)

Address	Register Name	Bit	Description	R/W	Default
00Ah	RSVD	15-4	Reserved.	RW	0
	ANC_DATA_SWITCH	3	Switches between ancillary data memory banks.	RW	0
	ANC_DATA_DEL	2	Remove Ancillary Data from output video stream, set to Luma and Chroma blanking values.	RW	0
	HD_ANC_Y1_C2	1	Extract Ancillary data from Luma and Chroma channels (HD inputs) Extract Ancillary data from DS1 and DS2 (Full HD inputs)	RW	0
	HD_ANC_C2	0	Extract Ancillary data only from Chroma channel (HD inputs) Extract Ancillary data only from DS2 (Full HD inputs)	RW	0
00Bh	RSVD	15-11	Reserved.	R/W	0
	ANC_LINE_A	10-0	Video Line to extract Ancillary data from.	R/W	0
00Ch	RSVD	15-11	Reserved.	R/W	0
	ANC_LINE_B	10-0	Second video Line to extract Ancillary data from.	R/W	0
00Dh	RSVD	15-0	Reserved.	R	0
00Eh	RSVD	15-0	Reserved.	R	0
00Fh	ANC_TYPE1	15-0	Programmable DID/SDID pair #1 to extract.	R/W	0
010h	ANC_TYPE2	15-0	Programmable DID/SDID pair #2 to extract.	R/W	0
011h	ANC_TYPE3	15-0	Programmable DID/SDID pair #3 to extract.	R/W	0
012h	ANC_TYPE4	15-0	Programmable DID/SDID pair #4 to extract.	R/W	0
013h	ANC_TYPE5	15-0	Programmable DID/SDID pair #5 to extract.	R/W	0
014h to 01Eh	RSVD	–	Reserved.	R/W	0
01Fh	RSVD	15-14	Reserved.	R	0
	WORDS_PER_ACTLINE	13-0	Words Per Active Line.	R	0
020h	RSVD	15-14	Reserved.	R	0
	WORDS_PER_LINE	13-0	Total Words Per Line.	R	0
021h	RSVD	15-11	Reserved.	R	0
	LINES_PER_FRAME	10-0	Total Lines Per Frame.	R	0

Table 4-34: Video Core Configuration and Status Registers (Continued)

Address	Register Name	Bit	Description	R/W	Default
022h	RATE_SEL_READBACK	15-14	Read back detected data rate: 0 = HD 1 & 3 =SD 2 = Full HD	R	0
	M	13	Specifies detected M value 0 = 1.000 1 = 1.001	R	0
	STD_LOCK	12	Video standard lock.	R	0
	INT_$\overline{\text{PROG}}$	11	Interlaced or progressive.	R	0
	ACTLINE_PER_FIELD	10-0	Active lines per frame.	R	0
023h	RSVD	15-2	Reserved.	R	0
	V_LOCK	1	Indicates that the timing signal generator is locked to vertical timing.	R	0
	H_LOCK	0	Indicates that the timing signal generator is locked to horizontal timing.	R	0
024h	RSVD	15-3	Reserved.	R	0
	AUTO/$\overline{\text{MAN}}$	2	Detect data rate automatically (1) or program manually (0).	R/W	1
	RATE_SEL_TOP	1-0	Programmable rate select in manual (slave) mode: 0 = HD 1 & 3 = SD 2 = Full HD	R/W	0
025h	RSVD	15-7	Reserved.	R	0
	FORMAT_ERR	6	Indicates standard is not recognized for CEA 861 conversion.	R	1
	FORMAT_ID_861	5-0	CEA-861 format ID of input video stream. Refer to Table 4-19: Supported CEA-861 Formats.	R	0
026h	RSVD	15-3	Reserved.	R	0
	VSYNC_INVERT	2	Invert output VSYNC pulse.	R/W	0
	HSYNC_INVERT	1	Invert output HSYNC pulse.	R/W	0
	TRS_861	0	For 525i video input format: When TRS_861 is set LOW (default), the DE output will be set HIGH for 480 lines as per CEA-861. When TRS_861 is set HIGH, the DE output will be set HIGH for 487 lines (based on ITU-R BT.656 TRS timing). Only valid when 861_EN is set to '1'. See Section 4.11.1.1.	R/W	0

Table 4-34: Video Core Configuration and Status Registers (Continued)

Address	Register Name	Bit	Description	R/W	Default
027h to 036h	RSVD	–	Reserved.	R	0
037h	RSVD	15-11	Reserved.	R	0
	ERROR_MASK	10-0	Error mask for global error vector: bit[0] = EAV_ERR mask bit[1] = SAV_ERR mask bit[2] = LNUM_ERR mask bit[3] = YCRC_ERR mask bit[4] = CCRC_ERR mask bit[5] = YCS_ERR mask bit[6] = CCS_ERR mask bit[7] = Reserved bit[8] = AP_CRC_ERR mask bit[9] = FF_CRC_ERR mask	R/W	0
038h	RSVD	15-0	Reserved.	R	0
039h	RSVD	15-5	Reserved.	R	0
	SCLK_INV	4	Invert polarity of output serial audio clock.	R/W	0
	MCLK_INV	3	Invert polarity of output audio master clock.	R/W	0
	RSVD	2	Reserved.	R/W	0
	MCLK_SEL	1-0	Audio Master Clock Select. 0 = 128 fs 1 = 256 fs 2 = 512 fs	R/W	0
03Ah to 06Bh	RSVD	–	Reserved.	R	0
06Ch	RSVD	15-6	Reserved.	R/W	0
	DEL_LINE_CLK_SEL	5	Choses between the in-phase (0) and quadrature (1) clocks for DDR mode.	R/W	0
	DEL_LINE_OFFSET	4-0	Controls the offset for the delay line.	R/W	0

Table 4-34: Video Core Configuration and Status Registers (Continued)

Address	Register Name	Bit	Description	R/W	Default
06Dh	RSVD	15-6	Reserved.	R/W	0
	IO_DS_CTRL_DOUT_MSB	5-4	Drive strength adjustment for DOUT[19:10] outputs and PCLK output: 00 = 4mA 01 = 8mA 10 = 10mA(1.8V), 12mA(3.3V) 11 = 12mA(1.8V), 16mA(3.3V)	R/W	2
	IO_DS_CTRL_STAT	3-2	Drive strength adjustment for STAT[5:0] outputs: 00 = 4mA 01 = 6mA 10 = 8mA(1.8V), 10mA(3.3V) 11 = 10mA(1.8V), 12mA(3.3V)	R/W	2
	IO_DS_CTRL_DOUT_LSB	1-0	Drive strength adjustment for DOUT[9:0] outputs: 00 = 4mA 01 = 6mA 10 = 8mA(1.8V), 10mA(3.3V) 11 = 10mA(1.8V), 12mA(3.3V)	R/W	3
06Eh to 085h	RSVD	–	Reserved.	R/W	0

4.19.2 SD Audio Core

Note: The GV7605 only accepts write/read commands to/from the SD Audio Register Map when the audio de-embedder is locked to the incoming SD video format.

Table 4-35: SD Audio Core Configuration and Status Registers

Address	Register Name	Bit	Description	R/W	Default
400h	RSVD	15-14	Reserved.	R/W	0
	ALL_DEL	13	Selects deletion of all audio data and all audio control packets. 0 = Do not delete existing audio packets 1 = Delete existing audio packets	R/W	0
	MUTE_ALL	12	Mute all output channels. 0 = Normal 1 = Muted	R/W	0
	ACS_USE_SECOND	11	Extract Audio Channel Status from second channel pair.	R/W	0
	RSVD	10-8	Reserved.	R/W	0
	LSB_FIRSTD	7	Causes the channel 7 and 8 output format to use LSB first. 0 = MSB first 1 = LSB first	R/W	0
	LSB_FIRSTC	6	Causes the channel 5 and 6 output format to use LSB first. 0 = MSB first 1 = LSB first	R/W	0
	LSB_FIRSTB	5	Causes the channel 3 and 4 output format to use LSB first. 0 = MSB first 1 = LSB first	R/W	0
	LSB_FIRSTA	4	Causes the channel 1 and 2 output format to use LSB first. 0 = MSB first 1 = LSB first	R/W	0
	IDB	3-2	Specifies the Secondary audio group to extract. 00 = Audio group #1 01 = Audio group #2 10 = Audio group #3 11 = Audio group #4 **Note**: Should IDA and IDB be set to the same value, they automatically revert to their default values.	R/W	1

Table 4-35: SD Audio Core Configuration and Status Registers (Continued)

Address	Register Name	Bit	Description	R/W	Default
400h	IDA	1-0	Specifies the Primary audio group to extract. 00 = Audio group #1 01 = Audio group #2 10 = Audio group #3 11 = Audio group #4 **Note**: Should IDA and IDB be set to the same value, they automatically revert to their default values.	R/W	0
401h	EXT_DET3_4B	15	Set when Secondary group channels 3 and 4 have extended data. Cleared on write.	ROCW	0
	EXT_DET1_2B	14	Set when Secondary group channels 1 and 2 have extended data. Cleared on write.	ROCW	0
	EXT_DET3_4A	13	Set when Primary group channels 3 and 4 have extended data. Cleared on write.	ROCW	0
	EXT_DET1_2A	12	Set when Primary group channels 1 and 2 have extended data. Cleared on write.	ROCW	0
	CTL_DBNB_ERR	11	Set when Secondary group control packet Data Block Number sequence is discontinuous. Cleared on write.	ROCW	0
	CTL_DBNA_ERR	10	Set when Primary group control packet Data Block Number sequence is discontinuous. Cleared on write.	ROCW	0
	EXT_DBNB_ERR	9	Set when Secondary group extended data packet Data Block Number sequence is discontinuous. Cleared on write.	ROCW	0
	EXT_DBNA_ERR	8	Set when Primary group extended data packet Data Block Number sequence is discontinuous. Cleared on write.	ROCW	0
	SAMP_DBNB_ERR	7	Set when Secondary group data packet Data Block Number sequence is discontinuous. Cleared on write.	ROCW	0
	SAMP_DBNA_ERR	6	Set when Primary group data packet Data Block Number sequence is discontinuous. Cleared on write.	ROCW	0
	CTRB_DET	5	Set when Secondary group audio control packet is detected. Cleared on write.	ROCW	0
	CTRA_DET	4	Set when Primary group audio control packet is detected. Cleared on write.	ROCW	0
	ACS_DET3_4B	3	Secondary group audio status detected for channels 3 and 4. Cleared on write.	ROCW	0
	ACS_DET1_2B	2	Secondary group audio status detected for channels 1 and 2. Cleared on write.	ROCW	0
	ACS_DET3_4A	1	Primary group audio status detected for channels 3 and 4. Cleared on write.	ROCW	0
	ACS_DET1_2A	0	Primary group audio status detected for channels 1 and 2. Cleared on write.	ROCW	0

Table 4-35: SD Audio Core Configuration and Status Registers (Continued)

Address	Register Name	Bit	Description	R/W	Default
402h	RSVD	15-2	Reserved.	R/W	0
	ACS_APPLY	1	Cause channel status data in ACSR[183:0] to be transferred to the channel status replacement mechanism. The transfer does not occur until the next status boundary.	R/W	0
	ACS_REGEN	0	Specifies that Audio Channel Status of all channels should be replaced with ACSR[183:0] field. 0 = Do not replace Channel Status 1 = Replace Channel Status of all channels	R/W	0
403h	IDB_READBACK	15-14	Actual value of IDB in the hardware.	R	1
	IDA_READBACK	13-12	Actual value of IDA in the hardware.	R	0
	XDPG4_DET	11	Set while embedded Group 4 audio extended packets are detected.	R	0
	XDPG3_DET	10	Set while embedded Group 3 audio extended packets are detected.	R	0
	XDPG2_DET	9	Set while embedded Group 2 audio extended packets are detected.	R	0
	XDPG1_DET	8	Set while embedded Group 1 audio extended packets are detected.	R	0
	ADPG4_DET	7	Set while Group 4 audio data packets are detected.	R	0
	ADPG3_DET	6	Set while Group 3 audio data packets are detected.	R	0
	ADPG2_DET	5	Set while Group 2 audio data packets are detected.	R	0
	ADPG1_DET	4	Set while Group 1 audio data packets are detected.	R	0
	ACS_APPLY_WAITD	3	Set while output channels 7 and 8 are waiting for a status boundary to apply the ACSR[183:0] data.	R	0
	ACS_APPLY_WAITC	2	Set while output channels 5 and 6 are waiting for a status boundary to apply the ACSR[183:0] data.	R	0
	ACS_APPLY_WAITB	1	Set while output channels 3 and 4 are waiting for a status boundary to apply the ACSR[183:0] data.	R	0
	ACS_APPLY_WAITA	0	Set while output channels 1 and 2 are waiting for a status boundary to apply the ACSR[183:0] data.	R	0
404h	RSVD	15-1	Reserved.	R/W	0
	CSUM_ERROR	0	Embedded packet checksum error detected. Cleared on write.	ROCW	0
405h	RSVD	15-8	Reserved.	R/W	0
	MUTE	7-0	Mute output channels 8..1 Where bits 7:0 = channel 8:1 1 = Mute 0 = Normal	R/W	0

Table 4-35: SD Audio Core Configuration and Status Registers (Continued)

Address	Register Name	Bit	Description	R/W	Default
406h	RSVD	15-8	Reserved.	R/W	0
	CH4_VALIDB	7	Secondary group channel 4 sample validity flag.	R	0
	CH3_VALIDB	6	Secondary group channel 3 sample validity flag.	R	0
	CH2_VALIDB	5	Secondary group channel 2 sample validity flag.	R	0
	CH1_VALIDB	4	Secondary group channel 1 sample validity flag.	R	0
	CH4_VALIDA	3	Primary group channel 4 sample validity flag.	R	0
	CH3_VALIDA	2	Primary group channel 3 sample validity flag.	R	0
	CH2_VALIDA	1	Primary group channel 2 sample validity flag.	R	0
	CH1_VALIDA	0	Primary group channel 1 sample validity flag.	R	0
407h	RSVD	15	Reserved.	R/W	0
	EN_NOT_LOCKED	14	Asserts *interrupt* when LOCKED signal is not asserted.	R/W	0
	EN_NO_VIDEO	13	Asserts *interrupt* when video format is unknown.	R/W	0
	EN_CSUM_ERROR	12	Asserts *interrupt* when checksum error is detected.	R/W	0
	EN_ACS_DET3_4B	11	Asserts *interrupt* when EN_ACS_DET3_4B flag is set.	R/W	0
	EN_ACS_DET1_2B	10	Asserts *interrupt* when EN_ACS_DET1_2B flag is set.	R/W	0
	EN_ACS_DET3_4A	9	Asserts *interrupt* when EN_ACS_DET3_4A flag is set.	R/W	0
	EN_ACS_DET1_2A	8	Asserts *interrupt* when EN_ACS_DET1_2A flag is set.	R/W	0
	EN_CTRB_DET	7	Asserts *interrupt* when EN_CTRB_DET flag is set.	R/W	0
	EN_CTRA_DET	6	Asserts *interrupt* when EN_CTRA_DET flag is set.	R/W	0
	EN_DBNB_ERR	5	Asserts *interrupt* when EN_DBNB_ERR flag is set.	R/W	0
	EN_DBNA_ERR	4	Asserts *interrupt* when EN_DBNA_ERR flag is set.	R/W	0
	EN_ADPG4_DET	3	Asserts *interrupt* when the ADPG4_DET flag is set.	R/W	0
	EN_ADPG3_DET	2	Asserts *interrupt* when the ADPG3_DET flag is set.	R/W	0
	EN_ADPG2_DET	1	Asserts *interrupt* when the ADPG2_DET flag is set.	R/W	0
	EN_ADPG1_DET	0	Asserts *interrupt* when the ADPG1_DET flag is set.	R/W	0

Table 4-35: SD Audio Core Configuration and Status Registers (Continued)

Address	Register Name	Bit	Description	R/W	Default
408h	ASWLD	15-14	Output channels 7 and 8 word length. 00 = 24-bit 01 = 20-bit 10 = 16-bit 11 = Automatic 20-bit or 24-bit	R/W	3
	ASWLC	13-12	Output channels 5 and 6 word length. (See above for decoding)	R/W	3
	ASWLB	11-10	Output channels 3 and 4 word length. (See above for decoding)	R/W	3
	ASWLA	9-8	Output channels 1 and 2 word length. (See above for decoding)	R/W	3
	AMD	7-6	Output channels 7 and 8 format selector. 00 = AES/EBU or S/PDIF audio output 01 = Serial audio output: Left justified; MSB first 10 = Serial audio output: Right justified; MSB first 11 = I^2S serial audio output	R/W	3
	AMC	5-4	Output channels 5 and 6 format selector. (See above for decoding).	R/W	3
	AMB	3-2	Output channels 3 and 4 format selector. (See above for decoding).	R/W	3
	AMA	1-0	Output channels 1 and 2 format selector. (See above for decoding).	R/W	3
409h	RSVD	15-12	Reserved.	R/W	0
	OP4_SRC	11-9	Output channel 4 source selector. 000 = Primary audio group channel 1 001 = Primary audio group channel 2 010 = Primary audio group channel 3 011 = Primary audio group channel 4 100 = Secondary audio group channel 1 101 = Secondary audio group channel 2 110 = Secondary audio group channel 3 111 = Secondary audio group channel 4	R/W	3
	OP3_SRC	8-6	Output channel 3 source selector (Decode as above).	R/W	2
	OP2_SRC	5-3	Output channel 2 source selector (Decode as above).	R/W	1
	OP1_SRC	2-0	Output channel 1 source selector (Decode as above).	R/W	0

Table 4-35: SD Audio Core Configuration and Status Registers (Continued)

Address	Register Name	Bit	Description	R/W	Default
40Ah	RSVD	15-12	Reserved.	R/W	0
	OP8_SRC	11-9	Output channel 8 source selector. 000 = Primary audio group channel 1 001 = Primary audio group channel 2 010 = Primary audio group channel 3 011 = Primary audio group channel 4 100 = Secondary audio group channel 1 101 = Secondary audio group channel 2 110 = Secondary audio group channel 3 110 = Secondary audio group channel 4	R/W	7
	OP7_SRC	8-6	Output channel 7 source selector (Decode as above).	R/W	6
	OP6_SRC	5-3	Output channel 6 source selector (Decode as above).	R/W	5
	OP5_SRC	2-0	Output channel 5 source selector (Decode as above).	R/W	4
40Bh to 41Fh	RSVD	–	Reserved.	–	–
420h	RSVD	15-9	Reserved.	R/W	0
	AFN1_2A	8-0	Primary group audio frame number for channels 1 and 2.	R	0
421h	RSVD	15-9	Reserved.	R/W	0
	AFN3_4A	8-0	Primary group audio frame number for channels 3 and 4.	R	0
422h	RSVD	15-8	Reserved.	R/W	0
	RATE3_4A	7-5	Primary group sampling frequency for channels 3 and 4	R	0
	ASX3_4A	4	Primary group asynchronous mode for channels 3 and 4.	R	0
	RATE1_2A	3-1	Primary group sampling frequency for channels 1 and 2.	R	0
	ASX1_2A	0	Primary group asynchronous mode for channels 1 and 2.	R	0
423h	RSVD	15-4	Reserved.	R/W	0
	ACTA	3-0	Primary group active channels.	R	0
424h	RSVD	15-9	Reserved.	R/W	0
	DEL1A_1	8-1	Primary Audio group delay data for channel 1.	R	0
	EBIT1A	0	Primary Audio group delay data valid flag for channel 1.	R	0
425h	RSVD	15-9	Reserved.	R/W	0
	DEL1A_2	8-0	Primary Audio group delay data for channel 1.	R	0

Table 4-35: SD Audio Core Configuration and Status Registers (Continued)

Address	Register Name	Bit	Description	R/W	Default
426h	RSVD	15-9	Reserved.	R/W	0
	DEL1A_3	8-0	Primary Audio group delay data for channel 1.	R	0
427h	RSVD	15-9	Reserved.	R/W	0
	DEL2A_4	8-1	Primary Audio group delay data for channel 2.	R	0
	EBIT2A	0	Primary Audio group delay data valid flag for channel 2.	R	0
428h	RSVD	15-9	Reserved.	R/W	0
	DEL2A_5	8-0	Primary Audio group delay data for channel 2.	R	0
429h	RSVD	15-9	Reserved.	R/W	0
	DEL2A_6	8-0	Primary Audio group delay data for channel 2.	R	0
42Ah	RSVD	15-9	Reserved.	R/W	0
	DEL3A_7	8-1	Primary Audio group delay data for channel 3.	R	0
	EBIT3A	0	Primary Audio group delay data valid flag for channel 3.	R	0
42Bh	RSVD	15-9	Reserved.	R/W	0
	DEL3A_8	8-0	Primary Audio group delay data for channel 3.	R	0
42Ch	RSVD	15-9	Reserved.	R/W	0
	DEL3A_9	8-0	Primary Audio group delay data for channel 3.	R	0
42Dh	RSVD	15-9	Reserved.	R/W	0
	DEL4A_10	8-1	Primary Audio group delay data for channel 4.	R	0
	EBIT4A	0	Primary Audio group delay data valid flag for channel 4.	R	0
42Eh	RSVD	15-9	Reserved.	R/W	0
	DEL4A_11	8-0	Primary Audio group delay data for channel 4.	R	0
42Fh	RSVD	15-9	Reserved.	R/W	0
	DEL4A_12	8-0	Primary Audio group delay data for channel 4.	R	0
430h	RSVD	15-9	Reserved.	R/W	0
	AFN1_2B	8-0	Secondary group audio frame number for channels 1 and 2.	R	0
431h	RSVD	15-9	Reserved.	R/W	0
	AFN3_4B	8-0	Secondary group audio frame number for channels 3 and 4.	R	0

Table 4-35: SD Audio Core Configuration and Status Registers (Continued)

Address	Register Name	Bit	Description	R/W	Default
432h	RSVD	15-8	Reserved.	R	0
	RATE3_4B	7-5	Secondary group sampling frequency for channels 3 and 4.	R	0
	ASX3_4B	4	Secondary group asynchronous mode for channels 3 and 4.	R	0
	RATE1_2B	3-1	Secondary group sampling frequency for channels 1 and 2.	R	0
	ASX1_2B	0	Secondary group asynchronous mode for channels 1 and 2.	R	0
433h	RSVD	15-4	Reserved.	R/W	0
	ACTB	3-0	Secondary group active channels.	R	0
434h	RSVD	15-9	Reserved.	R/W	0
	DEL1B_1	8-1	Secondary Audio group delay data for channel 1.	R	0
	EBIT1B	0	Secondary Audio group delay data valid flag for channel 1.	R	0
435h	RSVD	15-9	Reserved.	R/W	
	DEL1B_2	8-0	Secondary Audio group delay data for channel 1.	R	0
436h	RSVD	15-9	Reserved.	R/W	0
	DEL1B_3	8-0	Secondary Audio group delay data for channel 1.	R	0
437h	RSVD	15-9	Reserved.	R/W	0
	DEL2B_4	8-1	Secondary Audio group delay data for channel 2.	R	0
	EBIT2B	0	Secondary Audio group delay data valid flag for channel 2.	R	0
438h	RSVD	15-9	Reserved.	R/W	0
	DEL2B_5	8-0	Secondary Audio group delay data for channel 2.	R	0
439h	RSVD	15-9	Reserved.	R/W	0
	DEL2B_6	8-0	Secondary Audio group delay data for channel 2.	R	0
43Ah	RSVD	15-9	Reserved.	R/W	0
	DEL3B_7	8-1	Secondary Audio group delay data for channel 3.	R	0
	EBIT3B	0	Secondary Audio group delay data valid flag for channel 3.	R	0
43Bh	RSVD	15-9	Reserved.	R/W	0
	DEL3B_8	8-0	Secondary Audio group delay data for channel 3.	R	0

Table 4-35: SD Audio Core Configuration and Status Registers (Continued)

Address	Register Name	Bit	Description	R/W	Default
43Ch	RSVD	15-9	Reserved.	R/W	0
	DEL3B_9	8-0	Secondary Audio group delay data for channel 3.	R	0
43Dh	RSVD	15-9	Reserved.	R/W	0
	DEL4B_10	8-1	Secondary Audio group delay data for channel 4.	R	0
	EBIT4B	0	Secondary Audio group delay data valid flag for channel 4.	R	0
43Eh	RSVD	15-9	Reserved.	R/W	0
	DEL4B_11	8-0	Secondary Audio group delay data for channel 4.	R	0
43Fh	RSVD	15-9	Reserved.	R/W	0
	DEL4B_12	8-0	Secondary Audio group delay data for channel 4.	R	0
440h	ACSR1_2A_0	15-0	Bytes 0 and 1 of audio group A channel status for channels 1 and 2.	R	0
441h	ACSR1_2A_2	15-0	Bytes 2 and 3 of audio group A channel status for channels 1 and 2.	R	0
442h	ACSR1_2A_4	15-0	Bytes 4 and 5 of audio group A channel status for channels 1 and 2.	R	0
443h	ACSR1_2A_6	15-0	Bytes 6 and 7 of audio group A channel status for channels 1 and 2.	R	0
444h	ACSR1_2A_8	15-0	Bytes 8 and 9 of audio group A channel status for channels 1 and 2.	R	0
445H	ACSR1_2A_10	15-0	Bytes 10 and 11 of audio group A channel status for channels 1 and 2.	R	0
446H	ACSR1_2A_12	15-0	Bytes 12 and 13 of audio group A channel status for channels 1 and 2.	R	0
447h	ACSR1_2A_14	15-0	Bytes 14 and 15 of audio group A channel status for channels 1 and 2.	R	0
448h	ACSR1_2A_16	15-0	Bytes 16 and 17 of audio group A channel status for channels 1 and 2.	R	0
449h	ACSR1_2A_18	15-0	Bytes 18 and 19 of audio group A channel status for channels 1 and 2.	R	0
44Ah	ACSR1_2A_20	15-0	Bytes 20 and 21 of audio group A channel status for channels 1 and 2.	R	0
44Bh	ACSR1_2A_22	15-0	Bytes 22 of audio group A channel status for channels 1 and 2.	R	0
450h	ACSR3_4A_0	15-0	Bytes 0 and 1 of audio group A channel status for channels 3 and 4.	R	0
451h	ACSR3_4A_2	15-0	Bytes 2 and 3 of audio group A channel status for channels 3 and 4.	R	0

Table 4-35: SD Audio Core Configuration and Status Registers (Continued)

Address	Register Name	Bit	Description	R/W	Default
452h	ACSR3_4A_4	15-0	Bytes 4 and 5 of audio group A channel status for channels 3 and 4.	R	0
453h	ACSR3_4A_6	15-0	Bytes 6 and 7 of audio group A channel status for channels 3 and 4.	R	0
454h	ACSR3_4A_8	15-0	Bytes 8 and 9 of audio group A channel status for channels 3 and 4.	R	0
455h	ACSR3_4A_10	15-0	Bytes 10 and 11 of audio group A channel status for channels 3 and 4.	R	0
456h	ACSR3_4A_12	15-0	Bytes 12 and 13 of audio group A channel status for channels 3 and 4.	R	0
457h	ACSR3_4A_14	15-0	Bytes 14 and 15 of audio group A channel status for channels 3 and 4.	R	0
458h	ACSR3_4A_16	15-0	Bytes 16 and 17 of audio group A channel status for channels 3 and 4.	R	0
459h	ACSR3_4A_18	15-0	Bytes 18 and 19 of audio group A channel status for channels 3 and 4.	R	0
45Ah	ACSR3_4A_20	15-0	Bytes 20 and 21 of audio group A channel status for channels 3 and 4.	R	0
45Bh	RSVD	15-8	Reserved.	R/W	0
	ACSR3_4A_22	7-0	Bytes 22 of audio group A channel status for channels 3 and 4.	R	0
460h	ACSR1_2B_0	15-0	Bytes 0 and 1 of audio group B channel status for channels 1 and 2.	R	0
461h	ACSR1_2B_2	15-0	Bytes 2 and 3 of audio group B channel status for channels 1 and 2.	R	0
462h	ACSR1_2B_4	15-0	Bytes 4 and 5 of audio group B channel status for channels 1 and 2.	R	0
463h	ACSR1_2B_6	15-0	Bytes 6 and 7 of audio group B channel status for channels 1 and 2.	R	0
464h	ACSR1_2B_8	15-0	Bytes 8 and 9 of audio group B channel status for channels 1 and 2.	R	0
465h	ACSR1_2B_10	15-0	Bytes 10 and 11 of audio group B channel status for channels 1 and 2.	R	0
466h	ACSR1_2B_12	15-0	Bytes 12 and 13 of audio group B channel status for channels 1 and 2.	R	0
467h	ACSR1_2B_14	15-0	Bytes 14 and 15 of audio group B channel status for channels 1 and 2.	R	0
468h	ACSR1_2B_16	15-0	Bytes 16 and 17 of audio group B channel status for channels 1 and 2.	R	0

Table 4-35: SD Audio Core Configuration and Status Registers (Continued)

Address	Register Name	Bit	Description	R/W	Default
469h	ACSR1_2B_18	15-0	Bytes 18 and 19 of audio group B channel status for channels 1 and 2.	R	0
46Ah	ACSR1_2B_20	15-0	Bytes 20 and 21 of audio group B channel status for channels 1 and 2.	R	0
46Bh	RSVD	15-8	Reserved.	R/W	0
	ACSR1_2B_22	7-0	Bytes 22 of audio group B channel status for channels 1 and 2.	R	0
470h	ACSR3_4B_0	15-0	Bytes 0 and 1 of audio group B channel status for channels 3 and 4.	R	0
471h	ACSR3_4B_2	15-0	Bytes 2 and 3 of audio group B channel status for channels 3 and 4.	R	0
472h	ACSR3_4B_4	15-0	Bytes 4 and 5 of audio group B channel status for channels 3 and 4.	R	0
473h	ACSR3_4B_6	15-0	Bytes 6 and 7 of audio group B channel status for channels 3 and 4.	R	0
474h	ACSR3_4B_8	15-0	Bytes 8 and 9 of audio group B channel status for channels 3 and 4.	R	0
475h	ACSR3_4B_10	15-0	Bytes 10 and 11 of audio group B channel status for channels 3 and 4.	R	0
476h	ACSR3_4B_12	15-0	Bytes 12 and 13 of audio group B channel status for channels 3 and 4.	R	0
477h	ACSR3_4B_14	15-0	Bytes 14 and 15 of audio group B channel status for channels 3 and 4.	R	0
478h	ACSR3_4B_16	15-0	Bytes 16 and 17 of audio group B channel status for channels 3 and 4.	R	0
479h	ACSR3_4B_18	15-0	Bytes 18 and 19 of audio group B channel status for channels 3 and 4.	R	0
47Ah	ACSR3_4B_20	15-0	Bytes 20 and 21 of audio group B channel status for channels 3 and 4.	R	0
47Bh	ACSR3_4B_22	15-0	Bytes 22 of audio group B channel status for channels 3 and 4.	R	0
480h	ACSR_BYTE0	7-0	Audio channel status to use when ACS_REGEN is set or when adding audio channel status to non-AES/EBU audio. 8 bits per register for 23 registers.	R	0
481h	ACSR_BYTE1	7-0	–	W	0
482h	ACSR_BYTE2	7-0	–	W	0
483h	ACSR_BYTE3	7-0	–	W	0
484h	ACSR_BYTE4	7-0	–	W	0
485h	ACSR_BYTE5	7-0	–	W	0

Table 4-35: SD Audio Core Configuration and Status Registers (Continued)

Address	Register Name	Bit	Description	R/W	Default
486h	ACSR_BYTE6	7-0	–	W	0
487h	ACSR_BYTE7	7-0	–	W	0
488h	ACSR_BYTE8	7-0	–	W	0
489h	ACSR_BYTE9	7-0	–	W	0
48Ah	ACSR_BYTE10	7-0	–	W	0
48Bh	ACSR_BYTE11	7-0	–	W	0
48Ch	ACSR_BYTE12	7-0	–	W	0
48Dh	ACSR_BYTE13	7-0	–	W	0
48Eh	ACSR_BYTE14	7-0	–	W	0
48Fh	ACSR_BYTE15	7-0	–	W	0
490h	ACSR_BYTE16	7-0	–	W	0
491h	ACSR_BYTE17	7-0	–	W	0
492h	ACSR_BYTE18	7-0	–	W	0
493h	ACSR_BYTE19	7-0	–	W	0
494h	ACSR_BYTE20	7-0	–	W	0
495h	ACSR_BYTE21	7-0	–	W	0
496h	ACSR_BYTE22	7-0	–	W	0

4.19.3 HD Audio Core Registers

Note: The GV7605 only accepts write/read commands to/from the HD Audio Register Map when the device is locked to the incoming HD video format.

Table 4-36: HD Audio Core Configuration and Status Registers

Address	Register Name	Bit	Description	R/W	Default
200h	ECC_OFF	15	Disables ECC error correction.	R/W	0
	ALL_DEL	14	Selects deletion of all audio data and all audio control packets 0 = Do not delete existing audio control packets 1 = Delete existing audio control packets.	R/W	0
	MUTE_ALL	13	Mute all output channels 0 = Normal 1 = Muted	R/W	0
	ACS_USE_SECOND	12	Extract Audio Channel Status from second channel pair.	R/W	0
	ASWLB	11-10	Secondary group output word length. 00 = 24 bits 01 = 20 bits 10 = 16 bits 11 = invalid	R/W	3
	ASWLA	9-8	Primary group output word length 00 = 24 bits 01 = 20 bits 10 = 16 bits 11 = invalid	R/W	3
	AMB	7-6	Secondary group output format selector. 00 = AES/EBU or S/PDIF audio output 01 = Serial audio output: left justified MSB first 10 = Serial audio output: right justified. MSB first 11 = I^2S serial audio output	R/W	3
	AMA	5-4	Primary group output format selector. 00 = AES/EBU or S/PDIF audio output 01 = Serial audio output: left justified MSB first 10 = Serial audio output: right justified MSB first 11 = I^2S serial audio output	R/W	3

Table 4-36: HD Audio Core Configuration and Status Registers (Continued)

Address	Register Name	Bit	Description	R/W	Default
200h	IDB	3-2	Specifies the Secondary audio group to extract. 00 = Audio group #1 01 = Audio group #2 10 = Audio group #3 11 = Audio group #4 **Note**: Should IDA and IDB be set to the same value, they automatically revert to their default values.	R/W	1
	IDA	1-0	Specifies the Primary audio group to extract. 00 = Audio group #1 01 = Audio group #2 10 = Audio group #3 11 = Audio group #4 **Note**: Should IDA and IDB be set to the same value, they automatically revert to their default values.	R/W	0
201h	RSVD	15-8	Reserved.	R/W	0
	DBNB_ERR	7	Set when Secondary group audio Data Block Number sequence is discontinuous.	ROCW	0
	DBNA_ERR	6	Set when Primary group audio Data Block Number sequence is discontinuous.	ROCW	0
	CTRB_DET	5	Set when Secondary group audio control packet is detected.	ROCW	0
	CTRA_DET	4	Set when Primary group audio control packet is detected.	ROCW	0
	ACS_DET3_4B	3	Secondary group audio status detected for channels 3 and 4.	ROCW	0
	ACS_DET1_2B	2	Secondary group audio status detected for channels 1 and 2.	ROCW	0
	ACS_DET3_4A	1	Primary group audio status detected for channels 3 and 4.	ROCW	0
	ACS_DET1_2A	0	Primary group audio status detected for channels 1 and 2.	ROCW	0
202h	RSVD	15-9	Reserved.	R	0
	IDB_READBACK	8-7	Actual value of IDB in the hardware.	R	1
	IDA_READBACK	6-5	Actual value of IDA in the hardware.	R	0
	ADPG4_DET	4	Set while Group 4 audio data packets are detected.	R	0
	ADPG3_DET	3	Set while Group 3 audio data packets are detected.	R	0
	ADPG2_DET	2	Set while Group 2 audio data packets are detected.	R	0
	ADPG1_DET	1	Set while Group 1 audio data packets are detected.	R	0
	ACS_APPLY_WAIT	0	Set while output channels 1 and 2 are waiting for a status boundary to apply the ACSR[183:0] data.	R	0

Table 4-36: HD Audio Core Configuration and Status Registers (Continued)

Address	Register Name	Bit	Description	R/W	Default
203h	RSVD	15-2	Reserved.	R/W	0
	ECCA_ERROR	1	Primary group audio data packet error detected.	ROCW	0
	ECCB_ERROR	0	Secondary group audio data packet error detected.	ROCW	0
204h	RSVD	15-2	Reserved.	R/W	0
	ACS_APPLY	1	Cause channel status data in ACSR[183:0] to be transferred to the channel status replacement mechanism. The transfer does not occur until the next status boundary.	R/W	0
	ACS_REGEN	0	Specifies that Audio Channel Status of all channels should be replaced with ACSR[183:0] field. 0 = Do not replace Channel Status 1 = Replace Channel Status of all channels	R/W	0
205h	RSVD	15	Reserved.	R/W	0
	MUTEB	7-4	Mute Secondary output channels 4..1 where bits 7:4 = channel 4:1 1 = Mute 0 = Normal	R/W	0
	MUTEA	3-0	Mute Primary output channels 4..1 where bits 3:0 = channel 4:1 1 = Mute 0 = Normal	R/W	0
206h	RSVD	15-8	Reserved.	R/W	0
	CH4_VALIDB	7	Secondary group channel 4 sample validity flag.	R	0
	CH3_VALIDB	6	Secondary group channel 3 sample validity flag.	R	0
	CH2_VALIDB	5	Secondary group channel 2 sample validity flag.	R	0
	CH1_VALIDB	4	Secondary group channel 1 sample validity flag.	R	0
	CH4_VALIDA	3	Primary group channel 4 sample validity flag.	R	0
	CH3_VALIDA	2	Primary group channel 3 sample validity flag.	R	0
	CH2_VALIDA	1	Primary group channel 2 sample validity flag.	R	0
	CH1_VALIDA	0	Primary group channel 1 sample validity flag.	R	0

Table 4-36: HD Audio Core Configuration and Status Registers (Continued)

Address	Register Name	Bit	Description	R/W	Default
207h	RSVD	15	Reserved.	R/W	0
	EN_MISSING_PHASE	14	Asserts interrupt when chosen group's phase data is missing	R/W	0
	EN_ACS_DET3_4B	13	Asserts interrupt when ACS_DET3_4B flag is set.	R/W	0
	EN_ACS_DET1_2B	12	Asserts interrupt when ACS_DET1_2B flag is set.	R/W	0
	EN_ACS_DET3_4A	11	Asserts interrupt when ACS_DET3_4A flag is set.	R/W	0
	EN_ACS_DET1_2A	10	Asserts interrupt when ACS_DET1_2A flag is set.	R/W	0
	EN_CTRB_DET	9	Asserts interrupt when CTRB_DET flag is set.	R/W	0
	EN_CTRA_DET	8	Asserts interrupt when CTRA_DET flag is set.	R/W	0
	EN_DBNB_ERR	7	Asserts interrupt when DBNB_ERR flag is set.	R/W	0
	EN_DBNA_ERR	6	Asserts interrupt when DBNA_ERR flag is set.	R/W	0
	EN_ECCB_ERR	5	Asserts interrupt when ECCB_ERR flag is set.	R/W	0
	EN_ECCA_ERR	4	Asserts interrupt when ECCA_ERR flag is set.	R/W	0
	EN_ADPG4_DET	3	Asserts interrupt when ADPG4_DET flag is set.	R/W	0
	EN_ADPG3_DET	2	Asserts interrupt when ADPG3_DET flag is set.	R/W	0
	EN_ADPG2_DET	1	Asserts interrupt when ADPG2_DET flag is set.	R/W	0
	EN_ADPG1_DET	0	Asserts interrupt when ADPG1_DET flag is set.	R/W	0
208h	RSVD	15-11	Reserved.	R/W	0
	SEL_PHASE_SRC	10	Selects between the Primary and Secondary embedded phase info.	R/W	0
	LSB_FIRSTB	9	Causes the Secondary group serial output formats to use LSB first.	R/W	0
	LSB_FIRSTA	8	Causes the Primary group serial output formats to use LSB first.	R/W	0
	RSVD	7-4	Reserved.	R/W	0
	EN_NOT_LOCKED	3	Asserts interrupt when locked is not asserted.	R/W	0
	EN_NO_VIDEO	2	Asserts interrupt when the video format is unknown.	R/W	0
	EN_NO_PHASEB	1	Asserts interrupt when NO_PHASEB_DATA is set.	R/W	0
	EN_NO_PHASEA	0	Asserts interrupt when NO_PHASEA_DATA is set.	R/W	0

Table 4-36: HD Audio Core Configuration and Status Registers (Continued)

Address	Register Name	Bit	Description	R/W	Default
209h	RSVD	15-3	Reserved.	R/W	0
	MISSING_PHASE	2	Embedded phase info for chosen group missing or incorrect.	R	0
	NO_PHASEB_DATA	1	Secondary group has invalid embedded clock information.	R	0
	NO_PHASEA_DATA	0	Primary group has invalid embedded clock information.	R	0
20Ah	RSVD	15-12	Reserved.	R	0
	OP4_SRC	11-9	Output channel 4 source selector. 000: Primary audio group channel 1 001: Primary audio group channel 2 010: Primary audio group channel 3 011: Primary audio group channel 4 100: Secondary audio group channel 1 101: Secondary audio group channel 2 110: Secondary audio group channel 3 111: Secondary audio group channel 4	R/W	3
	OP3_SRC	8-6	Output channel 3 source selector (Decode as above).	R/W	2
	OP2_SRC	5-3	Output channel 2 source selector (Decode as above).	R/W	1
	OP1_SRC	2-0	Output channel 1 source selector (Decode as above).	R/W	0
20Bh	RSVD	15-12	Reserved.	R/W	0
	OP8_SRC	11-9	Output channel 8 source selector. 000: Primary audio group channel 1 001: Primary audio group channel 2 010: Primary audio group channel 3 011: Primary audio group channel 4 100: Secondary audio group channel 1 101: Secondary audio group channel 2 110: Secondary audio group channel 3 111: Secondary audio group channel 4	R/W	7
	OP7_SRC	8-6	Output channel 7 source selector (Decode as above).	R/W	6
	OP6_SRC	5-3	Output channel 6 source selector (Decode as above).	R/W	5
	OP5_SRC	2-0	Output channel 5 source selector (Decode as above).	R/W	4
20Ch to 21Fh	RSVD	–	Reserved.	–	–
220h	RSVD	15-9	Reserved.	R/W	0
	AFNA	8-0	Primary group audio frame number.	R	0

Table 4-36: HD Audio Core Configuration and Status Registers (Continued)

Address	Register Name	Bit	Description	R/W	Default
221h	RSVD	15-4	Reserved.	R/W	0
	RATEA	3-1	Primary group sampling frequency for channels 1 and 2.	R	0
	ASXA	0	Primary group asynchronous mode for channels 1 and 2.	R	0
222h	RSVD	15-4	Reserved.	R/W	0
	ACTA	3-0	Primary group active channels.	R	0
223h	RSVD	15-9	Reserved.	R/W	0
	DEL1_2A_1	8-1	Primary Audio group delay data for channels 1 and 2 [7:0].	R	0
	EBIT1_2A	0	Primary Audio group delay data valid flag for channels 1 and 2.	R	0
224h	RSVD	15-9	Reserved.	R/W	0
	DEL1_2A_2	8-0	Primary Audio group delay data for channels 1 and 2 [16:8].	R	0
225h	RSVD	15-9	Reserved.	R/W	0
	DEL1_2A_3	8-0	Primary Audio group delay data for channels 1 and 2 [25:17].	R	0
226h	RSVD	15-9	Reserved.	R/W	0
	DEL3_4A_4	8-1	Primary Audio group delay data for channels 3 and 4 [7:0].	R	0
	EBIT3_4A	0	Primary Audio group delay data valid flag for channels 3 and 4.	R	0
227h	RSVD	15-9	Reserved.	R/W	0
	DEL3_4A_5	8-0	Primary Audio group delay data for channels 3 and 4 [16:8].	R	0
228h	RSVD	15-9	Reserved.	R/W	0
	DEL3_4A_6	8-0	Primary Audio group delay data for channels 3 and 4 [25:17].	R	0
229h to 22Fh	RSVD	–	Reserved.	R/W	0
230h	RSVD	15-9	Reserved.	R/W	0
	AFNB	8-0	Secondary group audio frame number.	R	0

Table 4-36: HD Audio Core Configuration and Status Registers (Continued)

Address	Register Name	Bit	Description	R/W	Default
231h	RSVD	15-4	Reserved.	R/W	0
	RATEB	3-1	Secondary group sampling frequency for channels 1 and 2.	R	0
	ASXB	0	Secondary group asynchronous mode for channels 1 and 2.	R	0
232h	RSVD	15-4	Reserved.	R/W	0
	ACTB	3-0	Secondary group active channels.	R	0
233h	RSVD	15-9	Reserved.	R/W	0
	DEL1_2B_1	8-1	Secondary Audio group delay data valid flag for channels 1 and 2.	R	0
	EBIT1_2B	0	Secondary Audio group delay data for channels 1 and 2 [7:0].	R	0
234h	RSVD	15-9	Reserved.	R/W	0
	DEL1_2B_2	8-0	Secondary Audio group delay data for channels 1 and 2 [16:8].	R	0
235h	RSVD	15-9	Reserved.	R/W	0
	DEL1_2B_3	8-0	Secondary Audio group delay data for channels 1 and 2 [25:17].	R	0
236h	RSVD	15-9	Reserved.	R/W	0
	DEL3_4B_4	8-1	Secondary Audio group delay data for channels 3 and 4 [7:0].	R	0
	EBIT3_4B	0	Secondary Audio group delay data valid flag for channels 3 and 4.	R	0
237h	RSVD	15-9	Reserved.	R/W	0
	DEL3_4B_5	8-0	Secondary Audio group delay data for channels 3 and 4 [16:8].	R	0
238h	RSVD	15-9	Reserved.	R/W	0
	DEL3_4B_6	8-0	Secondary Audio group delay data for channels 3 and 4 [25:17].	R	0
239h to 23Fh	RSVD	–	Reserved.	R/W	0
240h	ACSR1_2A_0	15-0	Bytes 0 and 1 of audio group A channel status for channels 1 and 2.	R	0
241h	ACSR1_2A_2	15-0	Bytes 2 and 3 of audio group A channel status for channels 1 and 2.	R	0
242h	ACSR1_2A_4	15-0	Bytes 4 and 5 of audio group A channel status for channels 1 and 2.	R	0

Table 4-36: HD Audio Core Configuration and Status Registers (Continued)

Address	Register Name	Bit	Description	R/W	Default
243h	ACSR1_2A_6	15-0	Bytes 6 and 7 of audio group A channel status for channels 1 and 2.	R	0
244h	ACSR1_2A_8	15-0	Bytes 8 and 9 of audio group A channel status for channels 1 and 2.	R	0
245h	ACSR1_2A_10	15-0	Bytes 10 and 11 of audio group A channel status for channels 1 and 2.	R	0
246h	ACSR1_2A_12	15-0	Bytes 12 and 13 of audio group A channel status for channels 1 and 2.	R	0
247h	ACSR1_2A_14	15-0	Bytes 14 and 15 of audio group A channel status for channels 1 and 2.	R	0
248h	ACSR1_2A_16	15-0	Bytes 16 and 17 of audio group A channel status for channels 1 and 2.	R	0
249h	ACSR1_2A_18	15-0	Bytes 18 and 19 of audio group A channel status for channels 1 and 2.	R	0
24Ah	ACSR1_2A_20	15-0	Bytes 20 and 21 of audio group A channel status for channels 1 and 2.	R	0
24Bh	RSVD	15-8	Reserved.	R/W	0
	ACSR1_2A_22	7-0	Bytes 22 of audio group A channel status for channels 1 and 2.	R	0
24Ch to 24Fh	RSVD	–	Reserved.	R/W	0
250h	ACSR3_4A_0	15-0	Bytes 0 and 1 of audio group A channel status for channels 3 and 4.	R	0
251h	ACSR3_4A_2	15-0	Bytes 2 and 3 of audio group A channel status for channels 3 and 4.	R	0
252h	ACSR3_4A_4	15-0	Bytes 4 and 5 of audio group A channel status for channels 3 and 4.	R	0
253h	ACSR3_4A_6	15-0	Bytes 6 and 7 of audio group A channel status for channels 3 and 4.	R	0
254h	ACSR3_4A_8	15-0	Bytes 8 and 9 of audio group A channel status for channels 3 and 4.	R	0
255h	ACSR3_4A_10	15-0	Bytes 10 and 11 of audio group A channel status for channels 3 and 4.	R	0
256h	ACSR3_4A_12	15-0	Bytes 12 and 13 of audio group A channel status for channels 3 and 4.	R	0
257h	ACSR3_4A_14	15-0	Bytes 14 and 15 of audio group A channel status for channels 3 and 4.	R	0
258h	ACSR3_4A_16	15-0	Bytes 16 and 17 of audio group A channel status for channels 3 and 4.	R	0

Table 4-36: HD Audio Core Configuration and Status Registers (Continued)

Address	Register Name	Bit	Description	R/W	Default
259h	ACSR3_4A_18	15-0	Bytes 18 and 19 of audio group A channel status for channels 3 and 4.	R	0
25Ah	ACSR3_4A_20	15-0	Bytes 20 and 21 of audio group A channel status for channels 3 and 4.	R	0
25Bh	RSVD	15-8	Reserved.	R/W	0
	ACSR3_4A_22	7-0	Bytes 22 of audio group A channel status for channels 3 and 4.	R	0
25Ch to 25Fh	RSVD	–	Reserved.	R/W	0
260h	ACSR1_2B_0	15-0	Bytes 0 and 1 of audio group B channel status for channels 1 and 2.	R	0
261h	ACSR1_2B_2	15-0	Bytes 2 and 3 of audio group B channel status for channels 1 and 2.	R	0
262h	ACSR1_2B_4	15-0	Bytes 4 and 5 of audio group B channel status for channels 1 and 2.	R	0
263h	ACSR1_2B_6	15-0	Bytes 6 and 7 of audio group B channel status for channels 1 and 2.	R	0
264h	ACSR1_2B_8	15-0	Bytes 8 and 9 of audio group B channel status for channels 1 and 2.	R	0
265h	ACSR1_2B_10	15-0	Bytes 10 and 11 of audio group B channel status for channels 1 and 2.	R	0
266h	ACSR1_2B_12	15-0	Bytes 12 and 13 of audio group B channel status for channels 1 and 2.	R	0
267h	ACSR1_2B_14	15-0	Bytes 14 and 15 of audio group B channel status for channels 1 and 2.	R	0
268h	ACSR1_2B_16	15-0	Bytes 16 and 17 of audio group B channel status for channels 1 and 2.	R	0
269h	ACSR1_2B_18	15-0	Bytes 18 and 19 of audio group B channel status for channels 1 and 2.	R	0
26Ah	ACSR1_2B_20	15-0	Bytes 20 and 21 of audio group B channel status for channels 1 and 2.	R	0
26Bh	RSVD	15-8	Reserved.	R/W	0
	ACSR1_2B_22	7-0	Bytes 22 of audio group B channel status for channels 1 and 2.	R	0
26Ch to 26Fh	RSVD	–	Reserved.	R/W	0
270h	ACSR3_4B_0	15-0	Bytes 0 and 1 of audio group B channel status for channels 3 and 4.	R	0

Table 4-36: HD Audio Core Configuration and Status Registers (Continued)

Address	Register Name	Bit	Description	R/W	Default
271h	ACSR3_4B_2	15-0	Bytes 2 and 3 of audio group B channel status for channels 3 and 4.	R	0
272h	ACSR3_4B_4	15-0	Bytes 4 and 5 of audio group B channel status for channels 3 and 4.	R	0
273h	ACSR3_4B_6	15-0	Bytes 6 and 7 of audio group B channel status for channels 3 and 4.	R	0
274h	ACSR3_4B_8	15-0	Bytes 8 and 9 of audio group B channel status for channels 3 and 4.	R	0
275h	ACSR3_4B_10	15-0	Bytes 10 and 11 of audio group B channel status for channels 3 and 4.	R	0
276h	ACSR3_4B_12	15-0	Bytes 12 and 13 of audio group B channel status for channels 3 and 4.	R	0
277h	ACSR3_4B_14	15-0	Bytes 14 and 15 of audio group B channel status for channels 3 and 4.	R	0
278h	ACSR3_4B_16	15-0	Bytes 16 and 17 of audio group B channel status for channels 3 and 4.	R	0
279h	ACSR3_4B_18	15-0	Bytes 18 and 19 of audio group B channel status for channels 3 and 4.	R	0
27Ah	ACSR3_4B_20	15-0	Bytes 20 and 21 of audio group B channel status for channels 3 and 4.	R	0
27Bh	RSVD	15-8	Reserved.	R/W	0
	ACSR3_4B_22	7-0	Bytes 22 of audio group B channel status for channels 3 and 4.	R	0
27Ch to 27Fh	RSVD	–	Reserved.	R/W	0
280h	RSVD	15-8	Reserved.	R/W	0
	ACSR0	7-0	Audio channel status to use when ACS_REGEN is set or when adding audio channel status to non-AES/EBU or S/PDIF audio. 8 bits per register starting at register 280h and ending at register 296h.	W	0
281h	RSVD	15-8	Reserved.	R/W	0
	ACSR1	7-0	Audio channel status to use when ACS_REGEN is set or when adding audio channel status to non-AES/EBU or S/PDIF audio. 8 bits per register starting at register 280h and ending at register 296h.	W	0
282h	RSVD	15-8	Reserved.	R/W	0
	ACSR2	7-0	Audio channel status to use when ACS_REGEN is set or when adding audio channel status to non-AES/EBU or S/PDIF audio. 8 bits per register starting at register 280h and ending at register 296h.	W	0

Table 4-36: HD Audio Core Configuration and Status Registers (Continued)

Address	Register Name	Bit	Description	R/W	Default
283h	RSVD	15-8	Reserved.	R/W	0
	ACSR3	7-0	Audio channel status to use when ACS_REGEN is set or when adding audio channel status to non-AES/EBU or S/PDIF audio. 8 bits per register starting at register 280h and ending at register 296h.	W	0
284h	RSVD	15-8	Reserved.	R/W	0
	ACSR4	7-0	Audio channel status to use when ACS_REGEN is set or when adding audio channel status to non-AES/EBU or S/PDIF audio. 8 bits per register starting at register 280h and ending at register 296h.	W	0
285h	RSVD	15-8	Reserved.	R/W	0
	ACSR5	7-0	Audio channel status to use when ACS_REGEN is set or when adding audio channel status to non-AES/EBU or S/PDIF audio. 8 bits per register starting at register 280h and ending at register 296h.	W	0
286h	RSVD	15-8	Reserved.	R/W	0
	ACSR6	7-0	Audio channel status to use when ACS_REGEN is set or when adding audio channel status to non-AES/EBU or S/PDIF audio. 8 bits per register starting at register 280h and ending at register 296h.	W	0
287h	RSVD	15-8	Reserved.	R/W	0
	ACSR7	7-0	Audio channel status to use when ACS_REGEN is set or when adding audio channel status to non-AES/EBU or S/PDIF audio. 8 bits per register starting at register 280h and ending at register 296h.	W	0
288h	RSVD	15-8	Reserved.	R/W	0
	ACSR8	7-0	Audio channel status to use when ACS_REGEN is set or when adding audio channel status to non-AES/EBU or S/PDIF audio. 8 bits per register starting at register 280h and ending at register 296h.	W	0
289h	RSVD	15-8	Reserved.	R/W	0
	ACSR9	7-0	Audio channel status to use when ACS_REGEN is set or when adding audio channel status to non-AES/EBU or S/PDIF audio. 8 bits per register starting at register 280h and ending at register 296h.	W	0
28Ah	RSVD	15-8	Reserved.	R/W	0
	ACSR10	7-0	Audio channel status to use when ACS_REGEN is set or when adding audio channel status to non-AES/EBU or S/PDIF audio. 8 bits per register starting at register 280h and ending at register 296h.	W	0

Table 4-36: HD Audio Core Configuration and Status Registers (Continued)

Address	Register Name	Bit	Description	R/W	Default
28Bh	RSVD	15-8	Reserved.	R/W	0
	ACSR11	7-0	Audio channel status to use when ACS_REGEN is set or when adding audio channel status to non-AES/EBU or S/PDIF audio. 8 bits per register starting at register 280h and ending at register 296h.	W	0
28Ch	RSVD	15-8	Reserved.	R/W	0
	ACSR12	7-0	Audio channel status to use when ACS_REGEN is set or when adding audio channel status to non-AES/EBU or S/PDIF audio. 8 bits per register starting at register 280h and ending at register 296h.	W	0
28Dh	RSVD	15-8	Reserved.	R/W	0
	ACSR13	7-0	Audio channel status to use when ACS_REGEN is set or when adding audio channel status to non-AES/EBU or S/PDIF audio. 8 bits per register starting at register 280h and ending at register 296h.	W	0
28Eh	RSVD	15-8	Reserved.	R/W	0
	ACSR14	7-0	Audio channel status to use when ACS_REGEN is set or when adding audio channel status to non-AES/EBU or S/PDIF audio. 8 bits per register starting at register 280h and ending at register 296h.	W	0
28Fh	RSVD	15-8	Reserved.	R/W	0
	ACSR15	7-0	Audio channel status to use when ACS_REGEN is set or when adding audio channel status to non-AES/EBU or S/PDIF audio. 8 bits per register starting at register 280h and ending at register 296h.	W	0
290h	RSVD	15-8	Reserved.	R/W	0
	ACSR16	7-0	Audio channel status to use when ACS_REGEN is set or when adding audio channel status to non-AES/EBU or S/PDIF audio. 8 bits per register starting at register 280h and ending at register 296h.	W	0
291h	RSVD	15-8	Reserved.	R/W	0
	ACSR17	7-0	Audio channel status to use when ACS_REGEN is set or when adding audio channel status to non-AES/EBU or S/PDIF audio. 8 bits per register starting at register 280h and ending at register 296h.	W	0
292h	RSVD	15-8	Reserved.	R/W	0
	ACSR18	7-0	Audio channel status to use when ACS_REGEN is set or when adding audio channel status to non-AES/EBU or S/PDIF audio. 8 bits per register starting at register 280h and ending at register 296h.	W	0

Table 4-36: HD Audio Core Configuration and Status Registers (Continued)

Address	Register Name	Bit	Description	R/W	Default
293h	RSVD	15-8	Reserved.	R/W	0
	ACSR19	7-0	Audio channel status to use when ACS_REGEN is set or when adding audio channel status to non-AES/EBU or S/PDIF audio. 8 bits per register starting at register 280h and ending at register 296h.	W	0
294h	RSVD	15-8	Reserved.	R/W	0
	ACSR20	7-0	Audio channel status to use when ACS_REGEN is set or when adding audio channel status to non-AES/EBU or S/PDIF audio. 8 bits per register starting at register 280h and ending at register 296h.	W	0
295h	RSVD	15-8	Reserved.	R/W	0
	ACSR21	7-0	Audio channel status to use when ACS_REGEN is set or when adding audio channel status to non-AES/EBU or S/PDIF audio. 8 bits per register starting at register 280h and ending at register 296h.	W	0
296h	RSVD	15-8	Reserved.	R/W	0
	ACSR22	7-0	Audio channel status to use when ACS_REGEN is set or when adding audio channel status to non-AES/EBU or S/PDIF audio. 8 bits per register starting at register 280h and ending at register 296h.	W	0
297h	RSVD	15-0	Reserved.	R	29

Table 4-37: Ancillary Data Extraction Memory Access Registers

Address	Register Name	Bit	Description	R/W	Default
800h to BFFh	ANC_PACKET_BANK	15-0	Extracted Ancillary Data (1024 words). Bit 15-8: Most Significant Word (MSW) Bit 7-0: Least Significant Word (LSW) See 4.16.8 Ancillary Data Extraction.	R	0

Legend:

R = Read only
ROCW = Read Only, Clear on Write (must write ones to clear)
R/W = Read or Write
W = Write only

4.20 JTAG Test Operation

When the JTAG_EN pin of the GV7605 is set HIGH, the host interface port is configured for JTAG test operation. In this mode, pins E7, F8, F7, and E8 become TDO, TCK, TMS, and TDI. In addition, the $\overline{\text{RESET}}$ pin operates as the test reset pin.

Boundary scan testing using the JTAG interface is enabled in this mode.

There are two ways in which JTAG can be used:

1. As a stand-alone JTAG interface to be used at in-circuit ATE (Automatic Test Equipment) during PCB assembly.
2. Under control of a host processor for applications such as system power on self tests.

When the JTAG tests are applied by ATE, care must be taken to disable any other devices driving the digital I/O pins. If the tests are to be applied only at ATE, this can be accomplished with tri-state buffers used in conjunction with the JTAG_EN input signal. This is shown in Figure 4-65.

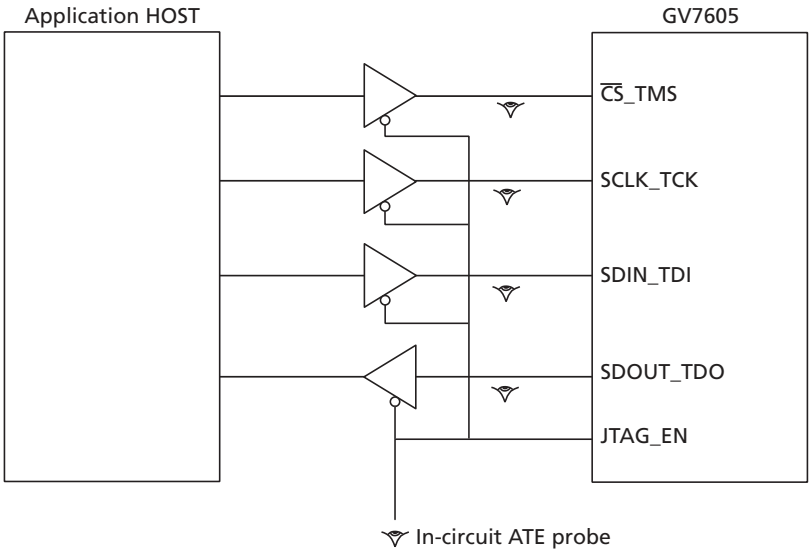


Figure 4-65: In-Circuit JTAG

Alternatively, if the test capabilities are to be used in the system, the host processor may still control the JTAG_EN input signal, but some means for tri-stating the host must exist in order to use the interface at ATE. This is represented in Figure 4-66.

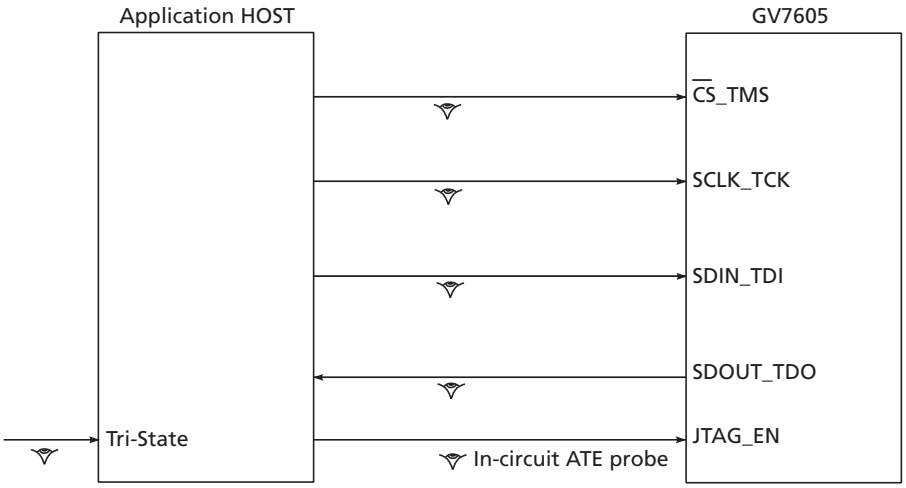


Figure 4-66: System JTAG

Scan coverage is limited to digital pins only. There is no scan coverage for analog pins VBG, SDO/$\overline{\text{SDO}}$, TERM, LF, and LB_CONT.

The JTAG_EN pin must be held LOW during scan and therefore has no scan coverage.

Please contact your Semtech representative to obtain the BSDL model for the GV7605.

4.21 Device Power-up

The GV7605 is designed to operate in a multi-voltage environment, therefore, any power-up sequence is allowed. The charge pump, phase detector, core logic, serial digital output and I/O buffers can all be powered up in any order.

4.22 Device Reset

Note: At power-up, the device must be reset to operate correctly.

In order to initialize all internal operating conditions to their default states, hold the $\overline{\text{RESET}}$ signal LOW for a minimum of t_{reset} = 1ms after all power supplies are stable. There are no requirements for power supply sequencing.

When held in reset, all device outputs are driven to a high-impedance state.

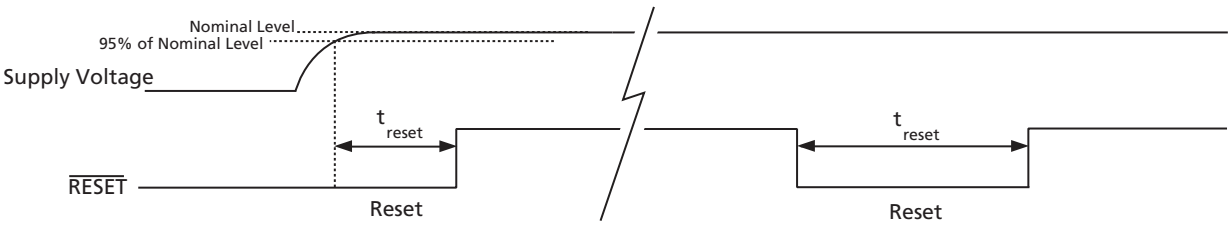


Figure 4-67: Reset Pulse

4.23 Standby Mode

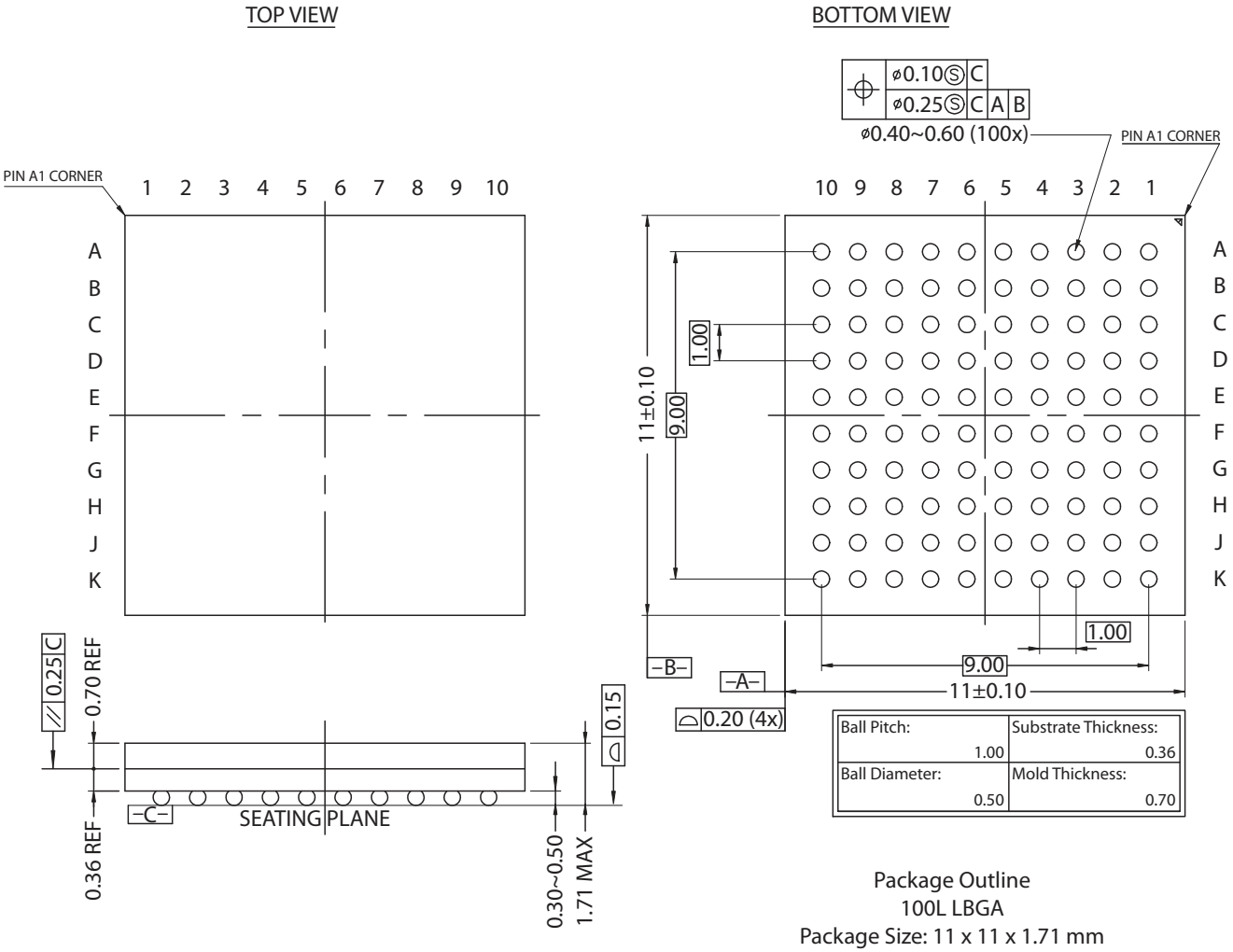
The STANDBY pin reduces power to a minimum by disabling all circuits except for the register configuration. Upon removal of the signal to the STANDBY pin, the device returns to its previous operating condition within 1 second, without requiring input from the host interface.

5. References & Relevant Standards

EN 50083-9	Interfaces for CATV/SMATV headends and similar professional equipment for DVG/MPEG-2 transport streams
ISO/IEC 13818-1	Generic Coding of Moving Pictures and Associated Audio Systems
ITU-R BT.1120-6	Digital interfaces for HDTV studio signals
ITU-R BT.656	Interface for digital component video signals
ITU-R BT.709	Parameter values for the HDTV standards for production and international programme exchange
SMPTE ST 272	Formatting AES Audio and Auxiliary Data into Digital Video Ancillary Data Space
SMPTE ST 291	Ancillary Data Packet and Space Formatting
SMPTE ST 296	1280 x 720 Progressive Image Sample Structure - Analog and Digital Representation and Analog Interface
SMPTE ST 299	24-Bit Digital Audio Format for SMPTE ST 292 Bit-Serial Interface
SMPTE RP165	Error Detection Checkwords and Status Flags for Use in Bit-Serial Digital Interfaces for Television

6. Package & Ordering Information

6.1 Package Dimensions



Package Outline
100L LBGA
Package Size: 11 x 11 x 1.71 mm

* The ball diameter, ball pitch, stand-off & package thickness are different from JEDEC spec M0192 (Low profile BGA family)

Figure 6-1: GV7605 Package Dimensions

6.2 Packaging Data

Table 6-1: Packaging Data

Parameter	Value
Package Type	11mm x 11mm 100-ball LBGA
Package Drawing Reference	JEDEC M0192 (with exceptions noted in Package Dimensions on page 143).
Moisture Sensitivity Level	3
Junction to Case Thermal Resistance, θ_{j-c}	15.4°C/W
Junction to Air Thermal Resistance, θ_{j-a} (at zero airflow)	37.1°C/W
Junction to Board Thermal Resistance, θ_{j-b}	26.4°C/W
Psi, ψ	0.4°C/W
Pb-free and RoHS Compliant	Yes

6.3 Marking Diagram

Figure 6-2: GV7605 Marking Diagram

6.4 Solder Reflow Profiles

The GV7605 is available in a Pb-free package. It is recommended that the Pb-free package be soldered with Pb-free paste using the reflow profile shown in Figure 6-3.

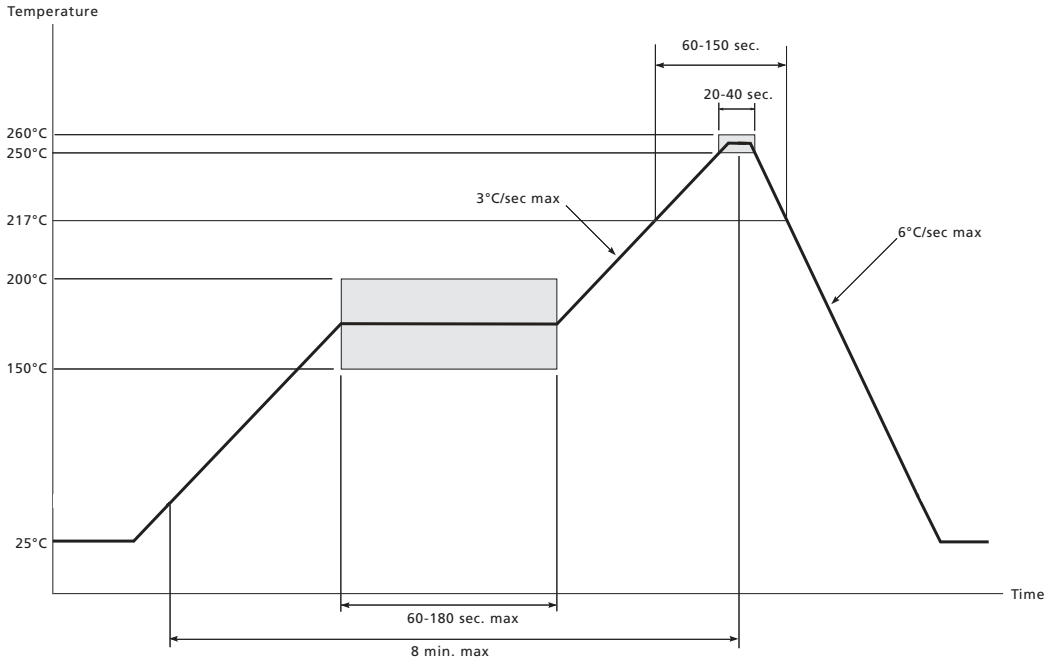


Figure 6-3: Pb-free Solder reflow Profile

6.5 Ordering Information

Part Number	Package	Pb-free	Temperature Range
GV7605-IBE3	100-ball BGA	Yes	-20°C to 85°C

Index

F

G

H

I

J

K

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M

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P

R

S

T

V

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