30-W, 48-V INPUT DC/DC CONVERTERS WITH AUTO-TRACK™ SEQUENCING

FEATURES

- **Input Voltage: 36 V to 75 V**
- **30-W Total Output Power**
- **Output Voltages: 3.3 V, 5 V, and 12 V**
- **Wide-Output Adjust/Trim**
- **Up To 88% Efficiency**
- **Overcurrent Protection**
- **Overtemperature Shutdown**
- **Undervoltage Lockout**
- **Input Overvoltage Protection**
- **Auto-Track™ Power-Up Sequencing (Includes Sequenced Output with PTB48560B)**
- **Smart-Sense Remote Sensing (PTB48560B)**
- **Dual-Logic Enable Control**
- **Space-Saving *1×2* Footprint**
- **Surface Mount Package**
- **1500-Vdc Isolation**
- **Agency Approvals (Pending): UL/cUL 60950, EN 60950**

APPLICATIONS

- **Intermediate Bus Architectures**
- **Telecom, High-End Computing Platforms**
- **Multi-Rail Power Systems with Power-Up Sequencing**

DESCRIPTION

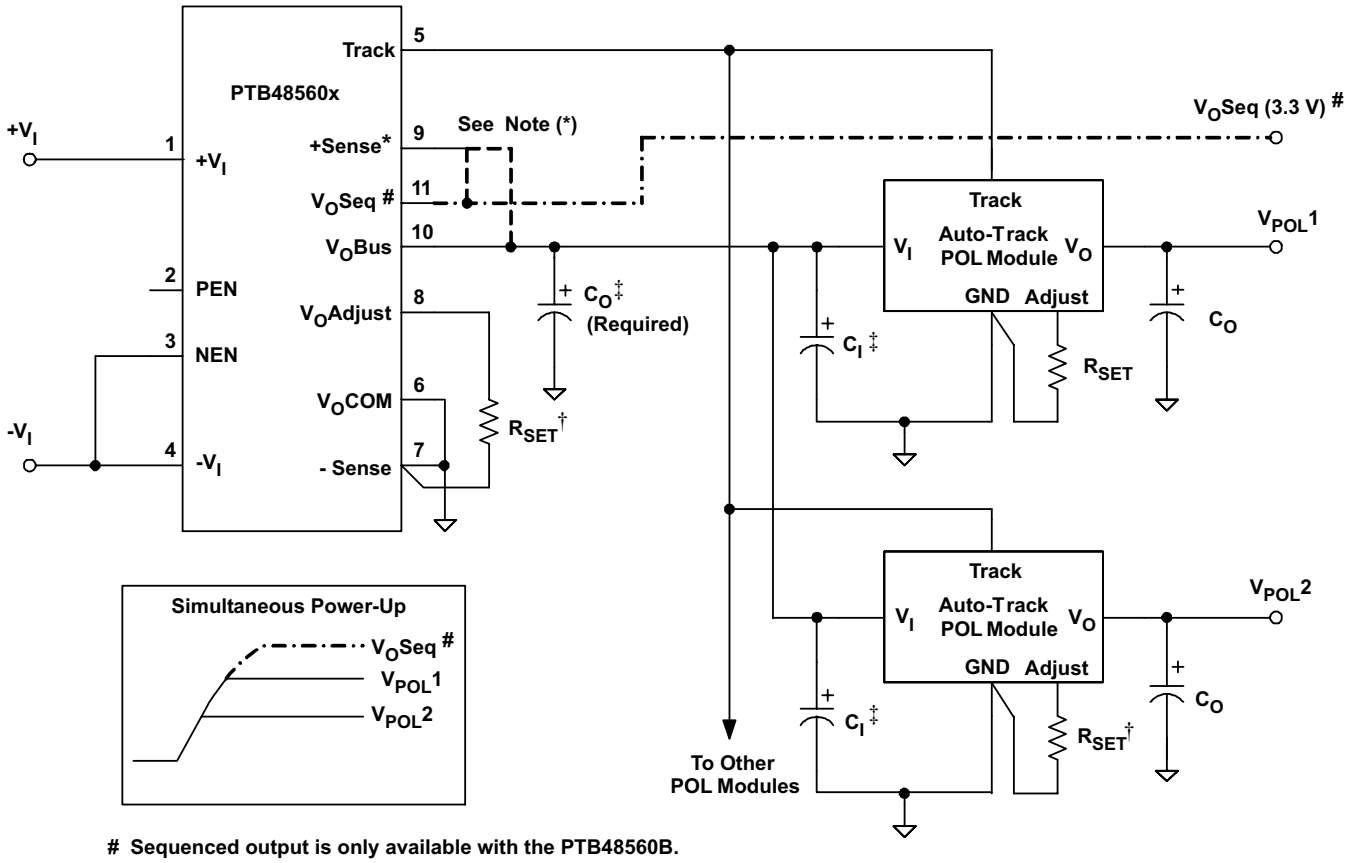
The PTB48560x is a series of 30–W rated isolated dc/dc converters, designed to operate from a standard -48–V telecom central office (CO) supply. Housed in a *1×2* package, each model has a wide-adjust output voltage that can be set to one of the common intermediate bus voltages of 3.3 V, 5 V, or 12 V.

The PTB48560 series incorporates Auto-Track™, a feature that simplifies the power-up sequencing of multiple power modules and operates from the same intermediate bus. During a power-up cycle, modules with this feature have the capability of following a common ramp voltage applied to an input called Track. The PTB48560 series is specifically designed to control the Track voltage of any number of nonisolated *downstream* modules powered from its output. This ensures that the outputs of the downstream modules all rise simultaneously during power up. The PTB48560B (3.3 V) has an additional sequenced output, V_O *Seq*, which also rises with the Track voltage. This allows the V_O *Seq* output to power up simultaneously with the outputs from other power modules under the control of Auto-Track.

Whether used to facilitate power-up sequencing, or operated as a stand-alone module, the PTB48560 series includes many other features expected of high-performance dc/dc converter modules. Precise output voltage regulation is ensured with a differential remote sense. Operational features include an input undervoltage lockout (UVLO) and a dual-logic output enable control. Overcurrent and overtemperature protection ensure survival against load faults.Typical applications include distributed power architectures in both telecom and computing environments, particularly complex digital systems requiring power sequencing of multiple power supply rails.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Typical Circuit



 # Sequenced output is only available with the PTB48560B.

*** The +Sense can be connected to either the V_OSeq or V_OBus output of the PTB48560B.**

† R_{SET} is required to set the output voltage higher than the minimum value; see the *Application Information* for values.

‡ The PTB48560x modules require a minimum total output capacitance for proper operation; see the *Electrical Characterisitics* for the value required by each model.

ORDERING INFORMATION

PTB48560 (Base Pt. Number)				
Output Voltage Range	**Part Number**	**DESCRIPTION**	**Pb – free and RoHS Compatible**	**Package Ref. (1)**
3.6 V to 5.5 V	PTB48560AAH	Horizontal T/H	Yes	ERW
	PTB48560AAS	Standard SMD (2)	No	ERY
	PTB48560AAZ	Optional SMD (3)	Yes	
1.8 V to 3.6 V	PTB48560BAH (4)	Horizontal T/H	Yes	ERW
	PTB48560BAS (4)	Standard SMD (2)	No	ERY
	PTB48560BAZ (4)	Optional SMD (3)	Yes	
9 V to o13.2 V	PTB48560CAH	Horizontal T/H	Yes	ERW
	PTB48560CAS	Standard SMD (2)	No	ERY
	PTB48560CAZ	Optional SMD (3)	Yes	

(1) See the applicable package reference drawing for the dimensions and PC board layout.
(2) *Standard* option specifies 63/37, Sn/Pb pin solder material.
(3) *Lead (Pb) – free option* specifies Sn/Ag pin solder material.
(4) Includes an Auto-Track compatible output, V_O *Seq*, which sequences with the *Track* control during power up.

ABSOLUTE MAXIMUM RATINGS

				PTB48560x	UNIT
V_I	Input Voltage		Continuous	75	V
			Surge, 1 s max	100 (1)	
$V_{(Track)}$	Track input voltage			0 to V_O Bus + 0.3	
$I_{(Track)}$ max	Track input current	From external source		10 (2)	mA
T_A 1	Operating temperature range	Over V_I range		–40 to 85	°C
	Overtemperature protection	PCB temperature (near pin 1)		115	
$T_{(WAVE)}$	Wave solder temperature	Surface temperature of module or pins **(5 seconds)**	PTB48560xAH	260 (3)	
$T_{(REFLOW)}$	Solder reflow temperature	Surface temperature of module or pins	PTB48560xAS	235 (3)	
			PTB48560xAZ	260 (3)	
T_{stg}	Storage temperature			–40 to 125	

(1) The converter's internal protection circuitry may cause the output to turn off when the applied input voltage is greater than 75 V.
(2) When the Track input is fed from an external voltage source, the input current must be limited. A 2.74-kΩ value series resistor is recommended.
(3) During solder reflow of SMD package version, do not elevate the module PCB, pins, or internal component temperatures this peak temperature.

PACKAGE SPECIFICATIONS

PTB48560x (Suffixes AH and AS)			
Weight			13.6 grams
Flammability	Meets UL94V-O		
Mechanical shock	Per Mil-STD-883D, Method 2002.3, 1 ms, 1/2 Sine, mounted	Horizontal T/H (Suffix AH)	500 Gs (1)
		Horizontal SMD (Suffix AS)	250 G (1)
Mechanical vibration	Mil-STD-883D, Method 2007.2, 20-2000 Hz, PCB mounted	Horizontal T/H (Suffix AH)	20 G (1)
		Horizontal SMD (Suffix AS)	5 G (1)

(1) Qualification limit.

PTB48560B ELECTRICAL CHARACTERISTICS

(Unless otherwise stated, T_A = 25°C, V_I = 48 V, V_O = 3.3 V, C_O = 220 µF, and I_O = $I_O$max)

PARAMETER		TEST CONDITIONS		PTB48560B			UNIT
				MIN	TYP	MAX	
I_O	Output current	Over V_I range	I_O Bus	0.25 (1)		8 (2)	A
			I_O Seq	0		4 (3)	
			Sum total, (I_O Bus + I_O Seq)	0.25		8	
V_I	Input voltage range	Over I_O range		36	48	75	V
V_O	Set-point voltage tolerance				±1 (4)		%V_O
	Temperature variation	-40°C ≤ T_A ≤ 85°C			±0.5		%V_O
	Line regulation	Over V_I range			±7	±33	mV
	Load regulation	Over I_O range			±13	±33	mV
	Total output voltage variation	Includes set-point, line, load, –40°C ≤ T_A ≤ 85°C			±2	±3 (4)	%V_O
	Adjust range	Over V_I range		1.8		3.6	V
η	Efficiency		R_{SET} = 5.36 kΩ, V_O = 3.3 V		82%		
			R_{SET} = 40.2 kΩ, V_O = 2.5 V		79%		
			R_{SET} = open , V_O = 1.8 V		74%		
	V_O Ripple (peak-to-peak)	20-MHz bandwidth			50		mV_{pp}
	Transient response	0.1 A/µs load step, 50% to 100% $I_O$max	Recovery time		100		µs
			V_O over/undershoot		±150		mV
	Track input (pin 5)	Input current	Track connected to -Sense		-0.13		mA
		Open-circuit voltage		0		V_O Bus	
		Input slew rate limits		0.1 (5)		1	V/ms
	Output enable inputs (pins 2, 3)	Referenced to -V_I	Input high voltage (V_{IH})	2		Open (6)	V
			Input low voltage (V_{IL})	-0.2		0.8	
			Input low current (I_{IL})		0.48		mA
	Standby input current	Pins 2 and 3 open			8	16	mA
I_O (tot)	Overcurrent threshold	Shutdown, followed by autorecovery			12		A
UVLO	Undervoltage lockout		V_I increasing		34		V
			V_I decreasing		33		
f_S	Switching frequency	Over V_I range		400	500	600	kHz
	Internal input capacitance				1		µF
	External output capacitance	Between both outputs and V_O COM		220		5,000	µF
	Isolation voltage	Input-output		1,500			Vdc
	Isolation capacitance	Input-output			2,000		pF
	Isolation resistance	Input-output		10			MΩ
MTBF	Reliability	Telcordia SR-332 50% stress, T_A = 40°C, ground benign		3.6			10^6 Hr

(1) The converter requires a minimum load current at either the *V_O Seq* or *V_O Bus* output for proper operation. The converter is not damaged when operated under a no-load condition.
(2) See temperature derating curves for safe operating area (SOA), to determine output current derating at elevated ambient temperatures.
(3) When load current is supplied from the V_O Seq output, the module exhibits higher power dissipation and slightly lower operating efficiency.
(4) The set-point voltage tolerance is affected by the tolerance and stability of R_{SET}. The stated limit is unconditionally met if R_{SET} has a tolerance of 1%, with 100 ppm/°C temperature stability.
(5) When controlling the Track input from an external source, the slew rate of the applied signal **must** be greater than the minimum limit. Failure to allow the voltage to completely rise to the voltage at the V_O (bus) output, at no less than the minimum specified rate, may thermally overstress the converter.
(6) The PEN and NEN inputs each have an internal pullup resistor. If the enable feature is not used, the PEN input (pin 2) should be left open circuit and the NEN input (pin 3) permanently connected to –V_I. A discrete MOSFET or bipolar transistor is recommended for the enable control. The open-circuit voltage is less than 10 V. See the *Application Information* for a more detailed description.

PTB48560A ELECTRICAL CHARACTERISTICS

(Unless otherwise stated, T_A = 25°C, V_I = 48 V, V_O = 5 V, C_O = 220 µF, and I_O = $I_O$max)

PARAMETER		TEST CONDITIONS		PTB48560A			UNIT
				MIN	TYP	MAX	
I_O	Output current	Over V_I range	I_O Bus	0.25 (1)		6 (2)	A
V_I	Input voltage range	Over I_O range		36	48	75	V
V_O	Set-point voltage tolerance				±1 (3)		%V_O
	Temperature variation	-40°C ≤ T_A ≤ 85°C			±0.5		%V_O
	Line regulation	Over V_I range			±0.2	±1	%V_O
	Load regulation	Over I_O range			±0.4	±1	%V_O
	Total output voltage variation	Includes set-point, line, load, –40°C ≤ T_A ≤ 85°C			±2	±3 (3)	%V_O
	Adjust range	Over V_I range		3.6		5.5	V
η	Efficiency	R_{SET} = 14.3 kΩ, V_O =5 V			84%		
	V_O Ripple (peak-to-peak)	20-MHz bandwidth			1		%V_O
	Transient response	0.1 A/µs load step, 50% to 100% $I_O$max	Recovery time		100		µs
			V_O over/undershoot		±150		mV
	Track input (pin 5)	Input current	Track connected to -Sense		–0.2		mA
		Open-circuit voltage		0		V_O Bus	
	Output enable inputs (pins 2, 3)	Referenced to -V_I	Input high voltage (V_{IH})	2		Open (4)	V
			Input low voltage (V_{IL})	-0.2		0.8	
			Input low current (I_{IL})		0.48		mA
	Standby input current	Pins 2 and 3 open			8	16	mA
I_O Bus	Overcurrent threshold	Shutdown, followed by autorecovery			9		A
UVLO	Undervoltage lockout		V_I increasing		34		V
			V_I decreasing		33		
f_S	Switching frequency	Over V_I range		400	500	600	kHz
	Internal input capacitance				1		µF
	External output capacitance	Between both outputs and V_O COM		220		5,000	µF
	Isolation voltage	Input-output		1,500			Vdc
	Isolation capacitance	Input-output			2,000		pF
	Isolation resistance	Input-output		10			MΩ
MTBF	Reliability	Telcordia SR-332 50% stress, T_A = 40°C, ground benign		3.6			10^6 Hr

(1) The converter requires a minimum load current for proper operation. The converter is not damaged when operated under a no-load condition.
(2) See temperature derating curves for safe operating area (SOA), to determine output current derating at elevated ambient temperatures.
(3) The set-point voltage tolerance is affected by the tolerance and stability of R_{SET}. The stated limit is unconditionally met if R_{SET} has a tolerance of 1%, with 100 ppm/°C temperature stability.
(4) The PEN and NEN inputs each have an internal pullup resistor. If the enable feature is not used, the PEN input (pin 2) should be left open circuit and the NEN input (pin 3) permanently connected to –V_I. A discrete MOSFET or bipolar transistor is recommended for the enable control. The open-circuit voltage is less than 10 V. See the *Application Information* for a more detailed description.

PTB48560C ELECTRICAL CHARACTERISTICS

(Unless otherwise stated, T_A = 25°C, V_I = 48 V, V_O = 12 V, C_O = 100 μF, and I_O = $I_O$max)

PARAMETER		TEST CONDITIONS		PTB48560C			UNIT
				MIN	TYP	MAX	
I_O	Output current	Over V_I range	I_O Bus	0.1 (1)		2.5 (2)	A
V_I	Input voltage range	Over I_O range		36	48	75	V
V_O	Set-point voltage tolerance				±1 (3)		%V_O
	Temperature variation	-40°C ≤ T_A ≤ 85°C			±0.5		%V_O
	Line regulation	Over V_I range			±0.2	±1	%V_O
	Load regulation	Over I_O range			±0.4	±1	%V_O
	Total output voltage variation	Includes set-point, line, load, –40°C ≤ T_A ≤ 85°C			±2	±3 (3)	%V_O
	Adjust range	Over V_I range		9		13.2	V
η	Efficiency		R_{SET} = 9.09 kΩ, V_O =12 V		88%		
			R_{SET} = open, V_O = 9 V		86%		
	V_O Ripple (peak-to-peak)	20-MHz bandwidth			1		%V_O
	Transient Response	0.1 A/μs load step, 50% to 100% $I_O$max	Recovery time		100		μs
			V_O over/undershoot		±150		mV
	Track input (pin 5)	Input current	Track connected to -Sense		0.48		mA
		Open-circuit voltage		0		V_O Bus	
	Output enable inputs (pins 2, 3)	Referenced to -V_I	Input high voltage (V_{IH})	2		Open (4)	V
			Input low voltage (V_{IL})	-0.2		0.8	
			Input low current (I_{IL})		–0.48		mA
	Standby input current	Pins 2 and 3 open			8	16	mA
I_O Bus	Overcurrent threshold	Shutdown, followed by autorecovery			3.75		A
UVLO	Undervoltage lockout		V_I increasing		34		V
			V_I decreasing		33		
f_S	Switching frequency	Over V_I range		400	500	600	kHz
	Internal input capacitance				1		μF
	External output capacitance	Between both outputs and V_O COM		100		1,500	μF
	Isolation voltage	Input-output		1,500			Vdc
	Isolation capacitance	Input-output			2,000		pF
	Isolation resistance	Input-output		10			MΩ
MTBF	Reliability	Telcordia SR-332 50% stress, T_A = 40°C, ground benign		3.4			10^6 Hrs

(1) The converter requires a minimum load current for proper operation. The converter is not damaged when operated under a no-load condition.
(2) See temperature derating curves for safe operating area (SOA), to determine output current derating at elevated ambient temperatures.
(3) The set-point voltage tolerance is affected by the tolerance and stability of R_{SET}. The stated limit is unconditionally met if R_{SET} has a tolerance of 1%, with 100 ppm/°C temperature stability.
(4) The PEN and NEN enable inputs each have an internal pullup resistor. If the enable feature is not used, the PEN input (pin 2) should be left open circuit and the NEN input (pin 3) permanently connected to –V_I. A discrete MOSFET or bipolar transistor is recommended for the enable control. The open-circuit voltage is less than 10 V. See the *Application Information* for a more detailed description.

TERMINAL FUNCTIONS

TERMINAL		DESCRIPTION
NAME	NO.	
$+V_I$ (1)	1	The positive input for the module with respect to $-V_I$. When powering the module from a negative input voltage, this input is connected to the input source ground.
$-V_I$ (1)	4	The negative input supply for the module, and the 0-V reference for the *PEN* and *NEN* enable inputs. When powering the module from a positive source, this input is connected to the input source return.
PEN (1)	2	An open-collector (open-drain) positive logic input that is referenced to $-V_I$. When this input is pulled to $-V_I$ potential the converter output is disabled. This input must be open circuit for the converter to operate. The converter then produces an output whenever a valid input source is applied.
NEN (1) (2)	3	An open-collector (open-drain) negative logic input that is referenced to $-V_I$. This input must be pulled to $-V_I$ potential to enable the converter. When the input is open circuit, the converter output is disabled. If the enable feature is not used, this input should be permanently connected to $-V_I$. The module then produces an output whenever a valid input source is applied.
V_O Bus	10	This is the positive power output with respect to *V_O COM*, and the main output from the converter. It is dc isolated from the input power pins and produces a valid output voltage approximately 20 ms before the voltage at the *Track* terminal is allowed to rise. This provides the required standby power source to any *downstream* nonisolated modules in power-up sequencing applications.
V_O Seq	11	This is a sequenced output voltage from the converter that is controlled by the *Track* terminal during power-up transitions. It is only available to the PTB48560B, and used with the output voltage set to 3.3 V (an I/O supply voltage). During power up, the voltage at *V_O Seq* rises with the *Track* terminal, typically 20 ms after the *V_O Bus* output has reached regulation.
V_O COM	6	This is the output power return for both the *V_O Bus* and *V_O Seq* output voltages. This terminal should be connected to the common of the load circuit.
Track	5	This terminal is used in power-up sequencing applications to control the output voltage of Auto-Track compatible modules, powered from the converter *V_OBus* output. This includes the converter *V_OSeq* output on the PTB48560B. The converter *Track* control has an internal transistor, which holds the voltage close to *V_OCOM* potential for approximately 20 ms (40 ms with the PTB48560C) after the *V_OBus* output is in regulation. Following this delay, the *Track* voltage and *V_OSeq* rises simultaneously with the output voltage of all other modules controlled by Auto-Track.
–Sense	7	Provides the converter with a remote sense capability when used with *+Sense*. For optimum output voltage accuracy, this pin should always be connected to *V_OCOM*, close to the load circuit. This terminal is also the reference connection for both the output voltage set-point resistor and *Track* control.
V_O Adjust	8	A resistor must be connected between this terminal and *-Sense* to set the converter output voltage. A 0.05-W rated resistor may be used, with tolerance and temperature stability of 1% and 100 ppm/°C, respectively. If left open circuit, the converter output voltage defaults to its lowest value. The specification table gives the standard resistor values for the most common output voltages.
+Sense	9	The *+Sense* pin can be connected to *V_OBus* (or *V_OSeq*) output. When connected to *V_OSeq*, remote sense compensation is delayed until the converter's power-up sequence is complete. The voltage at *V_OBus* is also raised slightly. The *+Sense* input may be left open circuit, but connecting it to one of the output terminals improves load regulation of that output.

(1) These functions indicate signals electrically common with the input.
(2) Denotes negative logic: Low ($-V_I$) = Normal operation, Open = Output off

TYPICAL CHARACTERISTICS

PTB48560B Characteristic Data (V_O = 3.3 V) (1) (2)

EFFICIENCY vs OUTPUT CURRENT

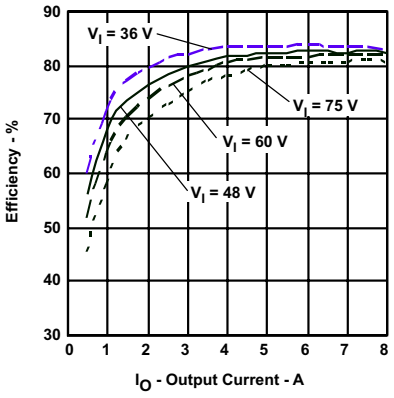


Figure 1.

OUTPUT VOLTAGE RIPPLE vs OUTPUT CURRENT

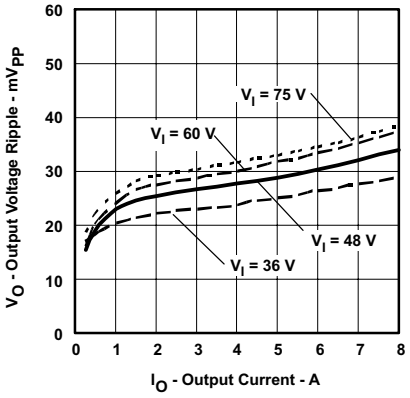


Figure 2.

POWER DISSIPATION vs OUTPUT CURRENT

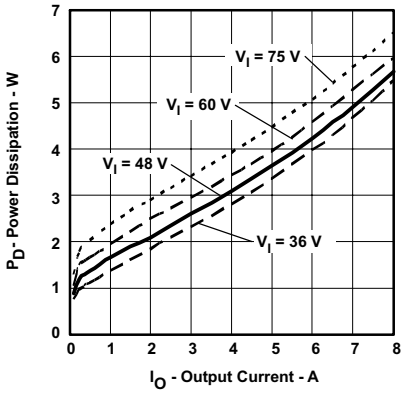


Figure 3.

TEMPERATURE DERATING vs OUTPUT CURRENT

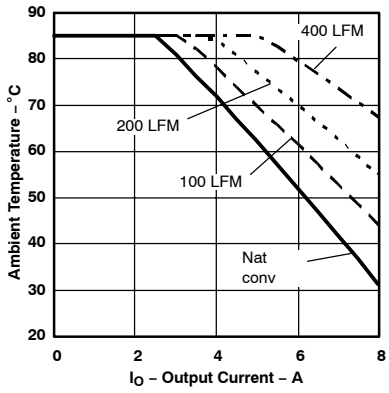


Figure 4.

(1) All data listed in Figure 1, Figure 2, and Figure 3 have been developed from actual products tested at 25°C. This data is considered typical data for the dc-dc converter.

(2) The temperature derating curves represent operating conditions at which internal components are at or below manufacturer's maximum rated operating temperature. Derating limits apply to modules soldered directly to a 100–mm × 100–mm, double-sided PCB with 2 oz. copper. For surface mount packages, multiple vias (plated through holes) are required to add thermal paths around the power pins. Please refer to the mechanical specification for more information. Applies to Figure 4.

TYPICAL CHARACTERISTICS (continued)

PTB48560A Characteristic Data (V_O = 5 V) (3) (4)

EFFICIENCY
VS
OUTPUT CURRENT

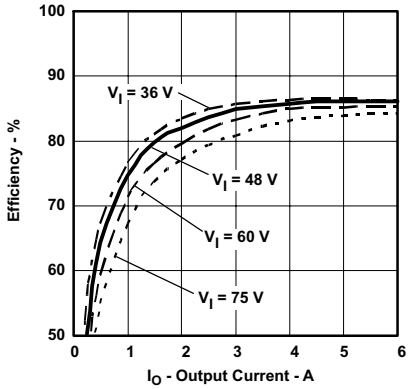


Figure 5.

OUTPUT VOLTAGE RIPPLE
VS
OUTPUT CURRENT

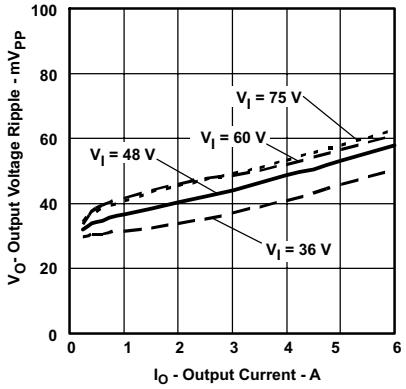


Figure 6.

POWER DISSIPATION
VS
OUTPUT CURRENT

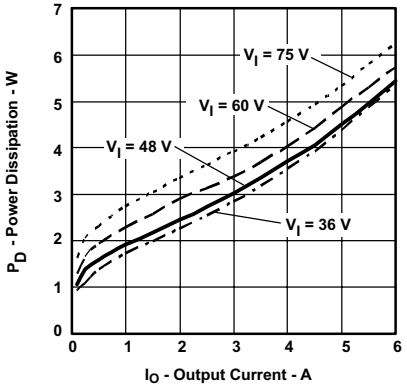


Figure 7.

TEMPERATURE DERATING
VS
OUTPUT CURRENT

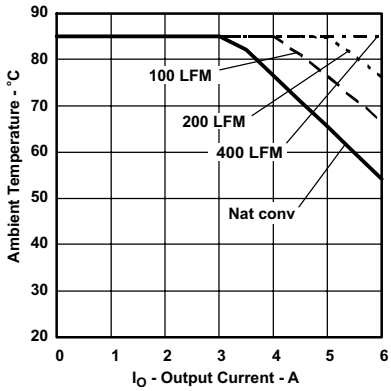


Figure 8.

(3) All data listed in Figure 5, Figure 6, and Figure 7 have been developed from actual products tested at 25°C. This data is considered typical data for the dc-dc converter.

(4) The temperature derating curves represent operating conditions at which internal components are at or below manufacturer's maximum rated operating temperature. Derating limits apply to modules soldered directly to a 100–mm × 100–mm, double-sided PCB with 2 oz. copper. For surface mount packages, multiple vias (plated through holes) are required to add thermal paths around the power pins. Please refer to the mechanical specification for more information. Applies to Figure 8.

TYPICAL CHARACTERISTICS (continued)

PTB48560C Characteristic Data (V_O = 12 V) (5)(6)

EFFICIENCY vs OUTPUT CURRENT

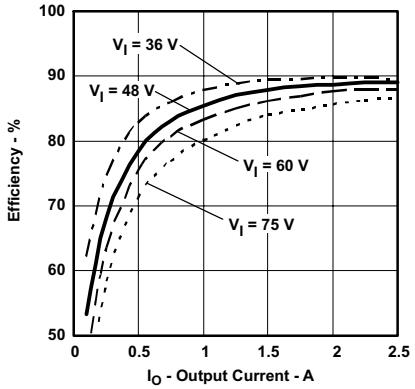


Figure 9.

OUTPUT VOLTAGE RIPPLE vs OUTPUT CURRENT

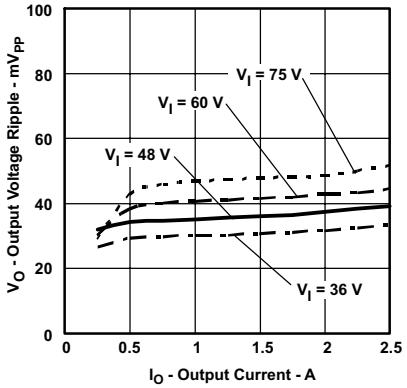


Figure 10.

POWER DISSIPATION vs OUTPUT CURRENT

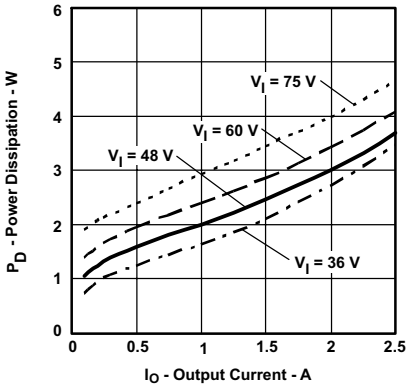


Figure 11.

TEMPERATURE DERATING vs OUTPUT CURRENT

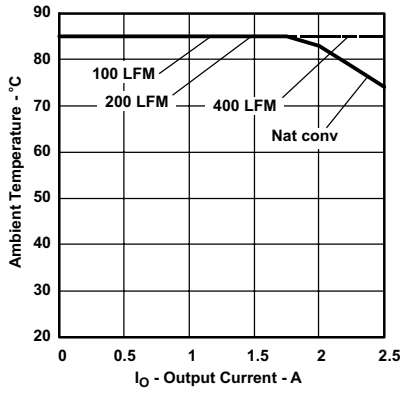


Figure 12.

(5) All data listed in Figure 9, Figure 10, and Figure 11 have been developed from actual products tested at 25°C. This data is considered typical data for the dc-dc converter.

(6) The temperature derating curves represent operating conditions at which internal components are at or below manufacturer's maximum rated operating temperature. Derating limits apply to modules soldered directly to a 100–mm × 100–mm, double-sided PCB with 2 oz. copper. For surface mount packages, multiple vias (plated through holes) are required to add thermal paths around the power pins. Please refer to the mechanical specification for more information. Applies to Figure 12.

APPLICATION INFORMATION

Operating Features and System Considerations for the PTB48560x DC/DC Converters

Primary-Secondary Isolation

These converters incorporate electrical isolation between the input terminals (primary) and the output terminals (secondary). All converters are tested to a withstand voltage of 1500 VDC. This complies with UL/cUL 60950 and EN 60950 and the requirements for functional isolation. It allows the converter to be configured for either a positive or negative input voltage source. The data sheet *Terminal Functions* table provides guidance as to the correct reference that must be used for the external control signals.

Undervoltage Lockout

The undervoltage lockout (UVLO) is designed to prevent the operation of the converter until the input voltage is close to the minimum operating voltage. The converter is held off when the input voltage is below the UVLO threshold, and turns on when the input voltage rises above the threshold. This prevents high start-up current during normal power up of the converter, and minimizes the current drain from the input source during low input voltage conditions. The converter meets full specifications when the minimum specified input voltage is reached. The UVLO circuitry also overrides the operation of the *PEN* and *NEN* enable controls. Only when the input voltage is above the UVLO threshold do these inputs become functional.

Soft-Start Power Up

When the converter is first powered, the internal soft-start circuit limits how fast the output voltage can rise. The soft-start circuit functions whenever the converter output is enabled from the PEN and NEN inputs, or when a valid input source is first applied with the output enabled. It also functions on a recovery from a load fault, overtemperature, or input overvoltage condition. The purpose of the soft-start feature is to limit the surge of current drawn from the input source when the converter begins to operate. By limiting the rate at which the output voltage rises, the magnitude of current required to charge up the load circuit capacitance is significantly reduced.

Figure 13 shows the power-up characteristic of a PTB48560C converter. The output voltage is set to 12 V. The soft-start circuit introduces a short time delay (typically 5-10 ms) before allowing the output to rise. The output then progressively rises to the voltage set-point. The waveforms were recorded with a resistive load of 2.5 A.

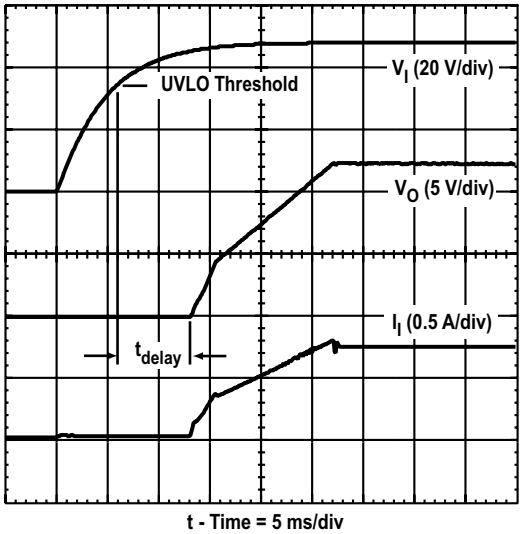


Figure 13. Soft-Start Waveform

Overcurrent Protection

To protect against load faults, these converters incorporate output overcurrent protection. Applying a load to the

APPLICATION INFORMATION (continued)

output that exceeds the converter overcurrent threshold (see applicable specification) causes the output voltage to momentarily fold back, and then shut down. Following shutdown, the module periodically attempts to automatically recover by initiating a soft-start power up. This is often described as a *hiccup* mode of operation, whereby the module continues in the cycle of successive shutdown and power up until the load fault is removed. Once the fault is removed, the converter automatically recovers and returns to normal operation.

Input Overvoltage Protection

The converter protects itself against input voltage surges and transients of up to 100 V. This is above the maximum continuous operating input voltage of 75 V. In order to protect itself, the converter output is disabled at some voltage above 75 V. This is to ensure that the converter internal components are not exposed to voltages above their stress ratings. The converter output remains off for some of the period that the input voltage is above the maximum continuous rating. Once the overvoltage event has passed, the output from the converter automatically restarts by executing a soft-start power up.

Differential Output Voltage Sense

A differential remote sense allows a converter regulation circuitry to compensate for limited amounts of IR drop, that may be incurred between the converter and load, in either the positive or return PCB traces. Connecting the *+Sense* and *–Sense* pins to the respective positive and ground reference of the load terminals improves the load regulation of the converter output voltage at that connection point. The *–Sense* pin should always be connected to the V_O *COM*. The *+Sense* pin may be connected to either the $+V_O$ *Bus* or $+V_O$ *Seq* outputs.

When the *+Sense* pin is connected to the V_O *Seq* output, the voltage at V_O *Bus* voltage regulates slightly higher. Depending on the load conditions on the V_O *Seq* output, the voltage at V_O *Bus* may be up to 100 mV higher than the converter set-point voltage. In addition, the Smart-Sense feature (incorporated into the converter) only engages sense compensation to the V_O *Seq* output when that output voltage is close to the set-point. During a power-up sequencing event, the sense circuit automatically defaults to sensing the V_O *Bus* voltage, internal to the converter.

Leaving the *+Sense* and *–Sense* pins open does not damage the converter or load circuit. The converter includes default circuitry that keeps the output voltage in regulation. However, if the remote sense feature is not used, the *–Sense* pin should still be connected to V_O*COM*.

Note: *The remote sense feature is not designed to compensate for the forward drop of nonlinear or frequency-dependent components that may be placed in series with the converter output. Examples include OR-ing diodes, filter inductors, ferrite beads, and fuses. When these components are enclosed by the sense pin connections, they are effectively placed inside the regulation control loop, which can adversely affect the stability of the converter.*

Overtemperature Protection

Overtemperature protection is provided by an internal temperature sensor, which monitors the temperature of the converter PCB (close to pin 1). If the PCB temperature exceeds a nominal 115°C, the converter shuts down. The converter then automatically restarts when the sensed temperature falls to approximately 105°C. When operated outside its recommended thermal derating envelope (see data sheet derating curves), the converter typcially cycles on and off at intervals from a few seconds to one or two minutes. This is to ensure that the internal components are not permanently damaged from excessive thermal stress.

Output Voltage Adjustment

An external resistor is required to set the nominal output voltage(s) of the converter to a voltage higher than its minimum value. The resistor, R_{SET}, must be connected directly between the V_O *Adjust* (pin 8) and *–Sense* (pin 7) terminals. A 0.05-W rated resistor can be used. The tolerance should be 1%, with a temperature stability of 100 ppm/°C (or better). Place the resistor close to the converter and connect it using dedicated PCB traces (see Figure 14). Table 1 gives the nearest standard value of external resistor for the common voltages within each model's adjust range. The actual output voltage that the resistor value provides is also provided.

Table 1. Standard Values of R_{SET} for Common Output Voltages

	PTB48560A		PTB48560B		PTB48560C	
V_O (Required)	R_{SET}	V_O (Actual)	R_{SET}	V_O (Actual)	R_{SET}	V_O (Actual)
1.8 V	–	–	Open	1.802 V	–	–
2 V	–	–	200 kΩ	2.004 V	–	–
2.5 V	–	–	40.2 kΩ	2.498 V	–	–
3.3 V	–	–	5.36 kΩ	3.300 V	–	–
3.6 V	Open	3.611 V	309 Ω	3.600 V	–	–
5 V	14.3 kΩ	5.005 V	–	–	–	–
9 V	–	–	–	–	Open	9.015 V
10 V	–	–	–	–	73.2 kΩ	9.993 V
12 V	–	–	–	–	9.09 kΩ	12 V
13.2 V	–	–	–	–	0 Ω	13.23 V

For other output voltages, the value of the required adjust resistor may be calculated using Equation 1.

$$R_{SET} = R_O \times \frac{V_R}{(V_O - Vmin)} - R_P \quad (1)$$

Table 2 gives the output voltage adjust range and the required equation constants for the converter model selected. To calculate the required value of R_{SET}, simply locate the applicable constants and substitute these into the formula along with the desired output voltage.

Table 2. Adjust Ranges and Equation Constants

Model #	PTB48560A	PTB48560B	PTB48560C
V_R	1.24 V	1.24 V	2.5 V
R_O	49.91 kΩ	36.55 kΩ	37.27 kΩ
R_P	30.1 kΩ	24.9 kΩ	22.1 kΩ
V_{MIN}	3.61 V	1.8 V	9.02 V
V_{MAX}	5.5 V	3.6 V	13.2 V

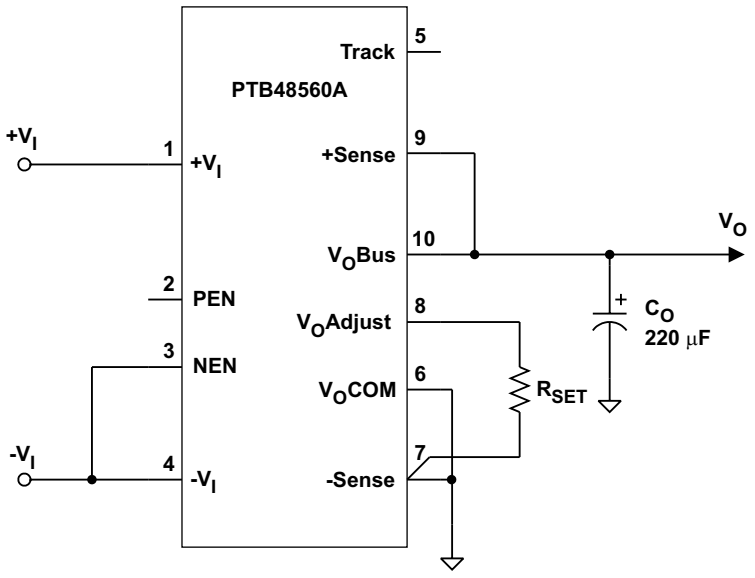


Figure 14. Output Voltage Adjustment

Input Current Limiting

The converter is not internally fused. For safety and overall system protection, the maximum input current to the converter must be limited. Active or passive current limiting can be used. Passive current limiting can be a fast-acting fuse. A 125-V fuse, rated no more than 5 A, is recommended. Active current limiting can be implemented with a current limited *Hot-Swap* controller.

Thermal Considerations

Airflow may be necessary to ensure that the module can supply the desired load current in environments with elevated ambient temperatures. The required airflow rate is determined from the safe operating area (SOA). The SOA is the area beneath the applicable airflow rate curve on the graph of temperature derating vs output current. (See the Typical Characteristics.) Operating the converter within the SOA limits ensures that all the internal components are at or below their stated maximum operating temperatures.

Using the On/Off Enable Controls on the PTB48560x Auto-Track Compatible DC/DC Converters

The converter incorporates two output enable controls. PEN (pin 2) is the positive enable input, and NEN (pin 3) is the negative enable input. Both inputs are electrically referenced to $-V_I$ (pin 4) on the primary or input side of the converter. The enable pins are ideally controlled with an open-collector (or open-drain) discrete transistor. Each input has an internal pullup resistor to a reference. There is no benefit to adding pullup resistors external to the module. If they are added, the maximum input voltage for these inputs must be limited to a maximum of 60 V.

Automatic (UVLO) Power Up

Connecting NEN (pin 3) to $-V_I$ (pin 4) and leaving PEN (pin 2) open-circuit, configures the converter for automatic power up. The converter control circuitry incorporates an undervoltage lockout (UVLO) function, which disables the converter until the minimum specified input voltage is present at $\pm V_I$ (see the Electrical Characteristics table). The UVLO circuitry ensures a clean transition during power up and power down, allowing the converter to tolerate a slow rising input voltage. For most applications, the PEN and NEN enable controls can be configured for automatic power up.

Positive Output Enable (Negative Inhibit)

To configure the converter for a positive enable function, connect NEN (pin 3) to $-V_I$ (pin 4), and apply the system On/Off control signal to PEN (pin 2). In this configuration, applying less than 0.8 V (with respect to $-V_I$ potential) to pin 2 disables the converter output. Figure 15 gives an example circuit that uses a MOSFET transistor.

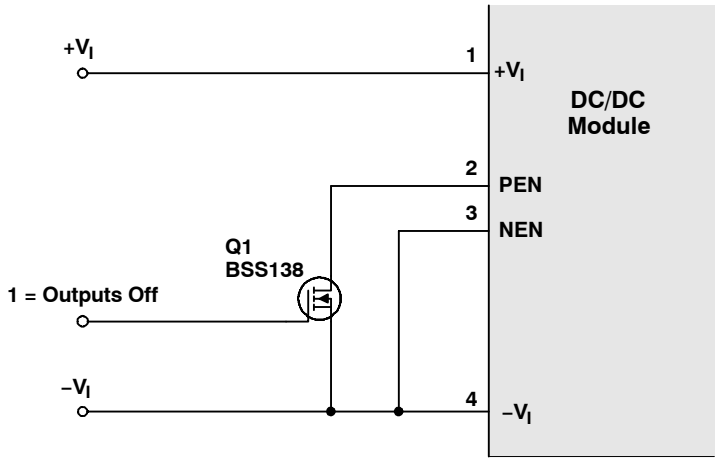


Figure 15. Positive Enable Configuration

Negative Output Enable (Positive Inhibit)

To configure the converter for a negative enable function, PEN (pin 2) is left open circuit, and the system On/Off control signal is applied to NEN (pin 3). A low-level control signal (less than 0.8 V) must then be applied to pin 3 to enable an output from the converter. An example of this configuration is detailed in Figure 16.

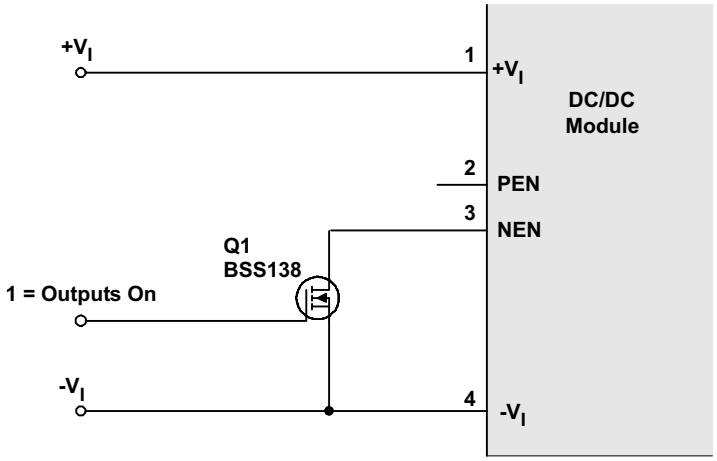


Figure 16. Negative Enable Configuration

On/Off Enable Turn-On Time

Once enabled, the converter executes a soft-start power up. The converter exibits a short delay of approximately 7 ms, measured from the transition of the enable signal to the instance the V_O Bus output begins to rise. The output is in regulation within 20 ms.

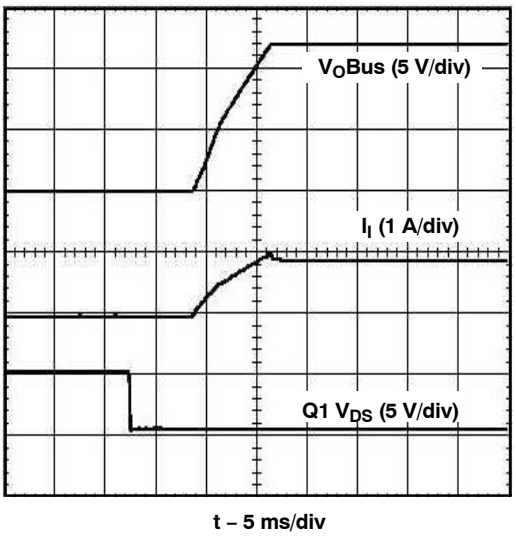


Figure 17. Output Enable Power-Up Characteristic

Sequenced Power Up with POL Modules

Overview

The main output from the PTB48560x converters is V_OBus. In power sequencing applications, V_OBus is used as the intermediate supply voltage for powering one or more *downstream* nonisolated power modules that incorporate Auto-Track™[1]. The output voltage from Auto-Track compliant modules can be sequenced using a control input called Track. The Track input directly controls the output of a module from zero to its set-point voltage. The control is on a *volt-for-volt* basis, and allows multiple modules to follow a common analog signal during power-up events.

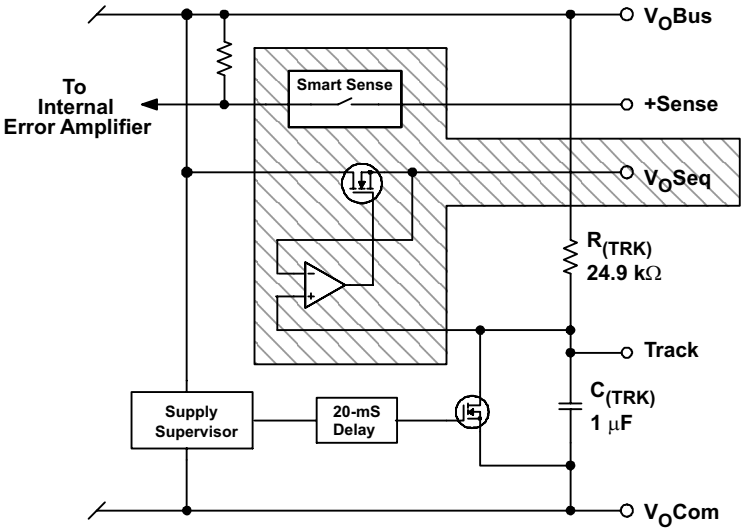
The Track signal attempts to start rising when the nonisolated modules are first powered from V_OBus. However, for proper sequencing, the voltage must be held at ground potential for at least 20 ms (40 ms for 12-V input modules) after V_OBus is in regulation. This is necessary to allow time for the nonisolated modules to complete their power-up initialization. The Track pin of each PTB48560x converter has an internal open-drain transistor that automatically holds the Track signal at ground potential to comply with this requirement.

The PTB48560B (1.8 V to 3.6 V) has a V_OSeq output. V_OSeq is internally derived from V_OBus and regulated to the same set-point voltage. It has the added feature of being controlled by the Track input. During power up, this output can sequence with the outputs of the nonisolated modules powered from V_OBus.

Auto-Track Features

Figure 18 shows a block diagram of the converter Auto-Track features. The components shaded are only present in the PTB48560B. During power up, V_OBus rises promptly, after the converter is connected to a valid input source and its output is enabled. V_OSeq (PTB48560B) is the Auto-Track compatible output that is controlled by the voltage presented at the Track terminal. The control is active from 0 V up to a voltage just below the V_OBus output. Between these limits, the voltage at V_OSeq follows that at the Track terminal. Once the Track voltage is at the V_OBus voltage, raising it higher has no further effect. The voltage at V_OSeq cannot go higher than V_OBus, and if connected to +Sense, it regulates at the set-point voltage.[2]

The Track input to the PTB48560x series of converters include a pullup resistor (R_{TRK}) to V_OBus, and a 1-μF capacitor (C_{TRK}) to -Sense. These components are standard on all Auto-Track compatible modules. They form an R–C time constant that cause the Track voltage to rise when the internal MOSFET is turned off. The unity-gain relationship between V_OSeq and the Track input is the same as all other Auto-Track compliant outputs.[3] The V_OSeq output also follows a compatible external ramp waveform applied to the Track pin.[4, 5] The internal MOSFET is designed to hold the Track voltage at ground potential for the required period after the V_OBus output is in regulation.



Note: The shaded functions are only available with the PTB48560B (3.3-V output).

Figure 18. Block Diagram of Auto-Track Features

Notes:

1. Auto-Track compatible modules incorporate a Track input that can take direct control of the output voltage during power-up transistions. The control relationship is on a volt-for-volt basis and is active between the 0 V and the module set-point voltage. Once the Track input is above the set-point voltage, the module remains at its set-point. Connecting the Track input of a number of such modules together allows their outputs to follow a common control voltage during power up.
2. When +Sense is connected to the V_OSeq output of the PTB48560B, the V_OSeq output is tightly regulated to the set-point voltage. In this configuration, the voltage at the V_OBus output is up to 100 mV higher.
3. The V_OSeq output on the PTB48560B cannot sink load current. This constraint does not allow the module to coordinate a sequenced power down.
4. The slew rate for the Track input signal must be between 0.1 V/ms and 1 V/ms. Above this range, the V_OSeq output may no longer accurately follow the Track input voltage. A slew rate below this range may thermally stress the converter. These slew rate limits are automatically met whenever the Track voltage is controlled by the internal R-C time constant of the modules being sequenced.
5. If an external voltage is used to control the Track terminal, the source current **must** be limited. A resistance value of 2.74-kΩ is recommended for this purpose. This is necessary to protect the internal transistor to the converter. This transistor holds the track control voltage at ground potential for 20 ms after the V_OBus output is in regulation.

Power-Up Sequencing With A V_O SEQ Output (PTB48560B)

Figure 19 shows the PTB48560B converter (U1) providing two 3.3-V sources. This allows it to both power and sequence with one or more *downstream* nonisolated modules. The example shows two 3.3-V input PTH03050W modules (U2 and U3), each rated for up to 6 A of output current. The selection and current rating of the nonisolated modules depends on the requirements of a specific application. The number of modules, their respective output voltage, and load current rating combine with the load required at the V_OSeq output. The total must be supplied by the PTB48560B, and cannot exceed that available at the V_OBus output.

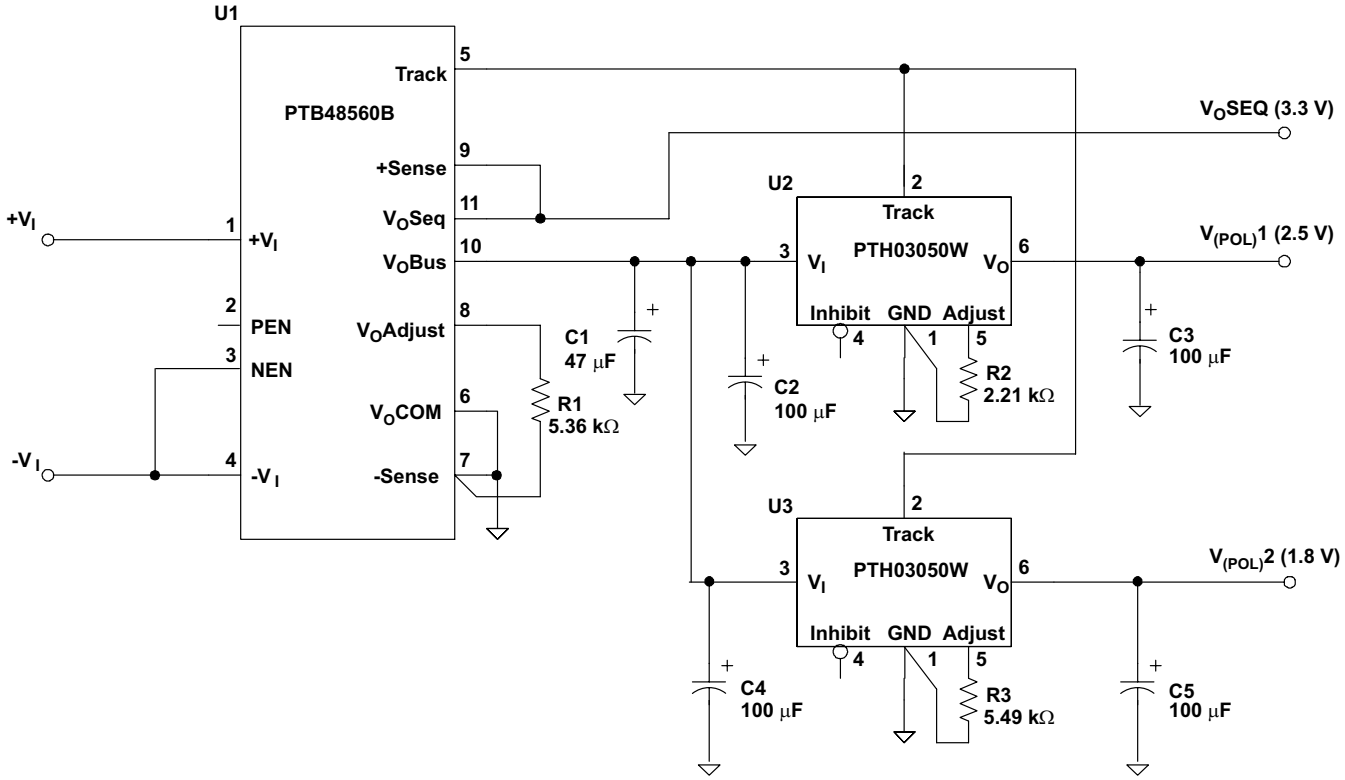


Figure 19. Power-Up Sequencing With Nonisolated POL Modules

The output voltage adjust range of the PTB48560B is 1.8 V to 3.6 V. In these applications, the output voltage must always be set to 3.3 V (R1 = 5.36 kΩ). This sets the output voltage of both the V_OBus and V_OSeq outputs. The output voltage of the 3.3-V input (nonisolated) modules, U2 and U3, can be set to any voltage over the range, 0.8 V to 2.5 V. In this example, they are set to 2.5 V (R2 = 2.21 kΩ) and 1.8 V (R3 = 5.49 kΩ), respectively. Figure 20 shows the power-up waveforms from Figure 19 when the Track input to all three modules are simply connected together.

The converter provides input power to the downstream nonisolated modules via the V_OBus output. This output rises first to allow the nonisolated modules to complete their power-up initialization. The V_OSeq (3.3 V), $V_{(POL)}1$ (2.5 V) and $V_{(POL)}2$ (1.8 V), outputs supply the load circuit, and rise simultaneously when the converter removes the internal ground signal to its own Track input. The V_OSeq output rises with the outputs from the nonisolated modules, until it reaches its set-point voltage.

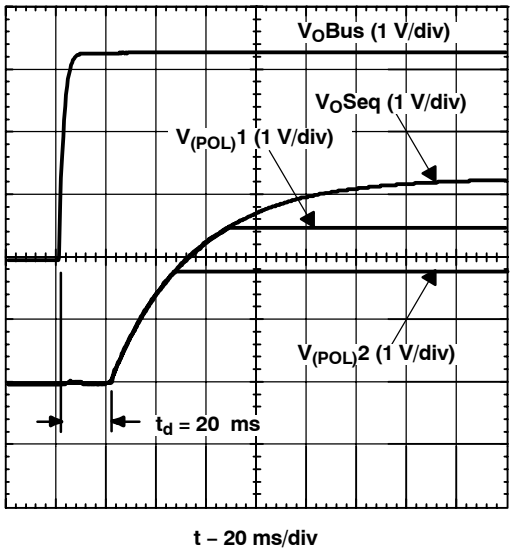


Figure 20. Power-Up Waveforms with POL Modules

Power-Up Sequencing Without A V_OSEQ Output (PTB48560A/C)

Although the PTB48560A or PTB48560C do not have a V_OSeq output, they can provide the input power and coordinate the power-up sequencing to two or more nonisolated, Auto-Track compliant power modules. Figure 21 shows the PTB48560A (5 V) converter (U1) configured to provide both the input source and the power-up sequence timing to two 5-V input nonisolated modules. The example shows two PTH05050W modules (U2 and U3), each rated for up to 6 A of output current. In this case, the number of downstream modules, and their respective output voltage and load current rating, is only limited by the amount of current available at the V_OBus output.

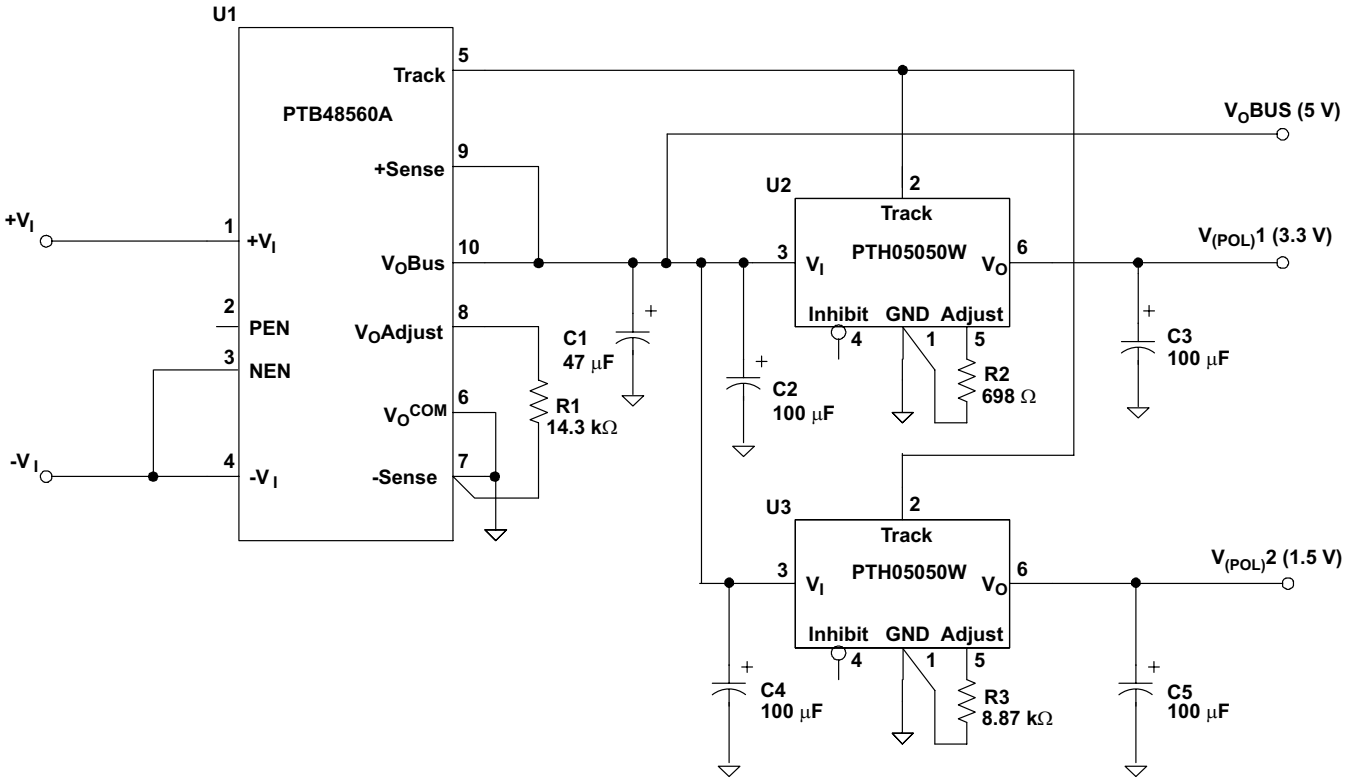


Figure 21. Power-Up Sequencing With Nonisolated POL Modules

The output voltage of the PTB48560 must be set to a valid intermediate supply voltage. This depends on the input voltage requirements of the downstream modules. For 5-V input modules, the PTB48560A is selected and adjusted for an output of 5 V. For 12-V input modules, the PTB48560C is used and adjusted for an output of 12 V. U2 and U3, can be set to any voltage over their applicable adjustment range. In this example, they are set to 3.3 V (R2 = 698 Ω) and 1.5 V (R3 = 8.87 kΩ), respectively. Figure 22 shows the power-up waveforms from Figure 21 when the Track control of all three modules are simply connected together.

The PTB48560 converter (U1) provides the required intermediate voltage from the V_OBus output to power the downstream modules, while holding the common Track control at ground potential. After allowing times for U2 and U3 to initialize, U1 removes the ground from the Track control, allowing this voltage to rise. The outputs from the two nonisolated modules then rise simultaneously to their respective set-point voltages.

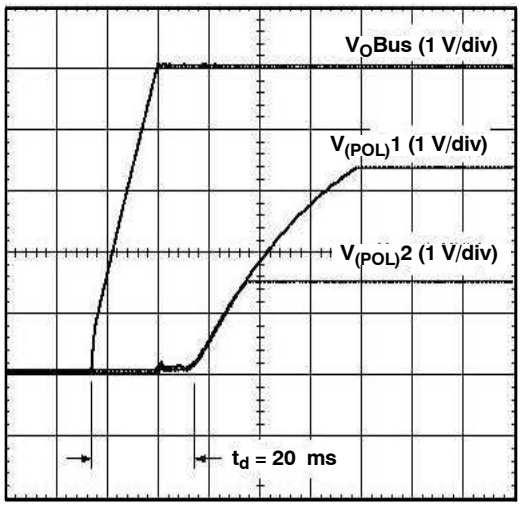


Figure 22. Power-Up Waveform

Stand-Alone Operation

The wide output voltage adjust range makes either model of the PTB48560 series of converters an attractive product as a stand-alone dc/dc converter. In these applications, it is not required to power up or sequence with any nonisolated POL modules. The output voltage can be adjusted to any value within the applicable adjust range. The Auto-Track features are simply not used.

Figure 23 shows the recommended configuration when these converters are used as a stand-alone regulator. The main output (V_O Bus) can be used to supply the load directly. Both the Track pin and the V_O Seq output (PTB48560B) are simply left open circuit. The +Sense pin should be connected to the V_O Bus output for improved load regulation.

When the converter is operated in this mode, the output from V_O Bus rises promptly on power up.

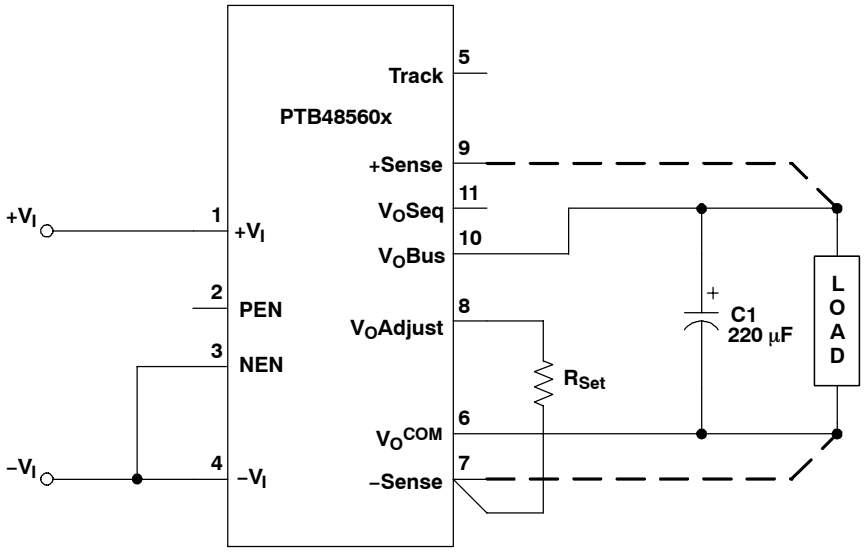
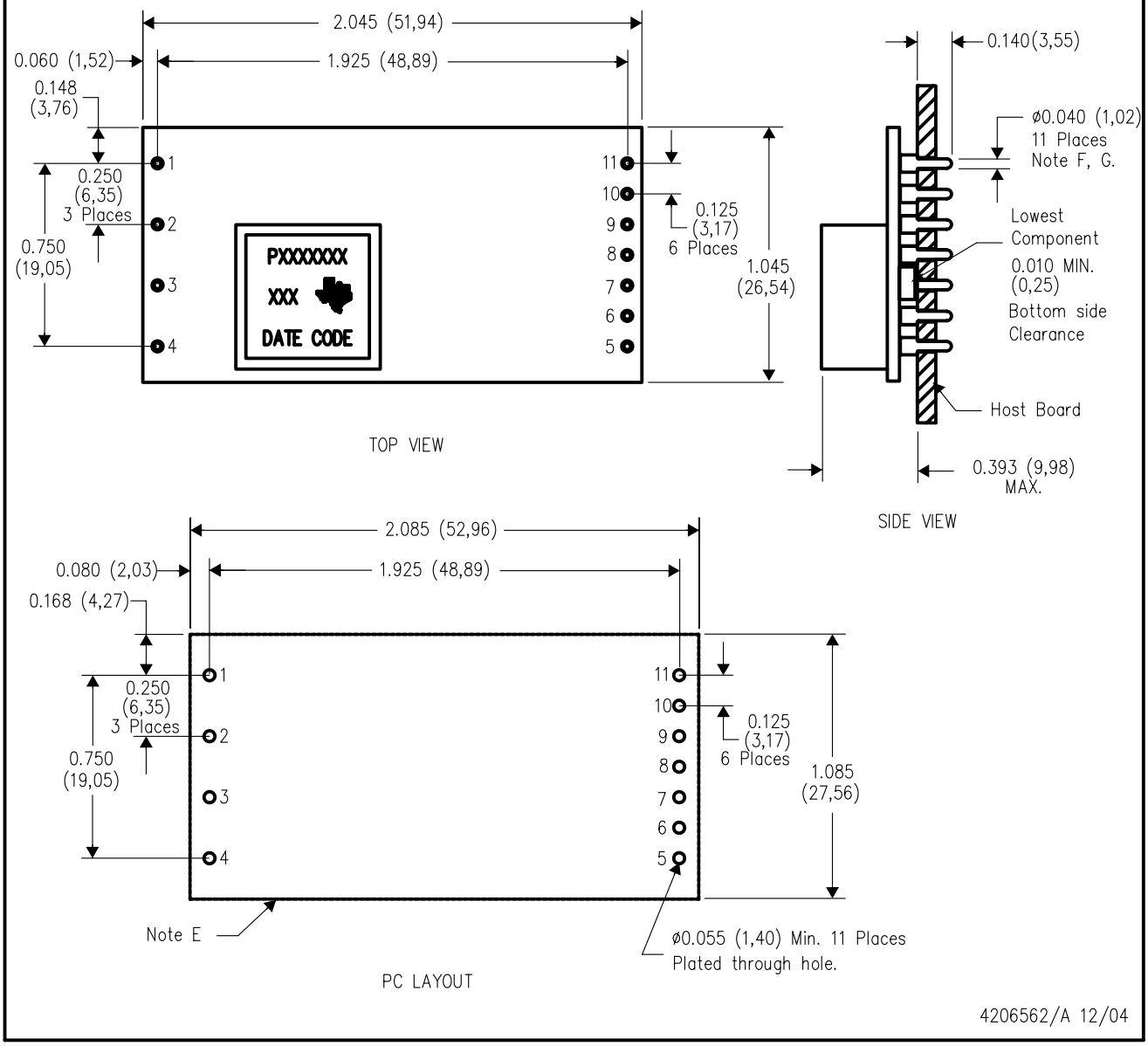


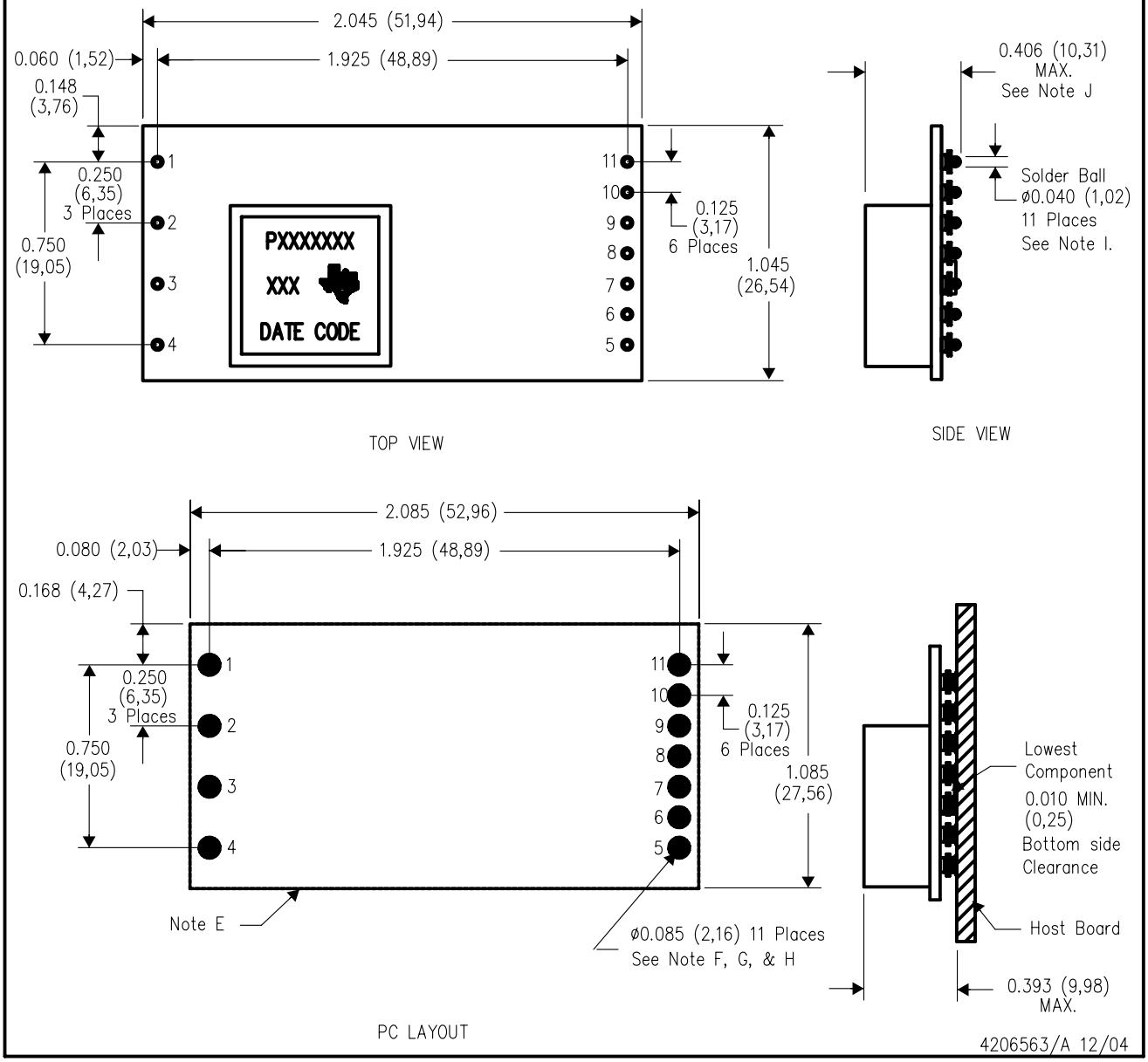
Figure 23. Stand-Alone Configuration

ERW (R–PDSS–T11) DOUBLE SIDED MODULE



NOTES:
A. All linear dimensions are in inches (mm).
B. This drawing is subject to change without notice.
C. 2 place decimals are ±0.030 (±0,76mm).
D. 3 place decimals are ±0.010 (±0,25mm).
E. Recommended keep out area for user components.
E. Pins are 0.040" (1,02) diameter with 0.070" (1,78) diameter standoff shoulder.
F. All pins: Material – Copper Alloy
Finish – Tin (100%) over Nickel plate

ERY (R–PDSS–B11) DOUBLE SIDED MODULE



NOTES:
A. All linear dimensions are in inches (mm).
B. This drawing is subject to change without notice.
C. 2 place decimals are ±0.030 (±0,76mm).
D. 3 place decimals are ±0.010 (±0,25mm).
E. Recommended keep out area for user components.
F. Power pin connection should utilize four or more vias to the interior power plane of 0.025 (0,63) I.D. per input, ground and output pin (or the electrical equivalent).
G. Paste screen opening: 0.080 (2,03) to 0.085 (2,16). Paste screen thickness: 0.006 (0,15).
H. Pad type: Solder mask defined.
I. All pins: Material – Copper Alloy
Finish – Tin (100%) over Nickel plate
Solder Ball – See product data sheet.
J. Dimension prior to reflow solder.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PTB48560AAH	NRND	Through-Hole Module	ERW	11	12	RoHS (In Work) & non-Green	SN	N / A for Pkg Type	-40 to 85		
PTB48560AAS	NRND	Surface Mount Module	ERY	11	12	Non-RoHS & non-Green	SNPB	Level-1-235C-UNLIM/ Level-3-260C-168HRS	-40 to 85		
PTB48560AAZ	NRND	Surface Mount Module	ERY	11	12	RoHS (In Work) & non-Green	SNAGCU	Level-3-260C-168 HR	-40 to 85		
PTB48560BAH	NRND	Through-Hole Module	ERW	11	12	RoHS (In Work) & non-Green	SN	N / A for Pkg Type	-40 to 85		
PTB48560BAS	NRND	Surface Mount Module	ERY	11	12	Non-RoHS & non-Green	SNPB	Level-1-235C-UNLIM/ Level-3-260C-168HRS	-40 to 85		
PTB48560BAZ	NRND	Surface Mount Module	ERY	11	12	RoHS (In Work) & non-Green	SNAGCU	Level-3-260C-168 HR	-40 to 85		
PTB48560CAH	NRND	Through-Hole Module	ERW	11	12	RoHS (In Work) & non-Green	SN	N / A for Pkg Type	-40 to 85		
PTB48560CAS	NRND	Surface Mount Module	ERY	11	12	Non-RoHS & non-Green	SNPB	Level-1-235C-UNLIM/ Level-3-260C-168HRS	-40 to 85		
PTB48560CAZ	NRND	Surface Mount Module	ERY	11	12	RoHS (In Work) & non-Green	SNAGCU	Level-3-260C-168 HR	-40 to 85		

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) RoHS: TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

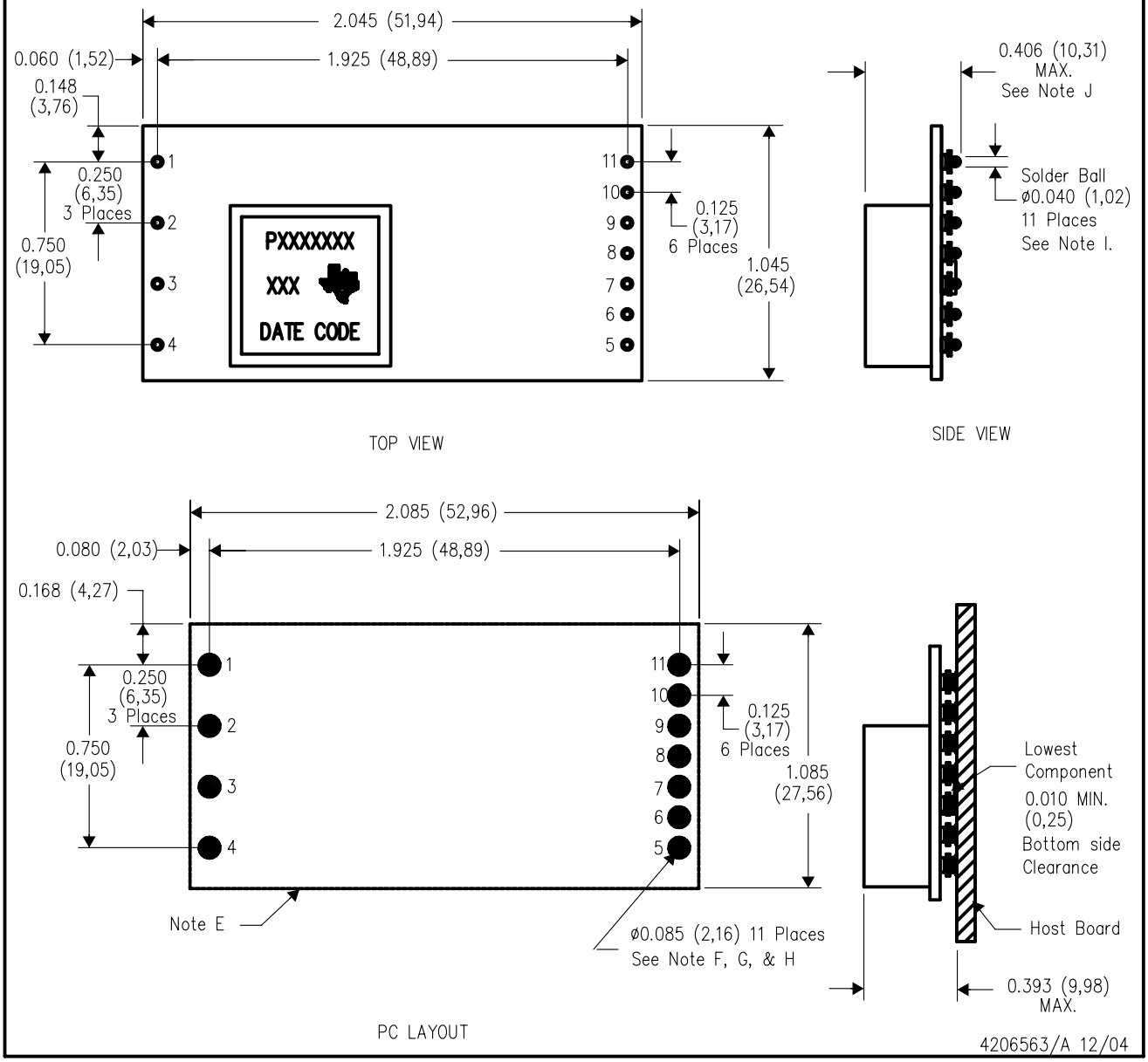
(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

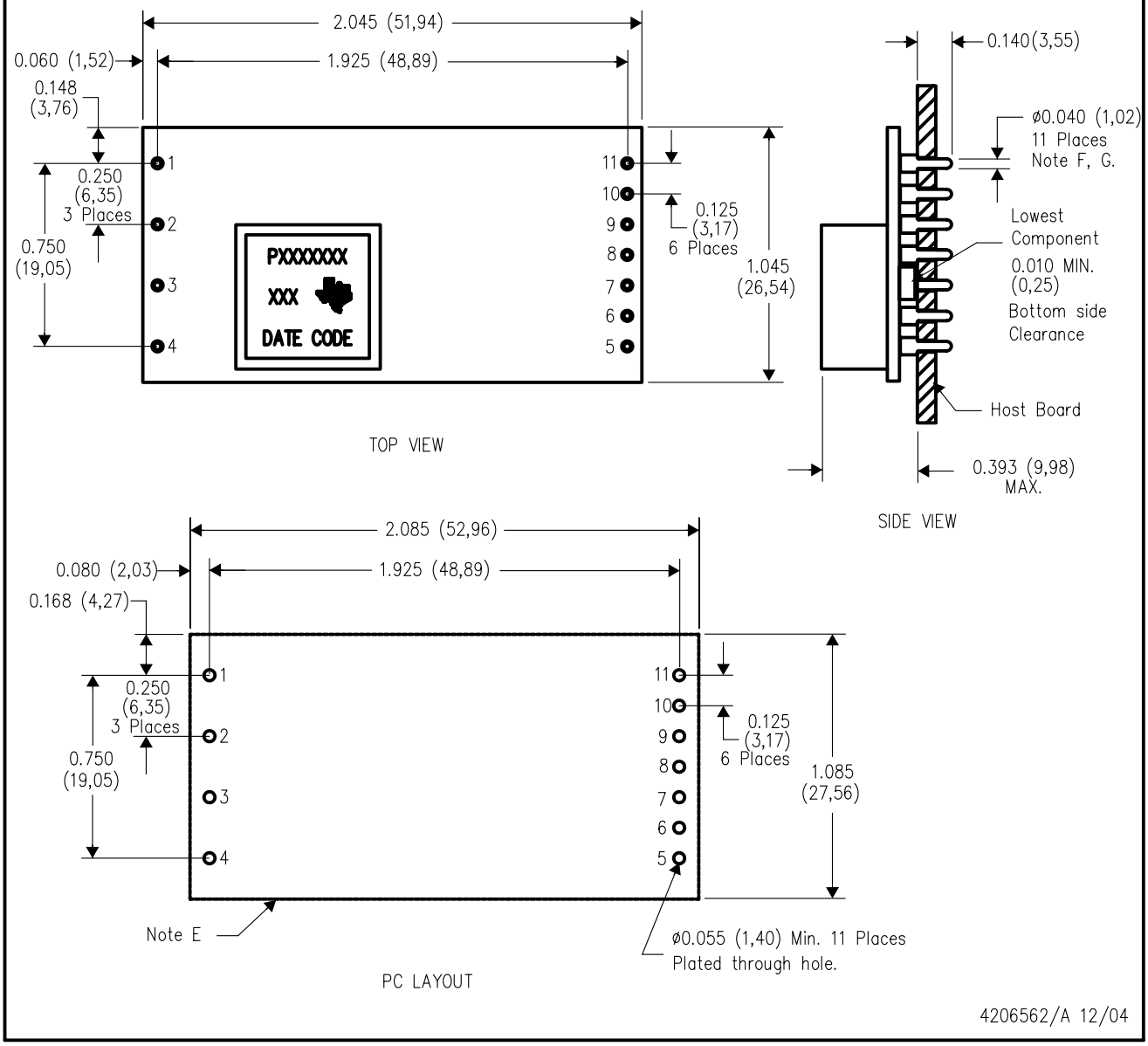
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

ERY (R–PDSS–B11) DOUBLE SIDED MODULE



NOTES:
A. All linear dimensions are in inches (mm).
B. This drawing is subject to change without notice.
C. 2 place decimals are ±0.030 (±0,76mm).
D. 3 place decimals are ±0.010 (±0,25mm).
E. Recommended keep out area for user components.
F. Power pin connection should utilize four or more vias to the interior power plane of 0.025 (0,63) I.D. per input, ground and output pin (or the electrical equivalent).
G. Paste screen opening: 0.080 (2,03) to 0.085 (2,16). Paste screen thickness: 0.006 (0,15).
H. Pad type: Solder mask defined.
I. All pins: Material – Copper Alloy
Finish – Tin (100%) over Nickel plate
Solder Ball – See product data sheet.
J. Dimension prior to reflow solder.

ERW (R–PDSS–T11) DOUBLE SIDED MODULE



NOTES:
A. All linear dimensions are in inches (mm).
B. This drawing is subject to change without notice.
C. 2 place decimals are ±0.030 (±0,76mm).
D. 3 place decimals are ±0.010 (±0,25mm).
E. Recommended keep out area for user components.
E. Pins are 0.040" (1,02) diameter with 0.070" (1,78) diameter standoff shoulder.
F. All pins: Material – Copper Alloy
Finish – Tin (100%) over Nickel plate

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265