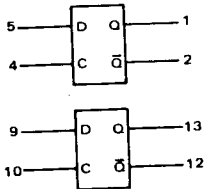


DUAL R-S FLIP-FLOPS  
WITH SINGLE RAIL INPUT  
AND POSITIVE CLOCK

**MC1033**  
**MC1233**

Two dc storage flip-flops with a negative clock input provided for each flip-flop. This device is useful as a dual storage element requiring only a single rail input, as a memory data register, a sample and hold register, or as a clocked R-S flip-flop with no undefined logic state. It may be teamed with the MC1016/MC1216 for shift register functions with a minimum number of packages.

**POSITIVE LOGIC**

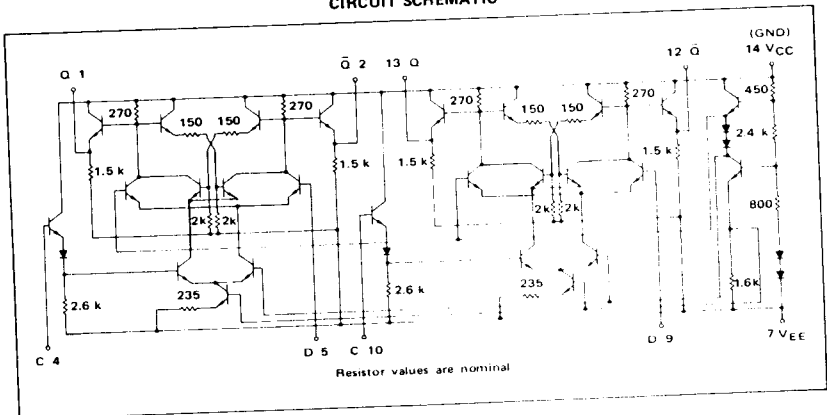


**TRUTH TABLE**

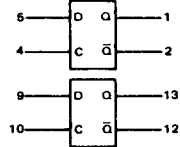
D	C	Q <sup>n+1</sup>
0	1	Q <sup>n</sup>
1	1	Q <sup>n</sup>
0	0	0
1	0	1

DC Input Loading Factor: C = 1; D = 1.5  
DC Output Loading Factor = 25  
Power Dissipation = 140 mW typ

**CIRCUIT SCHEMATIC**



MC1033, MC1233 (continued)



ELECTRICAL CHARACTERISTICS

Test procedures are shown for only one flip-flop. The other flip-flop is tested in the same manner.

Characteristic	Symbol	Pin Under Test	MC1233 Test Limits						Unit	MC1033 Test Limits						Unit
			-55°C		+25°C		+125°C			0°C		+25°C		+75°C		
			Min	Max	Min	Max	Min	Max		Min	Max	Min	Max	Min	Max	
Power Supply Drain Current	$I_E$	7	-	-	-	36	-	-	mAdc	-	-	-	36	-	-	mAdc
Input Current	$I_{in}$	4	-	-	-	100	-	-	$\mu$ Adc	-	-	-	100	-	-	$\mu$ Adc
		5	-	-	-	150	-	-	$\mu$ Adc	-	-	-	150	-	-	$\mu$ Adc
Input Leakage Current	$I_R$	4	-	-	-	0.2	-	1.0	$\mu$ Adc	-	-	-	0.2	-	1.0	$\mu$ Adc
		5	-	-	-	0.2	-	1.0	$\mu$ Adc	-	-	-	0.2	-	1.0	$\mu$ Adc
"Q" Logical "1" Output Voltage	$V_{OH}^1$	1	-0.990	-0.825	-0.850	-0.700	-0.700	-0.530	Vdc	-0.895	-0.740	-0.850	-0.700	-0.775	-0.615	Vdc
"Q" Logical "0" Output Voltage	$V_{OL}$	1	-1.890	-1.580	-1.800	-1.500	-1.720	-1.380	Vdc	-1.830	-1.525	-1.800	-1.500	-1.760	-1.435	Vdc
"Q-bar" Logical "1" Output Voltage	$V_{OH}^{\bar{1}}$	2	-0.990	-0.825	-0.850	-0.700	-0.700	-0.530	Vdc	-0.895	-0.740	-0.850	-0.700	-0.775	-0.615	Vdc
"Q-bar" Logical "0" Output Voltage	$V_{OL}$	2	-1.890	-1.580	-1.800	-1.500	-1.720	-1.380	Vdc	-1.830	-1.525	-1.800	-1.500	-1.760	-1.435	Vdc
Switching Times (Fan-Out = 3)			Typ	Max	Typ	Max	Typ	Max		Typ	Max	Typ	Max	Typ	Max	
Clock Inputs Propagation Delay	$t_{4-1}$	1	6.0	8.5	6.0	8.5	8.0	10.5	ns	6.0	8.5	6.0	8.5	7.0	9.5	ns
		1	5.0	10	5.0	10	7.0	12		5.0	10	5.0	10	6.0	11	
		2	5.0	8.5	5.0	8.5	7.0	10.5		5.0	8.5	5.0	8.5	6.0	9.5	
		2	6.0	10	6.0	10	8.0	12		6.0	10	6.0	10	7.0	11	
Rise Time	$t_{1+}$	1	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
		2	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
Fall Time	$t_{1-}$	1	5.0	8.5	5.0	8.5	7.0	11		5.0	8.5	5.0	8.5	6.0	9.5	
		2	5.0	8.5	5.0	8.5	7.0	11		5.0	8.5	5.0	8.5	6.0	9.5	
Set Inputs Propagation Delay	$t_{5+1}$	1	5.0	8.0	5.0	8.0	6.0	9.5	ns	5.0	8.0	5.0	8.0	5.0	8.5	ns
		1	↓	↓	↓	↓	7.0	10.5		↓	↓	↓	↓	↓	↓	
		2	↓	↓	↓	↓	7.0	10.5		↓	↓	↓	↓	↓	↓	
		2	↓	↓	↓	↓	6.0	9.5		↓	↓	↓	↓	↓	↓	
Rise Time	$t_{1+}$	1	↓	7.5	↓	7.5	9.0		↓	7.5	↓	7.5	8.0			
		2	↓	7.5	↓	7.5	9.0		↓	7.5	↓	7.5	8.0			
Fall Time	$t_{1-}$	1	↓	8.5	6.0	9.0	8.0	11		6.0	9.0	6.0	9.0	7.0	10	
		2	↓	8.5	6.0	9.0	8.0	11		6.0	9.0	6.0	9.0	7.0	10	

<sup>1</sup> $V_{OH}$  limits apply from no load (0 mA) to full load (-2.5 mA).

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		TEST VOLTAGE/CURRENT VALUES					
@Test Temperature		Vdc ± 1.0%					mAdc
		V <sub>IL min</sub> to V <sub>IL max</sub>	V <sub>IH min</sub> to V <sub>IH max</sub>	V <sub>IH max</sub>	V <sub>EE</sub>	I <sub>L</sub>	
MC1233	-55°C	-5.2 to -1.405	-1.165 to -0.825	-	-5.2	-2.5	
	+25°C	-5.2 to -1.325	-1.025 to -0.700	-0.700	-5.2	-2.5	
	+125°C	-5.2 to -1.205	-0.875 to -0.530	-	-5.2	-2.5	
MC1033	0°C	-5.2 to -1.350	-1.070 to -0.740	-	-5.2	-2.5	
	+25°C	-5.2 to -1.325	-1.025 to -0.700	-0.700	-5.2	-2.5	
	+75°C	-5.2 to -1.260	-0.950 to -0.615	-	-5.2	-2.5	

			TEST VOLTAGE/CURRENT APPLIED TO PINS LISTED BELOW:					
Characteristic	Symbol	Pin Under Test	V <sub>IL min</sub> to V <sub>IL max</sub>	V <sub>IH min</sub> to V <sub>IH max</sub>	V <sub>IH max</sub>	V <sub>EE</sub>	I <sub>L</sub>	V <sub>CC (Gnd)</sub>
Power Supply Drain Current	I <sub>E</sub>	7	-	4, 10	-	5, 7, 9	-	14
Input Current	I <sub>in</sub>	4, 5	-	-	4, 5	5, 7, 9, 10, 4, 7, 9, 10	-	14, 14
Input Leakage Current	I <sub>R</sub>	4, 5	-	-	-	4, 5, 7, 9, 10, 4, 5, 7, 9, 10	-	14, 14
Q <sup>1</sup> Logical "1" Output Voltage	V <sub>OH<sup>1</sup></sub>	1	4	5	-	7, 9, 10	1	14
Q <sup>1</sup> Logical "0" Output Voltage	V <sub>OL</sub>	1	4, 5	-	-	7, 9, 10	-	14
Q <sup>2</sup> Logical "1" Output Voltage	V <sub>OH<sup>2</sup></sub>	2	4, 5	-	-	7, 9, 10	2	14
Q <sup>2</sup> Logical "0" Output Voltage	V <sub>OL</sub>	2	4	5	-	7, 9, 10	-	14
Switching Times (Fan-Out = 3)			V <sub>IL max</sub> +1.2 Vdc	Pulse In	Pulse Out	V <sub>EE</sub> = -4.0 Vdc		(+1.2V)
Clock Inputs	Propagation Delay	t <sub>4-1</sub>	4	-	1	7, 9, 10	-	14
		t <sub>4-1</sub>		-	1		-	
Rise Time		t <sub>4-2+</sub>	2	-	2	7, 9, 10	-	14
		t <sub>4-2-</sub>		-	2		-	
Fall Time		t <sub>1+</sub>	2	-	1	7, 9, 10	-	14
		t <sub>2+</sub>		-	2		-	
Set Inputs	Propagation Delay	t <sub>1-</sub>	2	-	1	7, 9, 10	-	14
		t <sub>2-</sub>		-	2		-	
Rise Time		t <sub>5+1</sub>	5	4	1	7, 9, 10	-	14
		t <sub>5-1</sub>		-	1		-	
Fall Time		t <sub>5+2</sub>	2	-	2	7, 9, 10	-	14
		t <sub>5-2</sub>		-	2		-	
Rise Time		t <sub>1+</sub>	2	-	1	7, 9, 10	-	14
		t <sub>2+</sub>		-	2		-	
Fall Time		t <sub>1-</sub>	2	-	1	7, 9, 10	-	14
		t <sub>2-</sub>		-	2		-	

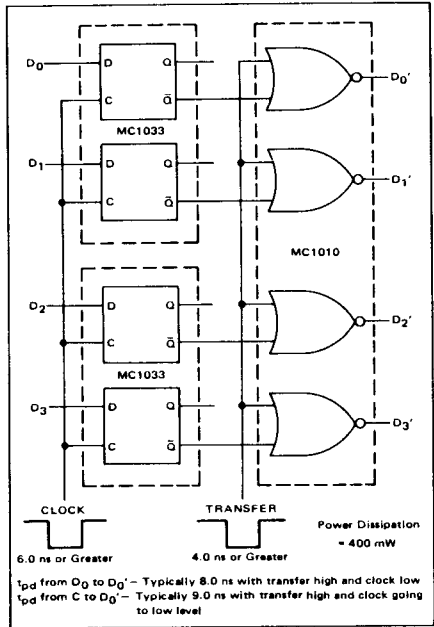
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# MC1033, MC1233 (continued)

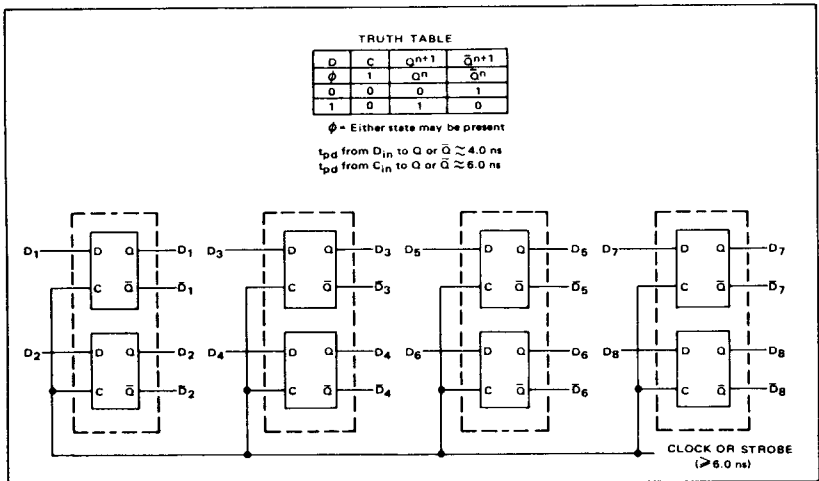
## APPLICATIONS INFORMATION

The MC1033/MC1233 is a single-rail storage element that has no undefined logic state. (Note the change in the truth table over that of the dual-rail type of device, such as MC1014/MC1214 or MC1015/MC1215.) The speed-power product is better than that obtained with any other bipolar technique. An example of a 4-bit storage register with both input and output gating is shown in Figure 1, and an 8-bit buffer register with input gating is shown in Figure 2.

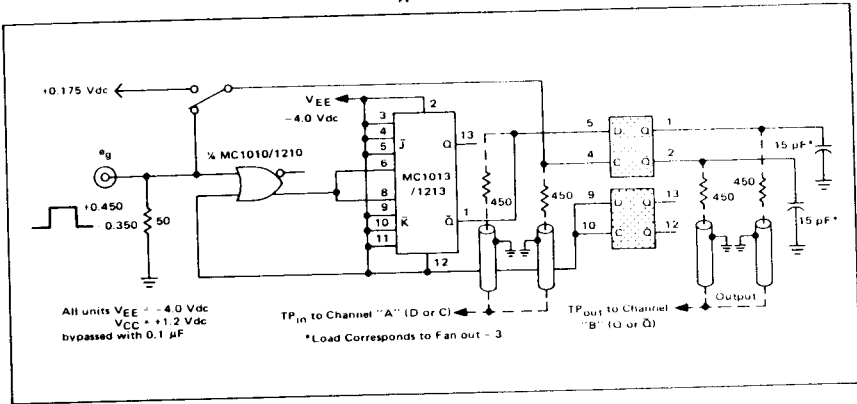
**FIGURE 1 - 4-BIT STORAGE REGISTER WITH GATED INPUTS AND OUTPUTS (THREE DEVICES)**



**FIGURE 2 - 8-BIT BUFFER REGISTER WITH INPUT GATING (FOUR DEVICES)**



SWITCHING TIME TEST CIRCUIT  
 $T_A = 25^\circ\text{C}$



SWITCHING TIME DEFINITIONS AND TIMING DIAGRAM

