

MC14070B, MC14077B

CMOS SSI

Quad Exclusive “OR” and “NOR” Gates

The MC14070B quad exclusive OR gate and the MC14077B quad exclusive NOR gate are constructed with MOS P-channel and N-channel enhancement mode devices in a single monolithic structure. These complementary MOS logic gates find primary use where low power dissipation and/or high noise immunity is desired.

Features

- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- All Outputs Buffered
- Capable of Driving Two Low-Power TTL Loads or One Low-Power Schottky TTL Load Over the Rated Temperature Range
- Double Diode Protection on All Inputs
- MC14070B – Replacement for CD4030B and CD4070B Types
- MC14077B – Replacement for CD4077B Type
- Pb-Free Packages are Available

MAXIMUM RATINGS (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V _{DD}	DC Supply Voltage Range	-0.5 to +18.0	V
V _{in} , V _{out}	Input or Output Voltage Range (DC or Transient)	-0.5 to V _{DD} + 0.5	V
I _{in} , I _{out}	Input or Output Current (DC or Transient) per Pin	± 10	mA
P _D	Power Dissipation, per Package (Note 1)	500	mW
T _A	Ambient Temperature Range	-55 to +125	°C
T _{stg}	Storage Temperature Range	-65 to +150	°C
T _L	Lead Temperature (8-Second Soldering)	260	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Temperature Derating:

Plastic “P and D/DW” Packages: - 7.0 mW/°C From 65°C To 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range V_{SS} ≤ (V_{in} or V_{out}) ≤ V_{DD}.

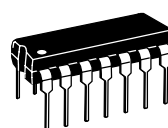
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.



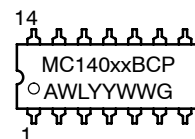
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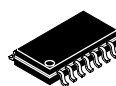
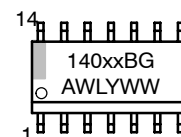
MARKING DIAGRAMS



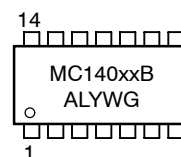
PDIP-14
P SUFFIX
CASE 646



SOIC-14
D SUFFIX
CASE 751A



SOEIAJ-14
F SUFFIX
CASE 965



xx = Specific Device Code
A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week
G = Pb-Free Package

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 3 of this data sheet.

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PIN ASSIGNMENT

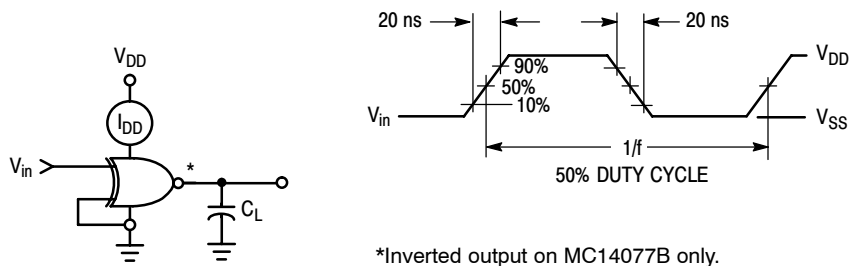
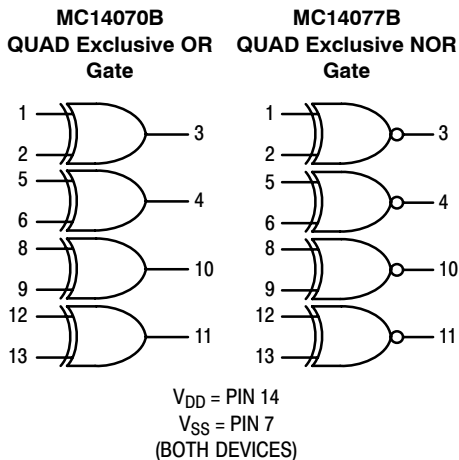
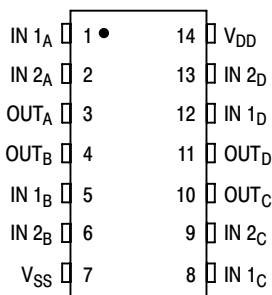


Figure 1. Power Dissipation Test Circuit and Waveform

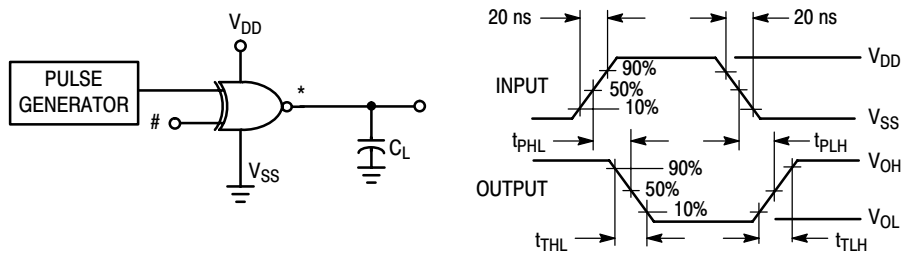


Figure 2. Switching Time Test Circuit and Waveforms

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ORDERING INFORMATION

Device	Package	Shipping†
MC14070BCP	PDIP-14	25 Units / Rail
MC14070BCPG	PDIP-14 (Pb-Free)	
MC14070BD	SOIC-14	55 Units / Rail
MC14070BDG	SOIC-14 (Pb-Free)	
MC14070BDR2	SOIC-14	2500 / Tape & Reel
MC14070BDR2G	SOIC-14 (Pb-Free)	
MC14070BFEL	SOEIAJ-14	2000 / Tape & Reel
MC14070BFELG	SOEIAJ-14 (Pb-Free)	
MC14077BCP	PDIP-14	25 Units / Rail
MC14077BCPG	PDIP-14 (Pb-Free)	
MC14077BD	SOIC-14	55 Units / Rail
MC14077BDG	SOIC-14 (Pb-Free)	
MC14077BDR2	SOIC-14	2500 / Tape & Reel
MC14077BDR2G	SOIC-14 (Pb-Free)	
MC14077BFEL	SOEIAJ-14	2000 / Tape & Reel
MC14077BFELG	SOEIAJ-14 (Pb-Free)	

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

Characteristic	Symbol	V _{DD} Vdc	- 55°C		25°C			125°C		Unit	
			Min	Max	Min	Typ (Note 2)	Max	Min	Max		
Output Voltage V _{in} = V _{DD} or 0 V _{in} = 0 or V _{DD}	"0" Level	V _{OL}	5.0	-	0.05	-	0	0.05	-	0.05	Vdc
			10	-	0.05	-	0	0.05	-	0.05	
			15	-	0.05	-	0	0.05	-	0.05	
	"1" Level	V _{OH}	5.0	4.95	-	4.95	5.0	-	4.95	-	Vdc
			10	9.95	-	9.95	10	-	9.95	-	
			15	14.95	-	14.95	15	-	14.95	-	
Input Voltage (V _O = 4.5 or 0.5 Vdc) (V _O = 9.0 or 1.0 Vdc) (V _O = 13.5 or 1.5 Vdc) (V _O = 0.5 or 4.5 Vdc) (V _O = 1.0 or 9.0 Vdc) (V _O = 1.5 or 13.5 Vdc)	"0" Level	V _{IL}	5.0	-	1.5	-	2.25	1.5	-	1.5	Vdc
			10	-	3.0	-	4.50	3.0	-	3.0	
			15	-	4.0	-	6.75	4.0	-	4.0	
	"1" Level	V _{IH}	5.0	3.5	-	3.5	2.75	-	3.5	-	Vdc
			10	7.0	-	7.0	5.50	-	7.0	-	
			15	11	-	11	8.25	-	11	-	
Output Drive Current (V _{OH} = 2.5 Vdc) (V _{OH} = 4.6 Vdc) (V _{OH} = 9.5 Vdc) (V _{OH} = 13.5 Vdc) (V _{OL} = 0.4 Vdc) (V _{OL} = 0.5 Vdc) (V _{OL} = 1.5 Vdc)	Source	I _{OH}	5.0	-3.0	-	-2.4	-4.2	-	-1.7	-	mAdc
			5.0	-0.64	-	-0.51	-0.88	-	-0.36	-	
			10	-1.6	-	-1.3	-2.25	-	-0.9	-	
			15	-4.2	-	-3.4	-8.8	-	-2.4	-	
	Sink	I _{OL}	5.0	0.64	-	0.51	0.88	-	0.36	-	mAdc
			10	1.6	-	1.3	2.25	-	0.9	-	
15			4.2	-	3.4	8.8	-	2.4	-		
Input Current	I _{in}	15	-	± 0.1	-	± 0.00001	± 0.1	-	± 1.0	µAdc	
Input Capacitance (V _{in} = 0)	C _{in}	-	-	-	-	5.0	7.5	-	-	pF	
Quiescent Current (Per Package)	I _{DD}	5.0	-	0.25	-	0.0005	0.25	-	7.5	µAdc	
		10	-	0.5	-	0.0010	0.5	-	15		
		15	-	1.0	-	0.0015	1.0	-	30		
Total Supply Current (Notes 3 & 4) (Dynamic plus Quiescent, Per Package) (C _L = 50 pF on all outputs, all buffers switching)	I _T	5.0 10 15	I _T = (0.3 µA/kHz) f + I _{DD} I _T = (0.6 µA/kHz) f + I _{DD} I _T = (0.9 µA/kHz) f + I _{DD}							µAdc	
Output Rise and Fall Times (Note 3) (C _L = 50 pF) t _{TLH} , t _{THL} = (1.35 ns/pF) C _L + 33 ns t _{TLH} , t _{THL} = (0.60 ns/pF) C _L + 20 ns t _{TLH} , t _{THL} = (0.40 ns/pF) C _L + 20 ns	t _{TLH} , t _{THL}	5.0	-	-	-	100	200	-	-	ns	
		10	-	-	-	50	100	-	-		
		15	-	-	-	40	80	-	-		
Propagation Delay Times (Note 3) (C _L = 50 pF) t _{PLH} , t _{PHL} = (0.90 ns/pF) C _L + 130 ns t _{PLH} , t _{PHL} = (0.36 ns/pF) C _L + 57 ns t _{PLH} , t _{PHL} = (0.26 ns/pF) C _L + 37 ns	t _{PLH} , t _{PHL}	5.0	-	-	-	175	350	-	-	ns	
		10	-	-	-	75	150	-	-		
		15	-	-	-	55	110	-	-		

2. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

3. The formulas given are for the typical characteristics only at 25°C.

4. To calculate total supply current at loads other than 50 pF:

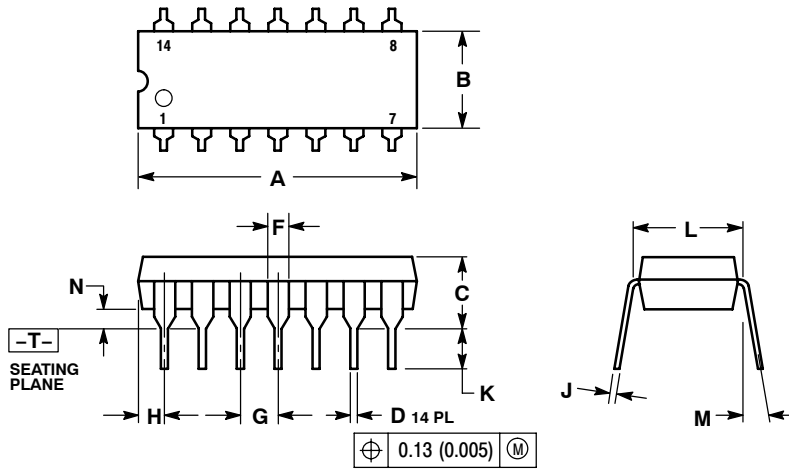
$$I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) V f k$$

where: I_T is in µH (per package), C_L in pF, V = (V_{DD} - V_{SS}) in volts, f in kHz is input frequency, and k = 0.002.

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PACKAGE DIMENSIONS

PDIP-14
CASE 646-06
ISSUE P



NOTES:

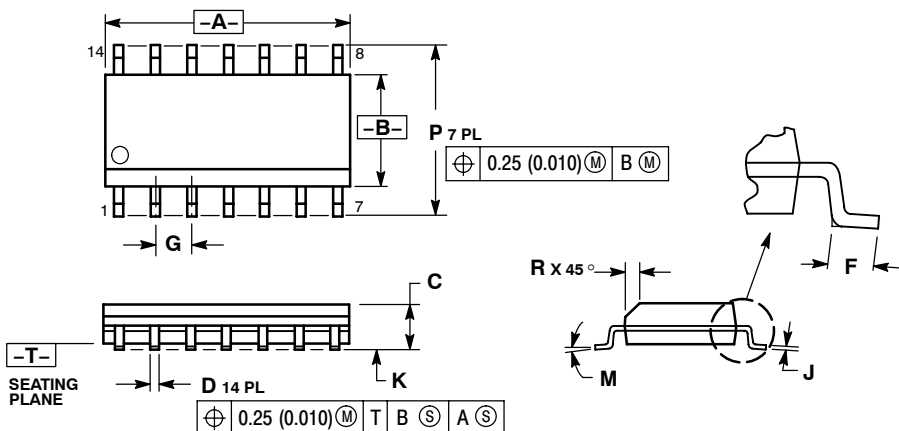
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.715	0.770	18.16	19.56
B	0.240	0.260	6.10	6.60
C	0.145	0.185	3.69	4.69
D	0.015	0.021	0.38	0.53
F	0.040	0.070	1.02	1.78
G	0.100 BSC		2.54 BSC	
H	0.052	0.095	1.32	2.41
J	0.008	0.015	0.20	0.38
K	0.115	0.135	2.92	3.43
L	0.290	0.310	7.37	7.87
M	---		10°	
N	0.015	0.039	0.38	1.01

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PACKAGE DIMENSIONS

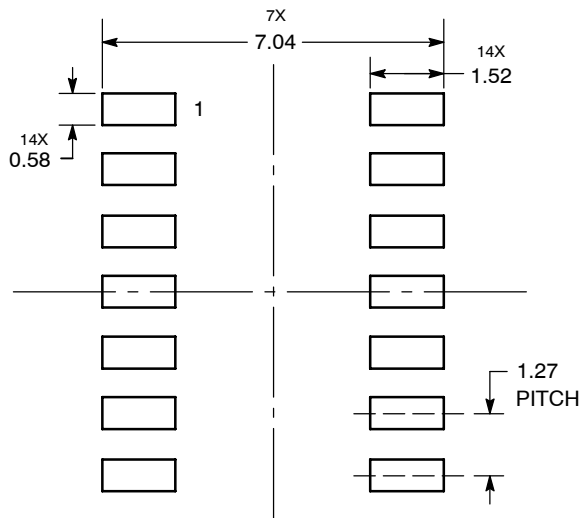
SOIC-14
CASE 751A-03
ISSUE H



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
 2. CONTROLLING DIMENSION: MILLIMETER.
 3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
 4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
 5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	8.55	8.75	0.337	0.344
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0°	7°	0°	7°
P	5.80	6.20	0.228	0.244
R	0.25	0.50	0.010	0.019

SOLDERING FOOTPRINT*



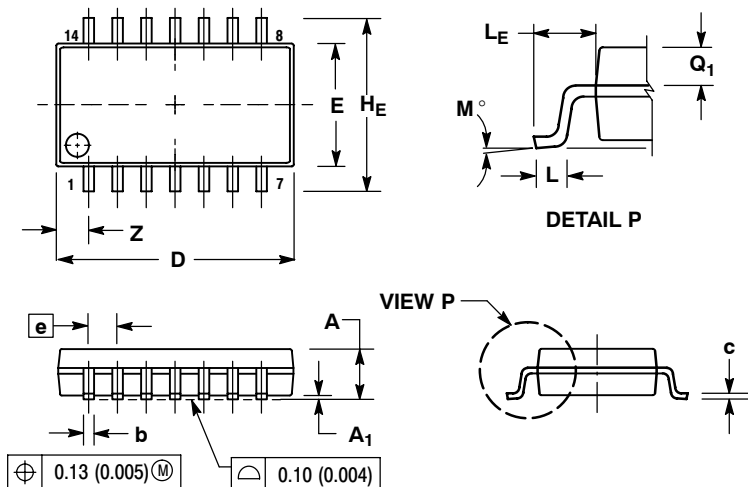
DIMENSIONS: MILLIMETERS

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

MC14070B, MC14077B

PACKAGE DIMENSIONS

SOEIAJ-14
CASE 965-01
ISSUE A



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
5. THE LEAD WIDTH DIMENSION (b) DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.46 (0.018).

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	---	2.05	---	0.081
A ₁	0.05	0.20	0.002	0.008
b	0.35	0.50	0.014	0.020
c	0.10	0.20	0.004	0.008
D	9.90	10.50	0.390	0.413
E	5.10	5.45	0.201	0.215
e	1.27 BSC		0.050 BSC	
H _E	7.40	8.20	0.291	0.323
0.50	0.50	0.85	0.020	0.033
L _E	1.10	1.50	0.043	0.059
M	0°	10°	0°	10°
Q ₁	0.70	0.90	0.028	0.035
Z	---	1.42	---	0.056

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