



ABSTRACT

This user's guide describes the characteristics, operation, and use of the TMUX7208EVM evaluation module (EVM). A complete schematic diagram, printed-circuit board layouts, and bill of materials are included in this document.

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1 Introduction

The TMUX7208EVM supports evaluation of the TMUX7208 device in the 16-pin TSSOP (PW) package. TMUX7208 is a complementary metal-oxide semiconductor (CMOS) switch with latch-up immunity in a 8:1 single channel configuration. The device supports dual supplies (± 4.5 V to ± 22 V), a single supply (4.5 V to 44 V), or asymmetric supplies (such as $V_{DD} = 12$ V, $V_{SS} = -5$ V). The TMUX7208 supports bidirectional analog and digital signals on the source (Sx) and drain (D) pins ranging from VSS to VDD. All logic control inputs support logic levels from 1.8 V to VDD, ensuring both TTL and CMOS logic compatibility when operating in the valid supply voltage range. The Fail-Safe Logic circuitry applies voltages on the control pins before the supply pin, which protects the device from potential damage.

2 Information About Cautions and Warnings



CAUTION

This EVM contains components that can potentially be damaged by electrostatic discharge. Always transport and store the EVM in its supplied ESD bag when not in use. Handle using an antistatic wristband. Operate on an antistatic work surface. For more information on proper handling, see [Electrostatic Discharge \(ESD\) application report](#)

3 Features of this EVM

The EVM has the following features:

- Quick prototyping and testing setup for the 16-pin TMUX7208 device in the TSSOP (PW) package.
- TMUX7208 control logic truth table listed on board.
- No specific TMUX7208 is supplied or soldered to the evaluation module. Allows flexibility to choose the desired IC for evaluation.
- Support for both single supply and dual supply operation.
- Six power supply decoupling capacitors ($2 \times 0.1 \mu\text{F}$, $2 \times 1 \mu\text{F}$, and $2 \times 10 \mu\text{F}$).
- Jumpers to nine signal lanes, VDD and VSS power rails, and control signals.
- Nine pads are available for placement of SMA connectors.
- Pads are available for pull-up or pull-down resistors on control signal pathways.
- Pads are available for surge protection diodes.
- 0805 capacitor pads are available on all signal pathways referenced to ground.

4 EVM Images

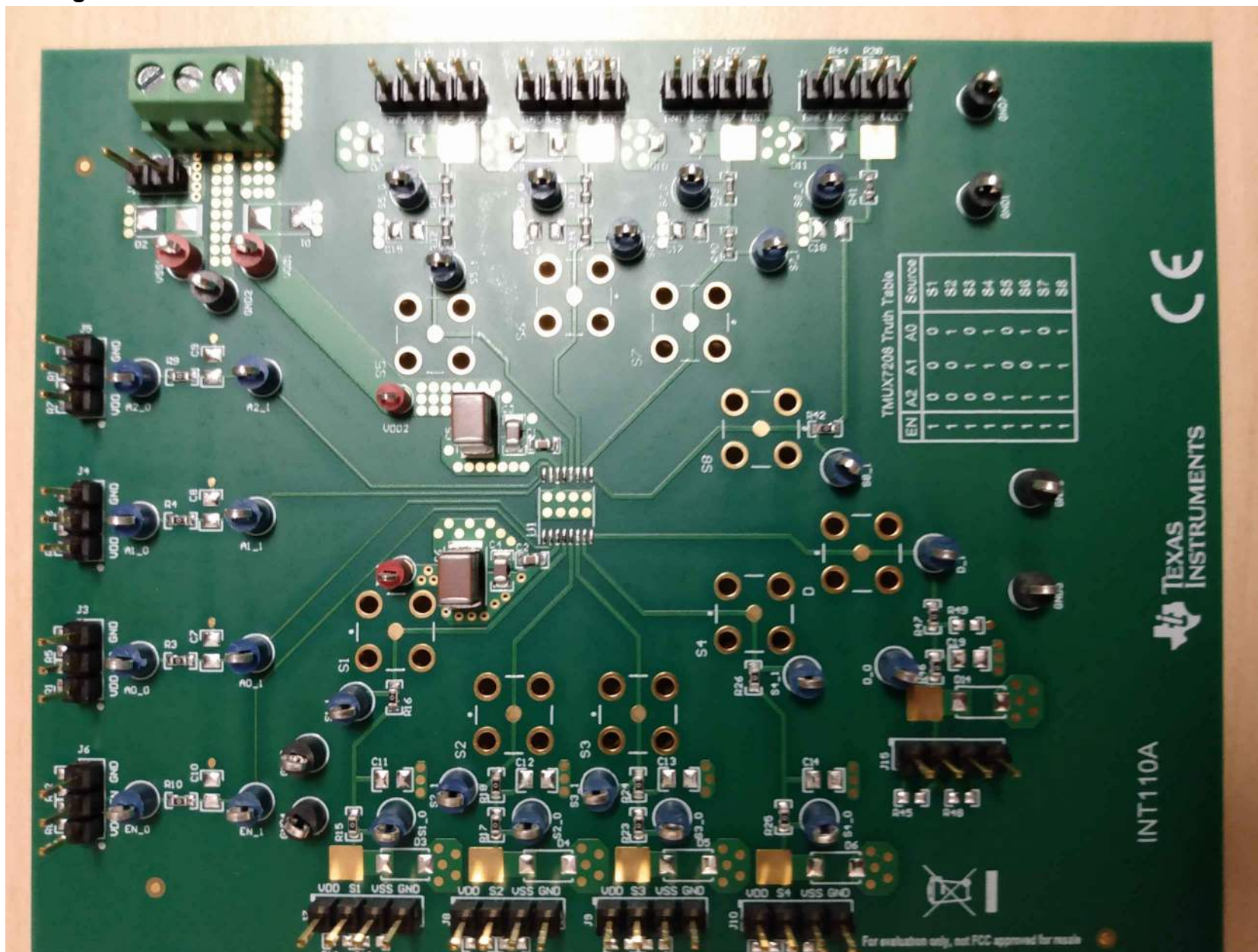


Figure 4-1. TMUX7208EVM Topside View

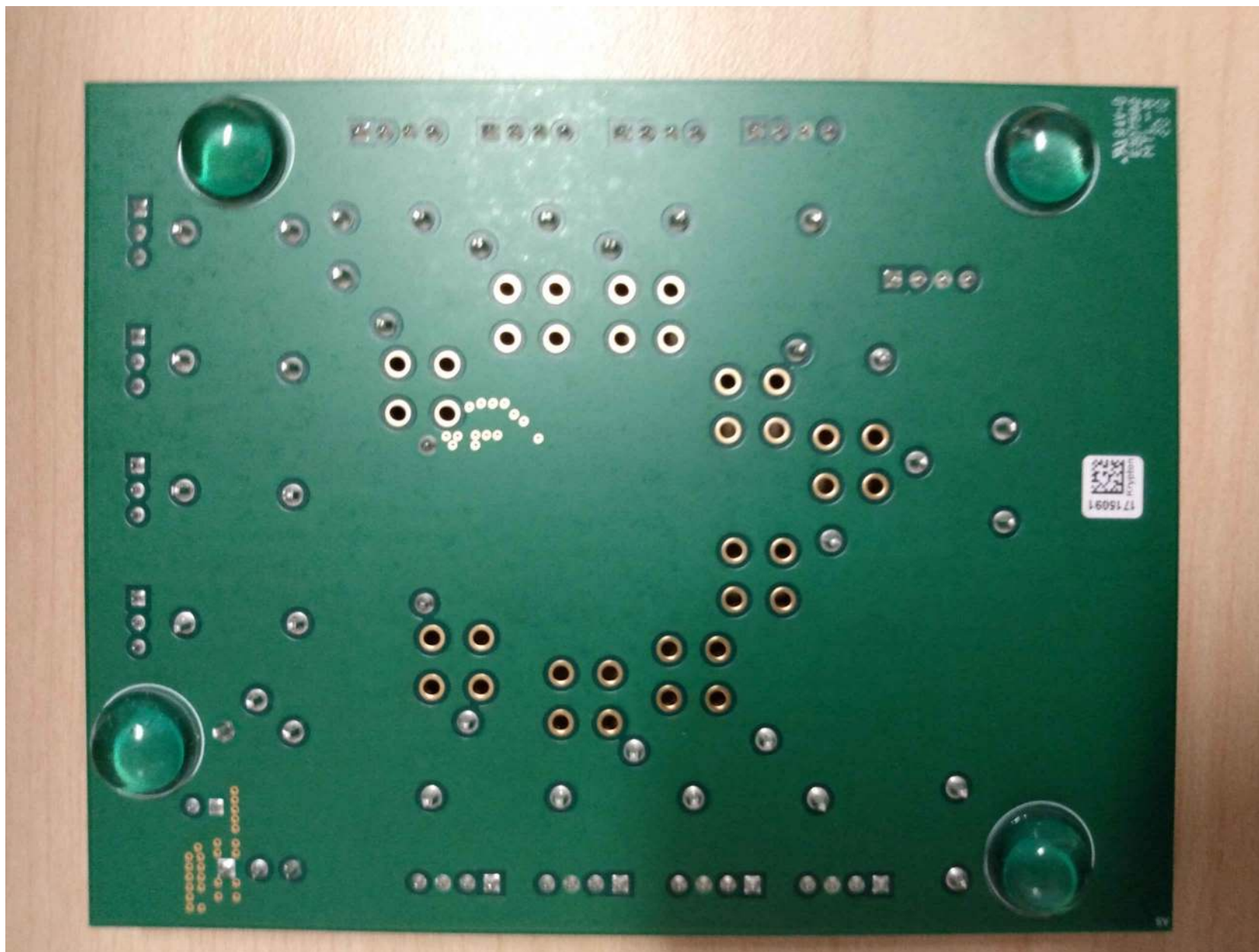


Figure 4-2. TMUX7208EVM Bottom View

5 EVM Setup

The following instructions are for setting up the EVM:

1. The control inputs and signal lines may be loaded by soldering components to signal path pads as needed. describes which load pads correspond to what pin on the DUT. SMA connectors can be soldered to corresponding pads accordingly.

Table 5-1. Component Pad to TMUX7208 Pin Matrix

Pin #	0805 Capacitor Pad ID	Protection Diode Pad	Protection Diode PN#	0603 Pull-up Pad	0603 Pull-Down Pad	Pad Locations
4	C11	D3	SMAJ36CA	R13	R19	Top Layer
5	C12	D4	SMAJ36CA	R14	R20	Top Layer
6	C13	D5	SMAJ36CA	R21	R27	Top Layer
7	C14	D6	SMAJ36CA	R22	R28	Top Layer
8	C19	D14	SMAJ36CA	R45	R48	Top Layer
9	C18	D11	SMAJ36CA	R38	R44	Top Layer
10	C17	D10	SMAJ36CA	R37	R43	Top Layer
11	C16	D8	SMAJ36CA	R30	R36	Top Layer
12	C15	D7	SMAJ36CA	R29	R35	Top Layer

2. The board is powered by attaching ± 5 V to ± 22 V dual power supply or 5 V to 44 V single power supply to the screw terminal J2, with VDD, VSS, and GND oriented as specified in [Table 6-1](#).
3. Jumpers should be placed according to desired functionality. [Figure 5-1](#) displays a generic four-pin jumper, with the indicating white corner to designate position 1.



Figure 5-1. Generic Jumper and Header Position 1 Designator

[Table 5-2](#) is the truth table for the TMUX7208, for reference to configure the corresponding control jumpers. Additional signal path jumpers may be configured as shown in [Table 6-1](#).

Table 5-2. TMUX7208 Truth Table

EN J6	A2 J5	A1 J4	A0 J3	Selected Source Connected to Drain (D) Pin
0	X ⁽¹⁾	X	X	All sources are off (HI-Z)
1	0	0	0	S1
1	0	0	1	S2
1	0	1	0	S3
1	0	1	1	S4
1	1	0	0	S5
1	1	0	1	S6
1	1	1	0	S7
1	1	1	1	S8

(1) X denote do not care.

6 EVM Connectors and Test Points

6.1 Connectors

Table 6-1. Jumper and Header Position Functions

Jumper ID	Header Pos. 1	Header Pos. 2	Header Pos. 3	Header Pos. 4	Header Pos. 5	Board Function	Fitted (Y/N)
J1	GND	VSS	N/A	N/A	N/A	Power	Y
J2	VSS	GND	VDD	N/A	N/A	Power	Y
J3	VDD	A0	GND	N/A	N/A	Control	Y
J4	VDD	A1	GND	N/A	N/A	Control	Y
J5	VDD	A2	GND	N/A	N/A	Control	Y
J6	VDD	EN	GND	N/A	N/A	Control	Y
J7	VDD	S1	VSS	GND	N/A	I/O	Y
J8	VDD	S2	VSS	GND	N/A	I/O	Y
J9	VDD	S3	VSS	GND	N/A	I/O	Y
J10	VDD	S4	VSS	GND	N/A	I/O	Y
J11	VDD	S5	VSS	GND	N/A	I/O	Y
J12	VDD	S6	VSS	GND	N/A	I/O	Y
J13	VDD	S7	VSS	GND	N/A	I/O	Y
J14	VDD	S8	VSS	GND	N/A	I/O	Y
J15	VDD	D	VSS	GND	N/A	I/O	Y
S1	I/O	GND	GND	GND	GND	I/O SMA	N
S2	I/O	GND	GND	GND	GND	I/O SMA	N
S3	I/O	GND	GND	GND	GND	I/O SMA	N
S4	I/O	GND	GND	GND	GND	I/O SMA	N
S5	I/O	GND	GND	GND	GND	I/O SMA	N
S6	I/O	GND	GND	GND	GND	I/O SMA	N
S7	I/O	GND	GND	GND	GND	I/O SMA	N
S8	I/O	GND	GND	GND	GND	I/O SMA	N
D	I/O	GND	GND	GND	GND	I/O SMA	N

6.2 Test Points

Table 6-2. Test Point Signal Connections

Signal	Test Point ID
VDD	TP1 and TP10
GND	TP3, TP4, TP5, TP6, TP7, TP8, and TP9
VSS	TP2 and TP11
D	TP20 and TP21
S1	TP22 and TP23
S2	TP24 and TP25
S3	TP26 and TP27
S4	TP28 and TP29
S5	TP30 and TP31
S6	TP32 and TP33
S7	TP34 and TP35
S8	TP36 and TP37
A0	TP12 and TP13
A1	TP14 and TP15
A2	TP16 and TP17

Table 6-2. Test Point Signal Connections (continued)

Signal	Test Point ID
EN	TP18 and TP19

7 PCB Layouts

Figure 7-1 and Figure 7-2 show the EVM PCB layout images.



Figure 7-1. Top View Illustration of the TMUX7208EVM Layout

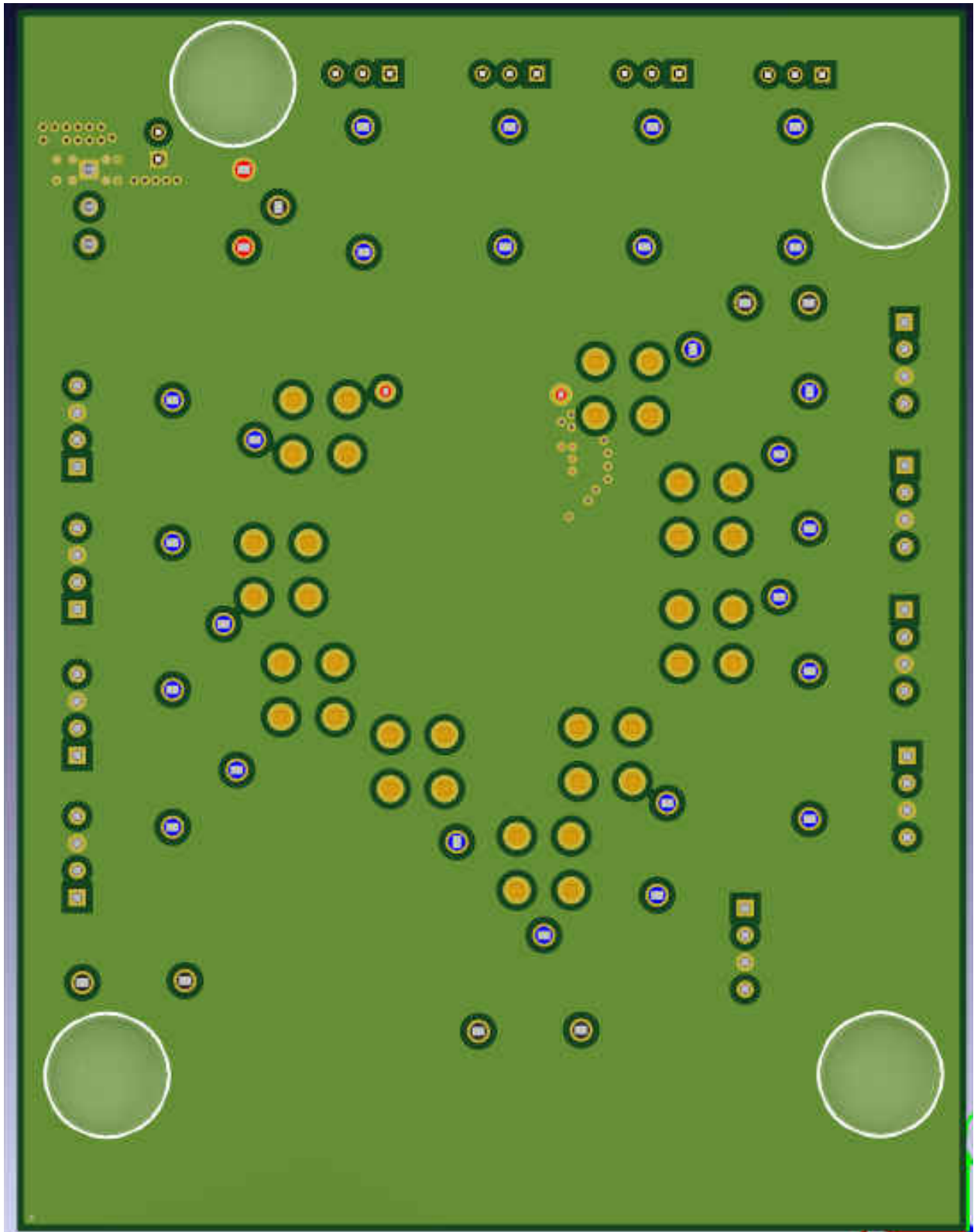


Figure 7-2. Bottom View Illustration of the TMUX7208EVM Layout

8 Schematics

Schematic views for the TMUX7208EVM. [Figure 8-1](#) shows the editor view, which includes all connections and parts that are DNI. [Figure 8-2](#) shows DNI view, removing DNI parts which are not included on the evaluation model out-of-the-box.

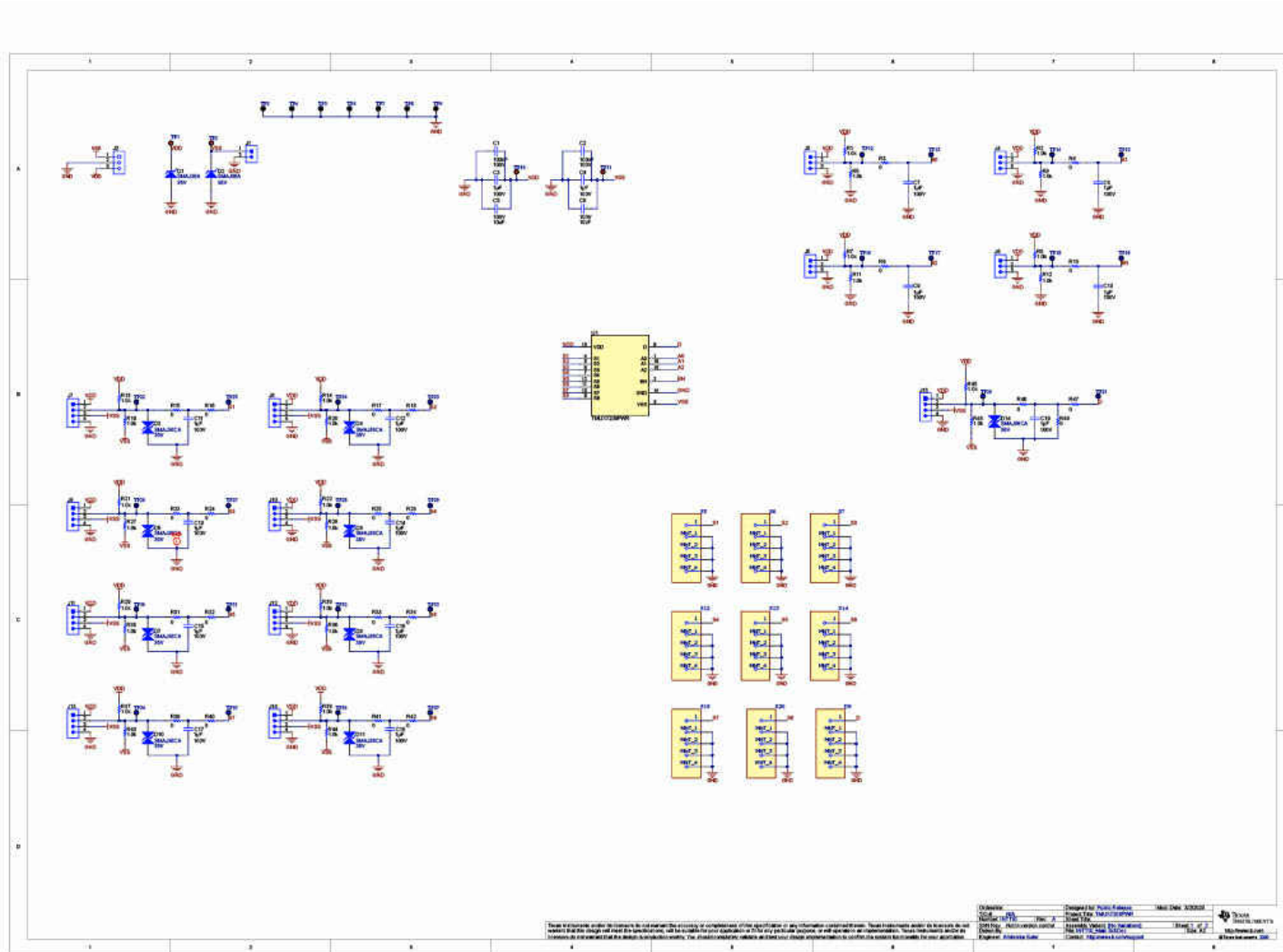


Figure 8-1. Schematic of the TMUX7208EVM (Editor View)

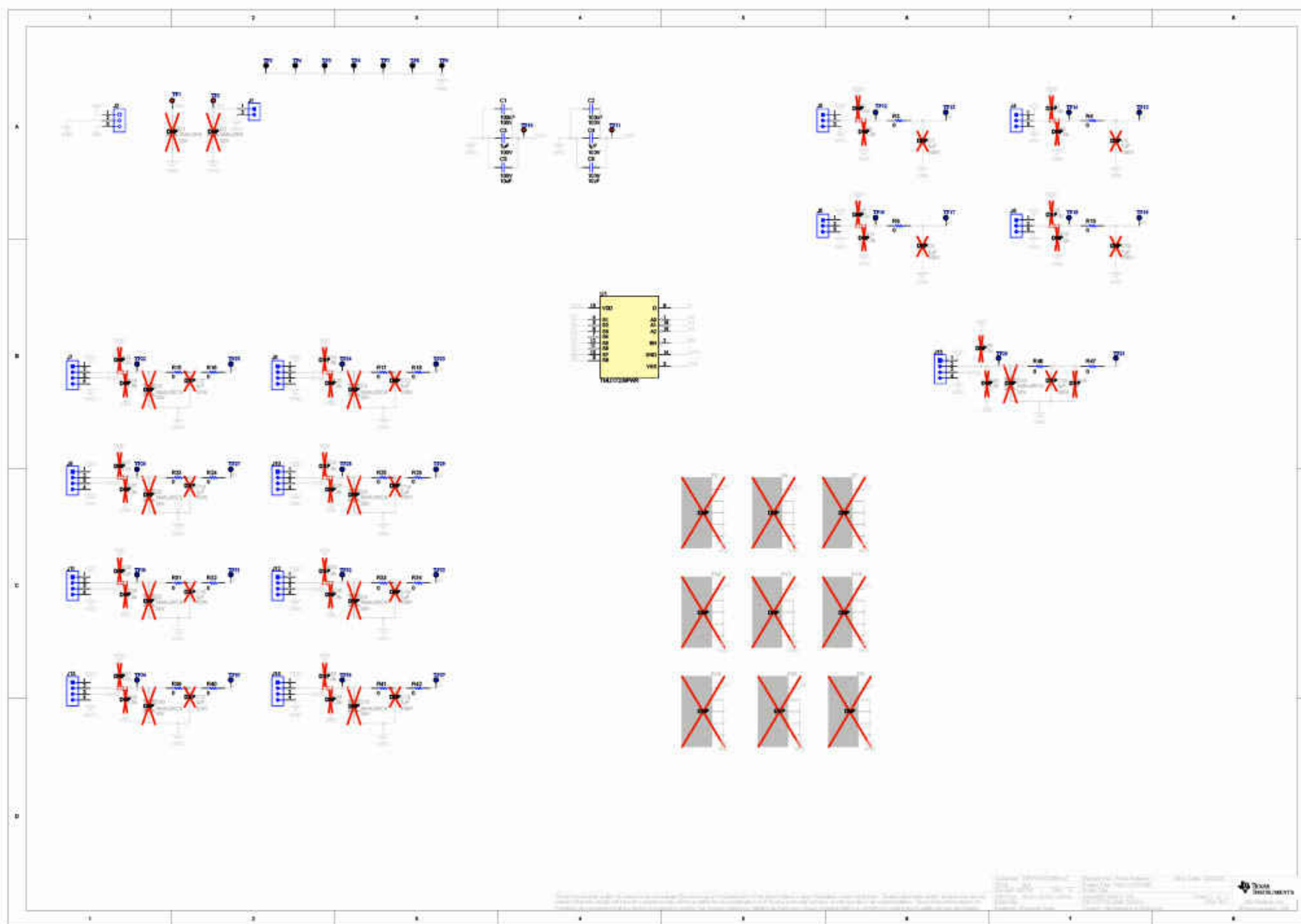


Figure 8-2. Schematic of the TMUX7208EVM (DNI View)

9 Bill of Materials

Table 9-1 details the EVM bill of materials.

Table 9-1. TMUX7208EVM Bill of Materials

Designator	Component	Manufacturer	Description	Quantity
C1, C2	CKG45NX7S2A106M500JJ	TDK	CAP, CERM, 10 μ F, 100 V, \pm 20%, X7S, AEC-Q200 Grade 1, 1812	2
C4, C5	C1608X7S2A104K080AB	TDK	CAP, CERM, 0.1 μ F, 100 V, \pm 10%, X7S, 0603	2
C6, C7	C2012X7S2A105K125AB	TDK	CAP, CERM, 1 μ F, 100 V, \pm 10%, X7S, 0805	2
H1, H2, H3, H4	SJ-5303 (CLEAR)	Bumper Specialties, Inc.	Bumpon, Hemisphere, 0.44 X 0.20, Clear	4
J1	691214110003	Würth Electronics	Terminal Block, 3.5 mm, 3 \times 1, Tin, TH	1
J2	PEC02SAAN	Sullins Connector Solutions	Header, 100 mil, 2 \times 1, Tin, TH	1
J3, J8, J5, J9, J10	PEC03SAAN	Sullins Connector Solutions	Header, 100 mil, 3 \times 1, Tin, TH	5
R3, R4, R5, R6, R9, R10, R13, R14	RMCF0603ZT0R00	Stackpole Electronics Inc	RES, 0, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	8
SH-J?	SPC02SYAN	Sullins Connector Solutions	Shunt, 100 mil, Flash Gold, Black	7
TP1, TP3, TP4, TP6, TP8, TP9, TP10, TP11, TP14, TP15, TP17, TP18	5000	Keystone	Test Point, Miniature, Red, TH	12
J2	691214110003	Würth Elektronik	Terminal Block, 3.5 mm, 3 \times 1, Tin, TH	1
J7, J8, J9, J10, J11, J12, J13, J14, J15	PEC04SAAN	Sullins Connector Solutions	Header, 100 mil, 4 \times 1, Tin, TH	9
A0.0, A0.1, A1.0, A1.1, A2.0, A2.1, D0, D1, EN0, EN1, S1.0, S1.1, S2.0, S2.1, S3.0, S3.1, S4.0, S4.1, S5.0, S5.1, S6.0, S6.1, S7.0, S7.1, S8.0, S8.1	5122	Keystone Electronics	Test Point, Compact, Blue, TH	26
GND1, GND2, GND3, GND4, GND5, GND6, GND7	5006	Keystone Electronics	Test Point, Compact, Black, TH	7
VDD1, VSS1	5005	Keystone Electronics	Test Point, Compact, Red, TH	2
VDD2	5000	Keystone Electronics	Test Point, Miniature, Red, TH	1
VSS2	5000	Keystone Electronics	Test Point, Miniature, Red, TH	1
J3, J4, J5, J6	PEC03SAAN	Sullins Connector Solutions	Header, 100 mil, 3 \times 1, Tin, TH	4
J1	PEC02SAAN	Sullins Connector Solutions	Header, 100 mil, 2 \times 1, Tin, TH	1
C5, C6	CKG45NX7S2A106M500JJ	TDK Corporation	CAP, CERM, 10 μ F, 100 V, \pm 20%, X7S, AEC-Q200 Grade 1, 1812	2
H9, H10, H11, H12	SJ-5303 (CLEAR)	3M	Bumpon, Hemisphere, 0.44 X 0.20, Clear	4
C3, C4	C2012X7S2A105K125AB	TDK Corporation	CAP, CERM, 1 μ F, 100 V, \pm 10%, X7S, 0805	2
C1, C2	C1608X7S2A104K080AB	TDK Corporation	CAP, CERM, 0.1 μ F, 100 V, \pm 10%, X7S, 0603	2
R3, R4, R9, R10, R15, R16, R17, R18, R23, R24, R25, R26, R31, R32, R33, R34, R39, R40, R41, R42, R46, R47, R49	RMCF0603ZT0R00	Stackpole Electronics Inc.	RES, 0, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	23

10 Related Documentation

- Texas Instruments, [Electrostatic Discharge \(ESD\) application report](#)

11 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision * (December 2020) to Revision A (December 2020)	Page
• Added link to Electrostatic Discharge (ESD) application report in the <i>Information About Cautions and Warnings</i> section.....	2

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