Military Grade SmartFusion Customizable System-on-Chip (cSoC)

Product Benefits

- 100% Military Temperature Tested and Qualified from –55°C to 125°C
- Not Susceptible to Neutron-Induced Configuration Loss

Microcontroller Subsystem (MSS)

- Hard 50 MHz 32-Bit ARM® Cortex®-M3
  - Fully Tested Across Military Temperature Range (–55°C to 125°C)
  - 1.25 DMIPS/MHz Throughput from Zero Wait State Memory
  - Memory Protection Unit (MPU)
  - Single Cycle Multiplication, Hardware Divide
  - JTAG Debug (4 wires), Serial Wire Debug (SWD, 2 wires), and Single Wire Viewer (SWV) Interfaces
- Internal Memory
  - Embedded Nonvolatile Flash Memory (eNVM), 128 Kbytes to 512 Kbytes
  - Embedded High-Speed SRAM (eSRAM), 16 Kbytes to 64 Kbytes, Implemented in 2 Physical Blocks to Enable Simultaneous Access from 2 Different Masters
- Multi-Layer AHB Communications Matrix
  - Provides up to 16 Gbps of On-Chip Memory Bandwidth,[1] Allowing Multi-Master Schemes
- 10/100 Ethernet MAC with RMII Interface[2]
- Programmable External Memory Controller, Which Supports:
  - Asynchronous Memories
  - NOR Flash, SRAM, PSRAM
  - Synchronous SRAMs
- Two I^2C Peripherals
- Two 16550 Compatible UARTs
- Two SPI Peripherals
- Two 32-Bit Timers
- 32-Bit Watchdog Timer
- 8-Channel DMA Controller to Offload the Cortex-M3 processor from Data Transactions
- Clock Sources
  - 32 kHz to 20 MHz Main Oscillator
  - Battery-Backed 32 KHz Low Power Oscillator with Real-Time Counter (RTC)
  - 100 MHz Embedded RC Oscillator; Up to 3% Accurate at Military Temperature
  - Embedded Analog PLL with 4 Output Phases (0, 90, 180, 270)

High-Performance FPGA

- Based on proven ProASIC®3 FPGA Fabric
- Low Power, Firm-Error Immune 130-nm, 7-Layer Metal, Flash-Based CMOS Process
- Nonvolatile, Live at Power-Up, Retains Program When Powered Off
- 350 MHz System Performance
- Embedded SRAMs and FIFOs
  - Variable Aspect Ratio 4,608-Bit SRAM Blocks
  - x1, x2, x4, x9, and x18 Organizations
  - True Dual-Port SRAM (excluding x18)
  - Programmable Embedded FIFO Control Logic
- Secure ISP with 128-Bit AES via JTAG
- FlashLock® to Secure FPGA Contents
- Five Clock Conditioning Circuits (CCCs) with up to 2 Integrated Analog PLLs
  - Phase Shift, Multiply/Divide, and Delay Capabilities
  - Frequency: Input 1.5–350 MHz, Output 0.75 to 350 MHz

Programmable Analog

Analog Front-End (AFE)

- Up to Three 12-Bit SAR ADCs
  - 500 Ksps in 12-Bit Mode
  - 550 Ksps in 10-Bit Mode
  - 600 Ksps in 8-Bit Mode
- Internal 2.56 V Reference or Optional External Reference
- One First-Order ΣΔ DAC (sigma-delta) per ADC
  - 12-Bit 500 Ksps Update Rate
- Up to 5 High-Performance Analog Signal Conditioning Blocks (SCB) per Device, Each Including:
  - Two High-Voltage Bipolar Voltage Monitors (with 4 input ranges from ±2.5 V to –11.5/12 V) with 4% Accuracy
  - High Gain Current Monitor, Differential Gain = 50, up to 12 V Common Mode
  - Temperature Monitor (Resolution = ¼°C in 12-Bit Mode; Accurate from –55°C to 150°C)
- Up to Ten High-Speed Voltage Comparators (t_{pd} = 15 ns)

Analog Compute Engine (ACE)

- Offloads Cortex-M3–Based MSS from Analog Initialization and Processing of ADC, DAC, and SCBs
- Sample Sequence Engine for ADC and DAC Parameter Set-Up
- Post-Processing Engine for Functions such as Low-Pass Filtering and Linear Transformation
- Easily Configured via GUI in Libero® System-on-Chip (SoC) Software

I/Os and Operating Voltage

- FPGA I/Os
  - LVDS, PCI, PCI-X, up to 24 mA IOH/IOL
  - Up to 350 MHz
- MSS I/Os
  - Schmitt Trigger, up to 6 mA IOH, 8 mA IOL
  - Up to 180 MHz
- Single 3.3 V Power Supply with On-Chip 1.5 V Regulator
- External 1.5 V Is Allowed by Bypassing Regulator (digital VCC = 1.5 V for FPGA and MSS, analog VCC = 3.3 V and 1.5 V)

1 Theoretical maximum
2 A2F500 devices

SmartFusion cSoC Family Product Table

SmartFusion® cSoC		A2F060	A2F500
FPGA Fabric	System Gates	60,000	500,000
	Tiles (D-flip-flops)	1,536	11,520
	RAM Blocks (4,608 bits)	8	24
Microcontroller Subsystem (MSS)	Flash (Kbytes)	128	512
	SRAM (Kbytes)	16	64
	Cortex-M3 with memory protection unit (MPU)	Yes	
	10/100 Ethernet MAC	No	Yes
	External Memory Controller (EMC)	24-bit address,16-bit data	
	DMA	8 Ch	
	I^2C	2	
	SPI	2	
	16550 UART	2	
	32-Bit Timer	2	
	PLL	1	2[1]
	32 KHz Low Power Oscillator	1	
	100 MHz On-Chip RC Oscillator	1	
	Main Oscillator (32 KHz to 20 MHz)	1	
Programmable Analog	ADCs (8-/10-/12-bit SAR)	1	3[3]
	DACs (12-bit sigma-delta)	1	3[3]
	Signal Conditioning Blocks (SCBs)	1	5[3]
	Comparator[2]	2	10[3]
	Current Monitors[2]	1	5[3]
	Temperature Monitors[2]	1	5[3]
	Bipolar High Voltage Monitors[2]	2	10[3]

Notes:

1. *Two PLLs are available in FG484 (one PLL in FG256).*
2. *These functions share I/O pins and may not all be available at the same time. See the "Analog Front-End Overview" section in the SmartFusion Programmable Analog User's Guide for details.*
3. *Available on FG484 only.*

Package I/Os: MSS + FPGA I/Os

Device	A2F060	A2F500	
Package	**FG256**	**FG256**	**FG484**
Direct Analog Inputs	11	8	12
Shared Analog Inputs[1]	4	16	20
Total Analog Inputs	15	24	32
Total Analog Outputs	1	2	3
MSS I/Os[2,3]	26[4]	25	41
FPGA I/Os	66	66	128
Total I/Os	108	117	204

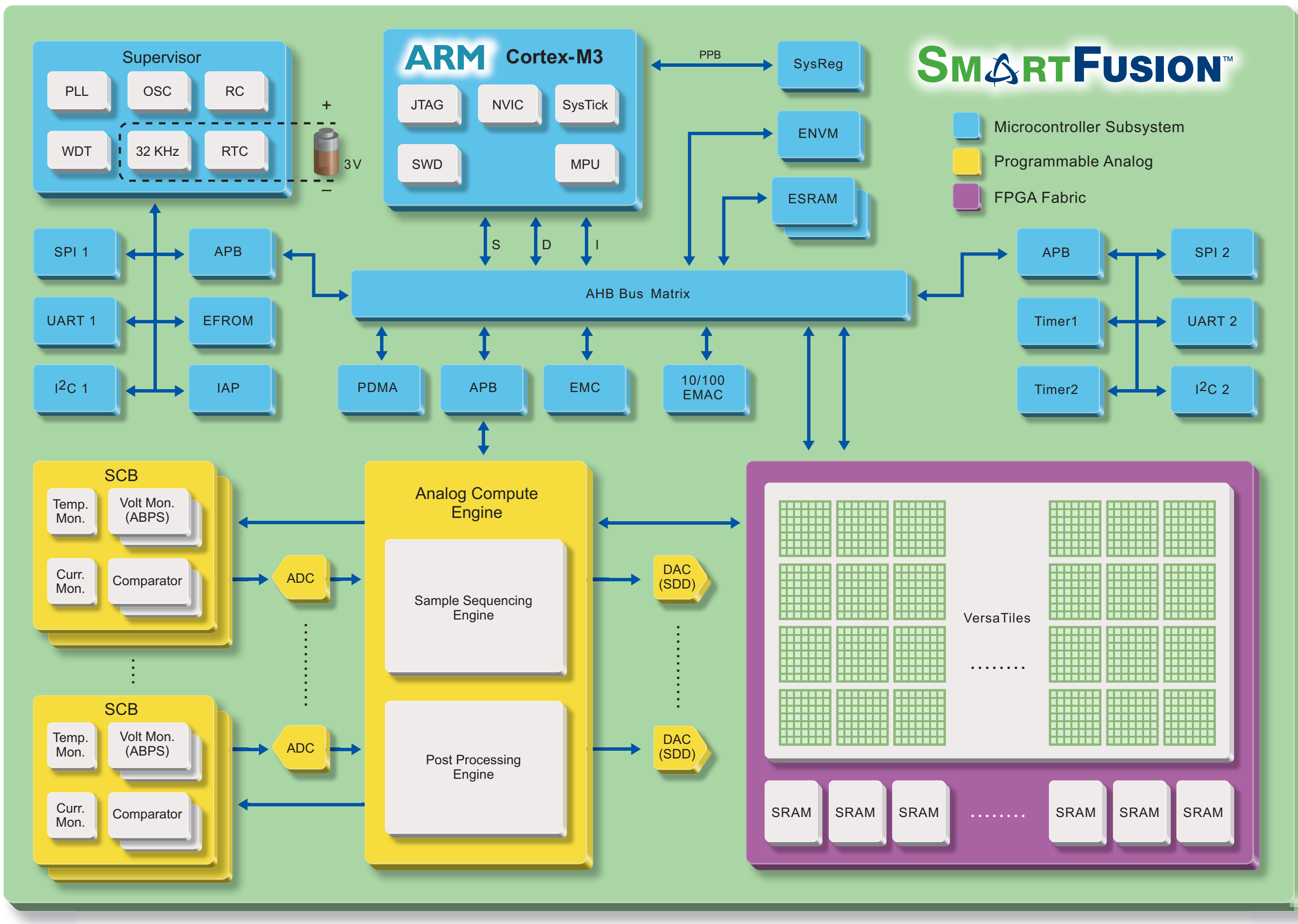
Notes:

1. *These pins are shared between direct analog inputs to the ADCs and voltage/current/temperature monitors.*
2. *16 MSS I/Os are multiplexed and can be used as FPGA I/Os, if not needed for MSS. These I/Os support Schmitt triggers and support only LVTTL and LVCMOS (1.5 / 1.8 / 2.5, 3.3 V) standards.*
3. *9 MSS I/Os are primarily for 10/100 Ethernet MAC and are also multiplexed and can be used as FPGA I/Os if Ethernet MAC is not used in a design. These I/Os support Schmitt triggers and support only LVTTL and LVCMOS (1.5 / 1.8 / 2.5, 3.3 V standards.*
4. *10/100 Ethernet MAC is not available on A2F060.*

SmartFusion cSoC Device Status

Device	Status
A2F060	Production
A2F500	Production

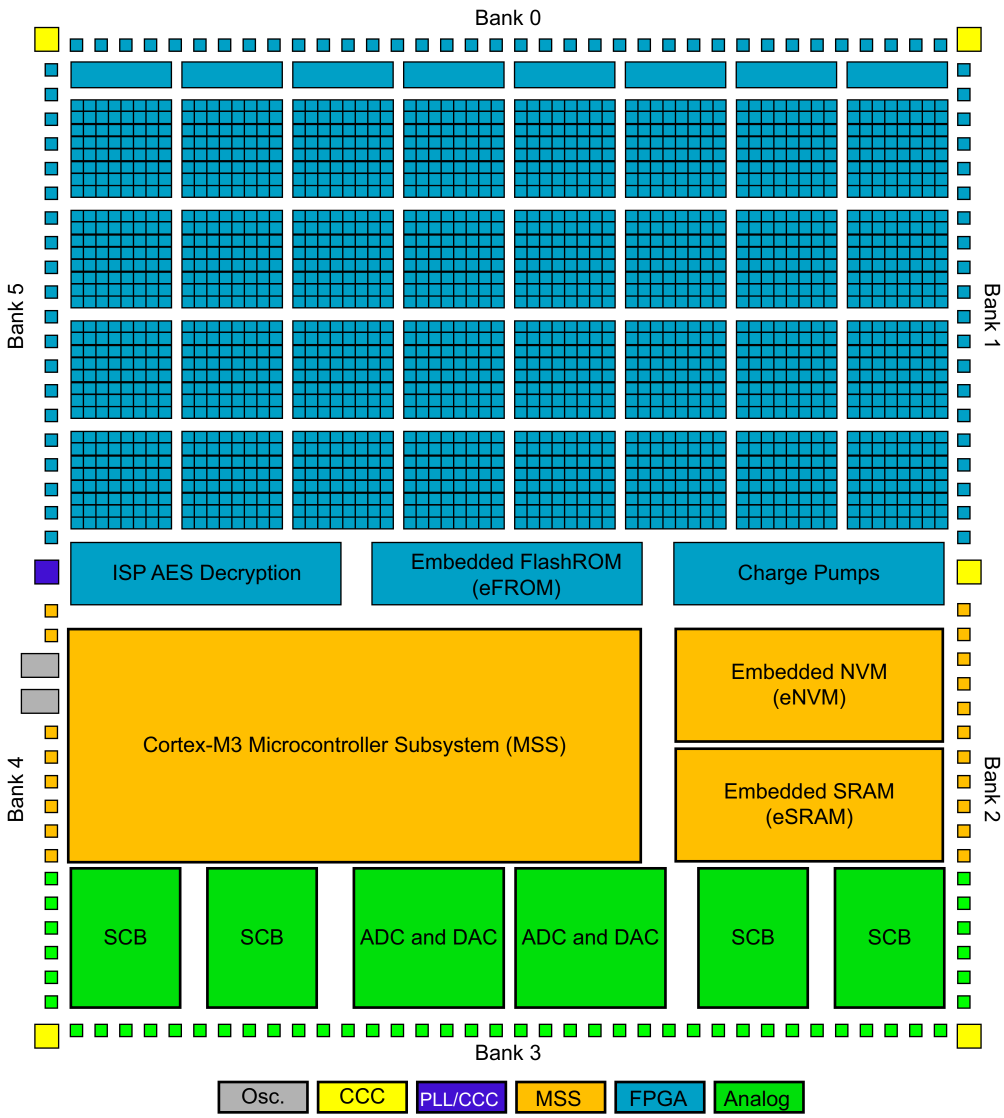
SmartFusion cSoC Block Diagram



Legend:

SDD – Sigma-delta DAC
SCB – Signal conditioning block
PDMA – Peripheral DMA
IAP – In-application programming
ABPS – Active bipolar prescaler
WDT – Watchdog Timer
SWD – Serial Wire Debug

SmartFusion cSoC System Architecture



Note: *Generic Architecture for the SmartFusion Family*

Product Ordering Codes

A2F500 M3 F – 1 FG G 484 Y M

- **M** — Application (junction temperature range)
  - Blank = Commercial (0 to +85°C)
  - I = Industrial (–40 to +100°C)
  - M = Military (–55 to 125°C)
- **Y** — Security Feature*
  - Y = Device Includes License to Implement IP Based on the Cryptography Research, Inc. (CRI) Patent Portfolio
- **484** — Package Lead Count
  - 256
  - 484
- **G** — Lead-Free Packaging Options
  - Blank = Standard Packaging
  - G = RoHS-Compliant (green) Packaging
- **FG** — Package Type
  - FG = Fine Pitch Ball Grid Array (1.0 mm pitch)
- **1** — Speed Grade
  - Blank = 40 MHz MSS Speed; FPGA Fabric at Standard Speed
  - –1 = 50 MHz MSS Speed; FPGA Fabric 15% Faster than Standard
- **F** — eNVM Size
  - A = 8 Kbytes
  - B = 16 Kbytes
  - C = 32 Kbytes
  - D = 64 Kbytes
  - E = 128 Kbytes
  - F = 256 Kbytes
  - G = 512 Kbytes
- **M3** — CPU Type
  - M3 = Cortex-M3
- **A2F500** — Part Number
  - **SmartFusion Devices**
  - A2F060 = 60,000 System Gates
  - A2F500 = 500,000 System Gates

*Note: *Most devices in the SmartFusion cSoC family can be ordered with the Y suffix. Devices with a package size greater or equal to 5x5 mm are supported. Contact your local Microsemi SoC Products Group sales representative for more information.*

Temperature Grade Offerings

SmartFusion cSoC	A2F060	A2F500
FG256	C, I, M	C, I, M
FG484	–	C, I, M

Notes:
1. *C = Commercial Temperature Range: 0°C to 85°C Junction*
2. *I = Industrial Temperature Range: –40°C to 100°C Junction*
3. *M = Military Temperature Range: –55°C to 125°C Junction*

Table of Contents

Datasheet Information

1 – SmartFusion Family Overview

Introduction

The SmartFusion® family of cSoCs builds on the technology first introduced with the Fusion mixed signal FPGAs. SmartFusion cSoCs are made possible by integrating FPGA technology with programmable high-performance analog and hardened ARM Cortex-M3 microcontroller blocks on a flash semiconductor process. The SmartFusion cSoC takes its name from the fact that these three discrete technologies are integrated on a single chip, enabling the lowest cost of ownership and smallest footprint solution to you.

General Description

Microcontroller Subsystem (MSS)

The MSS is composed of a 100 MHz Cortex-M3 processor and integrated peripherals, which are interconnected via a multi-layer AHB bus matrix (ABM). This matrix allows the Cortex-M3 processor, FPGA fabric master, Ethernet message authentication controller (MAC), when available, and peripheral DMA (PDMA) controller to act as masters to the integrated peripherals, FPGA fabric, embedded nonvolatile memory (eNVM), embedded synchronous RAM (eSRAM), external memory controller (EMC), and analog compute engine (ACE) blocks.

SmartFusion cSoCs of different densities offer various sets of integrated peripherals. Available peripherals include SPI, I^2C, and UART serial ports, embedded FlashROM (EFROM), 10/100 Ethernet MAC, timers, phase-locked loops (PLLs), oscillators, real-time counters (RTC), and peripheral DMA controller (PDMA).

Programmable Analog

Analog Front-End (AFE)

SmartFusion cSoCs offer an enhanced analog front-end compared to Fusion devices. The successive approximation register analog-to-digital converters (SAR ADC) are similar to those found on Fusion devices. SmartFusion cSoC also adds first order sigma-delta digital-to-analog converters (SDD DAC).

SmartFusion cSoCs can handle multiple analog signals simultaneously with its signal conditioning blocks (SCBs). SCBs are made of a combination of active bipolar prescalers (ABPS), comparators, current monitors and temperature monitors. ABPS modules allow larger bipolar voltages to be fed to the ADC. Current monitors take the voltage across an external sense resistor and convert it to a voltage suitable for the ADC input range. Similarly, the temperature monitor reads the current through an external PN-junction (diode or transistor) and converts it internally for the ADC. The SCB also includes comparators to monitor fast signal thresholds without using the ADC. The output of the comparators can be fed to the analog compute engine or the ADC.

Analog Compute Engine (ACE)

The mixed signal blocks found in SmartFusion cSoCs are controlled and connected to the rest of the system via a dedicated processor called the analog compute engine (ACE). The role of the ACE is to offload control of the analog blocks from the Cortex-M3, thus offering faster throughput or better power consumption compared to a system where the main processor is in charge of monitoring the analog resources. The ACE is built to handle sampling, sequencing, and post-processing of the ADCs, DACs, and SCBs.

ProASIC3 FPGA Fabric

The SmartFusion cSoC family, based on the proven, low power, firm-error immune ProASIC®3 flash FPGA architecture, benefits from the advantages only flash-based devices offer:

Reduced Cost of Ownership

Advantages to the designer extend beyond low unit cost, high performance, and ease of use. Flash-based SmartFusion cSoCs are live at power-up and do not need to be loaded from an external boot PROM at each power-up. On-board security mechanisms prevent access to the programming information and enable secure remote updates of the FPGA logic. Designers can perform secure remote in-system programming (ISP) to support future design iterations and critical field upgrades, with confidence that valuable IP cannot be compromised or copied. Secure ISP can be performed using the industry standard AES algorithm with MAC data authentication on the device.

Low Power

Flash-based SmartFusion cSoCs exhibit power characteristics similar to those of an ASIC, making them an ideal choice for power-sensitive applications. With SmartFusion cSoCs, there is no power-on current and no high current transition, both of which are common with SRAM-based FPGAs.

SmartFusion cSoCs also have low dynamic power consumption and support very low power time-keeping mode, offering further power savings.

Security

As the nonvolatile, flash-based SmartFusion cSoC family requires no boot PROM, there is no vulnerable external bitstream. SmartFusion cSoCs incorporate FlashLock®, which provides a unique combination of reprogrammability and design security without external overhead, advantages that only a device with nonvolatile flash programming can offer.

SmartFusion cSoCs utilize a 128-bit flash-based key lock and a separate AES key to provide security for programmed IP and configuration data. The FlashROM data in Fusion devices can also be encrypted prior to loading. Additionally, the flash memory blocks can be programmed during runtime using the AES-128 block cipher encryption standard (FIPS Publication 192).

SmartFusion cSoCs with AES-based security are designed to provide protection for remote field updates over public networks, such as the Internet, and help to ensure that valuable IP remains out of the hands of system overbuilders, system cloners, and IP thieves. As an additional security measure, the FPGA configuration data of a programmed Fusion device cannot be read back, although secure design verification is possible. During design, the user controls and defines both internal and external access to the flash memory blocks.

Security, built into the FPGA fabric, is an inherent component of the SmartFusion cSoC family. The flash cells are located beneath seven metal layers, and many device design and layout techniques have been used to make invasive attacks extremely difficult. SmartFusion cSoCs, with FlashLock and AES security, are unique in being highly resistant to both invasive and noninvasive attacks. Your valuable IP is protected with industry standard security measures, making remote ISP feasible. A SmartFusion cSoC provides the highest security available for programmable logic designs.

Single Chip

Flash-based FPGAs store their configuration information in on-chip flash cells. Once programmed, the configuration data is an inherent part of the FPGA structure, and no external configuration data needs to be loaded at system power-up (unlike SRAM-based FPGAs). Therefore, flash-based SmartFusion cSoCs do not require system configuration components such as electrically erasable programmable read-only memories (EEPROMs) or microcontrollers to load device configuration data during power-up. This reduces bill-of-materials costs and PCB area, and increases system security and reliability.

Live at Power-Up

Flash-based SmartFusion cSoCs are live at power-up (LAPU). LAPU SmartFusion cSoCs greatly simplify total system design and reduce total system cost by eliminating the need for complex programmable logic devices (CPLDs). SmartFusion LAPU clocking (PLLs) replace off-chip clocking resources. In addition, glitches and brownouts in system power will not corrupt the SmartFusion flash configuration. Unlike SRAM-based FPGAs, the device will not have to be reloaded when system power is restored. This enables reduction or complete removal of expensive voltage monitor and brownout detection devices from the PCB design. Flash-based SmartFusion cSoCs simplify total system design and reduce cost and design risk, while increasing system reliability.

Immunity to Firm Errors

Firm errors occur most commonly when high-energy neutrons, generated in the atmosphere, strike a configuration cell of an SRAM FPGA. The energy of the collision can change the state of the configuration cell and thus change the logic, routing, or I/O configuration behavior in an unpredictable way.

Another source of radiation-induced firm errors is alpha particles. For alpha radiation to cause a soft or firm error, its source must be in very close proximity to the affected circuit. The alpha source must be in the package molding compound or in the die itself. While low-alpha molding compounds are being used increasingly, this helps reduce but does not entirely eliminate alpha-induced firm errors.

Firm errors are impossible to prevent in SRAM FPGAs. The consequence of this type of error can be a complete system failure. Firm errors do not occur in SmartFusion cSoCs. Once it is programmed, the flash cell configuration element of SmartFusion cSoCs cannot be altered by high energy neutrons and is therefore immune to errors from them. Recoverable (or soft) errors occur in the user data SRAMs of all FPGA devices. These can easily be mitigated by using error detection and correction (EDAC) circuitry built into the FPGA fabric.

Specifying I/O States During Programming

You can modify the I/O states during programming in FlashPro. In FlashPro, this feature is supported for PDB files generated from Designer v8.5 or greater. See the *FlashPro User's Guide* for more information.

Note: PDB files generated from Designer v8.1 to Designer v8.4 (including all service packs) have limited display of Pin Numbers only.

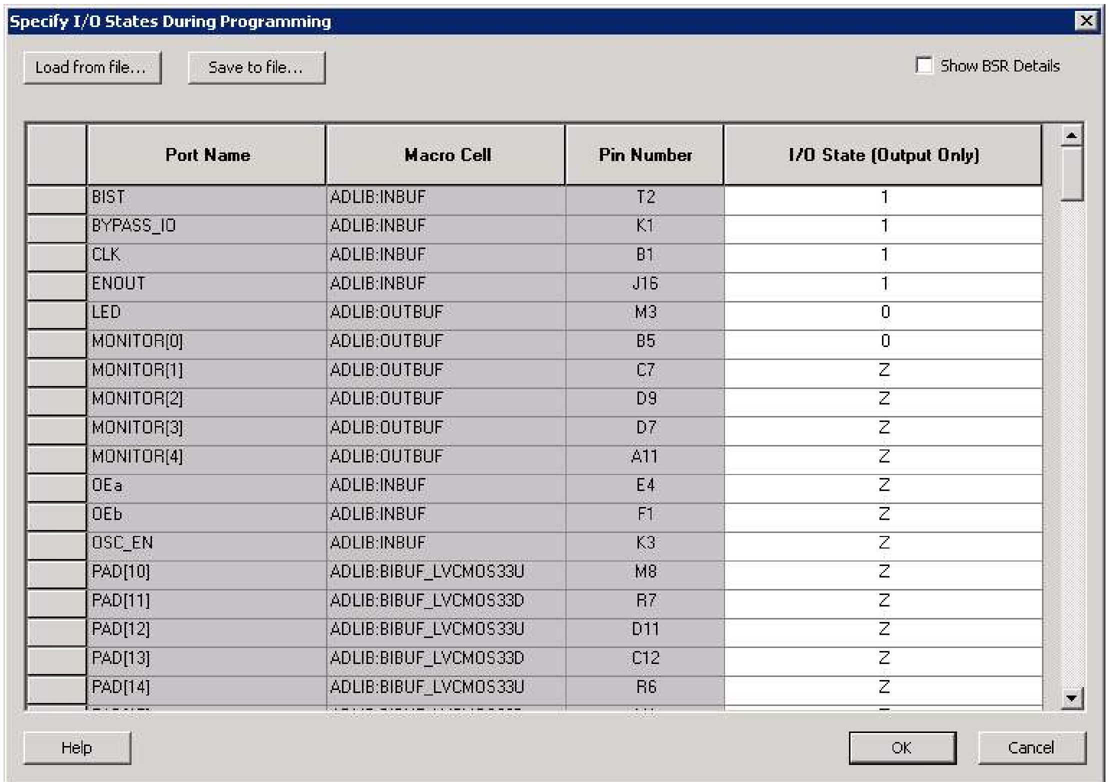
1. Load a PDB from the FlashPro GUI. You must have a PDB loaded to modify the I/O states during programming.
2. From the FlashPro GUI, click PDB Configuration. A FlashPoint – Programming File Generator window appears.
3. Click the Specify I/O States During Programming button to display the Specify I/O States During Programming dialog box.
4. Sort the pins as desired by clicking any of the column headers to sort the entries by that header. Select the I/Os you wish to modify (Figure 1-1 on page 1-4).
5. Set the I/O Output State. You can set Basic I/O settings if you want to use the default I/O settings for your pins, or use Custom I/O settings to customize the settings for each pin. Basic I/O state settings:

   1 – I/O is set to drive out logic High

   0 – I/O is set to drive out logic Low

   Last Known State – I/O is set to the last value that was driven out prior to entering the programming mode, and then held at that value during programming

   Z -Tri-State: I/O is tristated



Port Name	Macro Cell	Pin Number	I/O State (Output Only)
BIST	ADLIB:INBUF	T2	1
BYPASS_IO	ADLIB:INBUF	K1	1
CLK	ADLIB:INBUF	B1	1
ENOUT	ADLIB:INBUF	J16	1
LED	ADLIB:OUTBUF	M3	0
MONITOR[0]	ADLIB:OUTBUF	B5	0
MONITOR[1]	ADLIB:OUTBUF	C7	Z
MONITOR[2]	ADLIB:OUTBUF	D9	Z
MONITOR[3]	ADLIB:OUTBUF	D7	Z
MONITOR[4]	ADLIB:OUTBUF	A11	Z
OEa	ADLIB:INBUF	E4	Z
OEb	ADLIB:INBUF	F1	Z
OSC_EN	ADLIB:INBUF	K3	Z
PAD[10]	ADLIB:BIBUF_LVCMOS33U	M8	Z
PAD[11]	ADLIB:BIBUF_LVCMOS33D	R7	Z
PAD[12]	ADLIB:BIBUF_LVCMOS33U	D11	Z
PAD[13]	ADLIB:BIBUF_LVCMOS33D	C12	Z
PAD[14]	ADLIB:BIBUF_LVCMOS33U	R6	Z

Figure 1-1 • **I/O States During Programming Window**

6. Click OK to return to the FlashPoint – Programming File Generator window.

Note: I/O States During programming are saved to the ADB and resulting programming files after completing programming file generation.

2 – SmartFusion DC and Switching Characteristics

General Specifications

Operating Conditions

Stresses beyond the operating conditions listed in Table 2-1 may cause permanent damage to the device.

Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Absolute Maximum Ratings are stress ratings only; functional operation of the device at these or any other conditions beyond those listed under the Recommended Operating Conditions specified in Table 2-3 on page 2-3 is not implied.

Table 2-1 • **Absolute Maximum Ratings**

Symbol	Parameter	Limits	Units
VCC	DC core supply voltage	–0.3 to 1.65	V
VJTAG	JTAG DC voltage	–0.3 to 3.75	V
VPP	Programming voltage	–0.3 to 3.75	V
VCCPLLx	Analog power supply (PLL)	–0.3 to 1.65	V
VCCFPGAIOBx	DC FPGA I/O buffer supply voltage	–0.3 to 3.75	V
VCCMSSIOBx	DC MSS I/O buffer supply voltage	–0.3 to 3.75	V
VI	I/O input voltage	–0.3 V to 3.6 V (when I/O hot insertion mode is enabled) –0.3 V to (VCCxxxxIOBx + 1 V) or 3.6 V, whichever voltage is lower (when I/O hot-insertion mode is disabled)	V
VCC33A	Analog clean 3.3 V supply to the analog circuitry	–0.3 to 3.75	V
VCC33ADCx	Analog 3.3 V supply to ADC	–0.3 to 3.75	V
VCC33AP	Analog clean 3.3 V supply to the charge pump	–0.3 to 3.75	V
VCC33SDDx	Analog 3.3 V supply to the sigma-delta DAC	–0.3 to 3.75	V
VAREFx	Voltage reference for ADC	1.0 to 3.75	V
VCCRCOSC	Analog supply to the integrated RC oscillator	–0.3 to 3.75	V
VDDBAT	External battery supply	–0.3 to 3.75	V
VCCMAINXTAL	Analog supply to the main crystal oscillator	–0.3 to 3.75	V
VCCLPXTAL	Analog supply to the low power 32 kHz crystal oscillator	–0.3 to 3.75	V
VCCENVM	Embedded nonvolatile memory supply	–0.3 to 1.65	V
VCCESRAM	Embedded SRAM supply	–0.3 to 1.65	V
VCC15A	Analog 1.5 V supply to the analog circuitry	–0.3 to 1.65	V
VCC15ADCx	Analog 1.5 V supply to the ADC	–0.3 to 1.65	V
T_{STG} [1]	Storage temperature	–65 to +150	°C
T_J [1]	Junction temperature	125	°C

Notes:

1. *For flash programming and retention maximum limits, refer to Table 2-4 on page 2-4. For recommended operating conditions, refer to Table 2-3 on page 2-3.*
2. *The device should be operated within the limits specified by the datasheet. During transitions, the input signal may undershoot or overshoot according to the limits shown in Table 2-5 on page 2-4.*

Table 2-2 • **Analog Maximum Ratings**

Parameter	Conditions	Min.	Max.	Units
ABPS[n] pad voltage (relative to ground)	GDEC[1:0] = 00 (±15.36 V range)			
	Absolute maximum	–11.5	12.4	V
	Recommended	–11	12	V
	GDEC[1:0] = 01 (±10.24 V range)	–11.5	12	V
	GDEC[1:0] = 10 (±5.12 V range)	–6	6	V
	GDEC[1:0] = 11 (±2.56 V range)	–3	3	V
CM[n] pad voltage relative to ground)	CMB_DI_ON = 0 (ADC isolated) COMP_EN = 0 (comparator off, for the associated even-numbered comparator)			
	Absolute maximum	–0.3	12.4	V
	Recommended	–0.3	12	V
	CMB_DI_ON = 0 (ADC isolated) COMP_EN = 1 (comparator on)	–0.3	3	V
	TMB_DI_ON = 1 (direct ADC in)	–0.3	3	V
TM[n] pad voltage (relative to ground)	TMB_DI_ON = 0 (ADC isolated) COMP_EN = 1(comparator on)	–0.3	3	V
	TMB_DI_ON = 1 (direct ADC in)	–0.3	3	V
ADC[n] pad voltage (relative to ground)		–0.3	3.6	V

Table 2-3 • **Recommended Operating Conditions**

Symbol	Parameter[1]		Military	Units
T_J	Junction temperature		–55 to +125	°C
VCC [2]	1.5 V DC core supply voltage		1.425 to 1.575	V
VJTAG	JTAG DC voltage		1.425 to 3.6	V
VPP	Programming voltage	Programming mode	3.15 to 3.45	V
		Operation[3]	0 to 3.6	V
VCCPLLx	Analog power supply (PLL)		1.425 to 1.575	V
VCCFPGAIOBx/ VCCMSSIOBx[4]	1.5 V DC supply voltage		1.425 to 1.575	V
	1.8 V DC supply voltage		1.7 to 1.9	V
	2.5 V DC supply voltage		2.3 to 2.7	V
	3.3 V DC supply voltage		3.0 to 3.6	V
	LVDS differential I/O		2.375 to 2.625	V
	LVPECL differential I/O		3.0 to 3.6	V
VCC33A[5]	Analog clean 3.3 V supply to the analog circuitry		3.15 to 3.45	V
VCC33ADCx[5]	Analog 3.3 V supply to ADC		3.15 to 3.45	V
VCC33AP[5]	Analog clean 3.3 V supply to the charge pump		3.15 to 3.45	V
VCC33SDDx[5]	Analog 3.3 V supply to sigma-delta DAC		3.15 to 3.45	V
VAREFx	Voltage reference for ADC		2.527 to 3.3	V
VCCRCOSC	Analog supply to the integrated RC oscillator		3.15 to 3.45	V
VDDBAT	External battery supply		2.7 to 3.63	V
VCCMAINXTAL[5]	Analog supply to the main crystal oscillator		3.15 to 3.45	V
VCCLPXTAL[5]	Analog supply to the low power 32 KHz crystal oscillator		3.15 to 3.45	V
VCCENVM	Embedded nonvolatile memory supply		1.425 to 1.575	V
VCCESRAM	Embedded SRAM supply		1.425 to 1.575	V
VCC15A[2]	Analog 1.5 V supply to the analog circuitry		1.425 to 1.575	V
VCC15ADCx[2]	Analog 1.5 V supply to the ADC		1.425 to 1.575	V

Notes:

1. *All parameters representing voltages are measured with respect to GND unless otherwise specified.*
2. *The following 1.5 V supplies should be connected together while following proper noise filtering practices: VCC, VCC15A, and VCC15ADCx.*
3. *VPP can be left floating during operation (not programming mode).*
4. *The ranges given here are for power supplies only. The recommended input voltage ranges specific to each I/O standard are given in Table 2-19 on page 2-24. VCCxxxxIOBx should be at the same voltage within a given I/O bank.*
5. *The following 3.3 V supplies should be connected together while following proper noise filtering practices: VCC33A, VCC33ADCx, VCC33AP, VCC33SDDx, VCCMAINXTAL, and VCCLPXTAL.*

Table 2-4 • **Embedded Flash Programming, Storage and Operating Limits**

Product Grade	Storage Temperature	Element	Grade Programming Cycles	Retention
Military	Max. T_J = 125°C	Embedded Flash	< 1,000	6 years
			< 10,000	3 years
			< 15,000	1.5 years

Tj (°C)	HTR Lifetime (yrs)
70	102.7
85	43.8
100	20.0
105	15.6
110	12.3
115	9.7
120	7.7
125	6.2
130	5.0
135	4.0
140	3.3
145	2.7
150	2.2

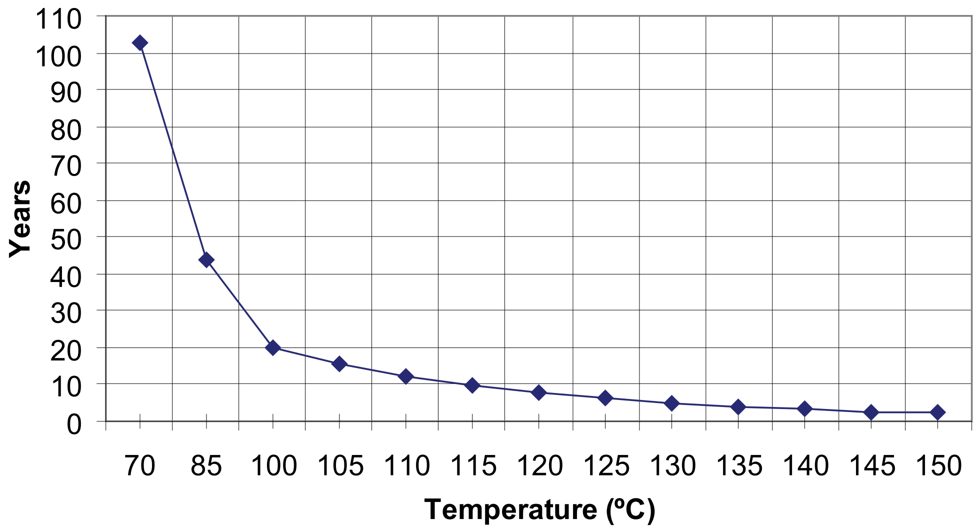


Figure 2-1 • **High Temperature Data Retention (HTR) for FPGA/FlashROM**

Table 2-5 • **Overshoot and Undershoot Limits** [1]

VCCxxxxIOBx	Average VCCxxxxIOBx–GND Overshoot or Undershoot Duration as a Percentage of Clock Cycle[1]	Maximum Overshoot/ Undershoot (125°C)
2.7 V or less	10%	0.72 V
	5%	0.82 V
3 V	10%	0.72 V
	5%	0.81 V
3.3 V	10%	0.69 V
	5%	0.70 V
3.6 V	10%	–
	5%	–

Notes:

1. *The duration is allowed at one out of six clock cycles. If the overshoot/undershoot occurs at one out of two cycles, the maximum overshoot/undershoot has to be reduced by 0.15 V.*
2. *This table does not provide PCI overshoot/undershoot limits.*

Power Supply Sequencing Requirement

SmartFusion cSoCs have an on-chip 1.5 V regulator, but usage of an external 1.5 V supply is also allowed while the on-chip regulator is disabled. In that case, the 3.3 V supplies (VCC33A, etc.) should be powered before 1.5 V (VCC, etc.) supplies. The 1.5 V supplies should be enabled only after 3.3 V supplies reach a value higher than 2.7 V.

I/O Power-Up and Supply Voltage Thresholds for Power-On Reset (Military)

Sophisticated power-up management circuitry is designed into every SmartFusion cSoC. These circuits ensure easy transition from the powered-off state to the powered-up state of the device. In addition, the I/O will be in a known state through the power-up sequence. The basic principle is shown in Figure 2-2 on page 2-6.

There are five regions to consider during power-up.

SmartFusion I/Os are activated only if ALL of the following three conditions are met:

1. VCC and VCCxxxxIOBx are above the minimum specified trip points (Figure 2-2 on page 2-6).
2. VCCxxxxIOBx > VCC – 0.75 V (typical)
3. Chip is in the SoC Mode.

VCCxxxxIOBx Trip Point:
Ramping up: 0.6 V < trip_point_up < 1.2 V
Ramping down: 0.5 V < trip_point_down < 1.1 V

VCC Trip Point:
Ramping up: 0.6 V < trip_point_up < 1.1 V
Ramping down: 0.5 V < trip_point_down < 1 V

VCC and VCCxxxxIOBx ramp-up trip points are about 100 mV higher than ramp-down trip points. This specifically built-in hysteresis prevents undesirable power-up oscillations and current surges. Note the following:

- During programming, I/Os become tristated and weakly pulled up to VCCxxxxIOBx.
- JTAG supply, PLL power supplies, and charge pump VPUMP supply have no influence on I/O behavior.

PLL Behavior at Brownout Condition

The Microsemi SoC Products Group recommends using monotonic power supplies or voltage regulators to ensure proper power-up behavior. Power ramp-up should be monotonic at least until VCC and VCCPLLx exceed brownout activation levels. The VCC activation level is specified as 1.1 V worst-case (see Figure 2-2 on page 2-6 for more details).

When PLL power supply voltage and/or VCC levels drop below the VCC brownout levels (0.75 V ± 0.25 V), the PLL output lock signal goes low and/or the output clock is lost. Refer to the "Power-Up/-Down Behavior of Low Power Flash Devices" chapter of the *ProASIC3 FPGA Fabric User's Guide* for information on clock and lock recovery.

Internal Power-Up Activation Sequence

1. Core
2. Input buffers

Output buffers, after 200 ns delay from input buffer activation

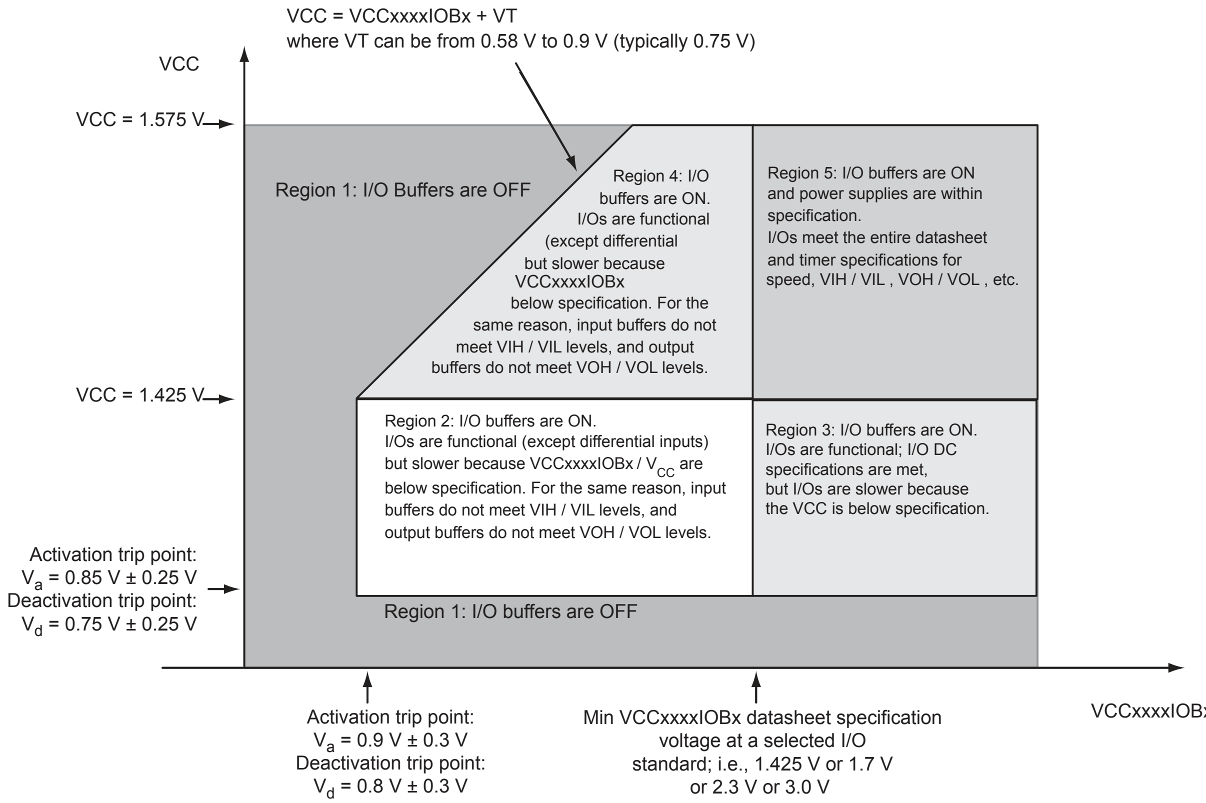


Figure 2-2 • **I/O State as a Function of VCCxxxxIOBx and VCC Voltage Levels**

Thermal Characteristics

Introduction

The temperature variable in the SoC Products Group Designer software refers to the junction temperature, not the ambient, case, or board temperatures. This is an important distinction because dynamic and static power consumption will cause the chip's junction temperature to be higher than the ambient, case, or board temperatures. EQ 1 through EQ 3 give the relationship between thermal resistance, temperature gradient, and power.

$$\theta_{JA} = \frac{T_J - \theta_A}{P}$$

EQ 1

$$\theta_{JB} = \frac{T_J - T_B}{P}$$

EQ 2

$$\theta_{JC} = \frac{T_J - T_C}{P}$$

EQ 3

where

θ_{JA} = Junction-to-air thermal resistance
θ_{JB} = Junction-to-board thermal resistance
θ_{JC} = Junction-to-case thermal resistance
T_J = Junction temperature
T_A = Ambient temperature
T_B = Board temperature (measured 1.0 mm away from the package edge)
T_C = Case temperature
P = Total power dissipated by the device

Table 2-6 • **Package Thermal Resistance**

Product	θ_{JA}			θ_{JC}	θ_{JB}	**Units**
	Still Air	**1.0 m/s**	**2.5 m/s**			
A2F060-FG256	36.9	31.1	29.4	TBD	23.7	°C/W
A2F500-FG256	26.2	20.6	18.9	TBD	13.2	°C/W
A2F500-FG484	21.9	18.6	16.4	7.5	11	°C/W

Theta-JA

Junction-to-ambient thermal resistance (θ_{JA}) is determined under standard conditions specified by JEDEC (JESD-51), but it has little relevance in actual performance of the product. It should be used with caution but is useful for comparing the thermal performance of one package to another.

A sample calculation showing the maximum power dissipation allowed for the A2F500-FG484 package under forced convection of 1.0 m/s and 75°C ambient temperature is as follows:

$$\text{Maximum Power Allowed} = \frac{T_{J(MAX)} - T_{A(MAX)}}{\theta_{JA}}$$

EQ 4

where

θ_{JA} = 18.6°C/W (taken from Table 2-6 on page 2-7).

T_A = 75.00°C

$$\text{Maximum Power Allowed} = \frac{100.00°C - 75.00°C}{18.6°C/W} = 1.61\ W$$

EQ 5

The power consumption of a device can be calculated using the Microsemi SoC Products Group power calculator. The device's power consumption must be lower than the calculated maximum power dissipation by the package. If the power consumption is higher than the device's maximum allowable power dissipation, a heat sink can be attached on top of the case, or the airflow inside the system must be increased.

Theta-JB

Junction-to-board thermal resistance (θ_{JB}) measures the ability of the package to dissipate heat from the surface of the chip to the PCB. As defined by the JEDEC (JESD-51) standard, the thermal resistance from junction to board uses an isothermal ring cold plate zone concept. The ring cold plate is simply a means to generate an isothermal boundary condition at the perimeter. The cold plate is mounted on a JEDEC standard board with a minimum distance of 5.0 mm away from the package edge.

Theta-JC

Junction-to-case thermal resistance (θ_{JC}) measures the ability of a device to dissipate heat from the surface of the chip to the top or bottom surface of the package. It is applicable for packages used with external heat sinks. Constant temperature is applied to the surface in consideration and acts as a boundary condition. This only applies to situations where all or nearly all of the heat is dissipated through the surface in consideration.

Calculation for Heat Sink

For example, in a design implemented in an A2F500-FG484 package with 2.5 m/s airflow, the power consumption value using the power calculator is 3.00 W. The user-dependent T_a and T_j are given as follows:

T_J = 100.00°C

T_A = 70.00°C

From the datasheet:

θ_{JA} = 16.4°C/W

θ_{JC} = 7.5°C/W

$$P = \frac{T_J - T_A}{\theta_{JA}} = \frac{100°C - 70°C}{16.4\ W} = 1.82\ W$$

EQ 6

The 1.82 W power is less than the required 3.00 W. The design therefore requires a heat sink, or the airflow where the device is mounted should be increased. The design's total junction-to-air thermal resistance requirement can be estimated by EQ 7:

$$\theta_{JA(total)} = \frac{T_J - T_A}{P} = \frac{100°C - 70°C}{3.00\ W} = 10.00°C/W$$

EQ 7

Determining the heat sink's thermal performance proceeds as follows:

$$\theta_{JA(TOTAL)} = \theta_{JC} + \theta_{CS} + \theta_{SA}$$

EQ 8

where

θ_{JA}	=	0.37°C/W
	=	Thermal resistance of the interface material between the case and the heat sink, usually provided by the thermal interface manufacturer
θ_{SA}	=	Thermal resistance of the heat sink in °C/W

$$\theta_{SA} = \theta_{JA(TOTAL)} - \theta_{JC} - \theta_{CS}$$

EQ 9

$$\theta_{SA} = 10°C/W - 7.5°C/W - 0.37°C/W = 2.5°C/W$$

A heat sink with a thermal resistance of 2.5°C/W or better should be used. Thermal resistance of heat sinks is a function of airflow. The heat sink performance can be significantly improved with increased airflow.

Carefully estimating thermal resistance is important in the long-term reliability of an FPGA. Design engineers should always correlate the power consumption of the device with the maximum allowable power dissipation of the package selected for that device.

Note: The junction-to-air and junction-to-board thermal resistances are based on JEDEC standard (JESD-51) and assumptions made in building the model. It may not be realized in actual application and therefore should be used with a degree of caution. Junction-to-case thermal resistance assumes that all power is dissipated through the case.

Temperature and Voltage Derating Factors

Table 2-7 • **Temperature and Voltage Derating Factors for Timing Delays (normalized to T_J = 125°C, worst-case VCC = 1.425 V)**

Array Voltage VCC (V)		Junction Temperature (°C)						
	–55°C	–40°C	0°C	25°C	70°C	85°C	100°C	125°C
1.425	0.81	0.82	0.87	0.89	0.94	0.96	0.97	1.00
1.500	0.76	0.78	0.82	0.84	0.89	0.91	0.92	0.95
1.575	0.73	0.75	0.79	0.81	0.86	0.87	0.89	0.91

Calculating Power Dissipation

Quiescent Supply Current

Table 2-8 • **Power Supplies Configuration**

Modes and Power Supplies	VCCxxxxIOBx VCCFPGAIOBx VCCMSSIOBx	VCC33A / VCC33ADCx VCC33AP / VCC33SDDx VCCMAINXTAL / VCCLPXTAL	VCC / VCC15A / VCC15ADCx VCCPLLx, VCCENVM, VCCESRAM	VDDBAT	VCCRCOSC	VJTAG	VPP	eNVM (reset/off)	LPXTAL (enable/disable)	MAINXTAL (enable/disable)
Time Keeping mode	0 V	0 V	0 V	3.3 V	0 V	0 V	0 V	Off	Enable	Disable
Standby mode	On*	3.3 V	1.5 V	N/A	3.3 V	N/A	N/A	Reset	Enable	Disable
SoC mode	On*	3.3 V	1.5 V	N/A	3.3 V	N/A	N/A	On	Enable	Enable

*Note: *On means proper voltage is applied. Refer to Table 2-3 on page 2-3 for recommended operating conditions.*

Table 2-9 • **Quiescent Supply Current Characteristics**

Parameter	Modes		Temperature	A2F060		A2F500	
				1.5 V Domain	3.3 V Domain	1.5 V Domain	3.3 V Domain
IDC1	SoC mode		25°C	3 mA	2 mA	16.5 mA	4 mA
		Nominal	125°C	9.2 mA	9.6 mA	47 mA	9.9 mA
		Worst case	125°C	31 mA	20.5 mA	92 mA	20.5 mA
IDC2	Standby mode		25°C	3 mA	2 mA	16.5 mA	4 mA
		Nominal	125°C	9.2 mA	9.6 mA	47 mA	9.9 mA
		Worst case	125°C	31 mA	20.5 mA	92 mA	20.5 mA
IDC3	Time Keeping mode		25°C	–	10 µA	–	10 µA
		Nominal	125°C	–	30 µA	–	30 µA
		Worst case	125°C	–	300 µA	–	300 µA

Power per I/O Pin

Table 2-10 • **Summary of I/O Input Buffer Power (per pin) – Default I/O Software Settings Applicable to FPGA I/O Banks, I/O Assigned to EMC I/O Pins**

	VCCFPGAIOBx (V)	Static Power PDC7 (mW)	Dynamic Power PAC9 (µW/MHz)
Single-Ended			
3.3 V LVTTL / 3.3 V LVCMOS	3.3	–	17.55
2.5 V LVCMOS	2.5	–	5.97
1.8 V LVCMOS	1.8	–	2.88
1.5 V LVCMOS (JESD8-11)	1.5	–	2.33
3.3 V PCI	3.3	–	19.21
3.3 V PCI-X	3.3	–	19.21
Differential			
LVDS	2.5	2.25	0.82
LVPECL	3.3	5.74	1.16

Table 2-11 • **Summary of I/O Input Buffer Power (per pin) – Default I/O Software Settings Applicable to MSS I/O Banks**

	VCCMSSIOBx (V)	Static Power PDC7 (mW)	Dynamic Power PAC9 (µW/MHz)
Single-Ended			
3.3 V LVTTL / 3.3 V LVCMOS	3.3	–	17.21
3.3 V LVCMOS / 3.3 V LVCMOS – Schmitt trigger	3.3	–	20.00
2.5 V LVCMOS	2.5	–	5.55
2.5 V LVCMOS – Schmitt trigger	2.5	–	7.03
1.8 V LVCMOS	1.8	–	2.61
1.8 V LVCMOS – Schmitt trigger	1.8	–	2.72
1.5 V LVCMOS (JESD8-11)	1.5	–	1.98
1.5 V LVCMOS (JESD8-11) – Schmitt trigger	1.5	–	1.93

Table 2-12 • Summary of I/O Output Buffer Power (per pin) – Default I/O Software Settings* Applicable to FPGA I/O Banks, I/O Assigned to EMC I/O Pins

	C_{LOAD} (pF)	VCCFPGAIOBx (V)	Static Power PDC8 (mW)	Dynamic Power PAC10 (µW/MHz)
Single-Ended				
3.3 V LVTTL / 3.3 V LVCMOS	35	3.3	–	475.66
2.5 V LVCMOS	35	2.5	–	270.50
1.8 V LVCMOS	35	1.8	–	152.17
1.5 V LVCMOS (JESD8-11)	35	1.5	–	104.44
3.3 V PCI	10	3.3	–	202.69
3.3 V PCI-X	10	3.3	–	202.69
Differential				
LVDS	–	2.5	7.75	88.26
LVPECL	–	3.3	19.54	164.99

*Note: *Dynamic power consumption is given for standard load and software default drive strength and output slew.*

Table 2-13 • Summary of I/O Output Buffer Power (per pin) – Default I/O Software Settings Applicable to MSS I/O Banks

	C_{LOAD} (pF)	VCCMSSIOBx (V)	Static Power PDC8 (mW)[2]	Dynamic Power PAC10 (µW/MHz)[3]
Single-Ended				
3.3 V LVTTL / 3.3 V LVCMOS	10	3.3	–	19.67
2.5 V LVCMOS	10	2.5	–	11.23
1.8 V LVCMOS	10	1.8	–	5.82
1.5 V LVCMOS (JESD8-11)	10	1.5	–	4.07

Power Consumption of Various Internal Resources

Table 2-14 • **Different Components Contributing to Dynamic Power Consumption in SmartFusion cSoCs**

Parameter	Definition	Power Supply		Device		Units
		Name	Domain	A2F060	A2F500	
PAC1	Clock contribution of a Global Rib	VCC	1.5 V	3.39	5.05	µW/MHz
PAC2	Clock contribution of a Global Spine	VCC	1.5 V	1.14	2.50	µW/MHz
PAC3	Clock contribution of a VersaTile row	VCC	1.5 V	1.15	1.15	µW/MHz
PAC4	Clock contribution of a VersaTile used as a sequential module	VCC	1.5 V	0.12	0.12	µW/MHz
PAC5	First contribution of a VersaTile used as a sequential module	VCC	1.5 V	0.07	0.07	µW/MHz
PAC6	Second contribution of a VersaTile used as a sequential module	VCC	1.5 V	0.29	0.29	µW/MHz
PAC7	Contribution of a VersaTile used as a combinatorial module	VCC	1.5 V	0.29	0.29	µW/MHz
PAC8	Average contribution of a routing net	VCC	1.5 V	1.04	0.79	µW/MHz
PAC9	Contribution of an I/O input pin (standard dependent)	VCCxxxxIOBx/VCC	See Table 2-10 and Table 2-11 on page 2-11			
PAC10	Contribution of an I/O output pin (standard dependent)	VCCxxxxIOBx/VCC	See Table 2-12 and Table 2-13 on page 2-12			
PAC11	Average contribution of a RAM block during a read operation	VCC	1.5 V	25.00		µW/MHz
PAC12	Average contribution of a RAM block during a write operation	VCC	1.5 V	30.00		µW/MHz
PAC13	Dynamic Contribution for PLL	VCC	1.5 V	2.60		µW/MHz
PAC15	Contribution of NVM block during a read operation (F < 33MHz)	VCC	1.5 V	358.00		µW/MHz
PAC16	1st contribution of NVM block during a read operation (F > 33MHz)	VCC	1.5 V	12.88		mW
PAC17	2nd contribution of NVM block during a read operation (F > 33MHz)	VCC	1.5 V	4.80		µW/MHz
PAC18	Main Crystal Oscillator contribution	VCCMAINXTAL	3.3 V	1.98		mW
PAC19a	RC Oscillator contribution	VCCRCOSC	3.3 V	3.30		mW
PAC19b	RC Oscillator contribution	VCC	1.5 V	3.00		mW
PAC20a	Analog Block Dynamic Power Contribution of the ADC	VCC33ADCx	3.3 V	8.25		mW
PAC20b	Analog Block Dynamic Power Contribution of the ADC	VCC15ADCx	1.5 V	3.00		mW
PAC21	Low Power Crystal Oscillator contribution	VCCLPXTAL	3.3 V	33.00		µW
PAC22	MSS Dynamic Power Contribution – Running Drysthone at 100MHz[1]	VCC	1.5 V	67.50		mW
PAC23	Temperature Monitor Power Contribution	See Table 2-94 on page 2-79	–	1.23		mW
PAC24	Current Monitor Power Contribution	See Table 2-93 on page 2-78	–	1.03		mW

Table 2-14 • Different Components Contributing to Dynamic Power Consumption in SmartFusion cSoCs

Parameter	Definition	Power Supply		Device		Units
		Name	Domain	A2F060	A2F500	
PAC25	ABPS Power Contribution	See Table 2-97 on page 2-83	–	0.70		mW
PAC26	Sigma-Delta DAC Power Contribution[2]	See Table 2-99 on page 2-86	–	0.58		mW
PAC27	Comparator Power Contribution	See Table 2-98 on page 2-85	–	1.02		mW
PAC28	Voltage Regulator Power Contribution[3]	See Table 2-100 on page 2-88	–	36.30		mW

Notes:

1. *For a different use of MSS peripherals and resources, refer to SmartPower.*
2. *Assumes Input = Half Scale Operation mode.*
3. *Assumes 100 mA load on 1.5 V domain.*

Table 2-15 • Different Components Contributing to the Static Power Consumption in SmartFusion cSoCs

Parameter	Definition	Power Supply		Device		Units
		Name	Domain	A2F060	A2F500	
PDC1	Core static power contribution in SoC mode	VCC	1.5 V	7.80	37.95	mW
PDC2	Device static power contribution in Standby Mode	See Table 2-8 on page 2-10	–	7.80	37.95	mW
PDC3	Device static power contribution in Time Keeping mode	See Table 2-8 on page 2-10	3.3 V	33.00	33.0	µW
PDC7	Static contribution per input pin (standard dependent contribution)	VCCxxxxIOBx/VCC	See Table 2-10 and Table 2-11 on page 2-11.			
PDC8	Static contribution per output pin (standard dependent contribution)	VCCxxxxIOBx/VCC	See Table 2-12 and Table 2-13 on page 2-12.			
PDC9	Static contribution per PLL	VCC	1.5 V	2.55	2.55	mW

Table 2-16 • eNVM Dynamic Power Consumption

Parameter	Description	Condition	Min.	Typ.	Max.	Units
eNVM System	eNVM array operating power	Idle		795		µA
		Read operation	See Table 2-14 on page 2-13.			
		Erase		900		µA
		Write		900		µA
PNVMCTRL	eNVM controller operating power			20		µW/MHz

Power Calculation Methodology

This section describes a simplified method to estimate power consumption of an application. For more accurate and detailed power estimations, use the SmartPower tool in the Libero SoC software.

The power calculation methodology described below uses the following variables:

- The number of PLLs/CCCs as well as the number and the frequency of each output clock generated
- The number of combinatorial and sequential cells used in the design
- The internal clock frequencies
- The number and the standard of I/O pins used in the design
- The number of RAM blocks used in the design
- The number of eNVM blocks used in the design
- The analog block used in the design, including the temperature monitor, current monitor, ABPS, sigma-delta DAC, comparator, low power crystal oscillator, RC oscillator and the main crystal oscillator
- Toggle rates of I/O pins as well as VersaTiles—guidelines are provided in Table 2-17 on page 2-19.
- Enable rates of output buffers—guidelines are provided for typical applications in Table 2-18 on page 2-19.
- Read rate and write rate to the memory—guidelines are provided for typical applications in Table 2-18 on page 2-19.
- Read rate to the eNVM blocks

The calculation should be repeated for each clock domain defined in the design.

Methodology

Total Power Consumption—P_{TOTAL}

SoC Mode, Standby Mode, and Time Keeping Mode.

$P_{TOTAL} = P_{STAT} + P_{DYN}$

P_{STAT} is the total static power consumption.

P_{DYN} is the total dynamic power consumption.

Total Static Power Consumption—P_{STAT}

SoC Mode

$P_{STAT} = P_{DC1} + (N_{INPUTS} * P_{DC7}) + (N_{OUTPUTS} * P_{DC8}) + (N_{PLLS} * P_{DC9})$

N_{INPUTS} is the number of I/O input buffers used in the design.

$N_{OUTPUTS}$ is the number of I/O output buffers used in the design.

N_{PLLS} is the number of PLLs available in the device.

Standby Mode

$P_{STAT} = P_{DC2}$

Time Keeping Mode

$P_{STAT} = P_{DC3}$

Total Dynamic Power Consumption—P_{DYN}

SoC Mode

$P_{DYN} = P_{CLOCK} + P_{S\text{-}CELL} + P_{C\text{-}CELL} + P_{NET} + P_{INPUTS} + P_{OUTPUTS} + P_{MEMORY} + P_{PLL} + P_{eNVM} + P_{XTL\text{-}OSC} + P_{RC\text{-}OSC} + P_{AB} + P_{LPXTAL\text{-}OSC} + P_{MSS}$

Standby Mode

$P_{DYN} = P_{RC\text{-}OSC} + P_{LPXTAL\text{-}OSC}$

Time Keeping Mode

$P_{DYN} = P_{LPXTAL\text{-}OSC}$

Global Clock Dynamic Contribution—P_{CLOCK}

SoC Mode

$P_{CLOCK} = (P_{AC1} + N_{SPINE} * P_{AC2} + N_{ROW} * PAC3 + N_{S\text{-}CELL} * P_{AC4}) * F_{CLK}$

N_{SPINE} is the number of global spines used in the user design—guidelines are provided in the "Device Architecture" chapter of the *SmartFusion FPGA Fabric User's Guide*.

N_{ROW} is the number of VersaTile rows used in the design—guidelines are provided in the "Device Architecture" chapter of the *SmartFusion FPGA Fabric User's Guide*.

F_{CLK} is the global clock signal frequency.

$N_{S\text{-}CELL}$ is the number of VersaTiles used as sequential modules in the design.

Standby Mode and Time Keeping Mode

$P_{CLOCK} = 0 W$

Sequential Cells Dynamic Contribution—$P_{S\text{-}CELL}$

SoC Mode

$P_{S\text{-}CELL} = N_{S\text{-}CELL} * (P_{AC5} + (\alpha_1 / 2) * P_{AC6}) * F_{CLK}$

$N_{S\text{-}CELL}$ is the number of VersaTiles used as sequential modules in the design. When a multi-tile sequential cell is used, it should be accounted for as 1.

α_1 is the toggle rate of VersaTile outputs—guidelines are provided in Table 2-17 on page 2-19.

F_{CLK} is the global clock signal frequency.

Standby Mode and Time Keeping Mode

$P_{S\text{-}CELL} = 0 W$

Combinatorial Cells Dynamic Contribution—$P_{C\text{-}CELL}$

SoC Mode

$P_{C\text{-}CELL} = N_{C\text{-}CELL} * (\alpha_1 / 2) * P_{AC7} * F_{CLK}$

$N_{C\text{-}CELL}$ is the number of VersaTiles used as combinatorial modules in the design.

α_1 is the toggle rate of VersaTile outputs—guidelines are provided in Table 2-17 on page 2-19.

F_{CLK} is the global clock signal frequency.

Standby Mode and Time Keeping Mode

$P_{C\text{-}CELL} = 0 W$

Routing Net Dynamic Contribution—P_{NET}

SoC Mode

$P_{NET} = (N_{S\text{-}CELL} + N_{C\text{-}CELL}) * (\alpha_1 / 2) * P_{AC8} * F_{CLK}$

$N_{S\text{-}CELL}$ is the number VersaTiles used as sequential modules in the design.

$N_{C\text{-}CELL}$ is the number of VersaTiles used as combinatorial modules in the design.

α_1 is the toggle rate of VersaTile outputs—guidelines are provided in Table 2-17 on page 2-19.

F_{CLK} is the frequency of the clock driving the logic including these nets.

Standby Mode and Time Keeping Mode

P_{NET} = 0 W

I/O Input Buffer Dynamic Contribution—P_{INPUTS}

SoC Mode

$P_{INPUTS} = N_{INPUTS} * (\alpha_2 / 2) * P_{AC9} * F_{CLK}$

Where:

N_{INPUTS} is the number of I/O input buffers used in the design.

α_2 is the I/O buffer toggle rate—guidelines are provided in Table 2-17 on page 2-19.

F_{CLK} is the global clock signal frequency.

Standby Mode and Time Keeping Mode

P_{INPUTS} = 0 W

I/O Output Buffer Dynamic Contribution—$P_{OUTPUTS}$

SoC Mode

$P_{OUTPUTS} = N_{OUTPUTS} * (\alpha_2 / 2) * \beta_1 * P_{AC10} * F_{CLK}$

Where:

$N_{OUTPUTS}$ is the number of I/O output buffers used in the design.

α_2 is the I/O buffer toggle rate—guidelines are provided in Table 2-17 on page 2-19.

β_1 is the I/O buffer enable rate—guidelines are provided in Table 2-18 on page 2-19.

F_{CLK} is the global clock signal frequency.

Standby Mode and Time Keeping Mode

$P_{OUTPUTS}$ = 0 W

FPGA Fabric SRAM Dynamic Contribution—P_{MEMORY}

SoC Mode

$P_{MEMORY} = (N_{BLOCKS} * P_{AC11} * \beta_2 * F_{READ\text{-}CLOCK}) + (N_{BLOCKS} * P_{AC12} * \beta_3 * F_{WRITE\text{-}CLOCK})$

Where:

N_{BLOCKS} is the number of RAM blocks used in the design.

$F_{READ\text{-}CLOCK}$ is the memory read clock frequency.

β_2 is the RAM enable rate for read operations—guidelines are provided in Table 2-18 on page 2-19.

β_3 the RAM enable rate for write operations—guidelines are provided in Table 2-18 on page 2-19.

$F_{WRITE\text{-}CLOCK}$ is the memory write clock frequency.

Standby Mode and Time Keeping Mode

P_{MEMORY} = 0 W

PLL/CCC Dynamic Contribution—P_{PLL}

SoC Mode

$P_{PLL} = P_{AC13} * F_{CLKOUT}$

F_{CLKIN} is the input clock frequency.

F_{CLKOUT} is the output clock frequency.[1]

Standby Mode and Time Keeping Mode

1. *The PLL dynamic contribution depends on the input clock frequency, the number of output clock signals generated by the PLL, and the frequency of each output clock. If a PLL is used to generate more than one output clock, include each output clock in the formula output clock by adding its corresponding contribution (P_{AC14} * F_{CLKOUT} product) to the total PLL contribution.*

$P_{PLL} = 0$ W

Embedded Nonvolatile Memory Dynamic Contribution—P_{eNVM}

SoC Mode

The eNVM dynamic power consumption is a piecewise linear function of frequency.

$P_{eNVM} = N_{eNVM-BLOCKS} * \beta_4 * P_{AC15} * F_{READ-eNVM}$ when $F_{READ-eNVM} \leq 33$ MHz,

$P_{eNVM} = N_{eNVM-BLOCKS} * \beta_4 * (P_{AC16} + P_{AC17} * F_{READ-eNVM})$ when $F_{READ-eNVM} > 33$ MHz

Where:

$N_{eNVM-BLOCKS}$ is the number of eNVM blocks used in the design.

β_4 is the eNVM enable rate for read operations. Default is 0 (eNVM mainly in idle state).

$F_{READ-eNVM}$ is the eNVM read clock frequency.

Standby Mode and Time Keeping Mode

$P_{eNVM} = 0$ W

Main Crystal Oscillator Dynamic Contribution—$P_{XTL-OSC}$

SoC Mode

$P_{XTL-OSC} = P_{AC18}$

Standby Mode

$P_{XTL-OSC} = 0$ W

Time Keeping Mode

$P_{XTL-OSC} = 0$ W

Low Power Oscillator Crystal Dynamic Contribution—$P_{LPXTAL-OSC}$

Operating, Standby, and Time Keeping Mode

$P_{LPXTAL-OSC} = P_{AC21}$

RC Oscillator Dynamic Contribution—P_{RC-OSC}

SoC Mode

$P_{RC-OSC} = P_{AC19A} + P_{AC19B}$

Standby Mode and Time Keeping Mode

$P_{RC-OSC} = 0$ W

Analog System Dynamic Contribution—P_{AB}

SoC Mode

$P_{AB} = P_{AC23} * N_{TM} + P_{AC24} * N_{CM} + P_{AC25} * N_{ABPS} + P_{AC26} * N_{SDD} + P_{AC27} * N_{COMP} + P_{ADC} * N_{ADC} + P_{VR}$

Where:

N_{CM} is the number of current monitor blocks

N_{TM} is the number of temperature monitor blocks

N_{SDD} is the number of sigma-delta DAC blocks

N_{ABPS} is the number of ABPS blocks

N_{ADC} is the number of ADC blocks

N_{COMP} is the number of comparator blocks

$P_{VR} = P_{AC28}$

$P_{ADC} = P_{AC20A} + P_{AC20B}$

Microcontroller Subsystem Dynamic Contribution—P_{MSS}

SoC Mode

$P_{MSS} = P_{AC22}$

Guidelines

Toggle Rate Definition

A toggle rate defines the frequency of a net or logic element relative to a clock. It is a percentage. If the toggle rate of a net is 100%, this means that the net switches at half the clock frequency. Below are some examples:

- The average toggle rate of a shift register is 100%, as all flip-flop outputs toggle at half of the clock frequency.
- The average toggle rate of an 8-bit counter is 25%:
  - Bit 0 (LSB) = 100%
  - Bit 1 = 50%
  - Bit 2 = 25%
  - …
  - Bit 7 (MSB) = 0.78125%
  - Average toggle rate = (100% + 50% + 25% + 12.5% + . . . 0.78125%) / 8.

Enable Rate Definition

Output enable rate is the average percentage of time during which tristate outputs are enabled. When non-tristate output buffers are used, the enable rate should be 100%.

Table 2-17 • **Toggle Rate Guidelines Recommended for Power Calculation**

Component	Definition	Guideline
α_1	Toggle rate of VersaTile outputs	10%
α_2	I/O buffer toggle rate	10%

Table 2-18 • **Enable Rate Guidelines Recommended for Power Calculation**

Component	Definition	Guideline
β_1	I/O output buffer enable rate	Toggle rate of the logic driving the output buffer
β_2	FPGA fabric SRAM enable rate for read operations	12.5%
β_3	FPGA fabric SRAM enable rate for write operations	12.5%
β_4	eNVM enable rate for read operations	< 5%

User I/O Characteristics

Timing Model

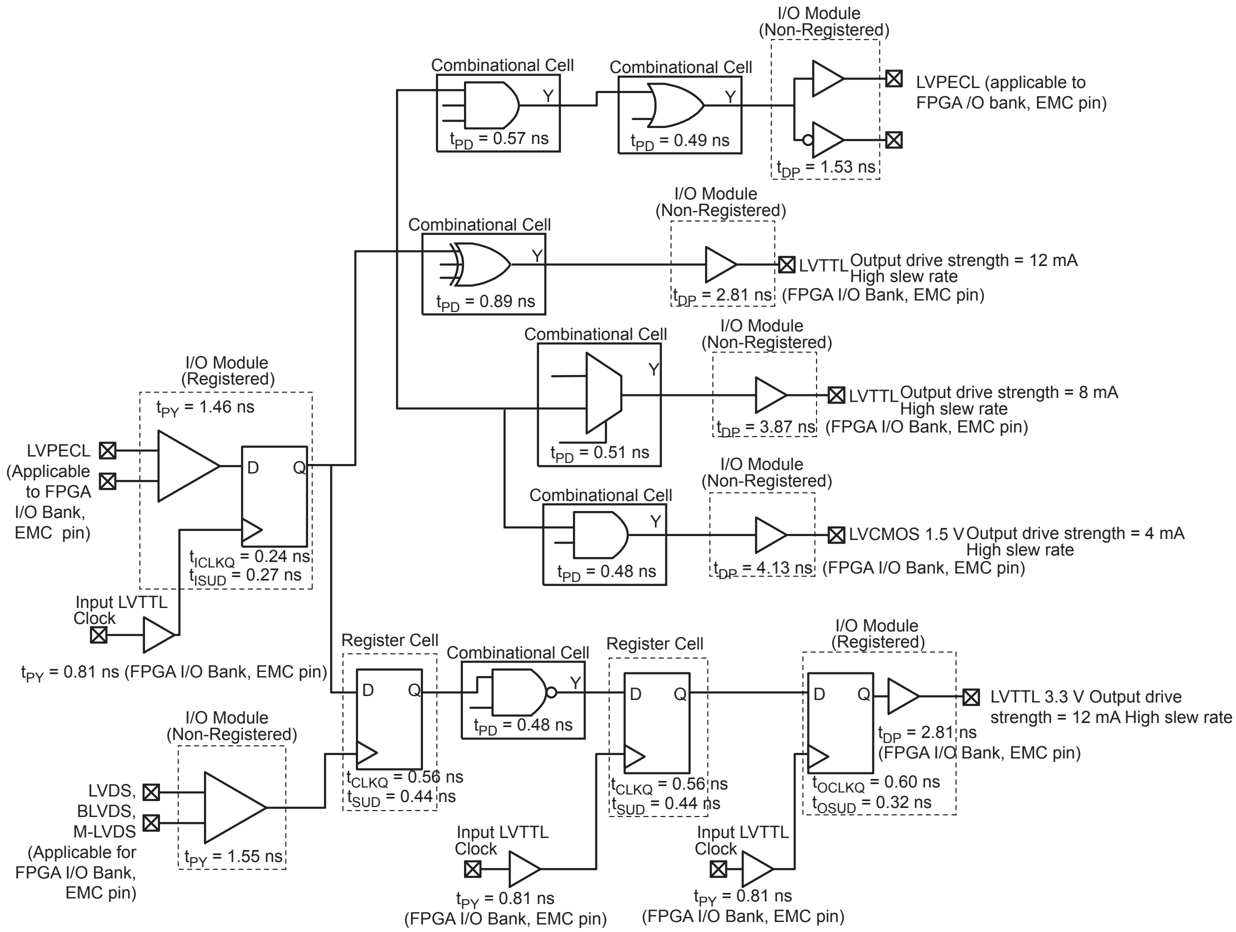


Figure 2-3 • **Timing Model**
Operating Conditions: –1 Speed, Military Temperature Range (T_J = 125°C), Worst Case VCC = 1.425 V

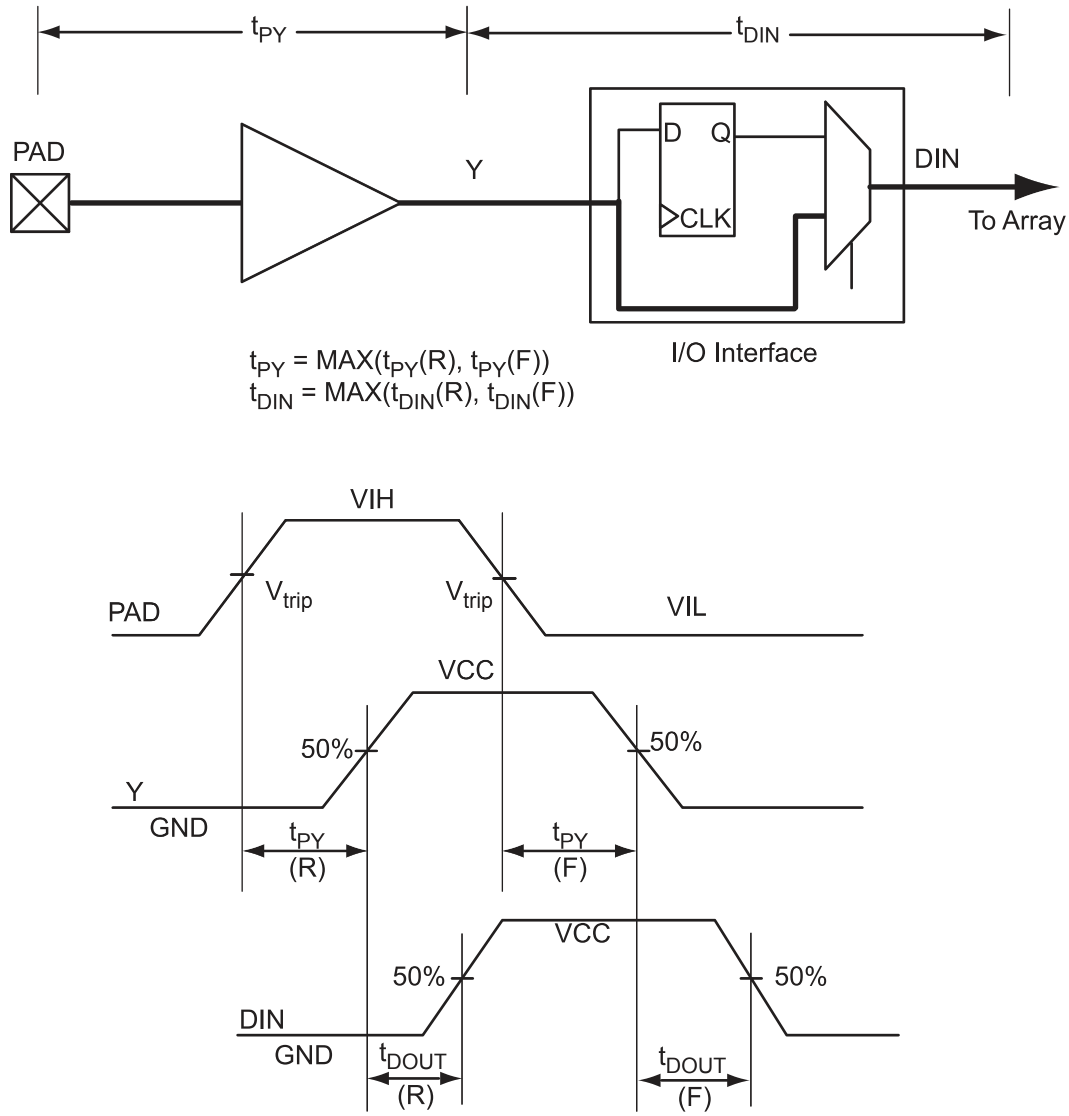


Figure 2-4 • **Input Buffer Timing Model and Delays (example)**

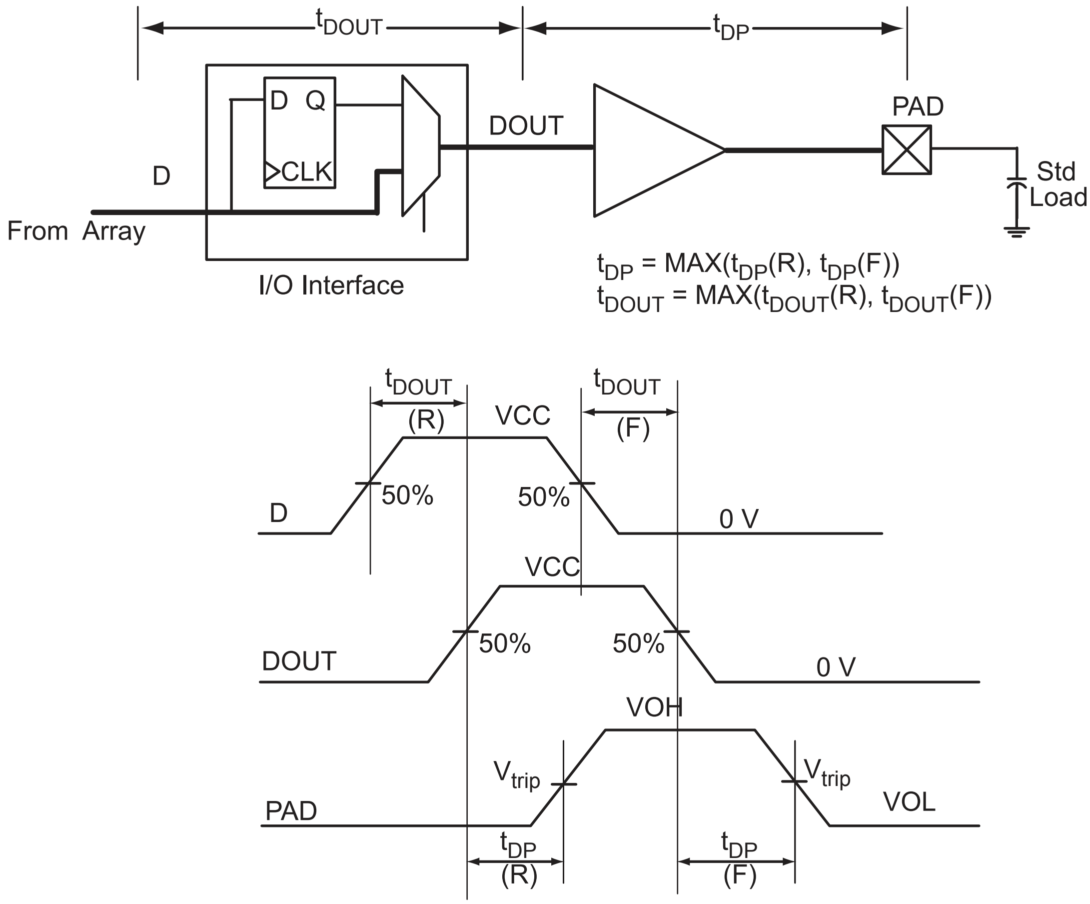


Figure 2-5 • **Output Buffer Model and Delays (example)**

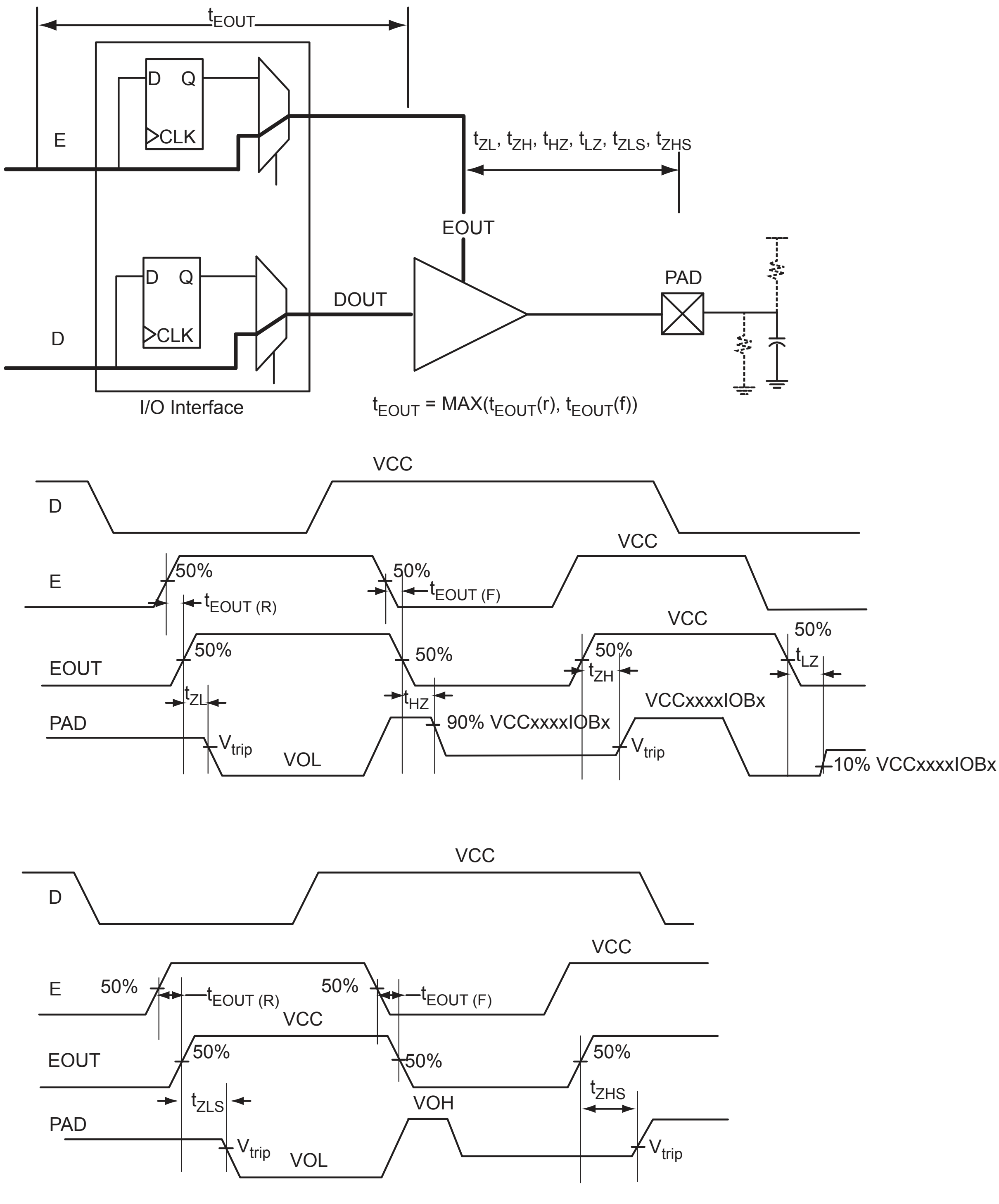


Figure 2-6 • Tristate Output Buffer Timing Model and Delays (example)

Overview of I/O Performance

Summary of I/O DC Input and Output Levels – Default I/O Software Settings

Table 2-19 • Summary of Maximum and Minimum DC Input and Output Levels Applicable to Military Conditions—Software Default Settings Applicable to FPGA I/O Banks

I/O Standard	Drive Strgth.	Slew Rate	VIL Min. V	VIL Max. V	VIH Min. V	VIH Max. V	VOL Max. V	VOH Min. V	IOL[1] mA	IOH[1] mA
3.3 V LVTTL / 3.3 V LVCMOS	12 mA	High	–0.3	0.8	2	3.6	0.4	2.4	12	12
2.5 V LVCMOS	12 mA	High	–0.3	0.7	1.7	3.6	0.7	1.7	12	12
1.8 V LVCMOS	12 mA	High	–0.3	0.35 * VCCxxxxIOBx	0.65* VCCxxxxIOBx	3.6	0.45	VCCxxxxIOBx – 0.45	12	12
1.5 V LVCMOS	12 mA	High	–0.3	0.35 * VCCxxxxIOBx	0.65* VCCxxxxIOBx	3.6	0.25 * VCCxxxxIOBx	0.75* VCCxxxxIOBx	12	12
3.3 V PCI	Per PCI specifications									
3.3 V PCI-X	Per PCI-X specifications									

Notes:

1. *Currents are measured at 125°C junction temperature.*
2. *Output slew rate can be extracted by the IBIS Models.*

Table 2-20 • Summary of Maximum and Minimum DC Input and Output Levels Applicable to Military Conditions—Software Default Settings Applicable to MSS I/O Banks

I/O Standard	Drive Strgth.	Slew Rate	VIL Min. V	VIL Max. V	VIH Min. V	VIH Max. V	VOL Max. V	VOH Min. V	IOL[1] mA	IOH[1] mA
3.3 V LVTTL / 3.3 V LVCMOS	8 mA	High	–0.3	0.8	2	3.6	0.4	2.4	8	8
2.5 V LVCMOS	8 mA	High	–0.3	0.7	1.7	3.6	0.7	1.7	8	8
1.8 V LVCMOS	4 mA	High	–0.3	0.35* VCCxxxxIOBx	0.65* VCCxxxxIOBx	3.6	0.45	VCCxxxxIOBx – 0.45	4	4
1.5 V LVCMOS	2 mA	High	–0.3	0.35* VCCxxxxIOBx	0.65* VCCxxxxIOBx	3.6	0.25* VCCxxxxIOBx	0.75* VCCxxxxIOBx	2	2

Notes:

1. *Currents are measured at 125°C junction temperature.*
2. *Output slew rate can be extracted by the IBIS Models.*

Table 2-21 • **Summary of Maximum and Minimum DC Input Levels Applicable to Military Conditions in all I/O Bank Types**

DC I/O Standards	Military*	
	IIL	IIH
	µA	µA
3.3 V LVTTL / 3.3 V LVCMOS	15	15
2.5 V LVCMOS	15	15
1.8 V LVCMOS	15	15
1.5 V LVCMOS	15	15
3.3 V PCI	15	15
3.3 V PCI-X	15	15

*Note: *Military temperature Range: –55°C to 125°C.*

Summary of I/O Timing Characteristics – Default I/O Software Settings

Table 2-22 • **Summary of AC Measuring Points Applicable to All I/O Bank Types**

Standard	Measuring Trip Point (V_{trip})
3.3 V LVTTL / 3.3 V LVCMOS	1.4 V
2.5 V LVCMOS	1.2 V
1.8 V LVCMOS	0.90 V
1.5 V LVCMOS	0.75 V
3.3 V PCI	0.285 * VCCxxxxIOBx (RR)
	0.615 * VCCxxxxIOBx (FF)
3.3 V PCI-X	0.285 * VCCxxxxIOBx (RR)
	0.615 * VCCxxxxIOBx (FF)
LVDS	Cross point
LVPECL	Cross point

Table 2-23 • **I/O AC Parameter Definitions**

Parameter	Parameter Definition
t_{DP}	Data to pad delay through the output buffer
t_{PY}	Pad to data delay through the input buffer
t_{DOUT}	Data to output buffer delay through the I/O interface
t_{EOUT}	Enable to output buffer tristate control delay through the I/O interface
t_{DIN}	Input buffer to data delay through the I/O interface
t_{HZ}	Enable to pad delay through the output buffer—High to Z
t_{ZH}	Enable to pad delay through the output buffer—Z to High
t_{LZ}	Enable to pad delay through the output buffer—Low to Z
t_{ZL}	Enable to pad delay through the output buffer—Z to Low
t_{ZHS}	Enable to pad delay through the output buffer with delayed enable—Z to High
t_{ZLS}	Enable to pad delay through the output buffer with delayed enable—Z to Low

Table 2-24 • Summary of I/O Timing Characteristics—Software Default Settings
–1 Speed Grade, Worst Military-Case Conditions: T_J = 125°C, Worst Case VCC = 1.425 V, Worst-Case VCCxxxxIOBx (per standard)
Applicable to FPGA I/O Banks, Assigned to EMC I/O Pins

I/O Standard	Drive Strength	Slew Rate	Capacitive Load (pF)	External Resistor (Ω)	t_{DOUT} (ns)	t_{DP} (ns)	t_{DIN} (ns)	t_{PY} (ns)	t_{EOUT} (ns)	t_{ZL} (ns)	t_{ZH} (ns)	t_{LZ} (ns)	t_{HZ} (ns)	t_{ZLS} (ns)	t_{ZHS} (ns)	Units
3.3 V LVTTL / 3.3 V LVCMOS	12 mA	High	35	–	0.52	3.01	0.03	0.86	0.34	3.06	2.39	2.74	3.02	4.90	4.22	ns
2.5 V LVCMOS	12 mA	High	35	–	0.52	3.03	0.03	1.10	0.34	3.09	2.88	2.81	2.90	4.93	4.72	ns
1.8 V LVCMOS	12 mA	High	35	–	0.52	3.01	0.03	1.02	0.34	3.07	2.55	3.12	3.41	4.91	4.39	ns
1.5 V LVCMOS	12 mA	High	35	–	0.52	3.47	0.03	1.20	0.34	3.54	2.98	3.32	3.50	5.37	4.82	ns
3.3 V PCI	Per PCI spec	High	10	25[1]	0.52	2.26	0.03	0.73	0.34	2.30	1.68	2.73	3.02	4.14	3.52	ns
3.3 V PCI-X	Per PCI-X spec	High	10	25[1]	0.52	2.26	0.03	0.69	0.34	2.30	1.68	2.73	3.02	4.14	3.52	ns
LVDS	24 mA	High	–	–	0.52	1.63	0.03	1.36	–	–	–	–	–	–	–	ns
LVPECL	24 mA	High	–	–	0.52	1.57	0.03	1.15	–	–	–	–	–	–	–	ns

Notes:

1. *Resistance is used to measure I/O propagation delays as defined in PCI specifications. See Figure 2-11 on page 2-41 for connectivity. This resistor is not required during normal operation.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-9 for derating values.*

Table 2-25 • Summary of I/O Timing Characteristics—Software Default Settings
–1 Speed Grade, Worst Military-Case Conditions: T_J = 125°C, Worst Case VCC = 1.425 V, Worst-Case VCCxxxxIOBx (per standard)
Applicable to MSS I/O Banks

I/O Standard	Drive Strength	Slew Rate	Capacitive Load (pF)	External Resistor	t_{DOUT} (ns)	t_{DP} (ns)	t_{DIN} (ns)	t_{PY} (ns)	t_{PYS} (ns)	t_{EOUT} (ns)	t_{ZL} (ns)	t_{ZH} (ns)	t_{LZ} (ns)	t_{HZ} (ns)	Units
3.3 V LVTTL / 3.3 V LVCMOS	8 mA	High	10	–	0.19	2.06	0.08	0.84	1.16	0.19	2.10	1.66	1.96	2.19	ns
2.5 V LVCMOS	8 mA	High	10	–	0.19	2.10	0.08	1.06	1.24	0.19	2.14	1.95	1.95	2.07	ns
1.8 V LVCMOS	4 mA	High	10	–	0.19	2.47	0.08	0.98	1.46	0.19	2.52	2.43	1.97	2.00	ns
1.5 V LVCMOS	2 mA	High	10	–	0.19	2.89	0.08	1.14	1.66	0.19	2.94	2.86	2.00	1.98	ns

Notes:

1. *Resistance is used to measure I/O propagation delays as defined in PCI specifications. See Figure 2-11 on page 2-41 for connectivity. This resistor is not required during normal operation.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-9 for derating values.*

Detailed I/O DC Characteristics

Table 2-26 • **Input Capacitance**

Symbol	Definition	Conditions	Min.	Max.	Units
C_{IN}	Input capacitance	V_{IN} = 0, f = 1.0 MHz		8	pF
C_{INCLK}	Input capacitance on the clock pin	V_{IN} = 0, f = 1.0 MHz		8	pF

Table 2-27 • **I/O Output Buffer Maximum Resistances[1] Applicable to FPGA I/O Banks**

Standard	Drive Strength	$R_{PULL-DOWN}$ (Ω)[2]	$R_{PULL-UP}$ (Ω)[3]
3.3 V LVTTL / 3.3 V LVCMOS	2 mA	100	300
	4 mA	100	300
	6 mA	50	150
	8 mA	50	150
	12 mA	25	75
	16 mA	17	50
	24 mA	11	33
2.5 V LVCMOS	2 mA	100	200
	4 mA	100	200
	6 mA	50	100
	8 mA	50	100
	12 mA	25	50
	16 mA	20	40
	24 mA	11	22
1.8 V LVCMOS	2 mA	200	225
	4 mA	100	112
	6 mA	50	56
	8 mA	50	56
	12 mA	20	22
	16 mA	20	22
1.5 V LVCMOS	2 mA	200	224
	4 mA	100	112
	6 mA	67	75
	8 mA	33	37
	12 mA	33	37
3.3 V PCI/PCI-X	Per PCI/PCI-X specification	25	75

Notes:

1. *These maximum values are provided for information only. Minimum output buffer resistance values depend on VCCxxxxIOBx, drive strength selection, temperature, and process. For board design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the Microsemi SoC Products Group website at http://www.microsemi.com/soc/download/ibis/default.aspx (also generated by the SoC Products Group Libero SoC toolset).*
2. *$R_{(PULL-DOWN-MAX)}$ = (VOLspec) / IOLspec*
3. *$R_{(PULL-UP-MAX)}$ = (VCCImax – VOHspec) / IOHspec*

Table 2-28 • I/O Output Buffer Maximum Resistances[1] Applicable to MSS I/O Banks

Standard	Drive Strength	$R_{PULL\text{-}DOWN}$ (Ω)[2]	$R_{PULL\text{-}UP}$ (Ω)[3]
3.3 V LVTTL / 3.3 V LVCMOS	8mA	50	150
2.5 V LVCMOS	8 mA	50	100
1.8 V LVCMOS	4 mA	100	112
1.5 V LVCMOS	2 mA	200	224

Notes:

1. *These maximum values are provided for informational reasons only. Minimum output buffer resistance values depend on VCCxxxxIOBx, drive strength selection, temperature, and process. For board design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the SoC Products Group website at http://www.microsemi.com/soc/download/ibis/default.aspx.*
2. $R_{(PULL\text{-}DOWN\text{-}MAX)} = (VOLspec) / IOLspec$
3. $R_{(PULL\text{-}UP\text{-}MAX)} = (VCCImax – VOHspec) / IOHspec$

Table 2-29 • I/O Weak Pull-Up/Pull-Down Resistances Minimum and Maximum Weak Pull-Up/Pull-Down Resistance Values

VCCxxxxIOBx	$R_{(WEAK\ PULL\text{-}UP)}$[1] (Ω)		$R_{(WEAK\ PULL\text{-}DOWN)}$[2] (Ω)	
	Min.	Max.	Min.	Max.
3.3 V	10 k	90 k	10 k	90 k
2.5 V	11 k	100 k	12 k	105 k
1.8 V	18 k	110 k	17 k	150 k
1.5 V	19 k	150 k	19 k	180 k

Notes:

1. $R_{(WEAK\ PULL\text{-}DOWN\text{-}MAX)} = (VOLspec) / I_{(WEAK\ PULL\text{-}DOWN\text{-}MIN)}$
2. $R_{(WEAK\ PULL\text{-}UP\text{-}MAX)} = (VCCImax – VOHspec) / I_{(WEAK\ PULL\text{-}UP\text{-}MIN)}$

Table 2-30 • I/O Short Currents IOSH/IOSL Applicable to FPGA I/O Banks

	Drive Strength	IOSL (mA)*	IOSH (mA)*
3.3 V LVTTL / 3.3 V LVCMOS	2 mA	27	25
	4 mA	27	25
	6 mA	54	51
	8 mA	54	51
	12 mA	109	103
	16 mA	127	132
	24 mA	181	268
2.5 V LVCMOS	2 mA	18	16
	4 mA	18	16
	6 mA	37	32
	8 mA	37	32
	12 mA	74	65
	16 mA	87	83
	24 mA	124	169
1.8 V LVCMOS	2 mA	11	9
	4 mA	22	17
	6 mA	44	35
	8 mA	51	45
	12 mA	74	91
	16 mA	74	91
1.5 V LVCMOS	2 mA	16	13
	4 mA	33	25
	6 mA	39	32
	8 mA	55	66
	12 mA	55	66
3.3 V PCI/PCI-X	Per PCI/PCI-X specification	109	103

*Note: *T_J = 100°C.*

Table 2-31 • I/O Short Currents IOSH/IOSL Applicable to MSS I/O Banks

	Drive Strength	I_{OSL} (mA)*	I_{OSH} (mA)*
3.3 V LVTTL / 3.3 V LVCMOS	8 mA	54	51
2.5 V LVCMOS	8 mA	37	32
1.8 V LVCMOS	4 mA	22	17
1.5 V LVCMOS	2 mA	16	13

*Note: *T_J = 100°C*

The length of time an I/O can withstand I_{OSH}/I_{OSL} events depends on the junction temperature. The reliability data below is based on a 3.3 V, 12 mA I/O setting, which is the worst case for this type of analysis.

For example, at 100°C, the short current condition would have to be sustained for more than 2200 operation hours to cause a reliability concern. The I/O design does not contain any short circuit protection, but such protection would only be needed in extremely prolonged stress conditions.

Table 2-32 • **Duration of Short Circuit Event before Failure**

Temperature	Time before Failure
–40°C	> 20 years
0°C	> 20 years
25°C	> 20 years
70°C	5 years
85°C	2 years
100°C	6 months
125°C	1 month

Table 2-33 • **Schmitt Trigger Input Hysteresis**
Hysteresis Voltage Value (typical) for Schmitt Mode Input Buffers

Input Buffer Configuration	Hysteresis Value (typical)
3.3 V LVTTL / LVCMOS / PCI / PCI-X (Schmitt trigger mode)	240 mV
2.5 V LVCMOS (Schmitt trigger mode)	140 mV
1.8 V LVCMOS (Schmitt trigger mode)	80 mV
1.5 V LVCMOS (Schmitt trigger mode)	60 mV

Table 2-34 • **I/O Input Rise Time, Fall Time, and Related I/O Reliability**

Input Buffer	Input Rise/Fall Time (min.)	Input Rise/Fall Time (max.)	Reliability
LVTTL/LVCMOS	No requirement	10 ns *	20 years (110°C)
LVDS/B-LVDS/ M-LVDS/LVPECL	No requirement	10 ns *	10 years (100°C)

*Note: *The maximum input rise/fall time is related to the noise induced into the input buffer trace. If the noise is low, then the rise time and fall time of input buffers can be increased beyond the maximum value. The longer the rise/fall times, the more susceptible the input signal is to the board noise. Microsemi SoC Products Group recommends signal integrity evaluation/characterization of the system to ensure that there is no excessive noise coupling into input signals.*

Single-Ended I/O Characteristics

3.3 V LVTTL / 3.3 V LVCMOS

Low-Voltage Transistor–Transistor Logic (LVTTL) is a general-purpose standard (EIA/JESD) for 3.3 V applications. It uses an LVTTL input buffer and push-pull output buffer.

Table 2-35 • **Minimum and Maximum DC Output Levels, 3.3 V LVTTL/ 3.3 V LVCMOS Applicable to FPGA I/O Banks**

	VOL	VOL	VOH	VOH	IOL	IOH	IOSL	IOSH
Drive Strgth.	Max. V	Max. V	Min. V		mA	mA	Max. mA[1]	Max. mA[1]
	$-55 \le T_J \le 100$ (°C)	$100 < T_J \le 125$ (°C)	$-55 \le T_J \le 100$ (°C)	$100 < T_J \le 125$ (°C)	$-55 \le T_J \le 125$ (°C)		$-55 \le T_J \le 100$ (°C)	
2 mA	0.4	0.4	2.4	2.4	2	2	27	25
4 mA	0.4	0.4	2.4	2.4	4	4	27	25
6 mA	0.4	0.4	2.4	2.4	6	6	54	51
8 mA	0.4	0.4	2.4	2.4	8	8	54	51
12 mA	0.4	0.4	2.4	2.4	12	12	109	103
16 mA	0.4	0.4	2.4	2.4	16	16	127	132
24 mA	0.4	0.44	2.4	2.16	24	24	181	268

Notes:

1. *Currents are measured at 100°C junction temperature and maximum voltage.*
2. *Software default selection highlighted in gray.*

Table 2-36 • **Minimum and Maximum DC Input Levels, 3.3 V LVTTL/ 3.3 V LVCMOS Applicable to FPGA I/O Banks**

VIL		VIH		IIL	IIH
Min. V	Max. V	Min. V	Max. V	µA*	µA*
$-55 \le T_J \le 125$ (°C)		$-55 \le T_J \le 125$ (°C)		$-55 \le T_J \le 125$ (°C)	
–0.3	0.8	2	3.6	15	15

*Note: *Currents are measured at 125°C junction temperature and maximum voltage.*

Table 2-37 • **Minimum and Maximum DC Input and Output Levels Applicable to MSS I/O Banks**

3.3 V LVTTL / 3.3 V LVCMOS	VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL	IIH
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA[1]	Max. mA[1]	µA[2]	µA[2]
8 mA	–0.3	0.8	2	3.6	0.4	2.4	8	8	54	51	15	15

Notes:

1. *Currents are measured at 100°C junction temperature and maximum voltage.*
2. *Currents are measured at 125°C junction temperature.*
3. *Software default selection highlighted in gray.*

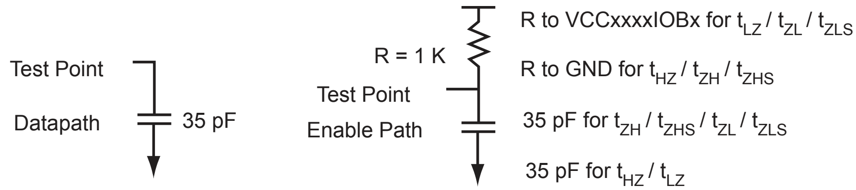


Figure 2-7 • **AC Loading**

Table 2-38 • **AC Waveforms, Measuring Points, and Capacitive Loads**

Input Low (V)	Input High (V)	Measuring Point* (V)	V_{REF} (typ.) (V)	C_{LOAD} (pF)
0	3.3	1.4	–	35

Note: **Measuring point = $V_{trip.}$ See Table 2-22 on page 2-25 for a complete table of trip points.*

Timing Characteristics

Table 2-39 • **3.3 V LVTTL / 3.3 V LVCMOS High Slew**
Worst Military-Case Conditions: T_J = 125°C, Worst-Case VCC = 1.425 V,
Worst-Case VCCxxxxIOBx = 3.0 V
Applicable to FPGA I/O Banks, I/O Assigned to EMC I/O Pins

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	Std.	0.62	7.71	0.04	1.04	0.41	7.85	6.61	2.70	2.64	10.06	8.82	ns
	–1	0.52	6.43	0.03	0.86	0.34	6.55	5.51	2.25	2.20	8.38	7.35	ns
8 mA	Std.	0.62	4.97	0.04	1.04	0.41	5.06	4.11	3.05	3.24	7.27	6.31	ns
	–1	0.52	4.14	0.03	0.86	0.34	4.22	3.42	2.54	2.70	6.05	5.26	ns
12 mA	Std.	0.62	3.61	0.04	1.04	0.41	3.68	2.86	3.28	3.63	5.88	5.07	ns
	–1	0.52	3.01	0.03	0.86	0.34	3.06	2.39	2.74	3.02	4.90	4.22	ns
16 mA	Std.	0.62	3.41	0.04	1.04	0.41	3.47	2.60	3.33	3.72	5.67	4.81	ns
	–1	0.52	2.84	0.03	0.86	0.34	2.89	2.17	2.78	3.10	4.73	4.01	ns
24 mA	Std.	0.62	3.14	0.04	1.04	0.41	3.20	2.17	3.39	4.10	5.40	4.38	ns
	–1	0.52	2.62	0.03	0.86	0.34	2.67	1.81	2.83	3.41	4.50	3.65	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-9 for derating values.*

Table 2-40 • **3.3 V LVTTL / 3.3 V LVCMOS Low Slew**
Worst Military-Case Conditions: T_J = 125°C, Worst-Case VCC = 1.425 V,
Worst-Case VCCxxxxIOBx = 3.0 V
Applicable to FPGA I/O Banks, I/O Assigned to EMC I/O Pins

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	Std.	0.62	10.44	0.04	1.04	0.41	10.63	8.80	2.70	2.48	12.83	11.01	ns
	–1	0.52	8.70	0.03	0.86	0.34	8.86	7.34	2.25	2.07	10.70	9.17	ns
8 mA	Std.	0.62	7.45	0.04	1.04	0.41	7.59	6.27	3.04	3.08	9.79	8.47	ns
	–1	0.52	6.21	0.03	0.86	0.34	6.32	5.22	2.54	2.56	8.16	7.06	ns
12 mA	Std.	0.62	5.73	0.04	1.04	0.41	5.84	4.90	3.28	3.46	8.04	7.11	ns
	–1	0.52	4.78	0.03	0.86	0.34	4.87	4.09	2.73	2.88	6.70	5.92	ns
16 mA	Std.	0.62	5.36	0.04	1.04	0.41	5.46	4.60	3.33	3.56	7.67	6.81	ns
	–1	0.52	4.47	0.03	0.86	0.34	4.55	3.83	2.77	2.97	6.39	5.67	ns
24 mA	Std.	0.62	5.00	0.04	1.04	0.41	5.09	4.58	3.39	3.92	7.29	6.79	ns
	–1	0.52	4.16	0.03	0.86	0.34	4.24	3.82	2.82	3.27	6.08	5.66	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-9 for derating values.

Table 2-41 • **3.3 V LVTTL / 3.3 V LVCMOS High Slew**
Worst Military-Case Conditions: T_J = 125°C, Worst-Case VCC = 1.425 V,
Worst-Case VCCxxxxIOBx = 3.0 V
Applicable to MSS I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
8 mA	Std.	0.23	2.47	0.09	1.00	1.40	0.23	2.52	1.99	2.35	2.62	ns
	–1	0.19	2.06	0.08	0.84	1.16	0.19	2.10	1.66	1.96	2.19	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-9 for derating values.*

2.5 V LVCMOS

Low-Voltage CMOS for 2.5 V is an extension of the LVCMOS standard (JESD8-5) used for general-purpose 2.5 V applications.

Table 2-42 • Minimum and Maximum DC Input and Output Levels Applicable to FPGA I/O Banks

2.5 V LVCMOS	VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL	IIH
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA[1]	Max. mA[1]	μA[2]	μA[2]
2 mA	–0.3	0.7	1.7	2.7	0.7	1.7	2	2	18	16	15	15
4 mA	–0.3	0.7	1.7	2.7	0.7	1.7	4	4	18	16	15	15
6 mA	–0.3	0.7	1.7	2.7	0.7	1.7	6	6	37	32	15	15
8 mA	–0.3	0.7	1.7	2.7	0.7	1.7	8	8	37	32	15	15
12 mA	–0.3	0.7	1.7	2.7	0.7	1.7	12	12	74	65	15	15
16 mA	–0.3	0.7	1.7	2.7	0.7	1.7	16	16	87	83	15	15
24 mA	–0.3	0.7	1.7	2.7	0.7	1.7	24	24	124	169	15	15

Notes:

1. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
2. *Currents are measured at 125°C junction temperature.*
3. *Software default selection highlighted in gray.*

Table 2-43 • Minimum and Maximum DC Input and Output Levels Applicable to MSS I/O Banks

2.5 V LVCMOS	VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL	IIH
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA[1]	Max., mA[1]	μA[2]	μA[2]
8 mA	–0.3	0.7	1.7	3.6	0.7	1.7	8	8	37	32	15	15

Notes:

1. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
2. *Currents are measured at 125°C junction temperature.*
3. *Software default selection highlighted in gray.*

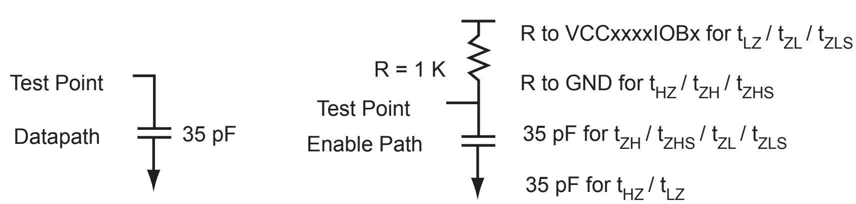


Figure 2-8 • AC Loading

Table 2-44 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	V_{REF} (typ.) (V)	C_{LOAD} (pF)
0	2.5	1.2	–	35

Note: *Measuring point = Vtrip. See Table 2-22 on page 2-25 for a complete table of trip points.

Timing Characteristics

Table 2-45 • 2.5 V LVCMOS High Slew
Worst Military-Case Conditions: T_J = 125°C, Worst-Case VCC = 1.425 V, Worst-Case VCCxxxxIOBx = 2.3 V
Applicable to FPGA I/O Banks, I/O Assigned to EMC I/O Pins

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	Std.	0.57	8.67	0.04	1.32	0.41	7.89	8.67	2.72	2.32	10.09	10.87	ns
	–1	0.47	7.22	0.03	1.10	0.34	6.57	7.22	2.27	1.94	8.41	9.06	ns
8 mA	Std.	0.57	5.19	0.04	1.32	0.41	5.10	5.19	3.11	3.03	7.30	7.40	ns
	–1	0.47	4.33	0.03	1.10	0.34	4.25	4.33	2.59	2.52	6.09	6.16	ns
12 mA	Std.	0.62	3.64	0.04	1.32	0.41	3.71	3.46	3.37	3.47	5.91	5.66	ns
	–1	0.52	3.03	0.03	1.10	0.34	3.09	2.88	2.81	2.90	4.93	4.72	ns
16 mA	Std.	0.62	3.44	0.04	1.32	0.41	3.50	3.09	3.43	3.59	5.70	5.29	ns
	–1	0.52	2.86	0.03	1.10	0.34	2.92	2.57	2.85	2.99	4.75	4.41	ns
24 mA	Std.	0.62	3.16	0.04	1.32	0.41	3.22	2.48	3.50	4.03	5.43	4.68	ns
	–1	0.52	2.64	0.03	1.10	0.34	2.68	2.06	2.92	3.35	4.52	3.90	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-9 for derating values.*

Table 2-46 • 2.5 V LVCMOS Low Slew
Worst Military-Case Conditions: T_J = 125°C, Worst-Case VCC = 1.425 V, Worst-Case VCCxxxxIOBx = 2.3 V
Applicable to FPGA I/O Banks, I/O Assigned to EMC I/O Pins

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	Std.	0.57	11.25	0.04	1.32	0.41	11.45	11.25	2.72	2.22	13.65	13.45	ns
	–1	0.47	9.37	0.03	1.10	0.34	9.54	9.37	2.27	1.85	11.37	11.21	ns
8 mA	Std.	0.57	8.15	0.04	1.32	0.41	8.30	7.73	3.11	2.92	10.50	9.94	ns
	–1	0.47	6.79	0.03	1.10	0.34	6.92	6.44	2.59	2.43	8.75	8.28	ns
12 mA	Std.	0.62	6.34	0.04	1.32	0.41	6.46	5.91	3.37	3.36	8.66	8.11	ns
	–1	0.52	5.28	0.03	1.10	0.34	5.38	4.92	2.81	2.80	7.22	6.76	ns
16 mA	Std.	0.62	5.92	0.04	1.32	0.41	6.03	5.52	3.42	3.48	8.23	7.72	ns
	–1	0.52	4.93	0.03	1.10	0.34	5.02	4.60	2.85	2.90	6.86	6.43	ns
24 mA	Std.	0.62	5.55	0.04	1.32	0.41	5.65	5.51	3.50	3.90	7.86	7.71	ns
	–1	0.52	4.62	0.03	1.10	0.34	4.71	4.59	2.92	3.25	6.55	6.43	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-9 for derating values.

Table 2-47 • 2.5 V LVCMOS High Slew
Worst Military-Case Conditions: T_J = 125°C, Worst-Case VCC = 1.425 V, Worst-Case VCCxxxxIOBx = 2.3 V
Applicable to MSS I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
8 mA	Std.	0.23	2.52	0.09	1.27	1.49	0.23	2.57	2.34	2.34	2.48	ns
	–1	0.19	2.10	0.08	1.06	1.24	0.19	2.14	1.95	1.95	2.07	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-9 for derating values.*

1.8 V LVCMOS

Low-voltage CMOS for 1.8 V is an extension of the LVCMOS standard (JESD8-5) used for general-purpose 1.8 V applications. It uses a 1.8 V input buffer and a push-pull output buffer.

Table 2-48 • Minimum and Maximum DC Input and Output Levels Applicable to FPGA I/O Banks

1.8 V LVCMOS	VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL	IIH
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA[1]	Max. mA[1]	µA[2]	µA[2]
2 mA	–0.3	0.35 * VCCxxxxIOBx	0.65 * VCCxxxxIOBx	1.9	0.45	VCCxxxxIOBx – 0.45	2	2	11	9	15	15
4 mA	–0.3	0.35 * VCCxxxxIOBx	0.65 * VCCxxxxIOBx	1.9	0.45	VCCxxxxIOBx – 0.45	4	4	22	17	15	15
6 mA	–0.3	0.35 * VCCxxxxIOBx	0.65 * VCCxxxxIOBx	1.9	0.45	VCCxxxxIOBx – 0.45	6	6	44	35	15	15
8 mA	–0.3	0.35 * VCCxxxxIOBx	0.65 * VCCxxxxIOBx	1.9	0.45	VCCxxxxIOBx – 0.45	8	8	51	45	15	15
12 mA	–0.3	0.35 * VCCxxxxIOBx	0.65 * VCCxxxxIOBx	1.9	0.45	VCCxxxxIOBx – 0.45	12	12	74	91	15	15
16 mA	–0.3	0.35 * VCCxxxxIOBx	0.65 * VCCxxxxIOBx	1.9	0.45	VCCxxxxIOBx – 0.45	16	16	74	91	15	15

Notes:

1. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
2. *Currents are measured at 125°C junction temperature.*
3. *Software default selection highlighted in gray.*

Table 2-49 • Minimum and Maximum DC Input and Output Levels Applicable to MSS I/O Banks

1.8 V LVCMOS	VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL	IIH
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA[1]	Max. mA[1]	µA[2]	µA[2]
4 mA	–0.3	0.35 * VCCxxxxIOBx	0.65 * VCCxxxxIOBx	3.6	0.45	VCCxxxxIOBx – 0.45	4	4	22	17	15	15

Notes:

1. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
2. *Currents are measured at 125°C junction temperature.*
3. *Software default selection highlighted in gray.*

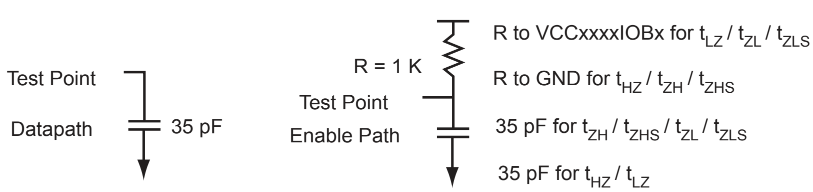


Figure 2-9 • AC Loading

Table 2-50 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	V_{REF} (typ.) (V)	C_{LOAD} (pF)
0	1.8	0.9	–	35

Note: *Measuring point = Vtrip. See Table 2-22 on page 2-25 for a complete table of trip points.

Timing Characteristics

Table 2-51 • 1.8 V LVCMOS High Slew
Worst Military-Case Conditions: T_J = 125°C, Worst-Case VCC = 1.425 V,
Worst-Case VCCxxxxIOBx = 1.7 V
Applicable to FPGA I/O Banks, I/O Assigned to EMC I/O Pins

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.62	11.85	0.04	1.22	0.41	9.22	11.85	2.80	1.70	11.42	14.05	ns
	–1	0.52	9.87	0.03	1.02	0.34	7.68	9.87	2.33	1.42	9.52	11.71	ns
4 mA	Std.	0.62	6.91	0.04	1.22	0.41	5.92	6.91	3.26	2.85	8.13	9.12	ns
	–1	0.52	5.76	0.03	1.02	0.34	4.94	5.76	2.72	2.38	6.77	7.60	ns
6 mA	Std.	0.62	4.46	0.04	1.22	0.41	4.27	4.46	3.58	3.40	6.48	6.66	ns
	–1	0.52	3.71	0.03	1.02	0.34	3.56	3.71	2.98	2.84	5.40	5.55	ns
8 mA	Std.	0.62	3.95	0.04	1.22	0.41	4.02	3.93	3.65	3.55	6.23	6.14	ns
	–1	0.52	3.29	0.03	1.02	0.34	3.35	3.28	3.04	2.96	5.19	5.12	ns
12 mA	Std.	0.62	3.62	0.04	1.22	0.41	3.68	3.06	3.75	4.09	5.89	5.26	ns
	–1	0.52	3.01	0.03	1.02	0.34	3.07	2.55	3.12	3.41	4.91	4.39	ns
16 mA	Std.	0.62	3.62	0.04	1.22	0.41	3.68	3.06	3.75	4.09	5.89	5.26	ns
	–1	0.52	3.01	0.03	1.02	0.34	3.07	2.55	3.12	3.41	4.91	4.39	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-9 for derating values.*

Table 2-52 • 1.8 V LVCMOS Low Slew
Worst Military-Case Conditions: T_J = 125°C, Worst-Case VCC = 1.425 V,
Worst-Case VCCxxxxIOBx = 1.7 V
Applicable to FPGA I/O Banks, I/O Assigned to EMC I/O Pins

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.62	15.25	0.04	1.22	0.41	14.43	15.25	2.80	1.65	16.63	17.46	ns
	–1	0.52	12.71	0.03	1.02	0.34	12.02	12.71	2.34	1.37	13.86	14.55	ns
4 mA	Std.	0.62	10.43	0.04	1.22	0.41	10.62	10.31	3.27	2.75	12.82	12.51	ns
	–1	0.52	8.69	0.03	1.02	0.34	8.85	8.59	2.72	2.29	10.69	10.42	ns
6 mA	Std.	0.62	8.21	0.04	1.22	0.41	8.36	7.75	3.58	3.30	10.57	9.96	ns
	–1	0.52	6.84	0.03	1.02	0.34	6.97	6.46	2.98	2.75	8.81	8.30	ns
8 mA	Std.	0.62	7.66	0.04	1.22	0.41	7.80	7.22	3.65	3.44	10.01	9.43	ns
	–1	0.52	6.38	0.03	1.02	0.34	6.50	6.02	3.04	2.87	8.34	7.86	ns
12 mA	Std.	0.62	7.24	0.04	1.22	0.41	7.38	7.23	3.75	3.96	9.58	9.43	ns
	–1	0.52	6.04	0.03	1.02	0.34	6.15	6.02	3.13	3.30	7.98	7.86	ns
16 mA	Std.	0.62	7.24	0.04	1.22	0.41	7.38	7.23	3.75	3.96	9.58	9.43	ns
	–1	0.52	6.04	0.03	1.02	0.34	6.15	6.02	3.13	3.30	7.98	7.86	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-9 for derating values.

Table 2-53 • 1.8 V LVCMOS High Slew
Worst Military-Case Conditions: T_J = 125°C, Worst-Case VCC = 1.425 V, Worst-Case VCCxxxxIOBx = 1.7 V
Applicable to MSS I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
4 mA	Std.	0.23	2.97	0.09	1.17	1.75	0.23	3.02	2.92	2.36	2.41	ns
	–1	0.19	2.47	0.08	0.98	1.46	0.19	2.52	2.43	1.97	2.00	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-9 for derating values.*

1.5 V LVCMOS (JESD8-11)

Low-Voltage CMOS for 1.5 V is an extension of the LVCMOS standard (JESD8-5) used for general-purpose 1.5 V applications. It uses a 1.5 V input buffer and a push-pull output buffer.

Table 2-54 • Minimum and Maximum DC Input and Output Levels Applicable to FPGA I/O Banks

1.5 V LVCMOS	VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL	IIH
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA[1]	Max. mA[1]	µA[2]	µA[2]
2 mA	–0.3	0.35 * VCCxxxxIOBx	0.65 * VCCxxxxIOBx	1.575	0.25* VCCxxxxIOBx	0.75 * VCCxxxxIOBx	2	2	16	13	15	15
4 mA	–0.3	0.35* VCCxxxxIOBx	0.65 * VCCxxxxIOBx	1.575	0.25* VCCxxxxIOBx	0.75 * VCCxxxxIOBx	4	4	33	25	15	15
6 mA	–0.3	0.35 * VCCxxxxIOBx	0.65 * VCCxxxxIOBx	1.575	0.25* VCCxxxxIOBx	0.75 * VCCxxxxIOBx	6	6	39	32	15	15
8 mA	–0.3	0.35 * VCCxxxxIOBx	0.65 * VCCxxxxIOBx	1.575	0.25* VCC	0.75 * VCCxxxxIOBx	8	8	55	66	15	15
12 mA	–0.3	0.35 * VCCxxxxIOBx	0.65 * VCCxxxxIOBx	1.575	0.25 * VCCxxxxIOBx	0.75 * VCCxxxxIOBx	12	12	55	66	15	15

Notes:

1. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
2. *Currents are measured at 125°C junction temperature.*
3. *Software default selection highlighted in gray.*

Table 2-55 • Minimum and Maximum DC Input and Output Levels Applicable to MSS I/O Banks

1.5 V LVCMOS	VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL	IIH
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA[1]	Max. mA[1]	µA[2]	µA[2]
2 mA	–0.3	0.35 * VCCxxxxIOBx	0.65 * VCCxxxxIOBx	1.575	0.25 * VCCxxxxIOBx	0.75 * VCCxxxxIOBx	2	2	16	13	15	15

Notes:

1. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
2. *Currents are measured at 125°C junction temperature.*
3. *Software default selection highlighted in gray.*

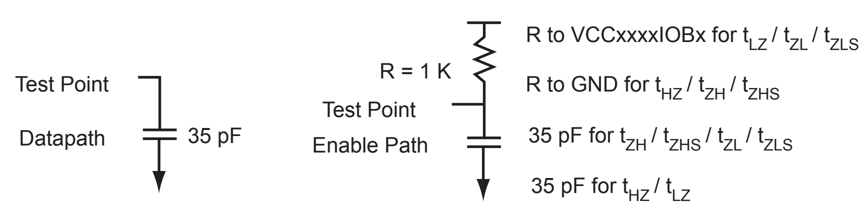


Figure 2-10 • AC Loading

Table 2-56 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	V_{REF} (typ.) (V)	C_{LOAD} (pF)
0	1.5	0.75	–	35

Note: *Measuring point = Vtrip. See Table 2-22 on page 2-25 for a complete table of trip points.

Timing Characteristics

Table 2-57 • **1.5 V LVCMOS High Slew**
Worst Military-Case Conditions: T_J = 125°C, Worst-Case VCC = 1.425 V,
Worst-Case VCCxxxxIOBx = 1.4 V
Applicable to FPGA I/O Banks, I/O Assigned to EMC I/O Pins

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 m	Std.	0.62	8.35	0.04	1.44	0.41	6.89	8.35	3.42	2.77	9.09	10.55	ns
	–1	0.52	6.95	0.03	1.20	0.34	5.74	6.95	2.85	2.31	7.58	8.79	ns
4 mA	Std.	0.62	5.31	0.04	1.44	0.41	4.94	5.31	3.78	3.41	7.15	7.51	ns
	–1	0.52	4.42	0.03	1.20	0.34	4.12	4.42	3.15	2.85	5.95	6.26	ns
6 mA	Std.	0.62	4.67	0.04	1.44	0.41	4.65	4.67	3.86	3.58	6.85	6.88	ns
	–1	0.52	3.89	0.03	1.20	0.34	3.87	3.89	3.22	2.98	5.71	5.73	ns
8 mA	Std.	0.62	4.17	0.04	1.44	0.41	4.24	3.58	3.98	4.20	6.45	5.78	ns
	–1	0.52	3.47	0.03	1.20	0.34	3.54	2.98	3.32	3.50	5.37	4.82	ns
12 mA	Std.	0.62	4.17	0.04	1.44	0.41	4.24	3.58	3.98	4.20	6.45	5.78	ns
	–1	0.52	3.47	0.03	1.20	0.34	3.54	2.98	3.32	3.50	5.37	4.82	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-9 for derating values.*

Table 2-58 • **1.5 V LVCMOS Low Slew**
Worst Military-Case Conditions: T_J = 85°C, Worst-Case VCC = 1.425 V,
Worst-Case VCCxxxxIOBx = 1.4 V
Applicable to FPGA I/O Banks, I/O Assigned to EMC I/O Pins

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	Std.	0.62	12.80	0.04	1.44	0.41	13.04	12.53	3.43	2.65	15.24	14.73	ns
	–1	0.52	10.67	0.03	1.20	0.34	10.87	10.44	2.86	2.21	12.70	12.28	ns
4 mA	Std.	0.62	10.18	0.04	1.44	0.41	10.37	9.38	3.79	3.28	12.57	11.59	ns
	–1	0.52	8.48	0.03	1.20	0.34	8.64	7.82	3.16	2.74	10.48	9.66	ns
6 mA	Std.	0.62	9.49	0.04	1.44	0.41	9.67	8.75	3.87	3.45	11.87	10.95	ns
	–1	0.52	7.91	0.03	1.20	0.34	8.05	7.29	3.22	2.87	9.89	9.13	ns
8 mA	Std.	0.62	9.04	0.04	1.44	0.41	9.21	8.76	3.99	4.05	11.41	10.96	ns
	–1	0.52	7.53	0.03	1.20	0.34	7.67	7.30	3.33	3.37	9.51	9.13	ns
12 mA	Std.	0.62	9.04	0.04	1.44	0.41	9.21	8.76	3.99	4.05	11.41	10.96	ns
	–1	0.52	7.53	0.03	1.20	0.34	7.67	7.30	3.33	3.37	9.51	9.13	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-9 for derating values.

Table 2-59 • **1.5 V LVCMOS High Slew**
Worst Military-Case Conditions: T_J = 85°C, Worst-Case VCC = 1.4 25 V,
Worst-Case VCCxxxxIOBx = 1.4 V
Applicable to MSS I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{PYS}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	Units
2 mA	Std.	0.23	3.47	0.09	1.37	2.00	0.23	3.53	3.43	2.40	2.37	ns
	–1	0.19	2.89	0.08	1.14	1.66	0.19	2.94	2.86	2.00	1.98	ns

Notes:

1. *Software default selection highlighted in gray.*
2. *For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-9 for derating values.*

3.3 V PCI, 3.3 V PCI-X

Peripheral Component Interface for 3.3 V standard specifies support for 33 MHz and 66 MHz PCI Bus applications.

Table 2-60 • **Minimum and Maximum DC Input and Output Levels**

3.3 V PCI/PCI-X	VIL		VIH		VOL	VOH	IOL	IOH	IOSL	IOSH	IIL	IIH
Drive Strength	Min. V	Max. V	Min. V	Max. V	Max. V	Min. V	mA	mA	Max. mA[1]	Max. mA[1]	µA[2]	µA[2]
Per PCI specification	Per PCI curves										15	15

Notes:

1. *Currents are measured at high temperature (100°C junction temperature) and maximum voltage.*
2. *Currents are measured at 125°C junction temperature.*

AC loadings are defined per the PCI/PCI-X specifications for the datapath; SoC Products Group loadings for enable path characterization are described in Figure 2-11.

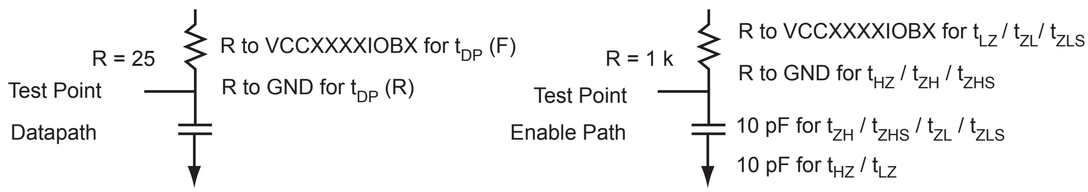


Figure 2-11 • **AC Loading**

AC loadings are defined per PCI/PCI-X specifications for the datapath; SoC Products Group loading for tristate is described in Table 2-61.

Table 2-61 • **AC Waveforms, Measuring Points, and Capacitive Loads**

Input Low (V)	Input High (V)	Measuring Point* (V)	V_{REF} (typ.) (V)	C_{LOAD} (pF)
0	3.3	0.285 * VCCxxxxIOBx for $t_{DP(R)}$ 0.615 * VCCxxxxIOBx for $t_{DP(F)}$	–	10

*Note: *Measuring point = Vtrip. See Table 2-22 on page 2-25 for a complete table of trip points.*

Timing Characteristics

Table 2-62 • **3.3 V PCI**
Worst Military-Case Conditions: T_J = 125°C, Worst-Case VCC = 1.425 V,
Worst-Case VCCxxxxIOBx = 3.0 V
Applicable to FPGA I/O Banks, I/O Assigned to EMC I/O Pins

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	0.62	2.72	0.04	0.88	0.41	2.77	2.02	3.28	3.62	4.97	4.22	ns
–1	0.52	2.26	0.03	0.73	0.34	2.30	1.68	2.73	3.02	4.14	3.52	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-9 for derating values.

Table 2-63 • **3.3 V PCI-X**
Worst Military-Case Conditions: T_J =125°C, Worst-Case VCC = 1.425 V,
Worst-Case VCCxxxxIOBx = 3.0 V
Applicable to FPGA I/O Banks, I/O Assigned to EMC I/O Pins

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	0.62	2.72	0.04	0.83	0.41	2.77	2.02	3.28	3.62	4.97	4.22	ns
–1	0.52	2.26	0.03	0.69	0.34	2.30	1.68	2.73	3.02	4.14	3.52	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-9 for derating values.

Differential I/O Characteristics

Physical Implementation

Configuration of the I/O modules as a differential pair is handled by SoC Products Group Designer software when the user instantiates a differential I/O macro in the design.

Differential I/Os can also be used in conjunction with the embedded Input Register (InReg), Output Register (OutReg), Enable Register (EnReg), and Double Data Rate (DDR). However, there is no support for bidirectional I/Os or tristates with the LVPECL standards.

LVDS

Low-Voltage Differential Signaling (ANSI/TIA/EIA-644) is a high-speed, differential I/O standard. It requires that one data bit be carried through two signal lines, so two pins are needed. It also requires external resistor termination.

The full implementation of the LVDS transmitter and receiver is shown in an example in Figure 2-12. The building blocks of the LVDS transmitter-receiver are one transmitter macro, one receiver macro, three board resistors at the transmitter end, and one resistor at the receiver end. The values for the three driver resistors are different from those used in the LVPECL implementation because the output standard specifications are different.

Along with LVDS I/O, SmartFusion cSoCs also support bus LVDS structure and multipoint LVDS (M-LVDS) configuration (up to 40 nodes).

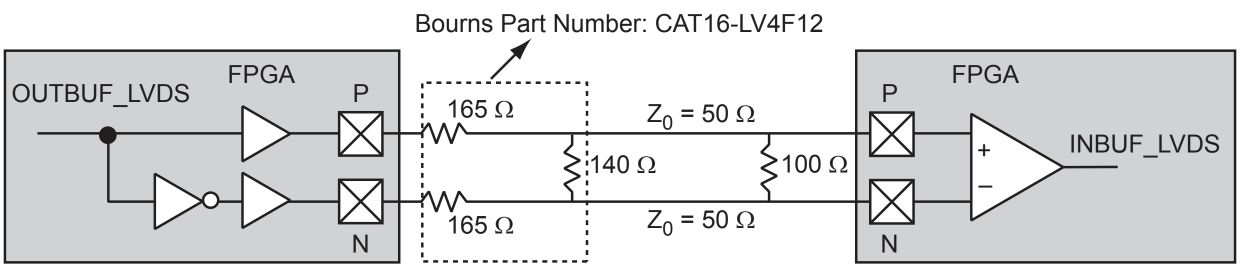


Figure 2-12 • **LVDS Circuit Diagram and Board-Level Implementation**

Table 2-64 • LVDS Minimum and Maximum DC Input and Output Levels

DC Parameter	Description	Min.	Typ.	Max.	Units
VCCFPGAIOBx	Supply voltage	2.375	2.5	2.625	V
VOL	Output low voltage	0.9	1.075	1.25	V
VOH	Output high voltage	1.25	1.425	1.6	V
I_{OL}[1]	Output lower current	0.65	0.91	1.16	mA
I_{OH}[1]	Output high current	0.65	0.91	1.16	mA
VI	Input voltage	0		2.925	V
I_{IH}[2]	Input high leakage current			15	µA
I_{IL}[2]	Input low leakage current			15	µA
V_{ODIFF}	Differential output voltage	250	350	450	mV
V_{OCM}	Output common mode voltage	1.125	1.25	1.375	V
V_{ICM}	Input common mode voltage	0.05	1.25	2.35	V
V_{IDIFF}	Input differential voltage	100	350		mV

Notes:

1. *IOL/IOH defined by VODIFF/(resistor network).*
2. *Currents are measured at 125°C junction temperature.*

Table 2-65 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	V_{REF} (typ.) (V)
1.075	1.325	Cross point	–

*Note: *Measuring point = Vtrip. See Table 2-22 on page 2-25 for a complete table of trip points.*

Timing Characteristics

Table 2-66 • LVDS
Worst Military-Case Conditions: T_J = 125°C, Worst-Case VCC = 1.425 V,
Worst-Case VCCFPGAIOBx = 2.3 V
Applicable to FPGA I/O Banks, I/O Assigned to EMC I/O Pins

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	Units
Std.	0.62	1.96	0.04	1.63	ns
–1	0.52	1.63	0.03	1.36	ns

Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-9 for derating values.

B-LVDS/M-LVDS

Bus LVDS (B-LVDS) and Multipoint LVDS (M-LVDS) specifications extend the existing LVDS standard to high-performance multipoint bus applications. Multidrop and multipoint bus configurations may contain any combination of drivers, receivers, and transceivers. SoC Products Group LVDS drivers provide the higher drive current required by B-LVDS and M-LVDS to accommodate the loading. The drivers require series terminations for better signal quality and to control voltage swing. Termination is also required at both ends of the bus since the driver can be located anywhere on the bus. These configurations can be implemented using the TRIBUF_LVDS and BIBUF_LVDS macros along with appropriate terminations. Multipoint designs using SoC Products Group LVDS macros can achieve up to 200 MHz with a maximum of 20 loads. A sample application is given in Figure 2-13. The input and output buffer delays are available in the LVDS section in Table 2-66.

Example: For a bus consisting of 20 equidistant loads, the following terminations provide the required differential voltage, in worst-case military operating conditions, at the farthest receiver: R_S = 60 Ω and R_T = 70 Ω, given Z_0 = 50 Ω (2") and Z_{stub} = 50 Ω (~1.5").

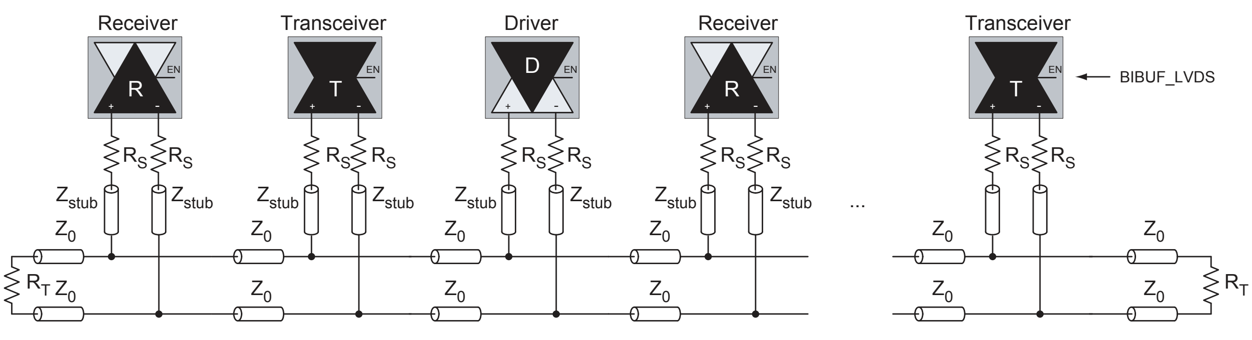


Figure 2-13 **• B-LVDS/M-LVDS Multipoint Application Using LVDS I/O Buffers**

LVPECL

Low-Voltage Positive Emitter-Coupled Logic (LVPECL) is another differential I/O standard. It requires that one data bit be carried through two signal lines. Like LVDS, two pins are needed. It also requires external resistor termination.

The full implementation of the LVDS transmitter and receiver is shown in an example in Figure 2-14. The building blocks of the LVPECL transmitter-receiver are one transmitter macro, one receiver macro, three board resistors at the transmitter end, and one resistor at the receiver end. The values for the three driver resistors are different from those used in the LVDS implementation because the output standard specifications are different.

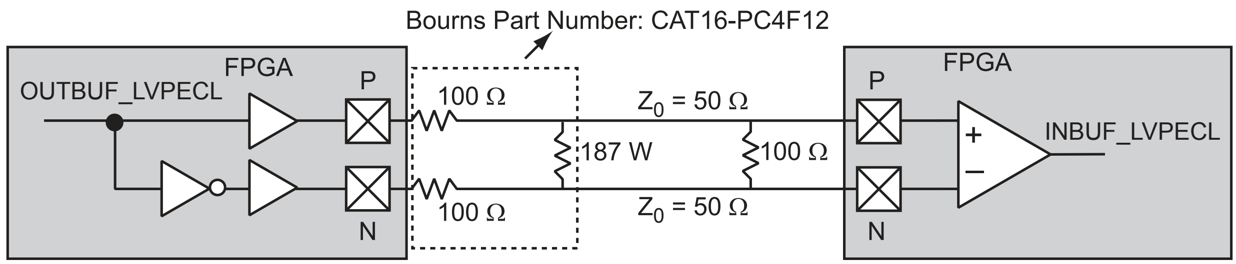


Figure 2-14 • LVPECL Circuit Diagram and Board-Level Implementation

Table 2-67 • Minimum and Maximum DC Input and Output Levels

DC Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	Units
VCCFPGAIOBx	Supply Voltage	3.0		3.3		3.6		V
VOL	Output Low Voltage	0.96	1.27	1.06	1.43	1.30	1.57	V
VOH	Output High Voltage	1.8	2.11	1.92	2.28	2.13	2.41	V
VIL, VIH	Input Low, Input High Voltages	0	3.6	0	3.6	0	3.6	V
VODIFF	Differential Output Voltage	0.625	0.97	0.625	0.97	0.625	0.97	V
VOCM	Output Common-Mode Voltage	1.762	1.98	1.762	1.98	1.762	1.98	V
VICM	Input Common-Mode Voltage	1.01	2.57	1.01	2.57	1.01	2.57	V
VIDIFF	Input Differential Voltage	300		300		300		mV

Table 2-68 • AC Waveforms, Measuring Points, and Capacitive Loads

Input Low (V)	Input High (V)	Measuring Point* (V)	V_{REF} (typ.) (V)
1.64	1.94	Cross point	–

*Note: *Measuring point = Vtrip. See Table 2-22 on page 2-25 for a complete table of trip points.*

Timing Characteristics

Table 2-69 • LVPECL
Worst Military-Case Conditions: T_J = 125°C, Worst-Case VCC = 1.425 V, Worst-Case VCCFPGAIOBx = 3.0 V
Applicable to FPGA I/O Banks, I/O Assigned to EMC I/O Pins

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	Units
Std.	0.62	1.88	0.04	1.38	ns
–1	0.52	1.57	0.03	1.15	ns

Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-9 for derating values.

I/O Register Specifications

Fully Registered I/O Buffers with Synchronous Enable and Asynchronous Preset

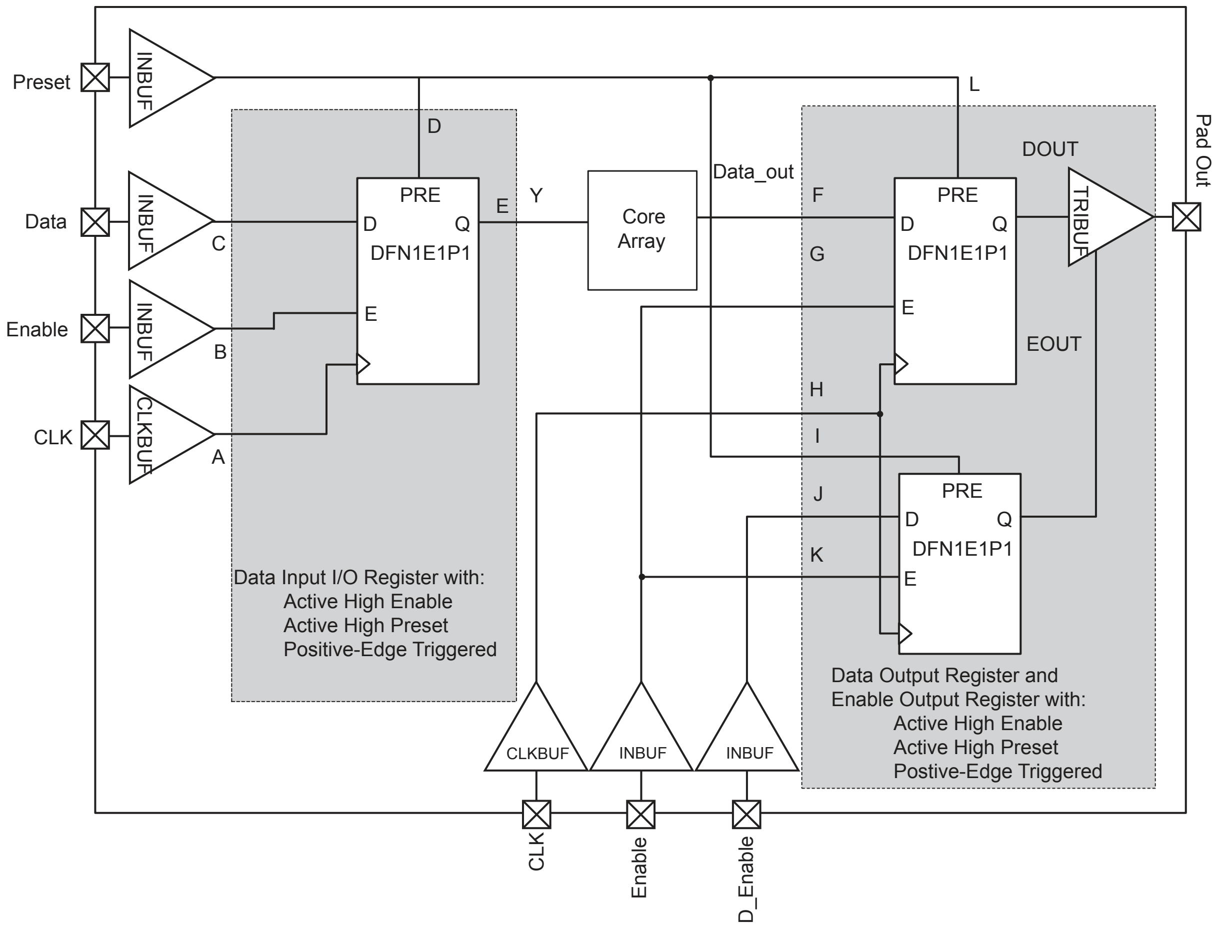


Figure 2-15 • **Timing Model of Registered I/O Buffers with Synchronous Enable and Asynchronous Preset**

Table 2-70 • **Parameter Definition and Measuring Nodes**

Parameter Name	Parameter Definition	Measuring Nodes (from, to)*
t_{OCLKQ}	Clock-to-Q of the Output Data Register	H, DOUT
t_{OSUD}	Data Setup Time for the Output Data Register	F, H
t_{OHD}	Data Hold Time for the Output Data Register	F, H
t_{OSUE}	Enable Setup Time for the Output Data Register	G, H
t_{OHE}	Enable Hold Time for the Output Data Register	G, H
t_{OPRE2Q}	Asynchronous Preset-to-Q of the Output Data Register	L, DOUT
$t_{OREMPRE}$	Asynchronous Preset Removal Time for the Output Data Register	L, H
$t_{ORECPRE}$	Asynchronous Preset Recovery Time for the Output Data Register	L, H
t_{OECLKQ}	Clock-to-Q of the Output Enable Register	H, EOUT
t_{OESUD}	Data Setup Time for the Output Enable Register	J, H
t_{OEHD}	Data Hold Time for the Output Enable Register	J, H
t_{OESUE}	Enable Setup Time for the Output Enable Register	K, H
t_{OEHE}	Enable Hold Time for the Output Enable Register	K, H
$t_{OEPRE2Q}$	Asynchronous Preset-to-Q of the Output Enable Register	I, EOUT
$t_{OEREMPRE}$	Asynchronous Preset Removal Time for the Output Enable Register	I, H
$t_{OERECPRE}$	Asynchronous Preset Recovery Time for the Output Enable Register	I, H
t_{ICLKQ}	Clock-to-Q of the Input Data Register	A, E
t_{ISUD}	Data Setup Time for the Input Data Register	C, A
t_{IHD}	Data Hold Time for the Input Data Register	C, A
t_{ISUE}	Enable Setup Time for the Input Data Register	B, A
t_{IHE}	Enable Hold Time for the Input Data Register	B, A
t_{IPRE2Q}	Asynchronous Preset-to-Q of the Input Data Register	D, E
$t_{IREMPRE}$	Asynchronous Preset Removal Time for the Input Data Register	D, A
$t_{IRECPRE}$	Asynchronous Preset Recovery Time for the Input Data Register	D, A

*Note: *See Figure 2-15 on page 2-46 for more information.*

Fully Registered I/O Buffers with Synchronous Enable and Asynchronous Clear

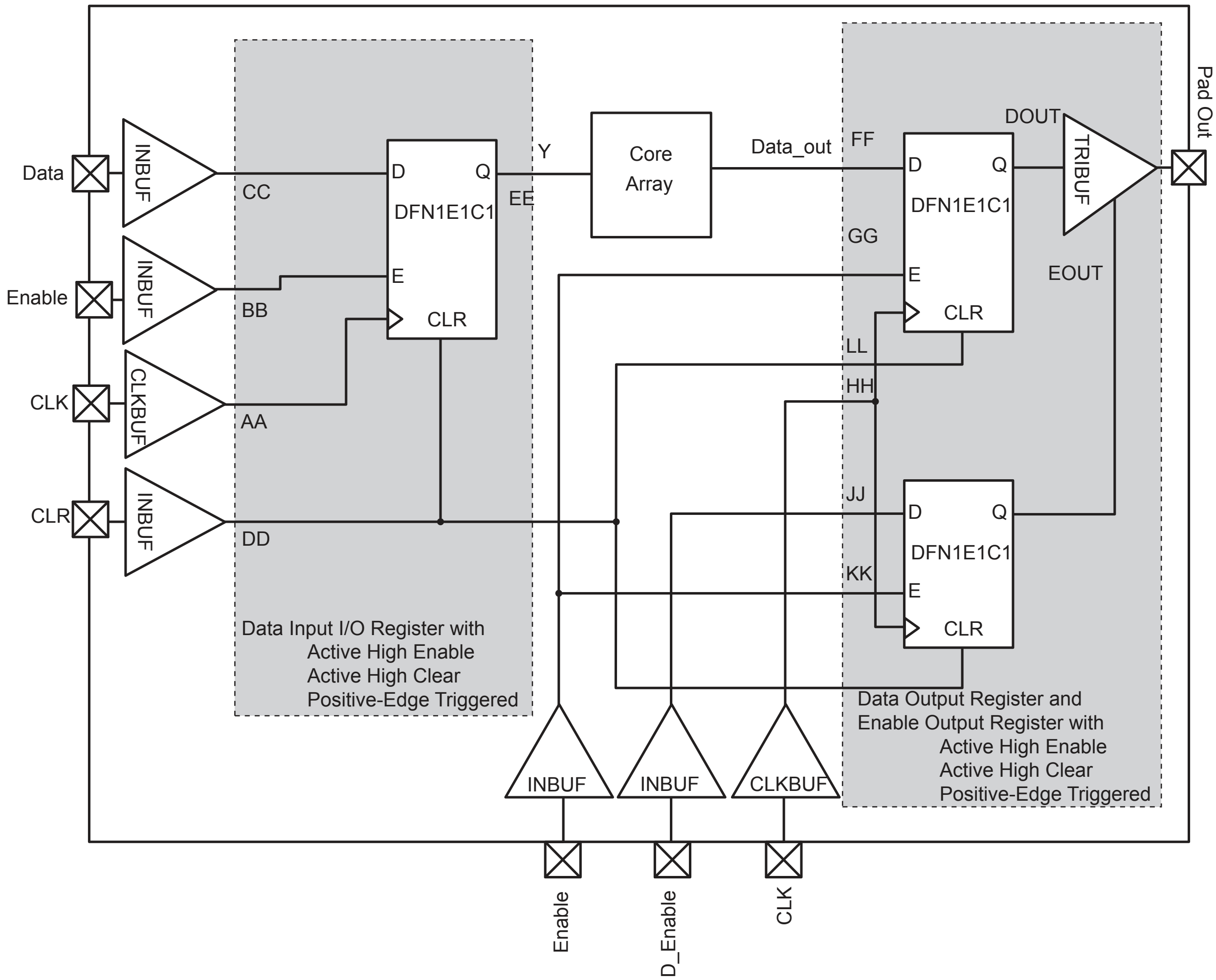


Figure 2-16 • **Timing Model of the Registered I/O Buffers with Synchronous Enable and Asynchronous Clear**

Table 2-71 • **Parameter Definition and Measuring Nodes**

Parameter Name	Parameter Definition	Measuring Nodes (from, to)*
t_{OCLKQ}	Clock-to-Q of the Output Data Register	HH, DOUT
t_{OSUD}	Data Setup Time for the Output Data Register	FF, HH
t_{OHD}	Data Hold Time for the Output Data Register	FF, HH
t_{OSUE}	Enable Setup Time for the Output Data Register	GG, HH
t_{OHE}	Enable Hold Time for the Output Data Register	GG, HH
t_{OCLR2Q}	Asynchronous Clear-to-Q of the Output Data Register	LL, DOUT
$t_{OREMCLR}$	Asynchronous Clear Removal Time for the Output Data Register	LL, HH
$t_{ORECCLR}$	Asynchronous Clear Recovery Time for the Output Data Register	LL, HH
t_{OECLKQ}	Clock-to-Q of the Output Enable Register	HH, EOUT
t_{OESUD}	Data Setup Time for the Output Enable Register	JJ, HH
t_{OEHD}	Data Hold Time for the Output Enable Register	JJ, HH
t_{OESUE}	Enable Setup Time for the Output Enable Register	KK, HH
t_{OEHE}	Enable Hold Time for the Output Enable Register	KK, HH
$t_{OECLR2Q}$	Asynchronous Clear-to-Q of the Output Enable Register	II, EOUT
$t_{OEREMCLR}$	Asynchronous Clear Removal Time for the Output Enable Register	II, HH
$t_{OERECCLR}$	Asynchronous Clear Recovery Time for the Output Enable Register	II, HH
t_{ICLKQ}	Clock-to-Q of the Input Data Register	AA, EE
t_{ISUD}	Data Setup Time for the Input Data Register	CC, AA
t_{IHD}	Data Hold Time for the Input Data Register	CC, AA
t_{ISUE}	Enable Setup Time for the Input Data Register	BB, AA
t_{IHE}	Enable Hold Time for the Input Data Register	BB, AA
t_{ICLR2Q}	Asynchronous Clear-to-Q of the Input Data Register	DD, EE
$t_{IREMCLR}$	Asynchronous Clear Removal Time for the Input Data Register	DD, AA
$t_{IRECCLR}$	Asynchronous Clear Recovery Time for the Input Data Register	DD, AA

Note: *See Figure 2-16 on page 2-48 for more information.

Input Register

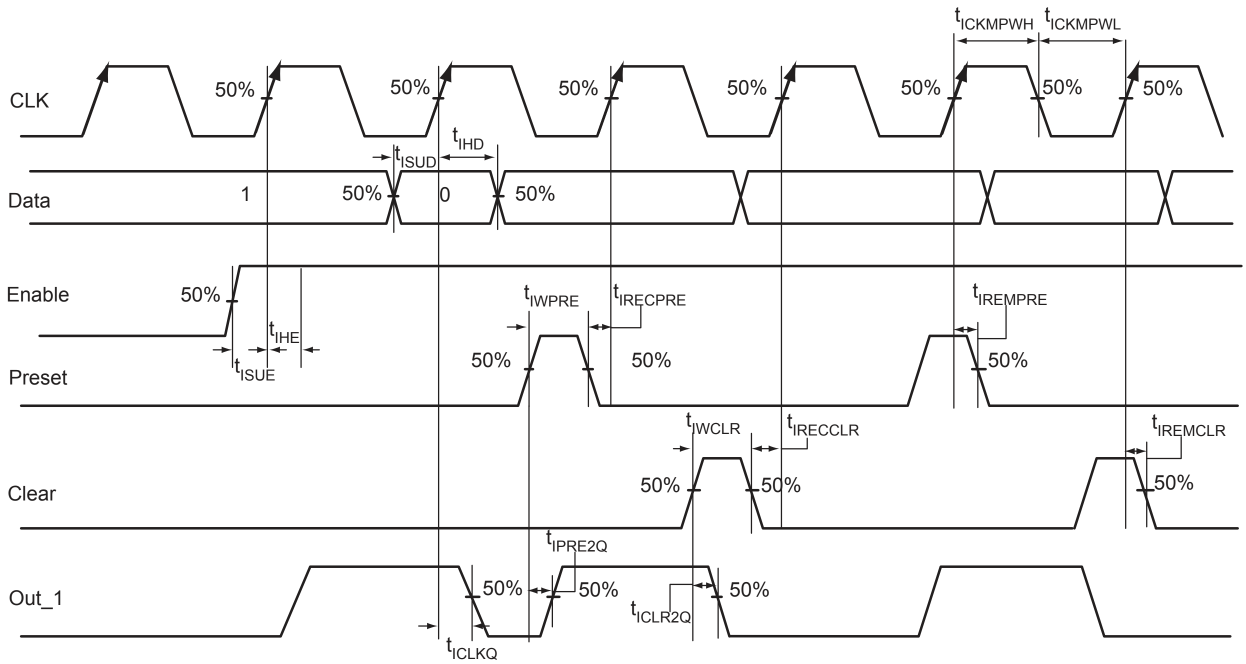


Figure 2-17 • **Input Register Timing Diagram**

Timing Characteristics

Table 2-72 • **Input Data Register Propagation Delays**
Worst Military-Case Conditions: T_J = 125°C, Worst-Case VCC = 1.425 V

Parameter	Description	–1	Std.	Units
t_{ICLKQ}	Clock-to-Q of the Input Data Register	0.25	0.30	ns
t_{ISUD}	Data Setup Time for the Input Data Register	0.28	0.33	ns
t_{IHD}	Data Hold Time for the Input Data Register	0.00	0.00	ns
t_{ISUE}	Enable Setup Time for the Input Data Register	0.39	0.47	ns
t_{IHE}	Enable Hold Time for the Input Data Register	0.00	0.00	ns
t_{ICLR2Q}	Asynchronous Clear-to-Q of the Input Data Register	0.48	0.58	ns
t_{IPRE2Q}	Asynchronous Preset-to-Q of the Input Data Register	0.48	0.58	ns
$t_{IREMCLR}$	Asynchronous Clear Removal Time for the Input Data Register	0.00	0.00	ns
$t_{IRECCLR}$	Asynchronous Clear Recovery Time for the Input Data Register	0.24	0.28	ns
$t_{IREMPRE}$	Asynchronous Preset Removal Time for the Input Data Register	0.00	0.00	ns
$t_{IRECPRE}$	Asynchronous Preset Recovery Time for the Input Data Register	0.24	0.28	ns
t_{IWCLR}	Asynchronous Clear Minimum Pulse Width for the Input Data Register	0.22	0.26	ns
t_{IWPRE}	Asynchronous Preset Minimum Pulse Width for the Input Data Register	0.22	0.26	ns
$t_{ICKMPWH}$	Clock Minimum Pulse Width High for the Input Data Register	0.36	0.42	ns
$t_{ICKMPWL}$	Clock Minimum Pulse Width Low for the Input Data Register	0.32	0.38	ns

Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-9 for derating values.

Output Register

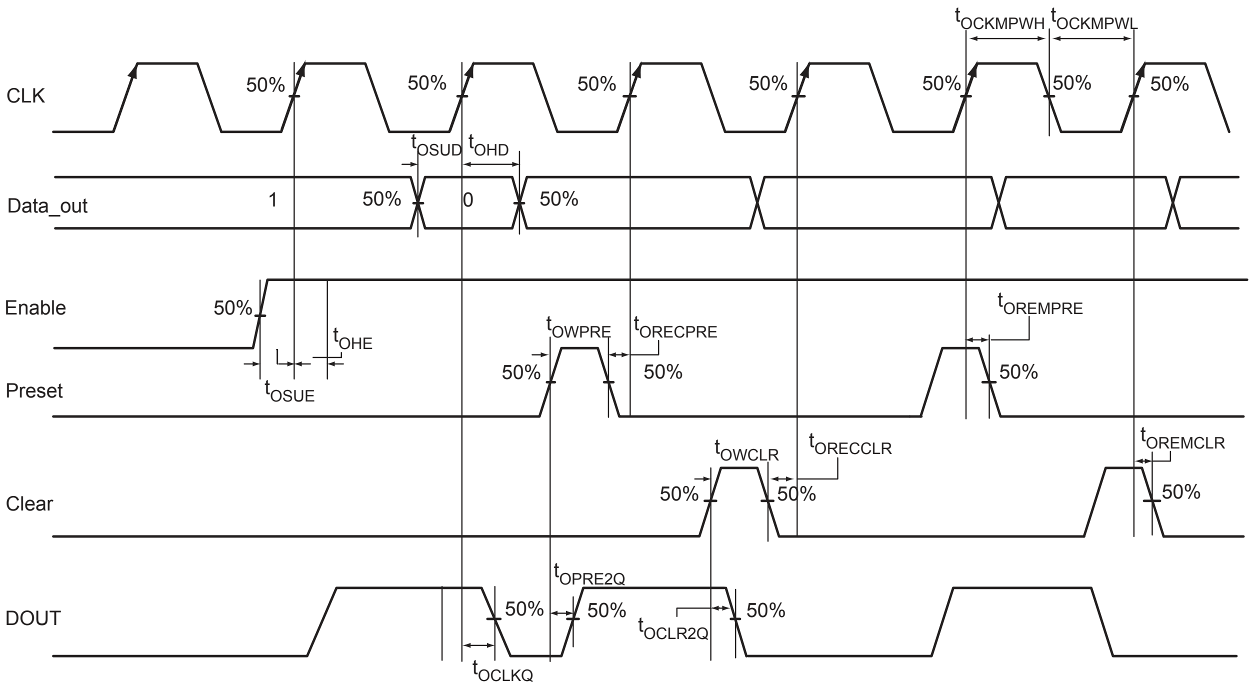


Figure 2-18 **• Output Register Timing Diagram**

Timing Characteristics

Table 2-73 **• Output Data Register Propagation Delays**
Worst Military-Case Conditions: T_J = 125°C, Worst-Case VCC = 1.425 V

Parameter	Description	–1	Std.	Units
t_{OCLKQ}	Clock-to-Q of the Output Data Register	0.62	0.75	ns
t_{OSUD}	Data Setup Time for the Output Data Register	0.33	0.40	ns
t_{OHD}	Data Hold Time for the Output Data Register	0.00	0.00	ns
t_{OSUE}	Enable Setup Time for the Output Data Register	0.46	0.56	ns
t_{OHE}	Enable Hold Time for the Output Data Register	0.00	0.00	ns
t_{OCLR2Q}	Asynchronous Clear-to-Q of the Output Data Register	0.85	1.02	ns
t_{OPRE2Q}	Asynchronous Preset-to-Q of the Output Data Register	0.85	1.02	ns
$t_{OREMCLR}$	Asynchronous Clear Removal Time for the Output Data Register	0.00	0.00	ns
$t_{ORECCLR}$	Asynchronous Clear Recovery Time for the Output Data Register	0.24	0.28	ns
$t_{OREMPRE}$	Asynchronous Preset Removal Time for the Output Data Register	0.00	0.00	ns
$t_{ORECPRE}$	Asynchronous Preset Recovery Time for the Output Data Register	0.24	0.28	ns
t_{OWCLR}	Asynchronous Clear Minimum Pulse Width for the Output Data Register	0.22	0.26	ns
t_{OWPRE}	Asynchronous Preset Minimum Pulse Width for the Output Data Register	0.22	0.26	ns
$t_{OCKMPWH}$	Clock Minimum Pulse Width High for the Output Data Register	0.36	0.42	ns
$t_{OCKMPWL}$	Clock Minimum Pulse Width Low for the Output Data Register	0.32	0.38	ns

Note: For the derating values at specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-9 for derating values.

Output Enable Register

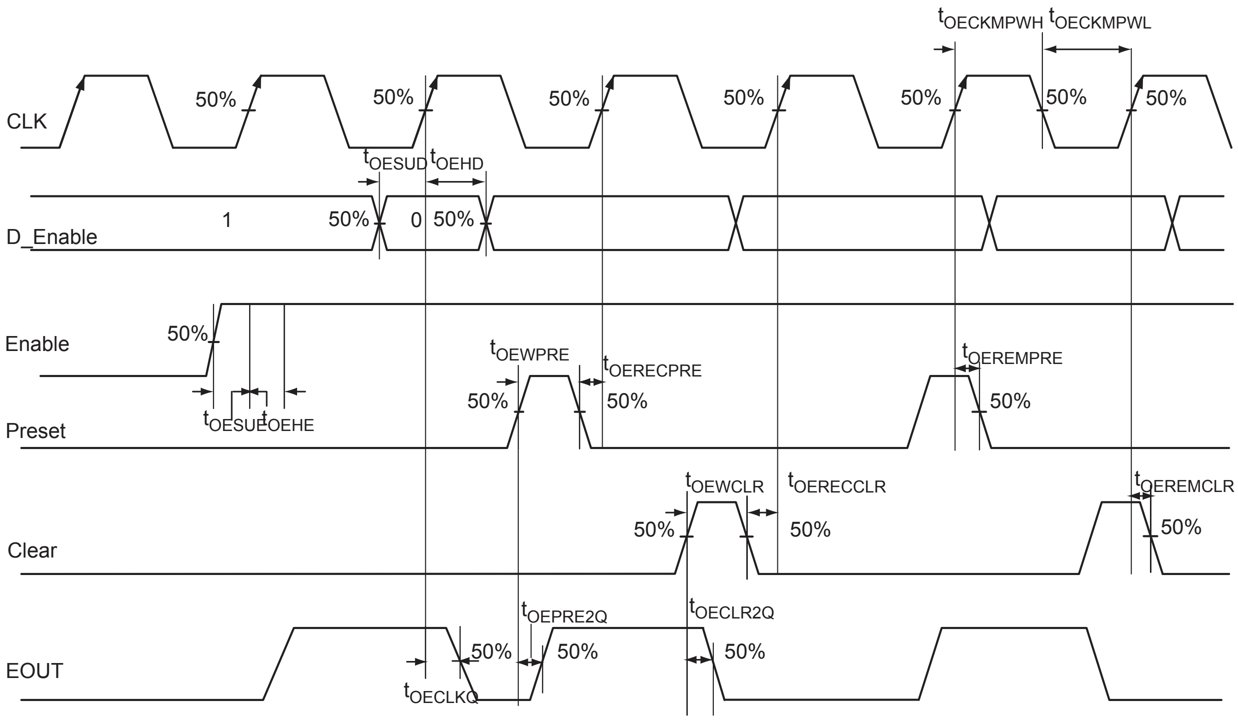


Figure 2-19 • **Output Enable Register Timing Diagram**

Timing Characteristics

Table 2-74 • **Output Enable Register Propagation Delays**
Worst Military-Case Conditions: T_J = 125°C, Worst-Case VCC = 1.425 V

Parameter	Description	–1	Std.	Units
t_{OECLKQ}	Clock-to-Q of the Output Enable Register	0.47	0.56	ns
t_{OESUD}	Data Setup Time for the Output Enable Register	0.33	0.40	ns
t_{OEHD}	Data Hold Time for the Output Enable Register	0.00	0.00	ns
t_{OESUE}	Enable Setup Time for the Output Enable Register	0.46	0.55	ns
t_{OEHE}	Enable Hold Time for the Output Enable Register	0.00	0.00	ns
$t_{OECLR2Q}$	Asynchronous Clear-to-Q of the Output Enable Register	0.70	0.84	ns
$t_{OEPRE2Q}$	Asynchronous Preset-to-Q of the Output Enable Register	0.70	0.84	ns
$t_{OEREMCLR}$	Asynchronous Clear Removal Time for the Output Enable Register	0.00	0.00	ns
$t_{OERECCLR}$	Asynchronous Clear Recovery Time for the Output Enable Register	0.24	0.28	ns
$t_{OEREMPRE}$	Asynchronous Preset Removal Time for the Output Enable Register	0.00	0.00	ns
$t_{OERECPRE}$	Asynchronous Preset Recovery Time for the Output Enable Register	0.24	0.28	ns
t_{OEWCLR}	Asynchronous Clear Minimum Pulse Width for the Output Enable Register	0.22	0.26	ns
t_{OEWPRE}	Asynchronous Preset Minimum Pulse Width for the Output Enable Register	0.22	0.26	ns
$t_{OECKMPWH}$	Clock Minimum Pulse Width High for the Output Enable Register	0.36	0.42	ns
$t_{OECKMPWL}$	Clock Minimum Pulse Width Low for the Output Enable Register	0.32	0.38	ns

Note: For specific junction temperature and voltage supply levels, refer to *Table 2-7 on page 2-9* *for derating values.*

DDR Module Specifications

Input DDR Module

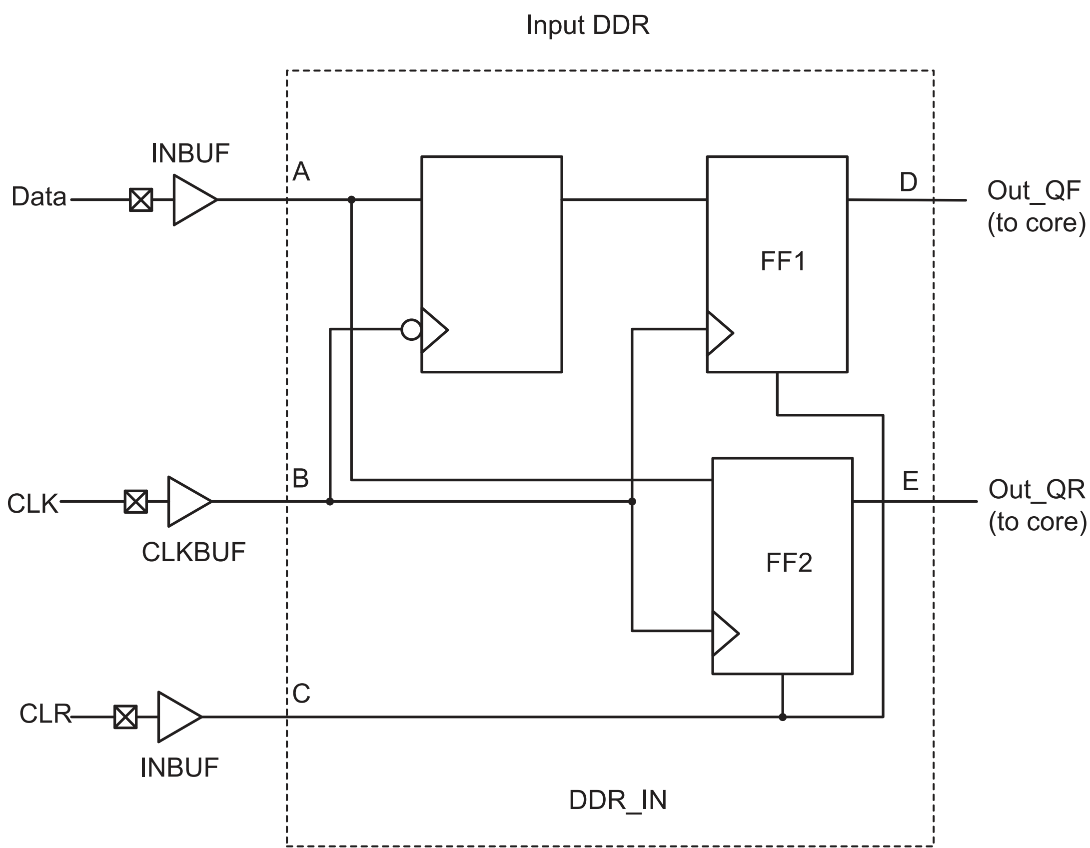


***Figure 2-20* • Input DDR Timing Model**

***Table 2-75* • Parameter Definitions**

Parameter Name	Parameter Definition	Measuring Nodes (from, to)
$t_{DDRICLKQ1}$	Clock-to-Out Out_QR	B, D
$t_{DDRICLKQ2}$	Clock-to-Out Out_QF	B, E
$t_{DDRISUD}$	Data Setup Time of DDR input	A, B
t_{DDRIHD}	Data Hold Time of DDR input	A, B
$t_{DDRICLR2Q1}$	Clear-to-Out Out_QR	C, D
$t_{DDRICLR2Q2}$	Clear-to-Out Out_QF	C, E
$t_{DDRIREMCLR}$	Clear Removal	C, B
$t_{DDRIRECCLR}$	Clear Recovery	C, B

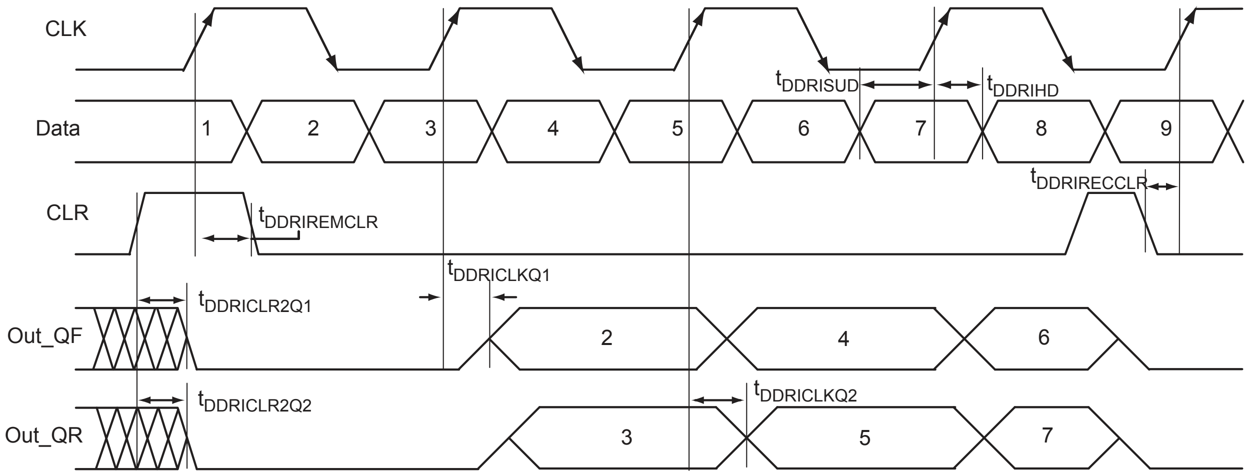


Figure 2-21 • **Input DDR Timing Diagram**

Timing Characteristics

Table 2-76 • **Input DDR Propagation Delays**
Worst Military-Case Conditions: T_J = 85°C, Worst Case VCC = 1.425 V

Parameter	Description	–1	Std.	Units
$t_{DDRICLKQ1}$	Clock-to-Out Out_QR for Input DDR	0.41	0.49	ns
$t_{DDRICLKQ2}$	Clock-to-Out Out_QF for Input DDR	0.29	0.35	ns
$t_{DDRISUD}$	Data Setup for Input DDR	0.30	0.36	ns
t_{DDRIHD}	Data Hold for Input DDR	0.00	0.00	ns
$t_{DDRICLR2Q1}$	Asynchronous Clear-to-Out Out_QR for Input DDR	0.60	0.72	ns
$t_{DDRICLR2Q2}$	Asynchronous Clear-to-Out Out_QF for Input DDR	0.49	0.59	ns
$t_{DDRIREMCLR}$	Asynchronous Clear Removal time for Input DDR	0.00	0.00	ns
$t_{DDRIRECCLR}$	Asynchronous Clear Recovery time for Input DDR	0.24	0.28	ns
$t_{DDRIWCLR}$	Asynchronous Clear Minimum Pulse Width for Input DDR	0.22	0.26	ns
$t_{DDRICKMPWH}$	Clock Minimum Pulse Width High for Input DDR	0.36	0.42	ns
$t_{DDRICKMPWL}$	Clock Minimum Pulse Width Low for Input DDR	0.32	0.38	ns
$F_{DDRIMAX}$	Maximum Frequency for Input DDR	350	350	MHz

Note: For derating values at specific junction temperature and voltage-supply levels, refer to Table 2-7 on page 2-9 for derating values.

Output DDR Module

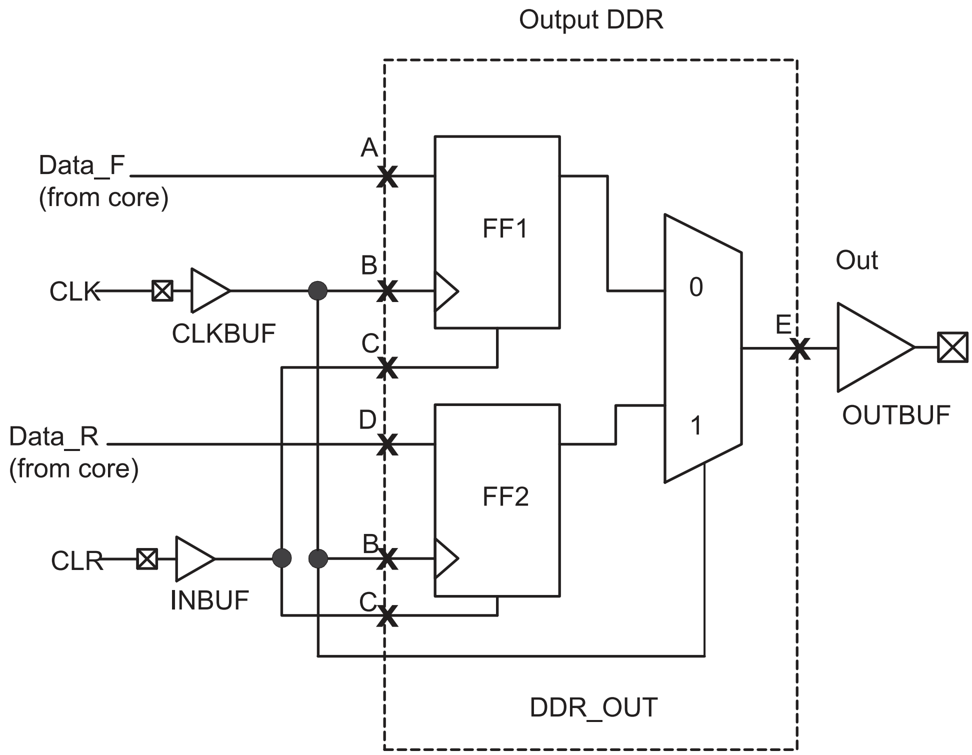


Figure 2-22 • Output DDR Timing Model

Table 2-77 • Parameter Definitions

Parameter Name	Parameter Definition	Measuring Nodes (from, to)
$t_{DDROCLKQ}$	Clock-to-Out	B, E
$t_{DDROCLR2Q}$	Asynchronous Clear-to-Out	C, E
$t_{DDROREMCLR}$	Clear Removal	C, B
$t_{DDRORECCLR}$	Clear Recovery	C, B
$t_{DDROSUD1}$	Data Setup Data_F	A, B
$t_{DDROSUD2}$	Data Setup Data_R	D, B
$t_{DDROHD1}$	Data Hold Data_F	A, B
$t_{DDROHD2}$	Data Hold Data_R	D, B

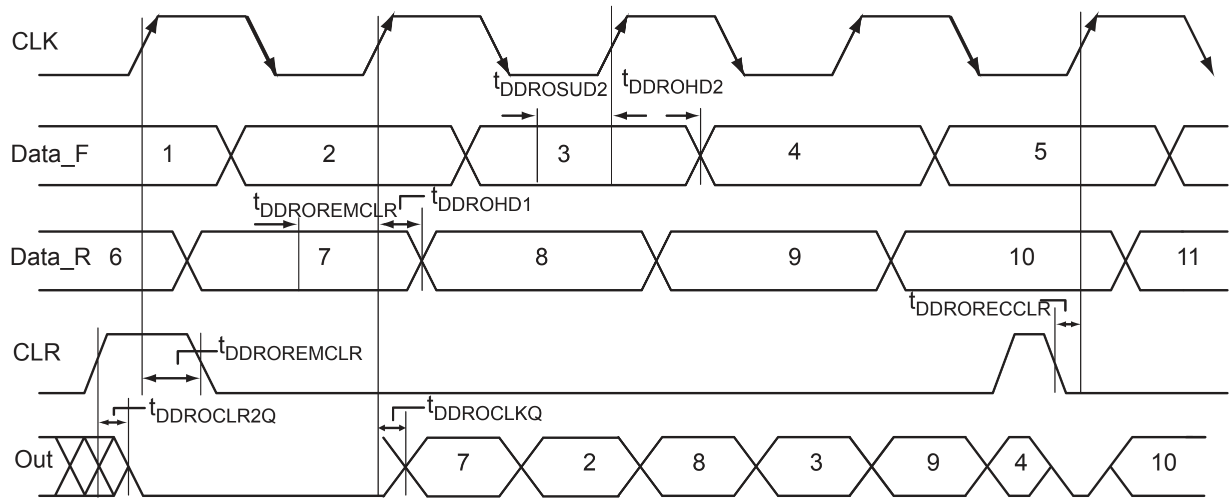


Figure 2-23 • **Output DDR Timing Diagram**

Timing Characteristics

Table 2-78 • **Output DDR Propagation Delays**
Worst Military-Case Conditions: T_J = 125°C, Worst-Case VCC = 1.425 V

Parameter	Description	–1	Std.	Units
$t_{DDROCLKQ}$	Clock-to-Out of DDR for Output DDR	0.74	0.89	ns
$t_{DDROSUD1}$	Data_F Data Setup for Output DDR	0.40	0.48	ns
$t_{DDROSUD2}$	Data_R Data Setup for Output DDR	0.40	0.48	ns
$t_{DDROHD1}$	Data_F Data Hold for Output DDR	0.00	0.00	ns
$t_{DDROHD2}$	Data_R Data Hold for Output DDR	0.00	0.00	ns
$t_{DDROCLR2Q}$	Asynchronous Clear-to-Out for Output DDR	0.85	1.02	ns
$t_{DDROREMCLR}$	Asynchronous Clear Removal Time for Output DDR	0.00	0.00	ns
$t_{DDRORECCLR}$	Asynchronous Clear Recovery Time for Output DDR	0.24	0.28	ns
$t_{DDROWCLR1}$	Asynchronous Clear Minimum Pulse Width for Output DDR	0.22	0.26	ns
$t_{DDROCKMPWH}$	Clock Minimum Pulse Width High for the Output DDR	0.36	0.42	ns
$t_{DDROCKMPWL}$	Clock Minimum Pulse Width Low for the Output DDR	0.32	0.38	ns
F_{DDOMAX}	Maximum Frequency for the Output DDR	350	350	MHz

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-9 for derating values.

VersaTile Characteristics

VersaTile Specifications as a Combinatorial Module

The SmartFusion library offers all combinations of LUT-3 combinatorial functions. In this section, timing characteristics are presented for a sample of the library. For more details, refer to the *IGLOO/e, Fusion, ProASIC3/E, and SmartFusion Macro Library Guide*.

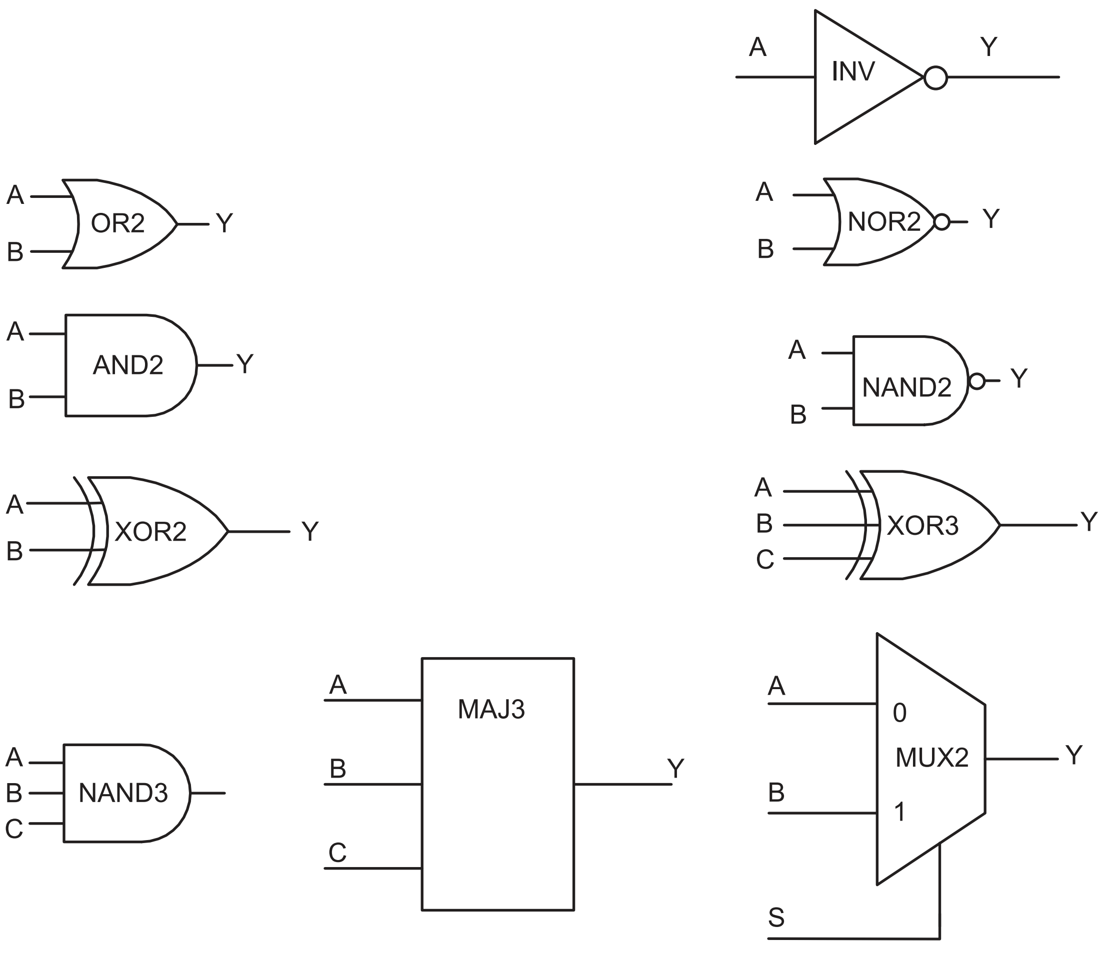


Figure 2-24 • **Sample of Combinatorial Cells**

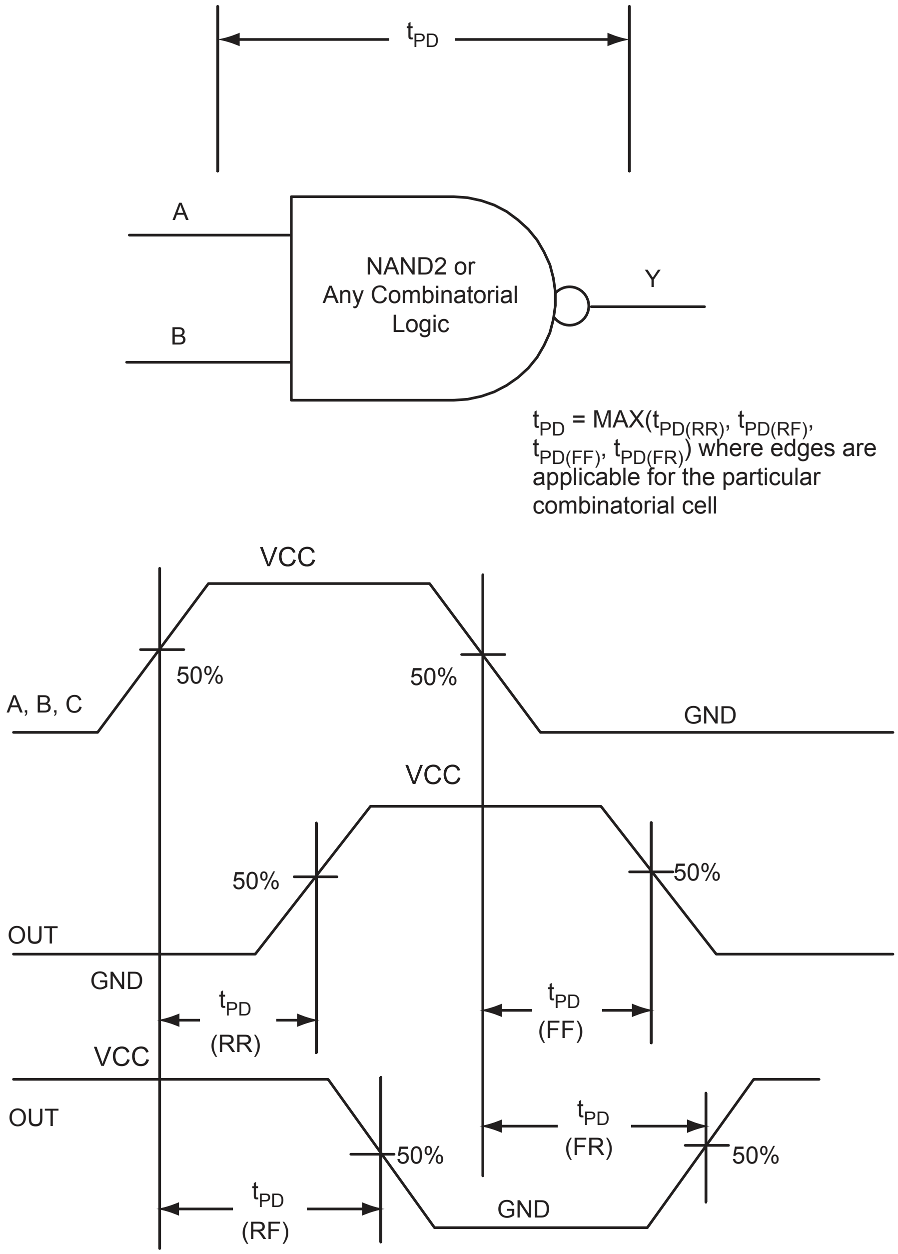


***Figure 2-25* • Timing Model and Waveforms**

Timing Characteristics

***Table 2-79 •* Combinatorial Cell Propagation Delays**
Worst Military-Case Conditions: T_J = 125°C, Worst-Case VCC = 1.425 V

Combinatorial Cell	Equation	Parameter	–1	Std.	Units
INV	Y = !A	t_{PD}	0.42	0.51	ns
AND2	Y = A · B	t_{PD}	0.50	0.60	ns
NAND2	Y = !(A · B)	t_{PD}	0.50	0.60	ns
OR2	Y = A + B	t_{PD}	0.51	0.62	ns
NOR2	Y = !(A + B)	t_{PD}	0.51	0.62	ns
XOR2	Y = A $\oplus$ B	t_{PD}	0.78	0.94	ns
MAJ3	Y = MAJ(A, B, C)	t_{PD}	0.74	0.88	ns
XOR3	Y = A $\oplus$ B $\oplus$ C	t_{PD}	0.92	1.11	ns
MUX2	Y = A !S + B S	t_{PD}	0.54	0.64	ns
AND3	Y = A · B · C	t_{PD}	0.59	0.71	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-9 for derating values.

VersaTile Specifications as a Sequential Module

The SmartFusion library offers a wide variety of sequential cells, including flip-flops and latches. Each has a data input and optional enable, clear, or preset. In this section, timing characteristics are presented for a representative sample from the library. For more details, refer to the *IGLOO/e, Fusion, ProASIC3/E, and SmartFusion Macro Library Guide*.

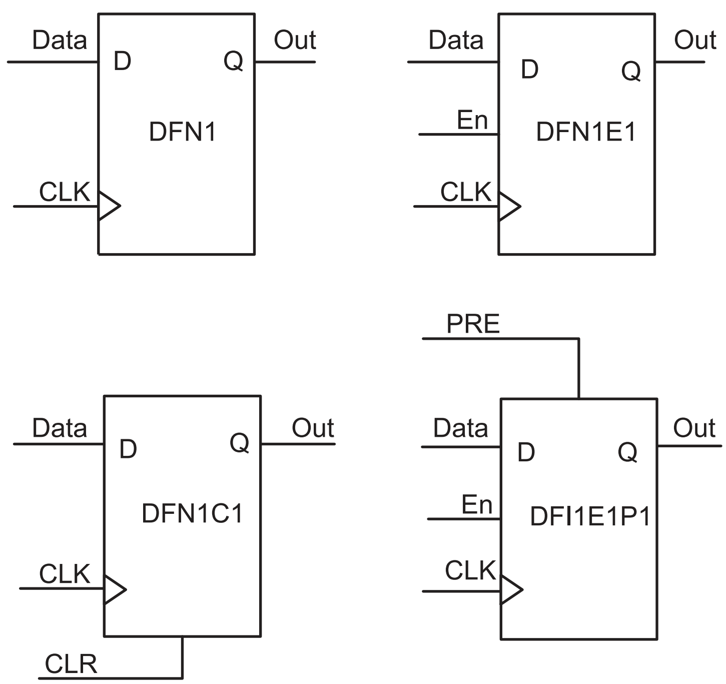


***Figure 2-26 •* Sample of Sequential Cells**

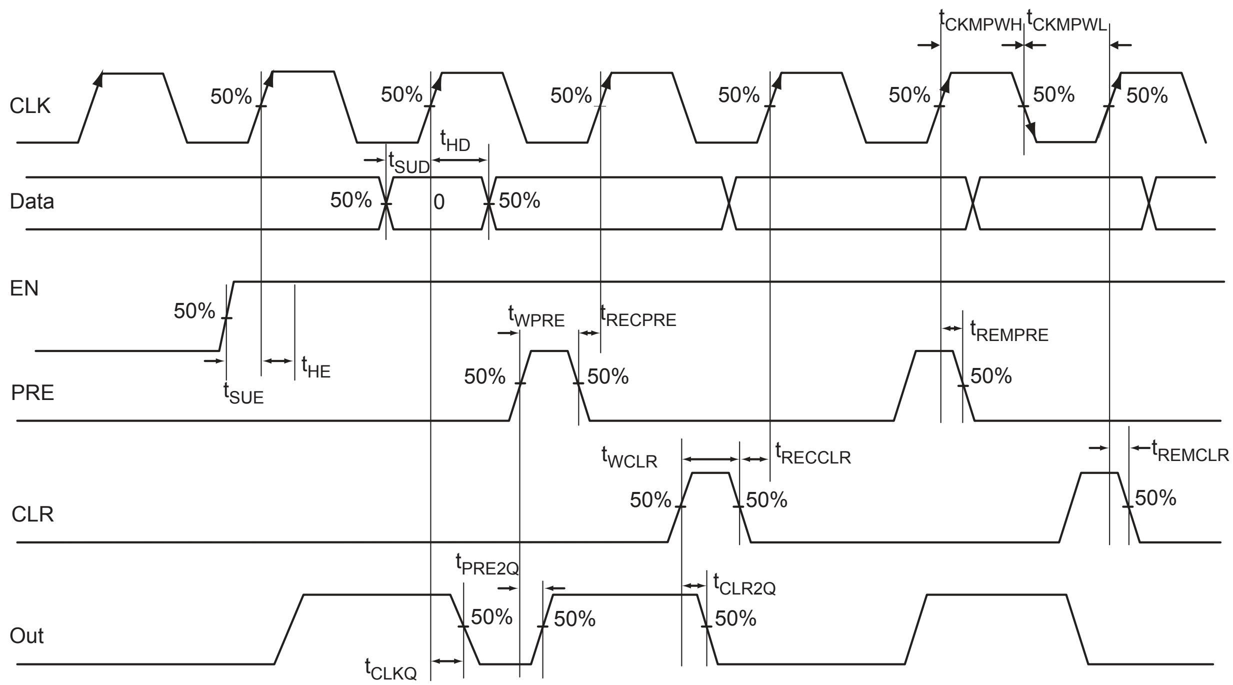


Figure 2-27 • Timing Model and Waveforms

Timing Characteristics

Table 2-80 • Register Delays
Worst Military-Case Conditions: T_J = 125°C, Worst-Case VCC = 1.425 V

Parameter	Description	–1	Std.	Units
t_{CLKQ}	Clock-to-Q of the Core Register	0.58	0.70	ns
t_{SUD}	Data Setup Time for the Core Register	0.45	0.54	ns
t_{HD}	Data Hold Time for the Core Register	0.00	0.00	ns
t_{SUE}	Enable Setup Time for the Core Register	0.48	0.58	ns
t_{HE}	Enable Hold Time for the Core Register	0.00	0.00	ns
t_{CLR2Q}	Asynchronous Clear-to-Q of the Core Register	0.42	0.51	ns
t_{PRE2Q}	Asynchronous Preset-to-Q of the Core Register	0.42	0.51	ns
t_{REMCLR}	Asynchronous Clear Removal Time for the Core Register	0.00	0.00	ns
t_{RECCLR}	Asynchronous Clear Recovery Time for the Core Register	0.24	0.28	ns
t_{REMPRE}	Asynchronous Preset Removal Time for the Core Register	0.00	0.00	ns
t_{RECPRE}	Asynchronous Preset Recovery Time for the Core Register	0.24	0.28	ns
t_{WCLR}	Asynchronous Clear Minimum Pulse Width for the Core Register	0.22	0.26	ns
t_{WPRE}	Asynchronous Preset Minimum Pulse Width for the Core Register	0.22	0.26	ns
t_{CKMPWH}	Clock Minimum Pulse Width High for the Core Register	0.32	0.38	ns
t_{CKMPWL}	Clock Minimum Pulse Width Low for the Core Register	0.36	0.42	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-9 for derating values.

Global Resource Characteristics

A2F500 Clock Tree Topology

Clock delays are device-specific. Figure 2-28 is an example of a global tree used for clock routing. The global tree presented in Figure 2-28 is driven by a CCC located on the west side of the A2F500 device. It is used to drive all D-flip-flops in the device.

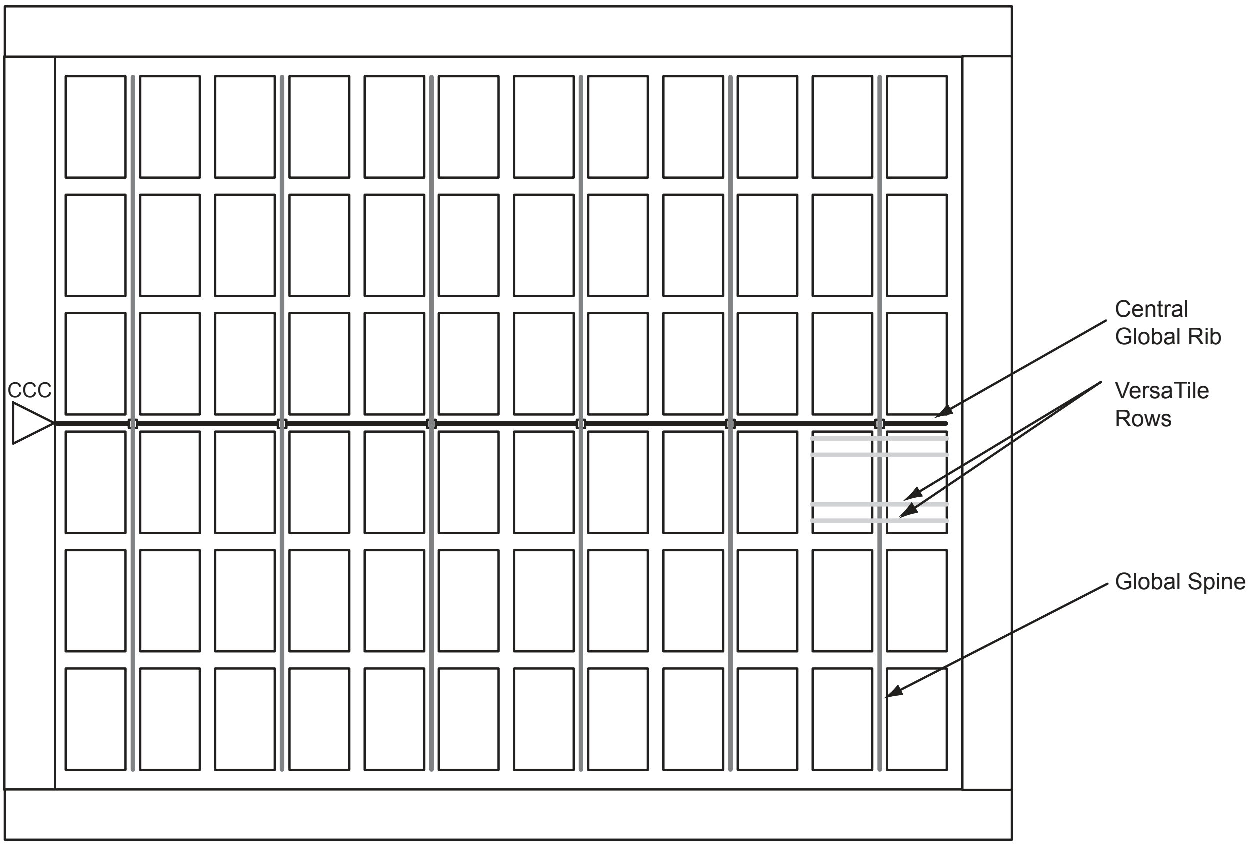


Figure 2-28 • **Example of Global Tree Use in an A2F500 Device for Clock Routing**

Global Tree Timing Characteristics

Global clock delays include the central rib delay, the spine delay, and the row delay. Delays do not include I/O input buffer clock delays, as these are I/O standard–dependent, and the clock may be driven and conditioned internally by the CCC module. For more details on clock conditioning capabilities, refer to the "Clock Conditioning Circuits" section on page 2-65. Table 2-81 through Table 2-82 on page 2-62 present minimum and maximum global clock delays for the SmartFusion cSoCs. Minimum and maximum delays are measured with minimum and maximum loading.

Timing Characteristics

Table 2-81 • **A2F500 Global Resource**
Worst Military-Case Conditions: T_J = 125°C, VCC = 1.425 V

Parameter	Description	–1		Std.		Units
		Min.[1]	Max.[2]	Min.[1]	Max.[2]	
t_{RCKL}	Input Low Delay for Global Clock	1.61	1.81	1.93	2.17	ns
t_{RCKH}	Input High Delay for Global Clock	1.60	1.85	1.92	2.21	ns
$t_{RCKMPWH}$	Minimum Pulse Width High for Global Clock	0.95		1.12		ns
$t_{RCKMPWL}$	Minimum Pulse Width Low for Global Clock	0.93		1.09		ns
t_{RCKSW}	Maximum Skew for Global Clock		0.25		0.30	ns

Notes:

1. *Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).*
2. *Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).*
3. *For specific junction temperature and voltage-supply levels, refer to Table 2-7 on page 2-9 for derating values.*

Table 2-82 • **A2F060 Global Resource**
Worst Military-Case Conditions: T_J = 125°C, VCC = 1.425 V

Parameter	Description	–1		Std.		Units
		Min.[1]	Max.[2]	Min.[1]	Max.[2]	
t_{RCKL}	Input Low Delay for Global Clock	0.78	1.01	0.94	1.21	ns
t_{RCKH}	Input High Delay for Global Clock	0.75	1.03	0.90	1.23	ns
$t_{RCKMPWH}$	Minimum Pulse Width High for Global Clock	0.95		1.12		ns
$t_{RCKMPWL}$	Minimum Pulse Width Low for Global Clock	0.93		1.09		ns
t_{RCKSW}	Maximum Skew for Global Clock		0.27		0.33	ns

Notes:

1. *Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).*
2. *Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).*
3. *For specific junction temperature and voltage-supply levels, refer to Table 2-7 on page 2-9 for derating values.*

RC Oscillator

The table below describes the electrical characteristics of the RC oscillator.

RC Oscillator Characteristics

Table 2-83 • **Electrical Characteristics of the RC Oscillator**

Parameter	Description	Condition	Min.	Typ.	Max.	Units
FRC	Operating frequency			100		MHz
	Accuracy	Temperature: –40°C to 100°C Voltage: 3.3 V ± 5%		1		%
		Temperature: –55°C to 125°C Voltage: 3.3 V ± 5%	–3		3	%
	Output jitter	Period jitter (at 5 K cycles)		100		ps RMS
		Cycle-to-cycle jitter (at 5 K cycles)		100		ps RMS
		Period jitter (at 5 K cycles) with 1 KHz / 300 mV peak-to-peak noise on power supply		150		ps RMS
		Cycle-to-cycle jitter (at 5 K cycles) with 1 KHz / 300 mV peak-to-peak noise on power supply		150		ps RMS
	Output duty cycle			50		%
IDYNRC	Operating current	3.3 V domain		1		mA
		1.5 V domain		2		mA

Main and Lower Power Crystal Oscillator

The tables below describes the electrical characteristics of the main and low power crystal oscillator.

Table 2-84 • **Electrical Characteristics of the Main Crystal Oscillator**

Parameter	Description	Condition	Min.	Typ.	Max.	Units
	Operating frequency	Using external crystal	0.032		20	MHz
		Using ceramic resonator	0.5		8	MHz
		Using RC Network	0.032		4	MHz
	Output duty cycle			50		%
	Output jitter	With 10 MHz crystal		1		ns RMS
IDYNXTAL	Operating current	RC		0.6		mA
		0.032–0.2		0.6		mA
		0.2–2.0		0.6		mA
		2.0–20.0		0.6		mA
ISTBXTAL	Standby current of crystal oscillator			10		µA
PSRRXTAL	Power supply noise tolerance			0.5		Vp-p
VIHXTAL	Input logic level High		90% of VCC			V
VILXTAL	Input logic level Low				10% of VCC	V
	Startup time	RC [tested at 3.24 MHz]		300	550	ns
		0.032–0.2 [tested at 32 KHz]		500	3,000	ms
		0.2–2.0 [tested at 2 MHz]		8	15	ms
		2.0–20.0 [tested at 20 MHz]		160	180	ns

Table 2-85 • **Electrical Characteristics of the Low Power Oscillator**

Parameter	Description	Condition	Min.	Typ.	Max.	Units
	Operating frequency			32		KHz
	Output duty cycle			50		%
	Output jitter			30		ns RMS
IDYNXTAL	Operating current	32 KHz		10		µA
ISTBXTAL	Standby current of crystal oscillator			2		µA
PSRRXTAL	Power supply noise tolerance			0.5		Vp-p
VIHXTAL	Input logic level High		90% of VCC			V
VILXTAL	Input logic level Low				10% of VCC	V
	Startup time	Test load used: 20 pF		2.5		s
		Test load used: 30 pF		3.7	13	s

Clock Conditioning Circuits

CCC Electrical Specifications

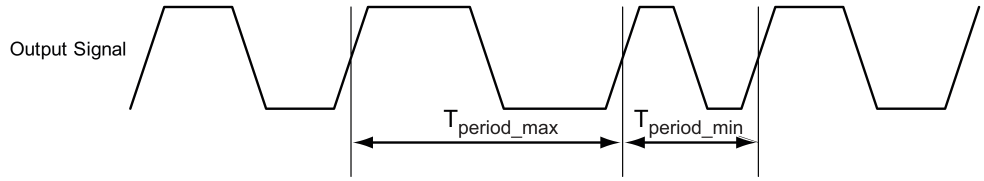
Timing Characteristics

Table 2-86 • **SmartFusion CCC/PLL Specification**

Parameter	Minimum		Typical		Maximum		Units	
Clock Conditioning Circuitry Input Frequency f_{IN_CCC}	1.5				350		MHz	
Clock Conditioning Circuitry Output Frequency f_{OUT_CCC}	0.75				350[1]		MHz	
Delay Increments in Programmable Delay Blocks[2, 3]			160[4]				ps	
Number of Programmable Values in Each Programmable Delay Block					32			
Input Period Jitter					1.5		ns	
Acquisition Time								
LockControl = 0					300		µs	
LockControl = 1					6.0		ms	
Tracking Jitter[5]								
LockControl = 0					1.6		ns	
LockControl = 1					0.8		ns	
Output Duty Cycle	48.5				5.15		%	
Delay Range in Block: Programmable Delay 1[2,3]	0.6				5.56		ns	
Delay Range in Block: Programmable Delay 2[2,3]	0.025				5.56		ns	
Delay Range in Block: Fixed Delay[2,3]			2.2				ns	
CCC Output Peak-to-Peak Period Jitter F_{CCC_OUT} [6.7]	Maximum Peak-to-Peak Period Jitter							
	SSO ≤ 2		SSO ≤ 4		SSO ≤ 8		SSO ≤ 16	
	FG/CS	PQ	FG/CS	PQ	FG/CS	PQ	FG/CS	PQ
0.75 MHz to 50 MHz	0.5%	1.6%	0.9%	1.6%	0.9%	1.6%	0.9%	1.8%
50 MHz to 250 MHz	1.75%	3.5%	9.3%	9.3%	9.3%	17.9%	10.0%	17.9%
250 MHz to 350 MHz	2.5%	5.2%	13.0%	13.0%	13.0%	25.0%	14.0%	25.0%

Notes:

1. *One of the CCC outputs (GLA0) is used as an MSS clock and is limited to 100 MHz (maximum) by software. Details regarding CCC/PLL are in the "PLLs, Clock Conditioning Circuitry, and On-Chip Crystal Oscillators" chapter of the SmartFusion Microcontroller Subsystem User's Guide.*
2. *This delay is a function of voltage and temperature. See Table 2-7 on page 2-9 for deratings.*
3. *T_J = 25°C, VCC = 1.5 V*
4. *When the CCC/PLL core is generated by Microsemi core generator software, not all delay values of the specified delay increments are available. Refer to SmartGen online help for more information.*
5. *Tracking jitter is defined as the variation in clock edge position of PLL outputs with reference to the PLL input clock edge. Tracking jitter does not measure the variation in PLL output period, which is covered by the period jitter parameter.*
6. *Measurement done with LVTTL 3.3 V 12 mA I/O drive strength and High slew rate. VCC/VCCPLL = 1.425 V, VCCI = 3.3V, 20 pF output load. All I/Os are placed outside of the PLL bank.*
7. *SSOs are outputs that are synchronous to a single clock domain and have their clock-to-out within ± 200 ps of each other.*
8. *VCO output jitter is calculated as a percentage of the VCO frequency. The jitter (in ps) can be calculated by multiplying the VCO period by the % jitter. The VCO jitter (in ps) applies to CCC_OUT regardless of the output divider settings. For example, if the jitter on VCO is 300 ps, the jitter on CCC_OUT is also 300 ps.*



Note: Peak-to-peak jitter measurements are defined by $T_{peak\text{-}to\text{-}peak} = T_{period\_max} - T_{period\_min}$.

Figure 2-29 **• Peak-to-Peak Jitter Definition**

FPGA Fabric SRAM and FIFO Characteristics

FPGA Fabric SRAM

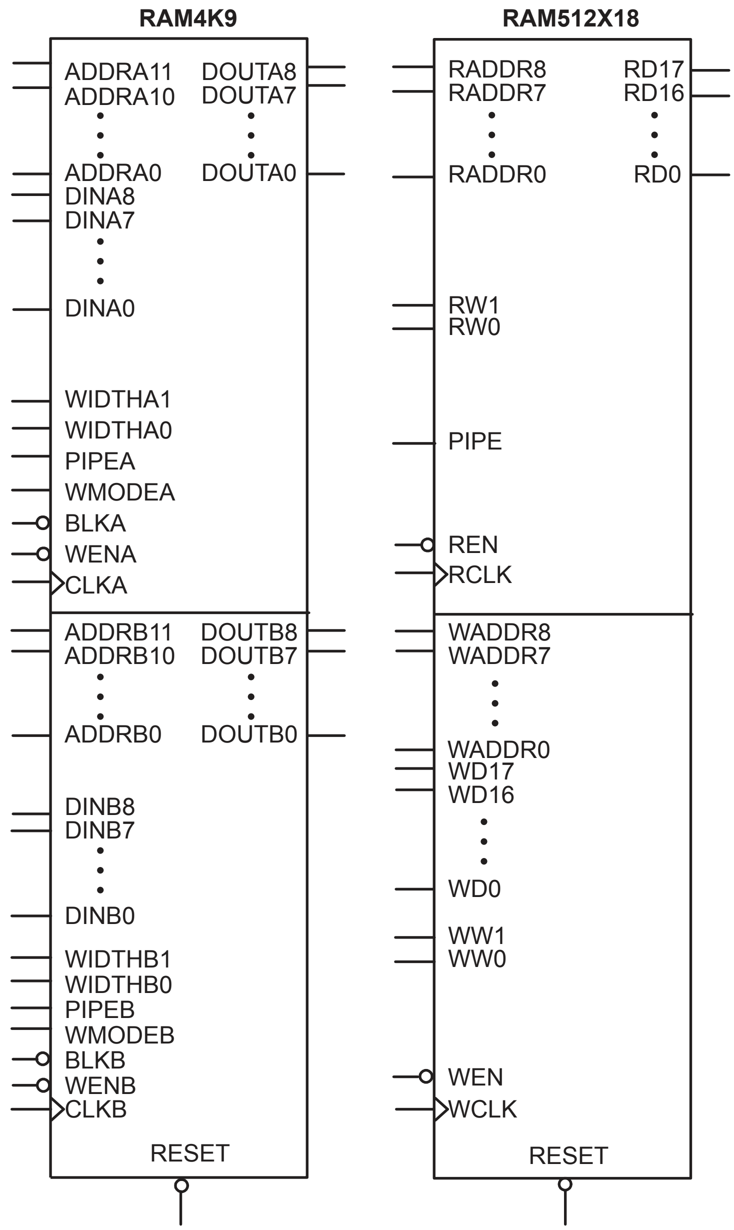


Figure 2-30 • **RAM Models**

Timing Waveforms

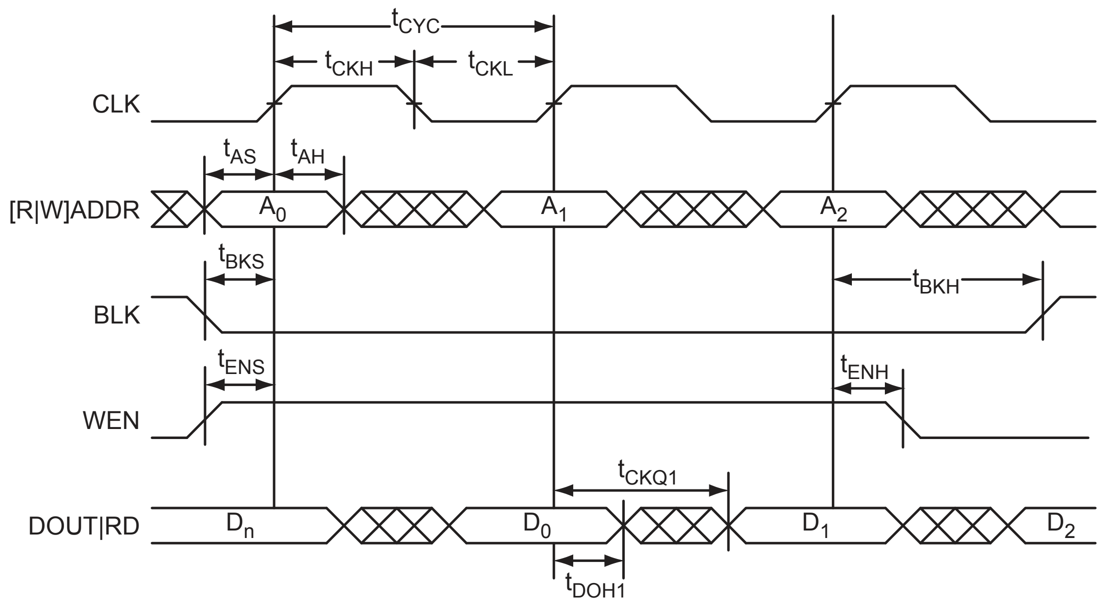


Figure 2-31 • **RAM Read for Pass-Through Output. Applicable to both RAM4K9 and RAM512x18.**

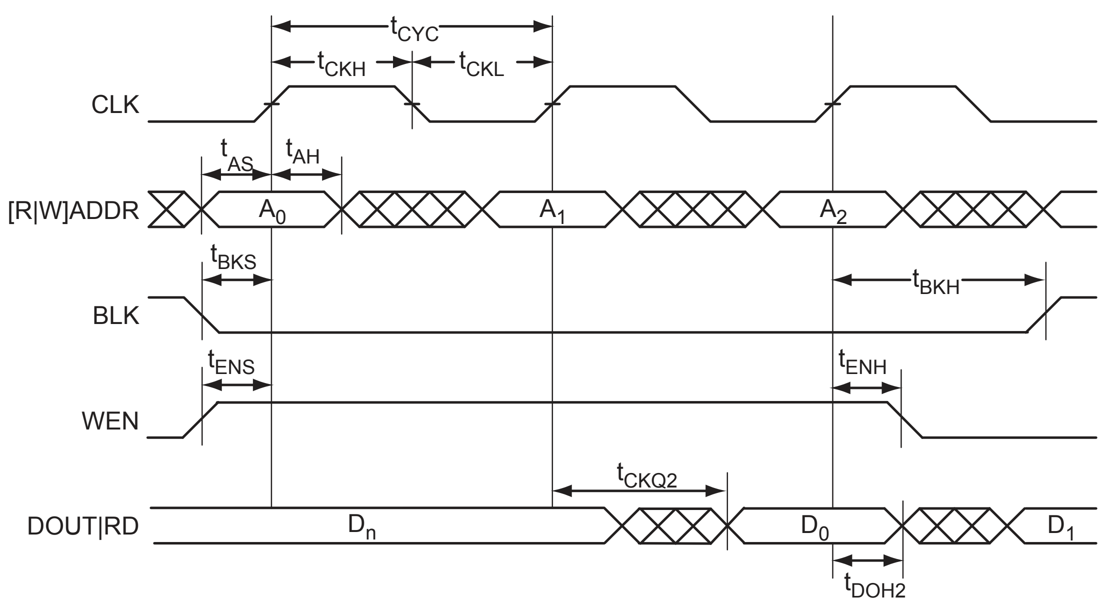


Figure 2-32 • **RAM Read for Pipelined Output Applicable to both RAM4K9 and RAM512x18.**

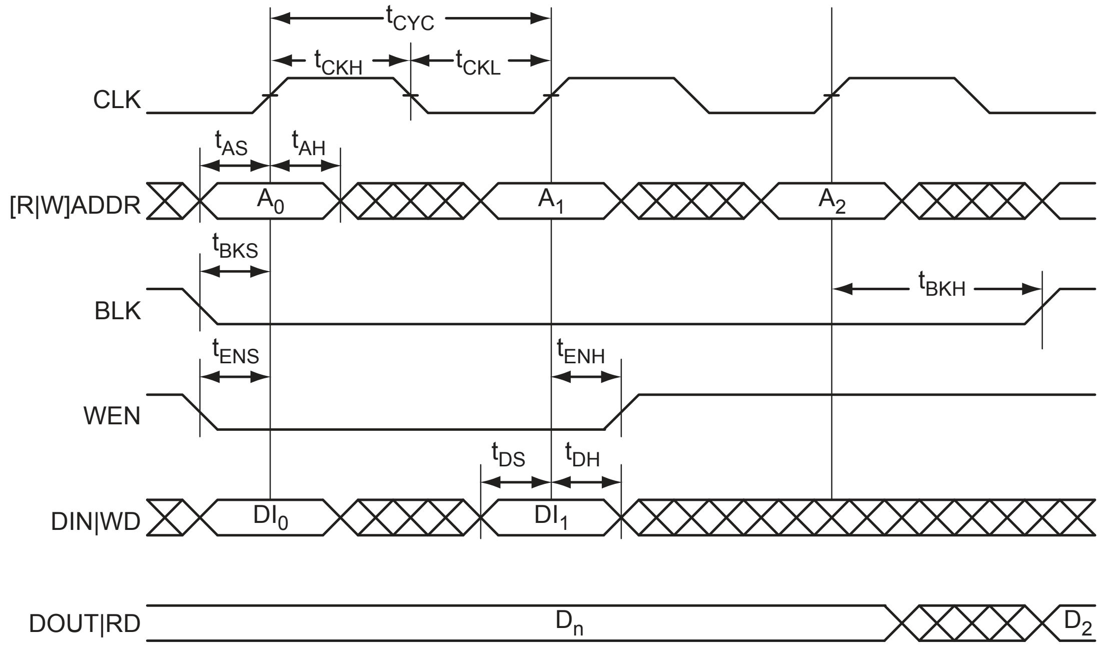


Figure 2-33 • **RAM Write, Output Retained. Applicable to both RAM4K9 and RAM512x18.**

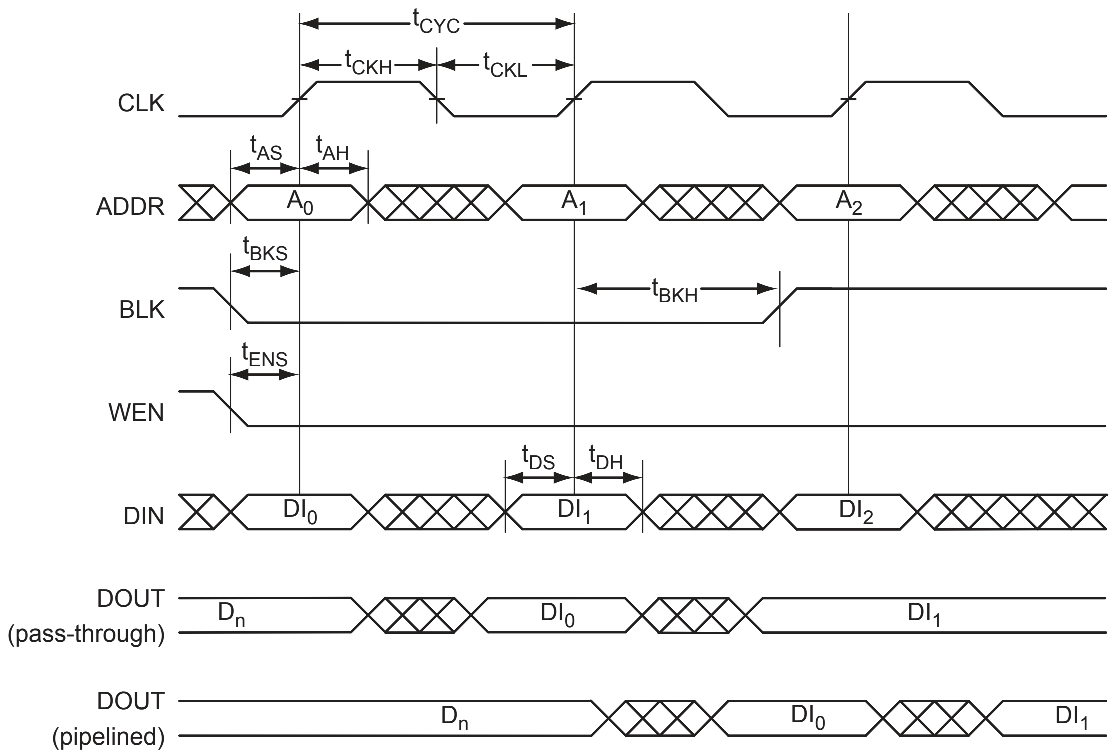


Figure 2-34 • **RAM Write, Output as Write Data (WMODE = 1). Applicable to RAM4K9 only.**

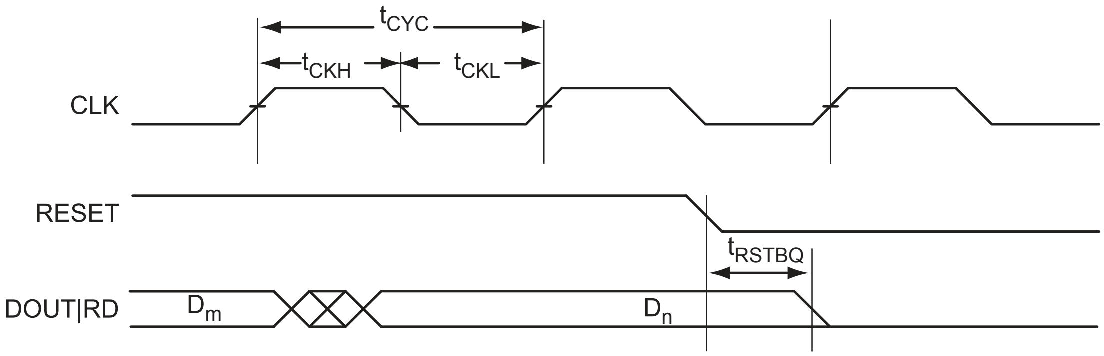


Figure 2-35 **• RAM Reset. Applicable to both RAM4K9 and RAM512x18.**

Timing Characteristics

Table 2-87 • RAM4K9
Worst Military-Case Conditions: T_J = 125°C, Worst-Case VCC = 1.425 V

Parameter	Description	–1	Std.	Units
t_{AS}	Address setup time	0.26	0.32	ns
t_{AH}	Address hold time	0.00	0.00	ns
t_{ENS}	REN, WEN setup time	0.15	0.18	ns
t_{ENH}	REN, WEN hold time	0.10	0.12	ns
t_{BKS}	BLK setup time	0.25	0.30	ns
t_{BKH}	BLK hold time	0.02	0.02	ns
t_{DS}	Input data (DIN) setup time	0.19	0.23	ns
t_{DH}	Input data (DIN) hold time	0.00	0.00	ns
t_{CKQ1}	Clock High to new data valid on DOUT (output retained, WMODE = 0)	1.89	2.27	ns
	Clock High to new data valid on DOUT (flow-through, WMODE = 1)	2.49	2.99	ns
t_{CKQ2}	Clock High to new data valid on DOUT (pipelined)	0.95	1.13	ns
t_{C2CWWH}[1]	Address collision clk-to-clk delay for reliable write after write on same address—applicable to rising edge	0.23	0.27	ns
t_{C2CRWH}[1]	Address collision clk-to-clk delay for reliable read access after write on same address—applicable to opening edge	0.34	0.40	ns
t_{C2CWRH}[1]	Address collision clk-to-clk delay for reliable write access after read on same address— applicable to opening edge	0.37	0.44	ns
t_{RSTBQ}	RESET Low to data out Low on DOUT (flow-through)	0.97	1.17	ns
	RESET Low to Data Out Low on DOUT (pipelined)	0.97	1.17	ns
$t_{REMRSTB}$	RESET removal	0.30	0.36	ns
$t_{RECRSTB}$	RESET recovery	1.59	1.90	ns
$t_{MPWRSTB}$	RESET minimum pulse width	0.23	0.26	ns
t_{CYC}	Clock cycle time	3.41	4.01	ns
F_{MAX}	Maximum clock frequency	293.08	249.12	MHz

Notes:

1. *For more information, refer to the application note* Simultaneous Read-Write Operations in Dual-Port SRAM for Flash-Based cSoCs and FPGAs.
2. *For the derating values at specific junction temperature and voltage supply levels, refer to* *Table 2-7 on page 2-9* *for derating values.*

Table 2-88 • **RAM512X18**
Worst Military-Case Conditions: T_J = 125°C, Worst-Case VCC = 1.425 V

Parameter	Description	–1	Std.	Units
t_{AS}	Address setup time	0.26	0.32	ns
t_{AH}	Address hold time	0.00	0.00	ns
t_{ENS}	REN, WEN setup time	0.10	0.12	ns
t_{ENH}	REN, WEN hold time	0.06	0.07	ns
t_{DS}	Input data (WD) setup time	0.19	0.23	ns
t_{DH}	Input data (WD) hold time	0.00	0.00	ns
t_{CKQ1}	Clock High to new data valid on RD (output retained, WMODE = 0)	2.28	2.74	ns
t_{CKQ2}	Clock High to new data valid on RD (pipelined)	0.95	1.14	ns
t_{C2CRWH}[1]	Address collision clk-to-clk delay for reliable read access after write on same address—applicable to opening edge	0.38	0.44	ns
t_{C2CWRH}[1]	Address collision clk-to-clk delay for reliable write access after read on same address—applicable to opening edge	0.44	0.52	ns
t_{RSTBQ}	RESET Low to data out Low on RD (flow-through)	0.97	1.17	ns
	RESET Low to data out Low on RD (pipelined)	0.97	1.17	ns
$t_{REMRSTB}$	RESET removal	0.30	0.36	ns
$t_{RECRSTB}$	RESET recovery	1.59	1.90	ns
$t_{MPWRSTB}$	RESET minimum pulse width	0.23	0.26	ns
t_{CYC}	Clock cycle time	3.41	4.01	ns
F_{MAX}	Maximum clock frequency	293.08	249.12	MHz

Notes:

1. *For more information, refer to the application note* Simultaneous Read-Write Operations in Dual-Port SRAM for Flash-Based cSoCs and FPGAs*.*
2. *For the derating values at specific junction temperature and voltage supply levels, refer to* *Table 2-7 on page 2-9* *for derating values.*

FIFO

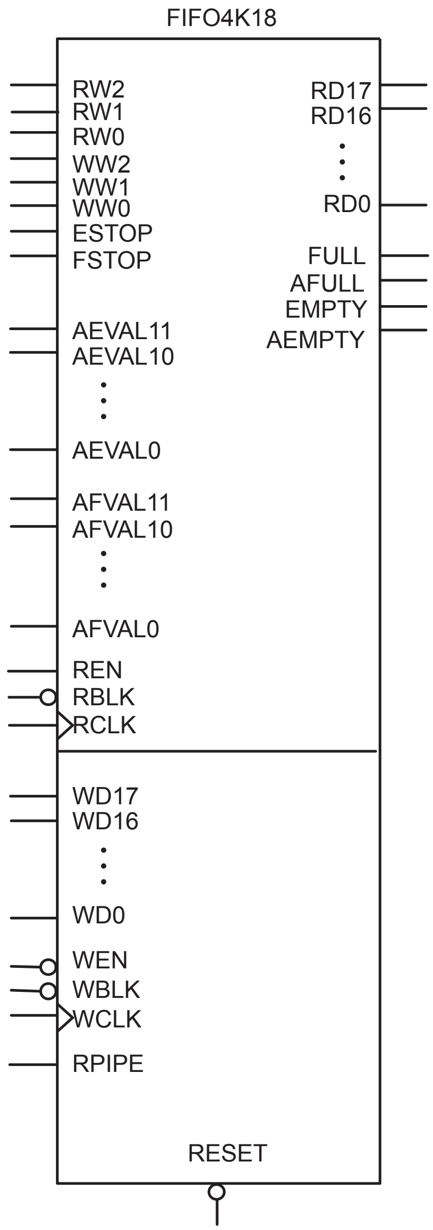


Figure 2-36 **• FIFO Model**

Timing Waveforms

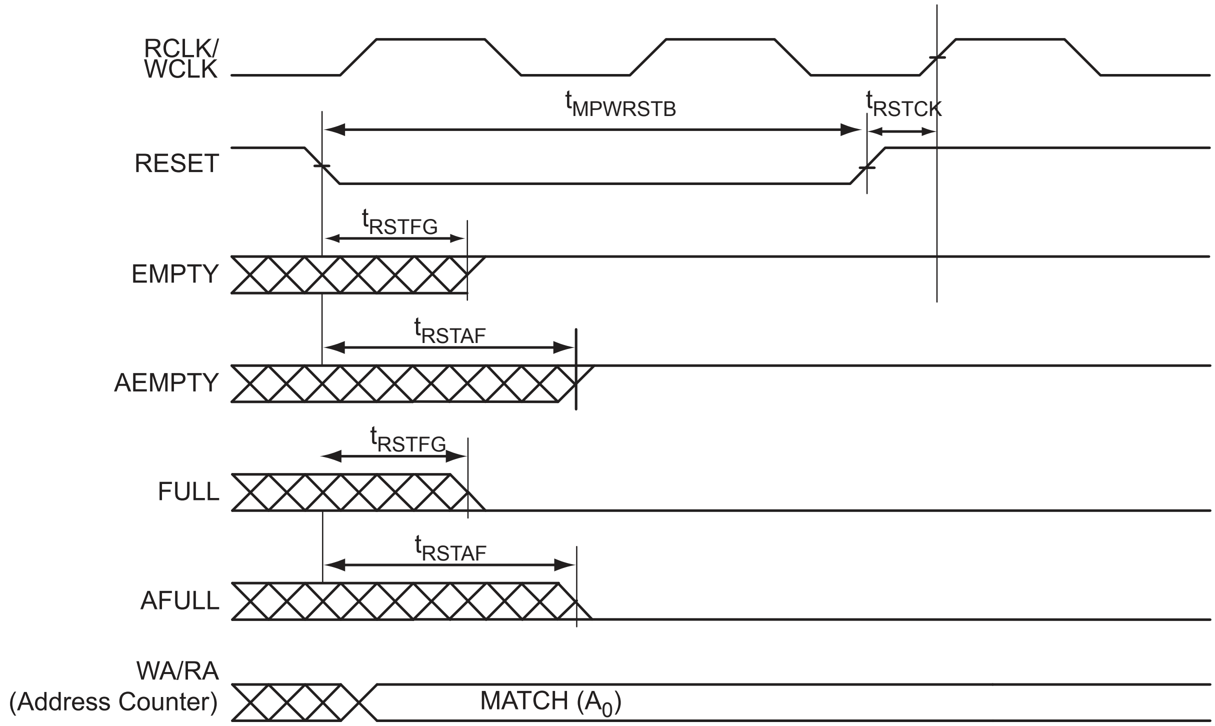


***Figure 2-37* • FIFO Reset**

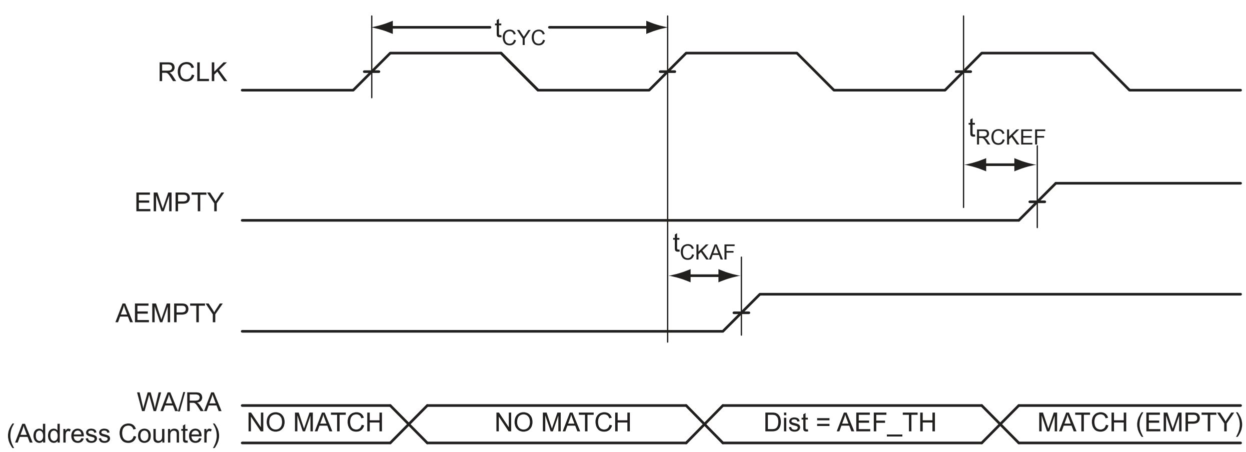


***Figure 2-38* • FIFO EMPTY Flag and AEMPTY Flag Assertion**

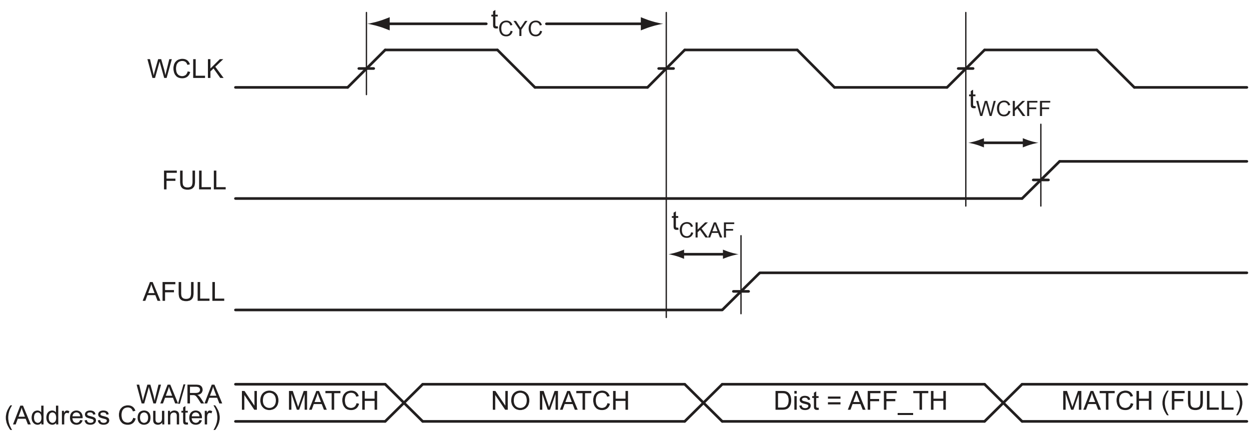


Figure 2-39 • **FIFO FULL Flag and AFULL Flag Assertion**

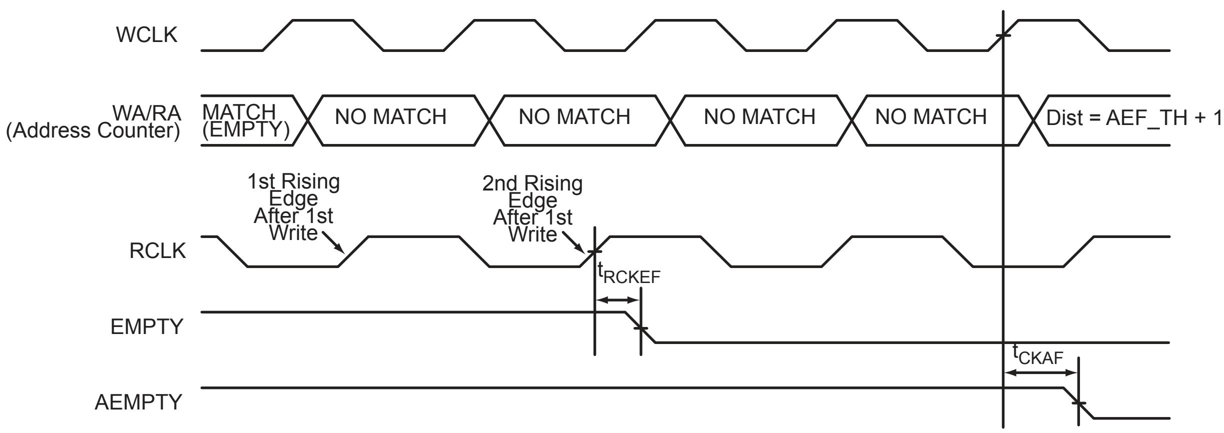


Figure 2-40 • **FIFO EMPTY Flag and AEMPTY Flag Deassertion**

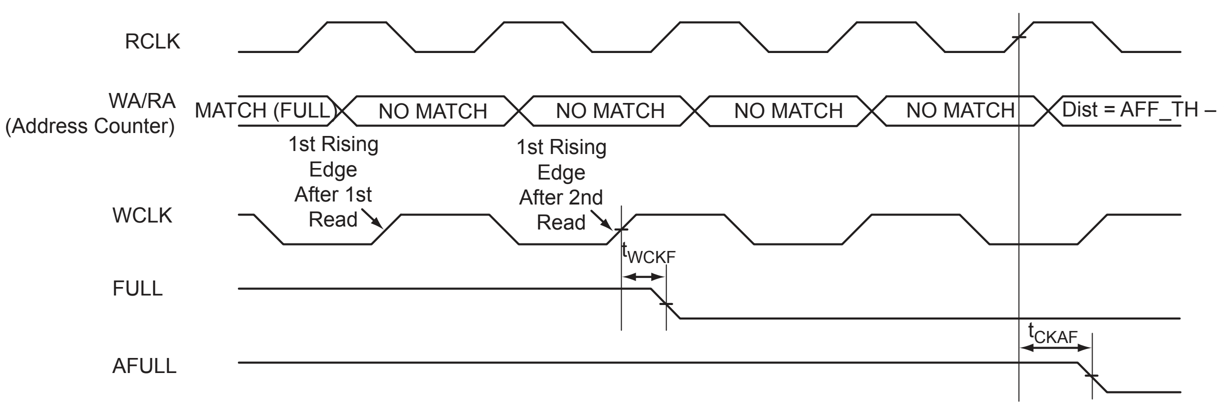


Figure 2-41 • **FIFO FULL Flag and AFULL Flag Deassertion**

Timing Characteristics

Table 2-89 • **FIFO**
Worst Military-Case Conditions: T_J = 125°C, VCC = 1.425 V

Parameter	Description	–1	Std.	Units
t_{ENS}	REN, WEN Setup Time	1.46	1.75	ns
t_{ENH}	REN, WEN Hold Time	0.02	0.02	ns
t_{BKS}	BLK Setup Time	0.19	0.19	ns
t_{BKH}	BLK Hold Time	0.00	0.00	ns
t_{DS}	Input Data (WD) Setup Time	0.19	0.23	ns
t_{DH}	Input Data (WD) Hold Time	0.00	0.00	ns
t_{CKQ1}	Clock High to New Data Valid on RD (flow-through)	2.49	2.99	ns
t_{CKQ2}	Clock High to New Data Valid on RD (pipelined)	0.95	1.13	ns
t_{RCKEF}	RCLK High to Empty Flag Valid	1.82	2.18	ns
t_{WCKFF}	WCLK High to Full Flag Valid	1.72	2.07	ns
t_{CKAF}	Clock HIGH to Almost Empty/Full Flag Valid	6.54	7.85	ns
t_{RSTFG}	RESET Low to Empty/Full Flag Valid	1.79	2.15	ns
t_{RSTAF}	RESET Low to Almost Empty/Full Flag Valid	6.48	7.77	ns
t_{RSTBQ}	RESET Low to Data Out Low on RD (flow-through)	0.97	1.17	ns
	RESET Low to Data Out Low on RD (pipelined)	0.97	1.17	ns
$t_{REMRSTB}$	RESET Removal	0.30	0.36	ns
$t_{RECRSTB}$	RESET Recovery	1.59	1.90	ns
$t_{MPWRSTB}$	RESET Minimum Pulse Width	0.23	0.26	ns
t_{CYC}	Clock Cycle Time	3.41	4.01	ns
F_{MAX}	Maximum Frequency for FIFO	293.08	249.12	MHz

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-9 for derating values.

Embedded Nonvolatile Memory Block (eNVM)

Electrical Characteristics

Table 2-90 describes the eNVM maximum performance.

Table 2-90 • **eNVM Block Timing, Worst Military-Case Conditions: T_J = 125°C, VCC = 1.425 V**

Parameter	Description	A2F060		A2F500		Units
		–1	Std.	–1	Std.	
$t_{FMAXCLKeNVM}$	Maximum frequency for clock for the control logic – 5 cycles (5:1:1:1*)	50	50	50	50	MHz
$t_{FMAXCLKeNVM}$	Maximum frequency for clock for the control logic – 6 cycles (6:1:1:1*)	50	50	50	50	MHz

*Note: *6:1:1:1 indicates 6 cycles for the first access and 1 each for the next three accesses. 5:1:1:1 indicates 5 cycles for the first access and 1 each for the next three accesses.*

Embedded FlashROM (eFROM)

Electrical Characteristics

Table 2-91 describes the eFROM maximum performance

Table 2-91 • **FlashROM Access Time, Worse Military-Case Conditions: T_J = 125°C, VCC = 1.425 V**

Parameter	Description	–1	Std.	Units
F_{max}	Maximum Clock frequency	15.00	15.00	MHz

JTAG 1532 Characteristics

JTAG timing delays do not include JTAG I/Os. To obtain complete JTAG timing, add I/O buffer delays to the corresponding standard selected; refer to the I/O timing characteristics in the "User I/O Characteristics" section on page 2-20 for more details.

Timing Characteristics

Table 2-92 • **JTAG 1532**
Worst Military-Case Conditions: T_J = 125°C, Worst-Case VCC = 1.425 V

Parameter	Description	–1	Std.	Units
t_{DISU}	Test Data Input Setup Time	0.53	0.63	ns
t_{DIHD}	Test Data Input Hold Time	1.07	1.25	ns
t_{TMSSU}	Test Mode Select Setup Time	0.53	0.63	ns
t_{TMDHD}	Test Mode Select Hold Time	1.07	1.25	ns
t_{TCK2Q}	Clock to Q (data out)	5.33	6.27	ns
t_{RSTB2Q}	Reset to Q (data out)	21.31	25.07	ns
F_{TCKMAX}	TCK Maximum Frequency	26.00	30.59	MHz
$t_{TRSTREM}$	ResetB Removal Time	0.00	0.00	ns
$t_{TRSTREC}$	ResetB Recovery Time	0.21	0.25	ns
$t_{TRSTMPW}$	ResetB Minimum Pulse	TBD	TBD	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-7 on page 2-9 for derating values.

Programmable Analog Specifications

Current Monitor

Unless otherwise noted, current monitor performance is specified at 25°C with nominal power supply voltages, with the output measured using the internal voltage reference with the internal ADC in 12-bit mode and 91 Ksps, after digital compensation. All results are based on averaging over 16 samples.

Table 2-93 • **Current Monitor Performance Specification**

Specification	Test Conditions	Min.	Typical	Max.	Units
Input voltage range (for driving ADC over full range)		0 – 48	0 – 50	1 – 51	mV
Analog gain	From the differential voltage across the input pads to the ADC input		50		V/V
Input referred offset voltage	Input referred offset voltage	0	0.1	0.5	mV
	–55ºC to +125ºC	0	0.1	0.5	mV
Gain error	Slope of BFSL vs. 50 V/V		±0.1	±0.7	% nom.
	–55ºC to +125ºC			±0.7	% nom.
Overall Accuracy	Peak error from ideal transfer function, 25°C		±(0.1 + 0.25%)	±(0.4 + 1.5%)	mV plus % reading
	–55ºC to +125ºC		±(0.1 + 0.25%)	±(1.5 + 1.5%)	mV plus % reading
Input referred noise	0 VDC input (no output averaging)	0.3	0.4	0.5	mVrms
Common-mode rejection ratio	0 V to 12 VDC common-mode voltage	–86	–87		dB
Analog settling time	To 0.1% of final value (with ADC load)				
	From CM_STB (High)	5			µs
	From ADC_START (High)	5		200	µs
Input capacitance			8		pF
Input biased current	CM[n] or TM[n] pad, –40°C to +100°C over maximum input voltage range (plus is into pad)				
	Strobe = 0; IBIAS on CM[n]		0		µA
	Strobe = 1; IBIAS on CM[n]		1		µA
	Strobe = 0; IBIAS on TM[n]		2		µA
	Strobe = 1; IBIAS on TM[n]		1		µA
Power supply rejection ratio	DC (0 – 10 KHz)	41	42		dB
Incremental operational current monitor power supply current requirements (per current monitor instance, not including ADC or VAREFx)	VCC33A		150		µA
	VCC33AP		140		µA
	VCC15A		50		µA

Note: *Under no condition should the TM pad ever be greater than 10 mV above the CM pad. This restriction is applicable only if current monitor is used.*

Temperature Monitor

Unless otherwise noted, temperature monitor performance is specified with a 2N3904 diode-connected bipolar transistor from National Semiconductor or Infineon Technologies, nominal power supply voltages, with the output measured using the internal voltage reference with the internal ADC in 12-bit mode and 62.5 Ksps. After digital compensation. Unless otherwise noted, the specifications pertain to conditions where the SmartFusion cSoC and the sensing diode are at the same temperature.

Table 2-94 • **Temperature Monitor Performance Specifications**

Specification	Test Conditions	Min.	Typical	Max.	Units
Input diode temperature range		–55		150	°C
		233.2		378.15	K
Temperature sensitivity			2.5		mV/K
Intercept	Extrapolated to 0K		0		V
Input referred temperature offset error	At 25°C (298.15K)		±1	1.5	°C
	At –55ºC to +125ºC			2	°C
Gain error	Slope of BFSL vs. 2.5 mV/K		±1	2.5	% nom.
Overall accuracy	Peak error from ideal transfer function		±2	±3	°C
	At –55ºC to +125ºC			±5	°C
Input referred noise	At 25°C (298.15K) – no output averaging		4		°C rms
	At –55ºC to +125ºC			6.5	°C rms
Output current	Idle mode		100		µA
	Final measurement phases		10		µA
Analog settling time	Measured to 0.1% of final value, (with ADC load)				
	From TM_STB (High)	5			µs
	From ADC_START (High)	5		105	µs
AT parasitic capacitance				500	pF
Power supply rejection ratio	DC (0–10 KHz)	1.2	0.7		°C/V
Input referred temperature sensitivity error	Variation due to device temperature (–40°C to +100°C). External temperature sensor held constant.		0.005	0.008	°C/°C
Temperature monitor (TM) operational power supply current requirements (per temperature monitor instance, not including ADC or VAREFx)	VCC33A		200		µA
	VCC33AP		150		µA
	VCC15A		50		µA

Note: All results are based on averaging over 64 samples.

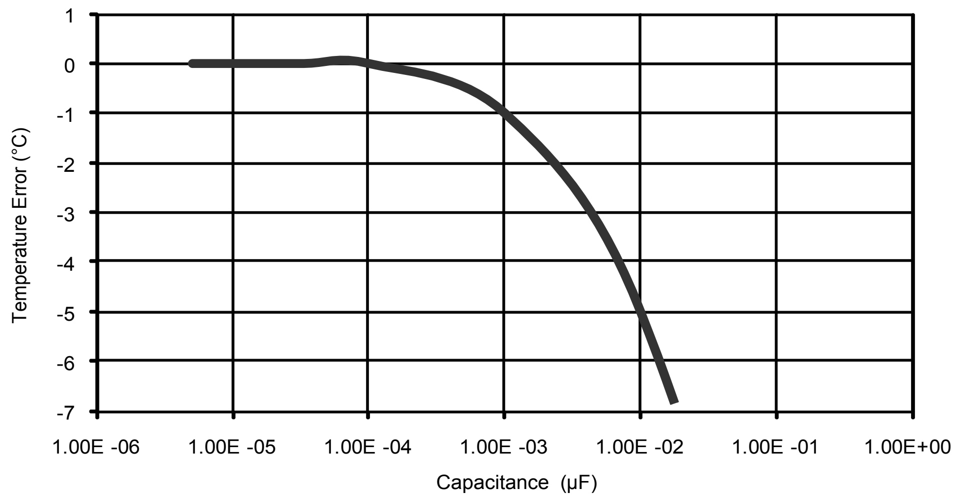


Figure 2-42 • **Temperature Error Versus External Capacitance**

Analog-to-Digital Converter (ADC)

Unless otherwise noted, ADC direct input performance is specified at 25°C with nominal power supply voltages, with the output measured using the external voltage reference with the internal ADC in 12-bit mode and 500 KHz sampling frequency, after trimming and digital compensation.

Table 2-95 • **ADC Specifications**

Specification	Test Conditions	Min.	Typ.	Max.	Units
Input voltage range (for driving ADC over its full range)			2.56		V
Gain error			±0.4	±0.7	%
	–55ºC to +125ºC		±0.4	±0.7	%
Input referred offset voltage			±1	±2	mV
	–55ºC to +125ºC		±1	±4	mV
Integral non-linearity (INL)	RMS deviation from BFSL				
	12-bit mode		1.71		LSB
	10-bit mode		0.60	1.00	LSB
	8-bit mode		0.2	0.33	LSB
Differential non-linearity (DNL)	12-bit mode		2.4		LSB
	10-bit mode		0.80	0.94	LSB
	8-bit mode		0.2	0.23	LSB
Signal to noise ratio		62	64		dB
Effective number of bits (ENOB)	–1 dBFS input				
$ENOB = \frac{SINAD - 1.76\ dB}{6.02\ dB/bit}$	12-bit mode 10 KHz	9.9	10		Bits
	12-bit mode 100 KHz	9.9	10		Bits
EQ 10	10-bit mode 10 KHz	9.5	9.6		Bits
	10-bit mode 100 KHz	9.5	9.6		Bits
	8-bit mode 10 KHz	7.8	7.9		Bits
	8-bit mode 100 KHz	7.8	7.9		Bits
Full power bandwidth	At –3 dB; –1 dBFS input	300			KHz
Analog settling time	To 0.1% of final value (with 1 Kohm source impedance and with ADC load)		2		µs
Input capacitance	Switched capacitance (ADC sample capacitor)		12	15	pF
	Cs: Static capacitance (Figure 2-43 on page 2-82)				
	CM[n] input		5	7	pF
	TM[n] input		5	7	pF
	ADC[n] input		5	7	pF
Input resistance	Rin: Series resistance (Figure 2-43)		2		KΩ
	Rsh: Shunt resistance, exclusive of switched capacitance effects (Figure 2-43)	10			MΩ

Note: All 3.3 V supplies are tied together and varied from 3.0 V to 3.6 V. 1.5 V supplies are held constant.

Table 2-95 • ADC Specifications (continued)

Specification	Test Conditions	Min.	Typ.	Max.	Units
Input leakage current	–40°C to +100°C		1		µA
Power supply rejection ratio	DC	44	53		dB
ADC power supply operational current requirements	VCC33ADCx			2.5	mA
	VCC15A			2	mA

Note: All 3.3 V supplies are tied together and varied from 3.0 V to 3.6 V. 1.5 V supplies are held constant.

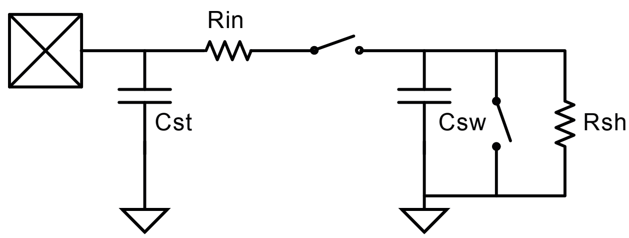


Figure 2-43 • ADC Input Model

Table 2-96 • VAREF Stabilization Time

VAREF Capacitor Value (µF)	Required Settling Time for 8-Bit and 10-Bit Mode (ms)	Required Settling Time for 12-Bit Mode (ms)
0.01	1	1
0.1	3	4
0.2	6	8
0.3	10	11
0.5	17	20
0.7	18	21
1	32	37
2.2	62	73
3.3	99	117
10	275	325
22	635	751
47	1318	1557

Analog Bipolar Prescaler (ABPS)

With the ABPS set to its high range setting (GDEC = 00), a hypothetical input voltage in the range –15.36 V to +15.36 V is scaled and offset by the ABPS input amplifier to match the ADC full range of 0 V to 2.56 V using a nominal gain of –0.08333 V/V. However, due to reliability considerations, the voltage applied to the ABPS input should never be outside the range of –11.5 V to +14.4 V, restricting the usable ADC input voltage to 2.238 V to 0.080 V and the corresponding 12-bit output codes to the range of 3581 to 128 (decimal), respectively.

Unless otherwise noted, ABPS performance is specified at 25°C with nominal power supply voltages, with the output measured using the internal voltage reference with the internal ADC in 12-bit mode and 100 KHz sampling frequency, after trimming and digital compensation; and applies to all ranges.

Table 2-97 • **ABPS Performance Specifications**

Specification	Test Conditions	Min.	Typ.	Max.	Units
Input voltage range (for driving ADC over its full range)	GDEC[1:0] = 11		±2.56		V
	GDEC[1:0] = 10		±5.12		V
	GDEC[1:0] = 01		±10.24		V
	GDEC[1:0] = 00 (limited by maximum rating)		See note 1		V
Analog gain (from input pad to ADC input)	GDEC[1:0] = 11		–0.5		V/V
	GDEC[1:0] = 10		–0.25		V/V
	GDEC[1:0] = 01		–0.125		V/V
	GDEC[1:0] = 00		–0.0833		V/V
Gain error		–2.8	–0.4	0.7	%
	–40ºC to +100ºC	–2.8	–0.4	0.7	%
	–55ºC to +125ºC	–4	–0.4	4	%
Input referred offset voltage					
	GDEC[1:0] = 11	–0.31	–0.07	0.31	% FS*
	–55ºC to +125ºC	–1.7		1.7	% FS*
	GDEC[1:0] = 10	–0.34	–0.07	0.34	% FS*
	–55ºC to +125ºC	–1.6		1.6	% FS*
	GDEC[1:0] = 01	–0.61	–0.07	0.35	% FS*
	–55ºC to +125ºC	–1.6		1.6	% FS*
	GDEC[1:0] = 00	–0.39	–0.07	0.35	% FS*
	–55ºC to +125ºC	–1.6		1.6	% FS*
SINAD		53	56		dB
Non-linearity	RMS deviation from BFSL			0.5	% FS*

*Note: *FS is full-scale error, defined as the difference between the actual value that triggers the transition to full-scale and the ideal analog full-scale transition value. Full-scale error equals offset error plus gain error. Refer to the Analog-to-Digital Converter chapter of the* SmartFusion Programmable Analog User's Guide *for more information.*

Table 2-97 • ABPS Performance Specifications (continued)

Specification	Test Conditions	Min.	Typ.	Max.	Units
Effective number of bits (ENOB) $$\text{ENOB} = \frac{\text{SINAD} - 1.76\text{ dB}}{6.02\text{ dB/bit}}$$ *EQ 11*	GDEC[1:0] = 11 (±2.56 range), –1 dBFS input				
	12-bit mode 10 KHz	8.6	9.1		Bits
	12-bit mode 100 KHz	8.6	9.1		Bits
	10-bit mode 10 KHz	8.5	8.9		Bits
	10-bit mode 100 KHz	8.5	8.9		Bits
	8-bit mode 10 KHz	7.7	7.8		Bits
	8-bit mode 100 KHz	7.7	7.8		Bits
Large-signal bandwidth	–1 dBFS input		1		MHz
Analog settling time	To 0.1% of final value (with ADC load)			10	µs
Input resistance			1		MΩ
Power supply rejection ratio	DC (0–1 KHz)	38	40		dB
ABPS power supply current requirements (not including ADC or VAREFx)	ABPS_EN = 1 (operational mode)				
	VCC33A		123	134	µA
	VCC33AP		89	94	µA
	VCC15A		1		µA

*Note: *FS is full-scale error, defined as the difference between the actual value that triggers the transition to full-scale and the ideal analog full-scale transition value. Full-scale error equals offset error plus gain error. Refer to the Analog-to-Digital Converter chapter of the SmartFusion Programmable Analog User's Guide for more information.*

Comparator

Unless otherwise specified, performance is specified at 25°C with nominal power supply voltages.

Table 2-98 • **Comparator Performance Specifications**

Specification	Test Conditions		Min.	Typ.	Max.	Units
Input voltage range	Minimum			0		V
	Maximum			2.56		V
Input offset voltage	HYS[1:0] = 00 (no hysteresis)			±1	±3	mV
Input bias current	Comparator 1, 3, 5, 7, 9 (measured at 2.56 V)			40	60	nA
	Comparator 0, 2, 4, 6, 8 (measured at 2.56 V)			150	300	nA
Input resistance			10			MΩ
Power supply rejection ratio	DC (0 – 10 KHz)		50	60		dB
Propagation delay	100 mV overdrive					
	HYS[1:0] = 00					
	(no hysteresis)			15	18	ns
	100 mV overdrive					
	HYS[1:0] = 10					
	(with hysteresis)			25	30	ns
Hysteresis (± refers to rising and falling threshold shifts, respectively)	HYS[1:0] = 00	Typical (25°C)	0	0	±5	mV
		Across all corners (–55ºC to +125ºC)	0		±5	mV
	HYS[1:0] = 01	Typical (25°C)	±3	± 16	±30	mV
		Across all corners (–55ºC to +125ºC)	0		±36	mV
	HYS[1:0] = 10	Typical (25°C)	±19	± 31	±48	mV
		Across all corners (–40ºC to +100ºC)	±12		±54	mV
		Across all corners (–55ºC to +125ºC)	±5		±54	mV
	HYS[1:0] = 11	Typical (25°C)	±80	± 105	±190	mV
		Across all corners (–40ºC to +100ºC)	±80		±194	mV
		Across all corners (–55ºC to +125ºC)	±60		±194	mV
Comparator current requirements (per comparator)	VCC33A = 3.3 V (operational mode); COMP_EN = 1					
	VCC33A			150	165	µA
	VCC33AP			140	165	µA
	VCC15A			1	15	µA

Analog Sigma-Delta Digital to Analog Converter (DAC)

Unless otherwise noted, sigma-delta DAC performance is specified at 25°C with nominal power supply voltages, using the internal sigma-delta modulators with 16-bit inputs, HCLK = 100 MHz, modulator inputs updated at a 100 KHz rate, in voltage output mode with an external 160 pF capacitor to ground, after trimming and digital [pre-]compensation.

Table 2-99 • **Analog Sigma-Delta DAC**

Specification	Test Conditions	Min.	Typ.	Max.	Units
Resolution		8		24	Bits
Output range			0 to 2.56		V
	Current output mode		0 to 256		µA
Output Impedance		6	10	12	KΩ
	Current output mode	10			MΩ
Output voltage compliance	Current output mode		0–3.0		V
	–40ºC to +100ºC	0–2.7		0–3.4	V
Gain error	Voltage output mode		0.3	±2	%
	–40ºC to +100ºC		0.3	±2	%
	–55ºC to +125ºC		0.3	±6	%
	Current output mode		0.3	±2	%
	–40ºC to +100ºC		0.3	±2	%
	–55ºC to +125ºC		0.3	±6	%
Output referred offset	DACBYTE0 = h'00 (8-bit)		0.25	±1	mV
	–40ºC to +100ºC		1	±2.5	mV
	Current output mode		0.3	±1	µA
	–40ºC to +100ºC		1	±2.5	µA
Integral non-linearity	RMS deviation from BFSL		0.1	0.4	% FS*
Differential non-linearity			0.05	0.4	% FS*
Analog settling time			Refer to Figure 2-44 on page 2-87		µs
Power supply rejection ratio	DC, full scale output	33	34		dB

*Note: *FS is full-scale error, defined as the difference between the actual value that triggers the transition to full-scale and the ideal analog full-scale transition value. Full-scale error equals offset error plus gain error. Refer to the Analog-to-Digital Converter chapter of the SmartFusion Programmable Analog User's Guide for more information.*

Table 2-99 • **Analog Sigma-Delta DAC (continued)**

Specification	Test Conditions	Min.	Typ.	Max.	Units
Sigma-delta DAC power supply current requirements (not including VAREFx)	Input = 0, EN = 1 (operational mode)				
	VCC33SDDx		30	40	µA
	VCC15A		3	5	µA
	Input = Half scale, EN = 1 (operational mode)				
	VCC33SDDx		160	165	µA
	VCC15A		33	35	µA
	Input = Full scale, EN = 1 (operational mode)				
	VCC33SDDx		280	285	µA
	VCC15A		70	75	µA

*Note: *FS is full-scale error, defined as the difference between the actual value that triggers the transition to full-scale and the ideal analog full-scale transition value. Full-scale error equals offset error plus gain error. Refer to the Analog-to-Digital Converter chapter of the* SmartFusion Programmable Analog User's Guide *for more information.*

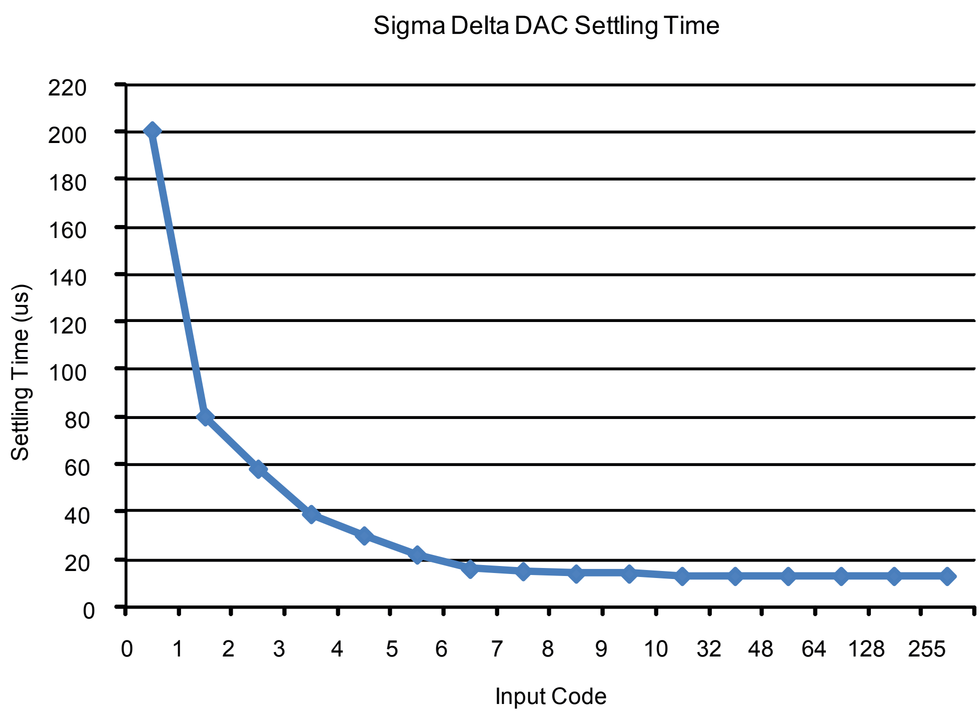


Figure 2-44 • **Sigma-Delta DAC Setting Time**

Voltage Regulator

Table 2-100 • **Voltage Regulator**

Symbol	Parameter	Test Conditions		Min.	Typ.	Max.	Unit
VOUT	Output voltage	T_J = 25°C		1.425	1.5	1.575	V
VOS	Output offset voltage	T_J = 25°C			11		mV
ICC33A	Operation current	T_J = 25°C	I_{LOAD} = 1 mA		3.4		mA
			I_{LOAD} = 100 mA		11		mA
			I_{LOAD} = 0.5 A		21		mA
∆VOUT	Load regulation	T_J = 25°C	I_{LOAD} = 1 mA to 0.5 A		5.8		mV
∆VOUT	Line regulation	T_J = 25°C	VCC33A = 2.97 V to 3.63 V I_{LOAD} = 1 mA		8		mV/V
			VCC33A = 2.97 V to 3.63 V I_{LOAD}= 100 mA		8		mV/V
			VCC33A = 2.97 V to 3.63 V I_{LOAD} = 500 mA		8		mV/V
	Dropout voltage[1]	T_J = 25°C	I_{LOAD} = 1 mA		0.65		V
			I_{LOAD} = 100 mA		0.84		V
			I_{LOAD} = 0.5 A		1.35		V
IPTBASE	PTBase current	T_J = 25°C	I_{LOAD} = 1 mA		48		µA
			I_{LOAD} = 100 mA		736		µA
			I_{LOAD} = 0.5 A		12		mA
	Startup time[2]	T_J = 25°C			200		ms

Notes:

1. *Dropout voltage is defined as the minimum VCC33A voltage. The parameter is specified with respect to the output voltage. The specification represents the minimum input-to-output differential voltage required to maintain regulation.*
2. *Assumes 10 µF.*

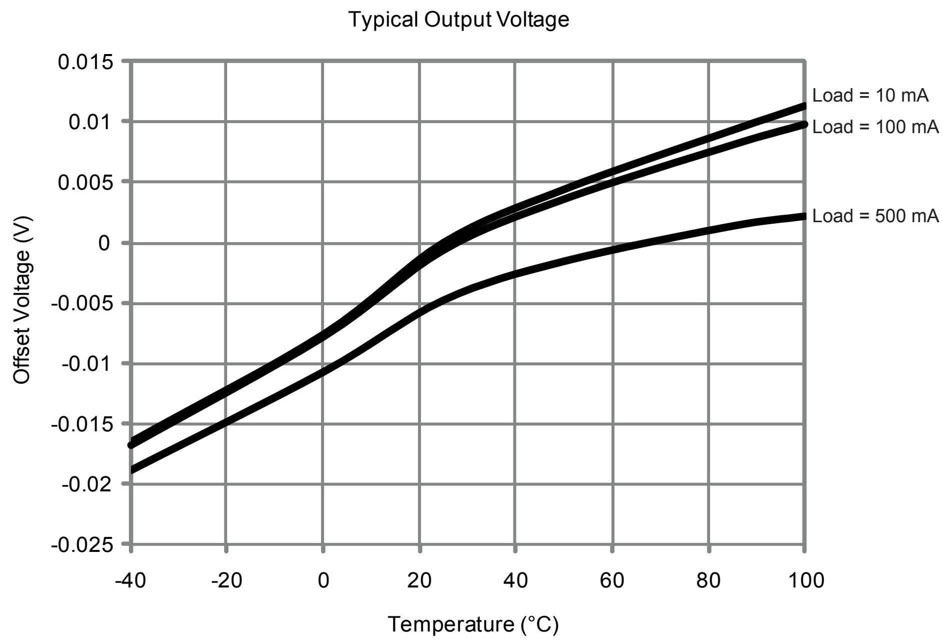


Figure 2-45 **• Typical Output Voltage**

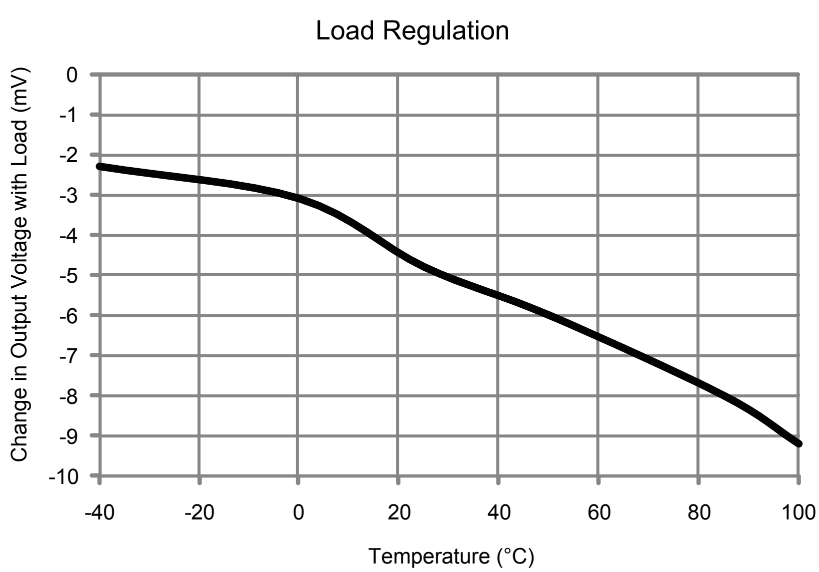


Figure 2-46 **• Load Regulation**

Serial Peripheral Interface (SPI) Characteristics

This section describes the DC and switching of the SPI interface. Unless otherwise noted, all output characteristics given for a 35 pF load on the pins and all sequential timing characteristics are related to SPI_x_CLK. For timing parameter definitions, refer to Figure 2-47 on page 2-91.

***Table 2-101* • SPI Characteristics**
Military-Case Conditions: T_J =125ºC, VDD = 1.425 V, –1 Speed Grade

Symbol	Description and Condition	A2F060	A2F500	Unit
sp1	SPI_x_CLK minimum period			
	SPI_x_CLK = PCLK/2	20	20	ns
	SPI_x_CLK = PCLK/4	40	40	ns
	SPI_x_CLK = PCLK/8	80	80	ns
	SPI_x_CLK = PCLK/16	0.16	0.16	µs
	SPI_x_CLK = PCLK/32	0.32	0.32	µs
	SPI_x_CLK = PCLK/64	0.64	0.64	µs
	SPI_x_CLK = PCLK/128	1.28	1.28	µs
	SPI_x_CLK = PCLK/256	2.56	2.56	µs
sp2	SPI_x_CLK minimum pulse width high			
	SPI_x_CLK = PCLK/2	10	10	ns
	SPI_x_CLK = PCLK/4	20	20	ns
	SPI_x_CLK = PCLK/8	40	40	ns
	SPI_x_CLK = PCLK/16	0.08	0.08	µs
	SPI_x_CLK = PCLK/32	0.16	0.16	µs
	SPI_x_CLK = PCLK/64	0.32	0.32	µs
	SPI_x_CLK = PCLK/128	0.64	0.64	µs
	SPI_x_CLK = PCLK/256	1.28	1.28	us
sp3	SPI_x_CLK minimum pulse width low			
	SPI_x_CLK = PCLK/2	10	10	ns
	SPI_x_CLK = PCLK/4	20	20	ns
	SPI_x_CLK = PCLK/8	40	40	ns
	SPI_x_CLK = PCLK/16	0.08	0.08	µs
	SPI_x_CLK = PCLK/32	0.16	0.16	µs
	SPI_x_CLK = PCLK/64	0.32	0.32	µs
	SPI_x_CLK = PCLK/128	0.64	0.64	µs
	SPI_x_CLK = PCLK/256	1.28	1.28	µs
sp4	SPI_x_CLK, SPI_x_DO, SPI_x_SS rise time (10%-90%) [1]	4.7	4.7	ns
sp5	SPI_x_CLK, SPI_x_DO, SPI_x_SS fall time (10%-90%) [1]	3.4	3.4	ns

Notes:

1. *These values are provided for a load of 35 pF. For board design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the Microsemi SoC Products Group website: http://www.microsemi.com/soc/download/ibis/default.aspx.*
2. *For allowable pclk configurations, refer to the Serial Peripheral Interface Controller section in the SmartFusion Microcontroller Subsystem User's Guide.*

Table 2-101 • **SPI Characteristics**
Military-Case Conditions: T_J =125ºC, VDD = 1.425 V, –1 Speed Grade (continued)

Symbol	Description and Condition	A2F060	A2F500	Unit
sp6	Data from master (SPI_x_DO) setup time [2]	1	1	pclk cycles
sp7	Data from master (SPI_x_DO) hold time [2]	1	1	pclk cycles
sp8	SPI_x_DI setup time [2]	1	1	pclk cycles
sp9	SPI_x_DI hold time [2]	1	1	pclk cycles

Notes:

1. *These values are provided for a load of 35 pF. For board design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the Microsemi SoC Products Group website: http://www.microsemi.com/soc/download/ibis/default.aspx.*
2. *For allowable pclk configurations, refer to the Serial Peripheral Interface Controller section in the SmartFusion Microcontroller Subsystem User's Guide.*

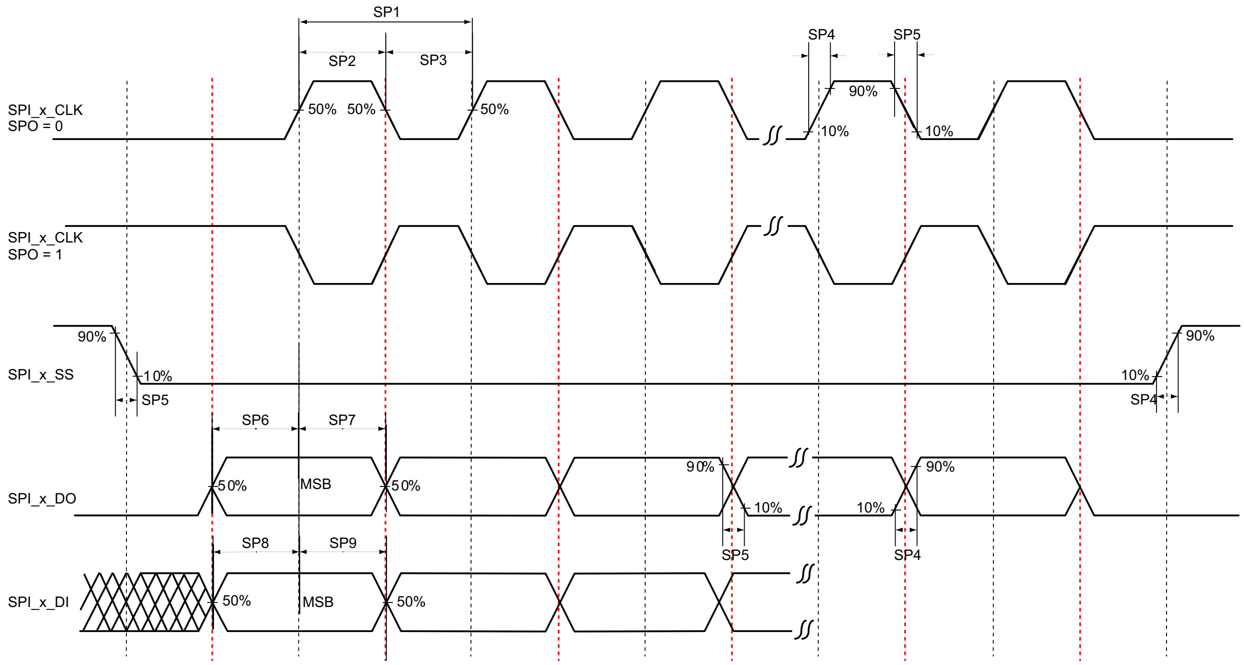


Figure 2-47 • **SPI Timing for a Single Frame Transfer in Motorola Mode (SPH = 1)**

Inter-Integrated Circuit (I^2C) Characteristics

This section describes the DC and switching of the I^2C interface. Unless otherwise noted, all output characteristics given are for a 100 pF load on the pins. For timing parameter definitions, refer to Figure 2-48 on page 2-93.

Table 2-102 **• I^2C Characteristics**
Military-Case Conditions: T_J = 125ºC, VDD = 1.425 V, –1 Speed Grade

Parameter	Definition	Condition	Value	Unit
V_{IL}	Minimum input low voltage	–	See Table 2-37 on page 2-31	–
	Maximum input low voltage	–	See Table 2-37	–
V_{IH}	Minimum input high voltage	–	See Table 2-37	–
	Maximum input high voltage	–	See Table 2-37	–
V_{OL}	Maximum output voltage low	I_{OL} = 8 mA	See Table 2-37	–
I_{IL}	Input current high	–	See Table 2-37	–
I_{IH}	Input current low	–	See Table 2-37	–
V_{hyst}	Hysteresis of Schmitt trigger inputs	–	See Table 2-33 on page 2-30	V
T_{FALL}	Fall time [2]	VIHmin to VILMax, C_{load} = 400 pF	15.0	ns
		VIHmin to VILMax, C_{load} = 100 pF	4.0	ns
T_{RISE}	Rise time [2]	VILMax to VIHmin, C_{load} = 400pF	19.5	ns
		VILMax to VIHmin, C_{load} = 100pF	5.2	ns
Cin	Pin capacitance	VIN = 0, f = 1.0 MHz	8.0	pF
$R_{pull-up}$	Output buffer maximum pull-down Resistance [1]	–	50	Ω
$R_{pull-down}$	Output buffer maximum pull-up Resistance [1]	–	150	Ω
D_{max}	Maximum data rate	Fast mode	400	Kbps
t_{LOW}	Low period of I2C_x_SCL [3]	–	1	pclk cycles
t_{HIGH}	High period of I2C_x_SCL [3]	–	1	pclk cycles
$t_{HD;STA}$	START hold time [3]	–	1	pclk cycles
$t_{SU;STA}$	START setup time [3]	–	1	pclk cycles
$t_{HD;DAT}$	DATA hold time [3]	–	1	pclk cycles
$t_{SU;DAT}$	DATA setup time [3]	–	1	pclk cycles

Notes:

1. *These maximum values are provided for information only. Minimum output buffer resistance values depend on VCCxxxxIOBx, drive strength selection, temperature, and process. For board design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the SoC Products Group website at http://www.microsemi.com/soc/download/ibis/default.aspx.*
2. *These values are provided for a load of 100 pF and 400 pF. For board design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the SoC Products Group website at http://www.microsemi.com/soc/download/ibis/default.aspx.*
3. *For allowable Pclk configurations, refer to the Inter-Integrated Circuit (I^2C) Peripherals section in the SmartFusion Microcontroller Subsystem User's Guide.*

Table 2-102 • I²C Characteristics
Military-Case Conditions: T_J = 125ºC, VDD = 1.425 V, –1 Speed Grade (continued)

Parameter	Definition	Condition	Value	Unit
$t_{SU;STO}$	STOP setup time [3]	–	1	pclk cycles
t_{FILT}	Maximum spike width filtered	–	50	ns

Notes:

1. *These maximum values are provided for information only. Minimum output buffer resistance values depend on VCCxxxxIOBx, drive strength selection, temperature, and process. For board design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the SoC Products Group website at http://www.microsemi.com/soc/download/ibis/default.aspx.*
2. *These values are provided for a load of 100 pF and 400 pF. For board design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the SoC Products Group website at http://www.microsemi.com/soc/download/ibis/default.aspx.*
3. *For allowable Pclk configurations, refer to the Inter-Integrated Circuit (I²C) Peripherals section in the SmartFusion Microcontroller Subsystem User's Guide.*

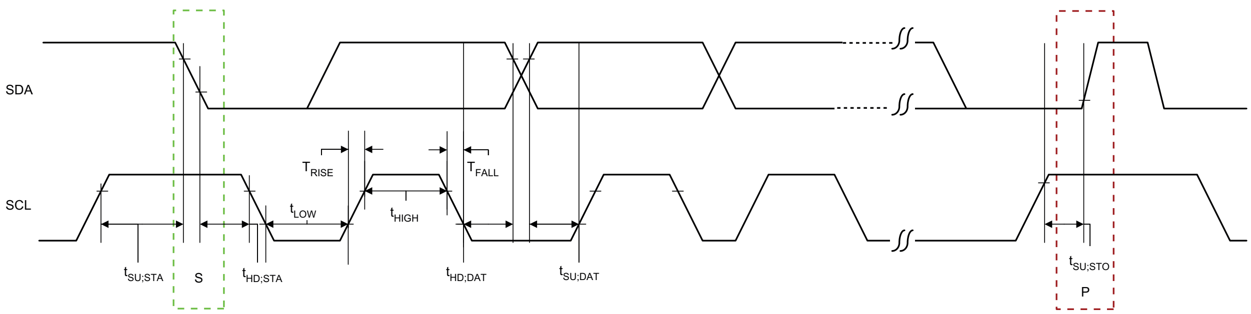


***Figure 2-48* • I2C Timing Parameter Definition**

3 – SmartFusion Development Tools

Designing with SmartFusion cSoCs involves three different types of design: FPGA design, embedded design and analog design. These roles can be filled by three different designers, two designers or even a single designer, depending on company structure and project complexity.

Types of Design Tools

Microsemi has developed design tools and flows to meet the needs of these three types of designers so they can work together smoothly on a single project (Figure 3-1).

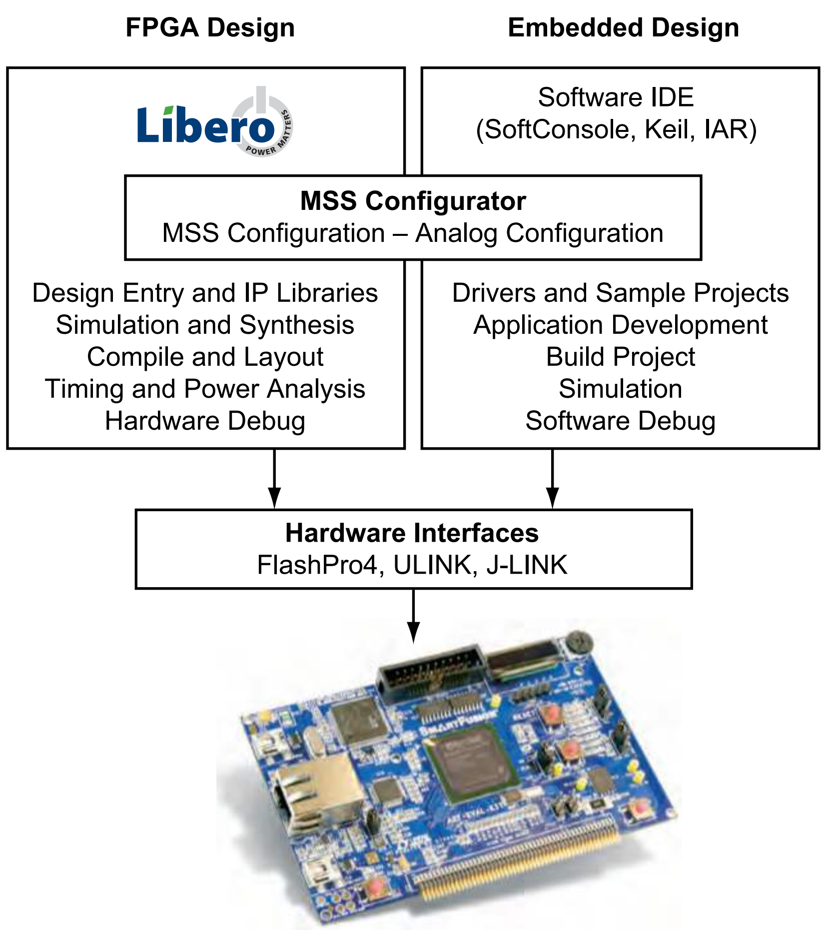


Figure 3-1 • **Three Design Roles**

FPGA Design

Libero System-on-Chip (SoC) software is Microsemi's comprehensive software toolset for designing with all Microsemi FPGAs and cSoCs. Libero SoC includes industry-leading synthesis, simulation and debug tools from Synopsys® and Mentor Graphics®, as well as innovative timing and power optimization and analysis.

Embedded Design

Microsemi offers FREE SoftConsole Eclipse based IDE, which includes the GNU C/C++ compiler and GDB debugger. Microsemi also offers evaluation versions of software from Keil and IAR, with full versions available from respective suppliers.

Analog Design

The MSS configurator provides graphical configuration for current, voltage and temperature monitors, sample sequencing setup and post-processing configuration, as well as DAC output.

The MSS configurator creates a bridge between the FPGA fabric and embedded designers so device configuration can be easily shared between multiple developers.

The MSS configurator includes the following:

- A simple configurator for the embedded designer to control the MSS peripherals and I/Os
- A method to import and view a hardware configuration from the FPGA flow into the embedded flow containing the memory map
- Automatic generation of drivers for any peripherals or soft IP used in the system configuration
- Comprehensive analog configuration for the programmable analog components
- Creation of a standard MSS block to be used in SmartDesign for connection of FPGA fabric designs and IP

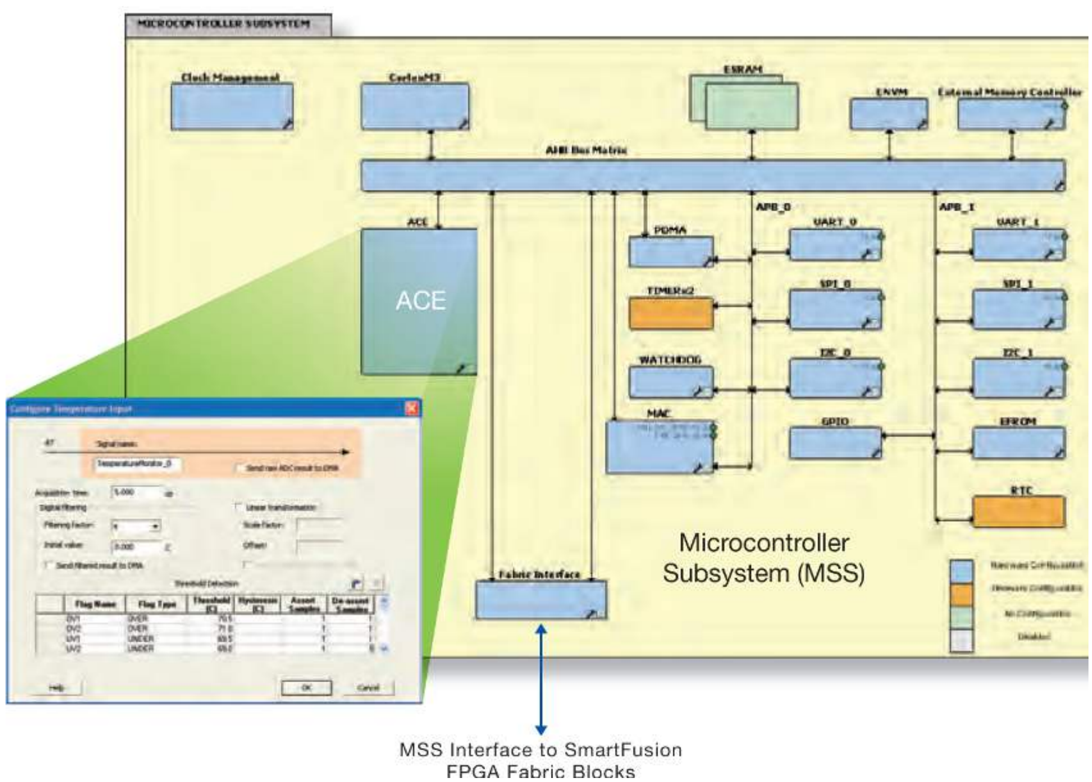


Figure 3-2 • **MSS Configurator**

SmartFusion Ecosystem

The Microsemi SoC Products Group has a long history of supplying comprehensive FPGA development tools and recognizes the benefit of partnering with industry leaders to deliver the optimum usability and productivity to customers. Taking the same approach with processor development, Microsemi has partnered with key industry leaders in the microcontroller space to provide the robust SmartFusion ecosystem.

Microsemi is partnering with Keil and IAR to provide Software IDE support to SmartFusion system designers. The result is a robust solution that can be easily adopted by developers who are already doing embedded design. The learning path is straightforward for FPGA designers.

Support for the SoC Products Group device and ecosystem resources is represented in Figure 3-3.

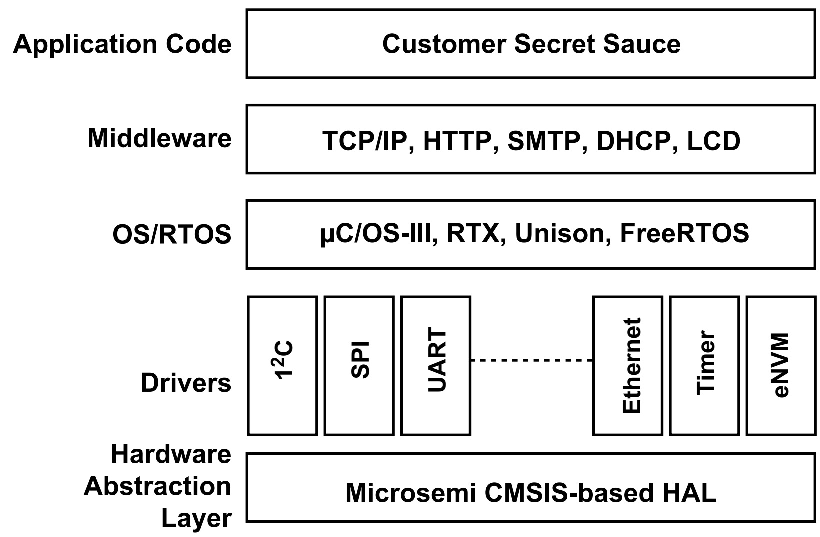


Figure 3-3 • **SmartFusion Ecosystem**

Figure 3-3 shows the SmartFusion stack with examples of drivers, RTOS, and middleware from Microsemi and partners. By leveraging the SmartFusion stack, designers can decide at which level to add their own customization to their design, thus speeding time to market and reducing overhead in the design.

ARM

Because an ARM processor was chosen for SmartFusion cSoCs, Microsemi's customers can benefit from the extensive ARM ecosystem. By building on Microsemi supplied hardware abstraction layer (HAL) and drivers, third party vendors can easily port RTOS and middleware for the SmartFusion cSoC.

- ARM Cortex-M Series Processors
- ARM Cortex-M3 Processor Resource
- ARM Cortex-M3 Technical Reference Manual
- *ARM Cortex-M3 Processor Software Development for ARM7TDMI Processor Programmers* White Paper

Compile and Debug

Microsemi's SoftConsole is a free Eclipse-based IDE that enables the rapid production of C and C++ executables for Microsemi FPGA and cSoCs using Cortex-M3, Cortex-M1 and Core8051s. For SmartFusion support, SoftConsole includes the GNU C/C++ compiler and GDB debugger. Additional examples can be found on the SoftConsole page:

- Using UART with SmartFusion: SoftConsole Standalone Flow Tutorial
  – Design Files
- Displaying POT Level with LEDs: Libero SoC and SoftConsole Flow Tutorial for SmartFusion
  – Design Files

IAR Embedded Workbench® for ARM/Cortex is an integrated development environment for building and debugging embedded ARM applications using assembler, C and C++. It includes a project manager, editor, build and debugger tools with support for RTOS-aware debugging on hardware or in a simulator.

- Designing SmartFusion cSoC with IAR Systems
- IAR Embedded Workbench IDE User Guide for ARM
- Download Evaluation or Kickstart version of IAR Embedded Workbench for ARM

Keil's Microcontroller Development Kit comes in two editions: MDK-ARM and MDK Basic. Both editions feature µVision®, the ARM Compiler, MicroLib, and RTX, but the MDK Basic edition is limited to 256K so that small applications are more affordable.

- Designing SmartFusion cSoC with Keil
- Using Keil µVision and Microsemi SmartFusion cSoC
  – Programming file for use with this tutorial
- Keil Microcontroller Development Kit for ARM Product Manuals
- Download Evaluation version of Keil MDK-ARM

CMSIS COMPLIANT	Microsemi	KEIL An ARM® Company	IAR SYSTEMS
Software IDE	**SoftConsole**	**Vision IDE**	**Embedded Workbench**
Website	www.microsemi.com/soc	www.keil.com	www.iar.com
Free versions from SoC Products Group	Free with Libero SoC	32 K code limited	32 K code limited
Available from Vendor	N/A	Full version	Full version
Compiler	GNU GCC	RealView C/C++	IAR ARM Compiler
Debugger	GDB debug	Vision Debugger	C-SPY Debugger
Instruction Set Simulator	No	Vision Simulator	Yes
Debug Hardware	FlashPro4	ULINK2 or ULINK-ME	J-LINK or J-LINK Lite

Operating Systems

FreeRTOS™ is a portable, open source, royalty free, mini real-time kernel (a free-to-download and free-to-deploy RTOS that can be used in commercial applications without any requirement to expose your proprietary source code). FreeRTOS is scalable and designed specifically for small embedded systems. This FreeRTOS version ported by Microsemi is 6.0.1. For more information, visit the FreeRTOS website: www.freertos.org.

- *SmartFusion Webserver Demo Using uIP and FreeRTOS*
- *SmartFusion cSoC: Running Webserver, TFTP on lwIP TCP/IP Stack* application note

Emcraft Systems provides porting of the open-source U-boot firmware and uClinux™ kernel to the SmartFusion cSoC, a Linux®-based cross-development framework, and other complementary components. Combined with the release of its A2F-Linux Evaluation Kit, this provides a low-cost platform for evaluation and development of Linux (uClinux) on the Cortex-M3 CPU core of the Microsemi SmartFusion cSoC.

- Emcraft Linux on Microsemi's SmartFusion cSoC

Keil offers the RTX Real-Time Kernel as a royalty-free, deterministic RTOS designed for ARM and Cortex-M devices. It allows you to create programs that simultaneously perform multiple functions and helps to create applications which are better structured and more easily maintained.

- The RTX Real-Time Kernel is included with MDK-ARM. Download the Evaluation version of Keil MDK-ARM.
- RTX source code is available as part of Keil/ARM Real-Time Library (RL-ARM), a group of tightly-coupled libraries designed to solve the real-time and communication challenges of embedded systems based on ARM-powered microcontroller devices. The RL-ARM library now supports SmartFusion cSoCs and designers with additional key features listed in the "Middleware" section on page 3-5.

Micrium supports SmartFusion cSoCs with the company's flagship µC/OS family, recognized for a variety of features and benefits, including unparalleled reliability, performance, dependability, impeccable source code and vast documentation. Micrium supports the following products for SmartFusion cSoCs and continues to work with Microsemi on additional projects.

- SmartFusion Quickstart Guide for Micrium µC/OS-III Examples
  - Design Files

µC/OS-III™, Micrium's newest RTOS, is designed to save time on your next embedded project and puts greater control of the software in your hands.

RoweBots provides an ultra tiny Linux-compatible RTOS called Unison for SmartFusion. Unison consists of a set of modular software components, which, like Linux, are either free or commercially licensed. Unison offers POSIX® and Linux compatibility with hard real-time performance, complete I/O modules and an easily understood environment for device driver programming. Seamless integration with FPGA and analog features are fast and easy.

- Unison V4-based products include a free Unison V4 Linux and POSIX-compatible kernel with serial I/O, file system, six demonstration programs, upgraded documentation and source code for Unison V4, and free (for non-commercial use) Unison V4 TCP/IP server. Commercial license upgrade is available for Unison V4 TCP/IP server with three demonstration programs, DHCP client and source code.
- Unison V5-based products include commercial Unison V5 Linux- and POSIX-compatible kernel with serial I/O, file system, extensive feature set, full documentation, source code and more than 20 demonstration programs, Unison V5 TCP/IPv4 with extended feature set, sockets interface, multiple network interfaces, PPP support, DHCP client, documentation, source code and six demonstration programs, and multiple other features.

Middleware

Microsemi has ported both uIP and lwIP for Ethernet support as well as including TFTP file service.

- SmartFusion Webserver Demo Using uIP and FreeRTOS
- SmartFusion: Running Webserver, TFTP on lwIP TCP/IP Stack Application Note

The Keil/ARM Real-Time Library (RL-ARM)[1], in addition to RTX source, includes the following:

- RL-TCPnet (TCP/IP) – The Keil RL-TCPnet library, supporting full TCP/IP and UDP protocols, is a full networking suite specifically written for small ARM and Cortex-M processor-based microcontrollers. TCPnet is now ported to and supports SmartFusion Cortex-M3. It is highly optimized, has a small code footprint, and gives excellent performance, providing a wide range of application level protocols and examples such as FTP, SNMP, SOAP and AJAX. An HTTP server example of TCPnet working in a SmartFusion design is available.

1. *The CAN and USB functions within RL-ARM are not supported for SmartFusion cSoC.*

- Flash File System (RL-Flash) allows your embedded applications to create, save, read, and modify files in standard storage devices such as ROM, RAM, or FlashROM, using a standard serial peripheral interface (SPI). Many ARM-based microcontrollers have a practical requirement for a standard file system. With RL-FlashFS you can implement new features in embedded applications such as data logging, storing program state during standby modes, or storing firmware upgrades.

Micrium, in addition to µC/OS-III®, offers the following support for SmartFusion cSoC:

- µC/TCP-IP™ is a compact, reliable, and high-performance stack built from the ground up by Micrium and has the quality, scalability, and reliability that translates into a rapid configuration of network options, remarkable ease-of-use, and rapid time-to-market.
- µC/Probe™ is one of the most useful tools in embedded systems design and puts you in the driver's seat, allowing you to take charge of virtually any variable, memory location, and I/O port in your embedded product, while your system is running.

4 – SmartFusion Programming

SmartFusion cSoCs have three separate flash areas that can be programmed:

1. The FPGA fabric
2. The embedded nonvolatile memories (eNVMs)
3. The embedded flash ROM (eFROM)

There are essentially three methodologies for programming these areas:

1. In-system programming (ISP)
2. In-application programming (IAP)
   – FPGA fabric, eNVM, and eFROM
3. Pre-programming (non-ISP)

Programming, whether ISP or IAP methodologies are employed, can be done in two ways:

1. Securely using the on chip AES decryption logic
2. In plain text

In-System Programming

In-System Programming is performed with the aid of external JTAG programming hardware. Table 4-1 describes the JTAG programming hardware that will program a SmartFusion cSoC and Table 4-2 defines the JTAG pins that provide the interface for the programming hardware.

***Table 4-1* • Supported JTAG Programming Hardware**

Dongle	Source	JTAG	SWD[1]	SWV[2]	Program FPGA	Program eFROM	Program eNVM
FlashPro3/4	SoC Products Group	Yes	No	No	Yes	Yes	Yes
ULINK Pro	Keil	Yes	Yes	Yes	Yes[3]	Yes[3]	Yes
ULINK2	Keil	Yes	Yes	Yes	Yes[3]	Yes[3]	Yes
IAR J-Link	IAR	Yes	Yes	Yes	Yes[3]	Yes[3]	Yes

Notes:

1. *SWD = ARM Serial Wire Debug*
2. *SWV = ARM Serial Wire Viewer*
3. *Planned support*

***Table 4-2* • JTAG Pin Descriptions**

Pin Name	Description
JTAGSEL	ARM Cortex-M3 or FPGA test access port (TAP) controller selection
TRSTB	Test reset bar
TCK	Test clock
TMS	Test mode select
TDI	Test data input
TDO	Test data output

The JTAGSEL pin selects the FPGA TAP controller or the Cortex-M3 debug logic. When JTAGSEL is asserted, the FPGA TAP controller is selected and the TRSTB input into the Cortex-M3 is held in a reset state (logic 0), as depicted in Figure 4-1. Users should tie the JTAGSEL pin high externally.

Microsemi's free Eclipse-based IDE, SoftConsole, has the ability to control the JTAGSEL pin directly with the FlashPro4 programmer. Manual jumpers are provided on the evaluation and development kits to allow manual selection of this function for the J-Link and ULINK debuggers.

Note: Standard ARM JTAG connectors do not have access to the JTAGSEL pin. SoftConsole automatically selects the appropriate TAP controller using the CTXSELECT JTAG command. When using SoftConsole, the state of JTAGSEL is a "don't care."

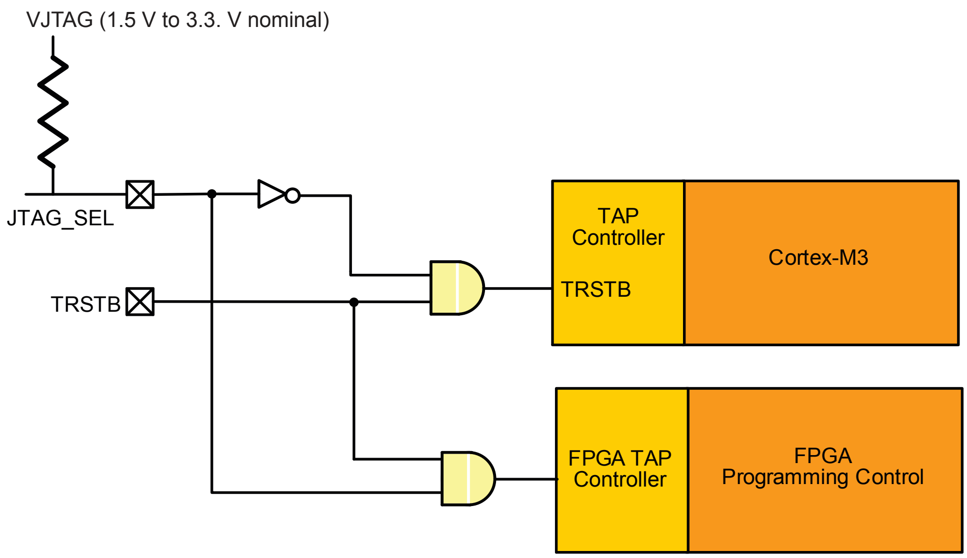


Figure 4-1 • **TRSTB Logic**

In-Application Programming

In-application programming refers to the ability to reprogram the various flash areas under direct supervision of the Cortex-M3.

Reprogramming the FPGA Fabric Using the Cortex-M3

In this mode, the Cortex-M3 is executing the programming algorithm on-chip. The IAP driver can be incorporated into the design project and executed from eNVM or eSRAM. The SoC Products Group provides working example projects for SoftConsole, IAR, and Keil development environments. These can be downloaded via the SoC Products Group Firmware Catalog. The new bitstream to be programmed into the FPGA can reside on the user's printed circuit board (PCB) in a separate SPI flash memory. Alternately, the user can modify the existing projects supplied by the SoC Products Group and, via custom handshaking software, throttle the download of the new image and program the FPGA a piece at a time in real time. A cost-effective and reliable approach would be to store the bitstream in an external SPI flash. Another option is storing a redundant bitstream image in an external SPI flash and loading the newest version into the FPGA only when receiving an IAP command. Since the FPGA I/Os are tristated or held at predefined or last known state during FPGA programming, the user must use MSS I/Os to interface to external memories. Since there are two SPI controllers in the MSS, the user can dedicate one to an SPI flash and the other to the particulars of an application. The amount of flash memory required to program the FPGA always exceeds the size of the eNVM block that is on-chip. The external memory controller (EMC) cannot be used as an interface to a memory device for storage of a bitstream because its I/O pads are FPGA I/Os; hence they are tristated when the FPGA is in a programming state.

Re-Programming the eNVM Blocks Using the Cortex-M3

In this mode the Cortex-M3 is executing the eNVM programming algorithm from eSRAM. Since individual pages (132 bytes) of the eNVM can be write-protected, the programming algorithm software can be protected from inadvertent erasure. When reprogramming the eNVM, both MSS I/Os and FPGA I/Os are available as interfaces for sourcing the new eNVM image. The SoC Products Group provides working example projects for SoftConsole, IAR, and Keil development environments. These can be downloaded via the SoC Products Group Firmware Catalog.

Alternately, the eNVM can be reprogrammed by the Cortex-M3 via the IAP driver. This is necessary when using an encrypted image.

Secure Programming

For background, refer to the "Security in Low Power Flash Devices" chapter of the *Fusion FPGA Fabric User's Guide* on the SoC Products Group website. SmartFusion ISP behaves identically to Fusion ISP. IAP of SmartFusion cSoCs is accomplished by using the IAP driver. Only the FPGA fabric and the eNVM can be reprogrammed with the protection of security measures by using the IAP driver.

Typical Programming and Erase Times

Table 4-3 documents the typical programming and erase times for two components of SmartFusion cSoCs, FPGA fabric and eNVM, using the SoC Products Group's FlashPro hardware and software. These times will be different for other ISP and IAP methods. The **Program** action in FlashPro software includes erase, program, and verify to complete.

The typical programming (including erase) time per page of the eNVM is 8 ms.

***Table 4-3* • Typical Programming and Erase Times**

	FPGA Fabric (seconds)	eNVM (seconds)
Device	**A2F500**	**A2F500**
Erase	21	N/A
Program	15	26
Verify	16	42

References

User's Guides

DirectC User's Guide

http://www.microsemi.com/soc/documents/DirectC_UG.pdf

Fusion FPGA Fabric User's Guide

http://www.microsei.com/soc/documents/Fusion_UG.pdf

Chapters:

"In-System Programming (ISP) of Actel's Low-Power Flash Devices Using FlashPro4/3/3X"

"Security in Low Power Flash Devices"

"Programming Flash Devices"

"Microprocessor Programming of Actel's Low-Power Flash Devices"

5 – Pin Descriptions

Supply Pins

Name	Type	Description
GND	Ground	Digital ground to the FPGA fabric, microcontroller subsystem and GPIOs
GND15ADC0	Ground	Quiet analog ground to the 1.5 V circuitry of the first analog-to-digital converter (ADC)
GND15ADC1	Ground	Quiet analog ground to the 1.5 V circuitry of the second ADC
GND15ADC2	Ground	Quite analog ground to the 1.5 V circuitry of the third ADC
GND33ADC0	Ground	Quiet analog ground to the 3.3 V circuitry of the first ADC
GND33ADC1	Ground	Quiet analog ground to the 3.3 V circuitry of the second ADC
GND33ADC2	Ground	Quiet analog ground to the 3.3 V circuitry of the third ADC
GNDA	Ground	Quiet analog ground to the analog front-end
GNDAQ	Ground	Quiet analog ground to the analog I/O of SmartFusion cSoCs
GNDENVM	Ground	Digital ground to the embedded nonvolatile memory (eNVM)
GNDLPXTAL	Ground	Analog ground to the low power 32 KHz crystal oscillator circuitry
GNDMAINXTAL	Ground	Analog ground to the main crystal oscillator circuitry
GNDQ	Ground	Quiet digital ground supply voltage to input buffers of I/O banks. Within the package, the GNDQ plane is decoupled from the simultaneous switching noise originated from the output buffer ground domain. This minimizes the noise transfer within the package and improves input signal integrity. GNDQ needs to always be connected on the board to GND.
GNDRCOSC	Ground	Analog ground to the integrated RC oscillator circuit
GNDSDD0	Ground	Analog ground to the first sigma-delta DAC
GNDSDD1	Ground	Common analog ground to the second and third sigma-delta DACs
GNDTM0	Ground	Analog temperature monitor common ground for signal conditioning blocks SCB 0 and SCB 1 (see information for pins "TM0" and "TM1" in the "Analog Front-End (AFE)" section on page 5-13).
GNDTM1	Ground	Analog temperature monitor common ground for signal conditioning block SCB 2 and SBCB 3 (see information for pins "TM2" and "TM3" in the "Analog Front-End (AFE)" section on page 5-13).
GNDTM2	Ground	Analog temperature monitor common ground for signal conditioning block SCB4
GNDVAREF	Ground	Analog ground reference used by the ADC. This pad should be connected to a quiet analog ground.
VCC	Supply	Digital supply to the FPGA fabric and MSS, nominally 1.5 V. VCC is also required for powering the JTAG state machine, in addition to VJTAG. Even when a SmartFusion cSoC is in bypass mode in a JTAG chain of interconnected devices, both VCC and VJTAG must remain powered to allow JTAG signals to pass through the SmartFusion cSoC.
VCC15A	Supply	Clean analog 1.5 V supply to the analog circuitry. Always power this pin.

Notes:

1. *The following 3.3 V supplies should be connected together while following proper noise filtering practices: VCC33A, VCC33ADCx, VCC33AP, VCC33SDDx, VCCMAINXTAL, and VCCLPXTAL.*
2. *The following 1.5 V supplies should be connected together while following proper noise filtering practices: VCC, VCC15A, and VCC15ADCx.*

Name	Type	Description
VCC15ADC0	Supply	Analog 1.5 V supply to the first ADC. Always power this pin.
VCC15ADC1	Supply	Analog 1.5 V supply to the second ADC. Always power this pin.
VCC15ADC2	Supply	Analog 1.5 V supply to the third ADC. Always power this pin.
VCC33A	Supply	Clean 3.3 V analog supply to the analog circuitry. VCC33A is also used to feed the 1.5 V voltage regulator for designs that do not provide an external supply to VCC. Refer to the Voltage Regulator (VR), Power Supply Monitor (PSM), and Power Modes section in the *SmartFusion Microcontroller Subsystem User's Guide* for more information.
VCC33ADC0	Supply	Analog 3.3 V supply to the first ADC. Never ground this pin. Can be left floating if unused.[1]
VCC33ADC1	Supply	Analog 3.3 V supply to the second ADC. Never ground this pin. Can be left floating if unused.[1]
VCC33ADC2	Supply	Analog 3.3 V supply to the third ADC. Never ground this pin. Can be left floating if unused.[1]
VCC33AP	Supply	Analog clean 3.3 V supply to the charge pump. To avoid high current draw, VCC33AP should be powered up simultaneously with or after VCC33A. Can be pulled down if unused.[1]
VCC33N	Supply	–3.3 V output from the voltage converter. A 2.2 µF capacitor must be connected from this pin to GND. Analog charge pump capacitors are not needed if none of the analog SCB features are used and none of the SDDs are used. In that case it should be left unconnected.
VCC33SDD0	Supply	Analog 3.3 V supply to the first sigma-delta DAC
VCC33SDD1	Supply	Common analog 3.3 V supply to the second and third sigma-delta DACs
VCCENVM	Supply	Digital 1.5 V power supply to the embedded nonvolatile memory blocks. To avoid high current draw, VCC should be powered up before or simultaneously with VCCENVM.
VCCESRAM	Supply	Digital 1.5 V power supply to the embedded SRAM blocks. Available only on the 208PQFP package. It should be connected to VCC (in other packages, it is internally connected to VCC).
VCCFPGAIOB0	Supply	Digital supply to the FPGA fabric I/O bank 0 (north FPGA I/O bank) for the output buffers and I/O logic. Each bank can have a separate VCCFPGAIO connection. All I/Os in a bank will run off the same VCCFPGAIO supply. VCCFPGAIO can be 1.5 V, 1.8 V, 2.5 V, or 3.3 V, nominal voltage. Unused I/O banks should have their corresponding VCCFPGAIO pins tied to GND.
VCCFPGAIOB1	Supply	Digital supply to the FPGA fabric I/O bank 1 (east FPGA I/O bank) for the output buffers and I/O logic. Each bank can have a separate VCCFPGAIO connection. All I/Os in a bank will run off the same VCCFPGAIO supply. VCCFPGAIO can be 1.5 V, 1.8 V, 2.5 V, or 3.3 V, nominal voltage. Unused I/O banks should have their corresponding VCCFPGAIO pins tied to GND.
VCCFPGAIOB5	Supply	Digital supply to the FPGA fabric I/O bank 5 (west FPGA I/O bank) for the output buffers and I/O logic. Each bank can have a separate VCCFPGAIO connection. All I/Os in a bank will run off the same VCCFPGAIO supply. VCCFPGAIO can be 1.5 V, 1.8 V, 2.5 V, or 3.3 V, nominal voltage. Unused I/O banks should have their corresponding VCCFPGAIO pins tied to GND.

Notes:

1. *The following 3.3 V supplies should be connected together while following proper noise filtering practices: VCC33A, VCC33ADCx, VCC33AP, VCC33SDDx, VCCMAINXTAL, and VCCLPXTAL.*
2. *The following 1.5 V supplies should be connected together while following proper noise filtering practices: VCC, VCC15A, and VCC15ADCx.*

Name	Type	Description
VCCLPXTAL	Supply	Analog supply to the low power 32 KHz crystal oscillator. Always power this pin.[1]
VCCMAINXTAL	Supply	Analog supply to the main crystal oscillator circuit. Always power this pin.[1]
VCCMSSIOB2	Supply	Supply voltage to the microcontroller subsystem I/O bank 2 (east MSS I/O bank) for the output buffers and I/O logic. Each bank can have a separate VCCMSSIO connection. All I/Os in a bank will run off the same VCCMSSIO supply. VCCMSSIO can be 1.5 V, 1.8 V, 2.5 V, or 3.3 V, nominal voltage. Unused I/O banks should have their corresponding VCCMSSIO pins tied to GND.
VCCMSSIOB4	Supply	Supply voltage to the microcontroller subsystem I/O bank 4 (west MSS I/O bank) for the output buffers and I/O logic. Each bank can have a separate VCCMSSIO connection. All I/Os in a bank will run off the same VCCMSSIO supply. VCCMSSIO can be 1.5 V, 1.8 V, 2.5 V, or 3.3 V, nominal voltage. Unused I/O banks should have their corresponding VCCMSSIO pins tied to GND.
VCCPLLx	Supply	Analog 1.5 V supply to the PLL. Always power this pin.
VCCRCOSC	Supply	Analog supply to the integrated RC oscillator circuit. Always power this pin.[1]
VCOMPLAx	Supply	Analog ground for the PLL
VDDBAT	Supply	External battery connection to the low power 32 KHz crystal oscillator (along with VCCLPXTAL), RTC, and battery switchover circuit. Can be pulled down if unused.
VJTAG	Supply	Digital supply to the JTAG controller SmartFusion cSoCs have a separate bank for the dedicated JTAG pins. The JTAG pins can be run at any voltage from 1.5 V to 3.3 V (nominal). Isolating the JTAG power supply in a separate I/O bank gives greater flexibility in supply selection and simplifies power supply and PCB design. If the JTAG interface is neither used nor planned to be used, the V_{JTAG} pin together with the TRSTB pin could be tied to GND. Note that VCC is required to be powered for JTAG operation; VJTAG alone is insufficient. If a SmartFusion cSoC is in a JTAG chain of interconnected boards and it is desired to power down the board containing the device, this can be done provided both VJTAG and VCC to the device remain powered; otherwise, JTAG signals will not be able to transition the device, even in bypass mode. See "JTAG Pins" section on page 5-9.
VPP	Supply	Digital programming circuitry supply SmartFusion cSoCs support single-voltage in-system programming (ISP) of the configuration flash, embedded FlashROM (eFROM), and embedded nonvolatile memory (eNVM). For programming, VPP should be in the 3.3 V ± 5% range. During normal device operation, VPP can be left floating or can be tied to any voltage between 0 V and 3.6 V. When the VPP pin is tied to ground, it shuts off the charge pump circuitry, resulting in no sources of oscillation from the charge pump circuitry. For proper programming, 0.01 µF and 0.33 µF capacitors (both rated at 16 V) are to be connected in parallel across VPP and GND, and positioned as close to the FPGA pins as possible.

Notes:

1. *The following 3.3 V supplies should be connected together while following proper noise filtering practices: VCC33A, VCC33ADCx, VCC33AP, VCC33SDDx, VCCMAINXTAL, and VCCLPXTAL.*
2. *The following 1.5 V supplies should be connected together while following proper noise filtering practices: VCC, VCC15A, and VCC15ADCx.*

User-Defined Supply Pins

Name	Type	Polarity/ Bus Size	Description
VAREF0	Input	1	Analog reference voltage for first ADC The SmartFusion cSoC can be configured to generate a 2.56 V internal reference that can be used by the ADC. While using the internal reference, the reference voltage is output on the VAREFOUT pin for use as a system reference. If a different reference voltage is required, it can be supplied by an external source and applied to this pin. The valid range of values that can be supplied to the ADC is 1.0 V to 3.3 V. When VAREF0 is internally generated, a bypass capacitor must be connected from this pin to ground. The value of the bypass capacitor should be between 3.3 µF and 22 µF, which is based on the needs of the individual designs. The choice of the capacitor value has an impact on the settling time it takes the VAREF0 signal to reach the required specification of 2.56 V to initiate valid conversions by the ADC. If the lower capacitor value is chosen, the settling time required for VAREF0 to achieve 2.56 V will be shorter than when selecting the larger capacitor value. The above range of capacitor values supports the accuracy specification of the ADC, which is detailed in the datasheet. Designers choosing the smaller capacitor value will not obtain as much margin in the accuracy as that achieved with a larger capacitor value. See the Analog-to-Digital Converter (ADC) section in the *SmartFusion Programmable Analog User's Guide* for more information. The SoC Products Group recommends customers use 10 µF as the value of the bypass capacitor. Designers choosing to use an external VAREF0 need to ensure that a stable and clean VAREF0 source is supplied to the VAREF0 pin before initiating conversions by the ADC. To use the internal voltage reference, you must connect the VAREFOUT pin to the appropriate ADC VAREFx input—either the VAREF0 or VAREF1 pin—on the PCB.
VAREF1	Input	1	Analog reference voltage for second ADC See "VAREF0" above for more information.
VAREF2	Input	1	Analog reference voltage for third ADC See "VAREF0" above for more.
VAREFOUT	Out	1	Internal 2.56 V voltage reference output. Can be used to provide the two ADCs with a unique voltage reference externally by connecting VAREFOUT to both VAREF0 and VAREF1. To use the internal voltage reference, you must connect the VAREFOUT pin to the appropriate ADC VAREFx input—either the VAREF0 or VAREF1 pin—on the PCB.

Global I/O Naming Conventions

Gmn (Gxxx) refers to Global I/Os. These Global I/Os are used to connect the input to global networks. Global networks have high fanout and low skew. The naming convention for Global I/Os is as follows:

G = Global

m = Global pin location associated with each CCC on the device:

- A (northwest corner)
- B (northeast corner)
- C (east middle)
- D (southeast corner)
- E (southwest corner)
- F (west middle)

n = Global input MUX and pin number of the associated Global location m—A0, A1, A2, B0, B1, B2, C0, C1, or C2.

Global (GL) I/Os have access to certain clock conditioning circuitry (and the PLL) and/or have direct access to the global network (spines). Additionally, the global I/Os can be used as regular I/Os, since they have identical capabilities.

Unused GL pins are configured as inputs with pull-up resistors. See more detailed descriptions of global I/O connectivity in the clocking resources chapter of the *SmartFusion FPGA Fabric User's Guide* and the clock conditioning circuitry chapter of the *SmartFusion Microcontroller Subsystem User's Guide*.

All inputs labeled GC/GF are direct inputs into the quadrant clocks. The inputs to the global network are multiplexed, and only one input can be used as a global input. For example, if GAA0 is used as a quadrant global input, GAA1 and GAA2 are no longer available for input to the quadrant globals. All inputs labeled GC/GF are direct inputs into the chip-level globals, and the rest are connected to the quadrant globals.

User Pins

Name	Type	Polarity/Bus Size	Description
GPIO_x	In/out	32	Microcontroller Subsystem (MSS) General Purpose I/O (GPIO). The MSS GPIO pin functions as an input, output, tristate, or bidirectional buffer with configurable interrupt generation and Schmitt trigger support. Input and output signal levels are compatible with the I/O standard selected. Unused GPIO pins are tristated and do not include pull-up or pull-down resistors. During power-up, the used GPIO pins are tristated with no pull-up or pull-down resistors until Sys boot configures them. Some of these pins are also multiplexed with integrated peripherals in the MSS (SPI, I^2C, and UART). GPIOs can be routed to dedicated I/O buffers (MSSIOBUF) or in some cases to the FPGA fabric interface through an IOMUX. This allows GPIO pins to be multiplexed as either I/Os for the FPGA fabric, the ARM® Cortex-M3 or for given integrated MSS peripherals. The MSS peripherals are not multiplexed with each other; they are multiplexed only with the GPIO block. For more information, see the General Purpose I/O Block (GPIO) section in the *SmartFusion Microcontroller Subsystem User's Guide*.
IO	In/out		FPGA user I/O

User I/O Naming Conventions

The naming convention used for each FPGA user I/O is Gmn/IOuxwByVz, where:

Gmn is only used for I/Os that also have CCC access—i.e., global pins. Refer to the "Global I/O Naming Conventions" section on page 5-5.

u = I/O pair number in bank, starting at 00 from the northwest I/O bank and proceeding in a clockwise direction.

x = P (positive) or N (negative) or S (single-ended) or R (regular, single-ended).

w = D (Differential Pair), P (Pair), or S (Single-Ended). D (Differential Pair) if both members of the pair are bonded out to adjacent pins or are separated only by one GND or NC pin; P (Pair) if both members of the pair are bonded out but do not meet the adjacency requirement; or S (Single-Ended) if the I/O pair is not bonded out. For Differential Pairs (D), adjacency for ball grid packages means only vertical or horizontal. Diagonal adjacency does not meet the requirements for a true differential pair.

B = Bank

y = Bank number starting at 0 from northwest I/O bank and incrementing clockwise.

V = Reference voltage

z = VREF mini bank number.

The FPGA user I/O pin functions as an input, output, tristate or bidirectional buffer. Input and output signal levels are compatible with the I/O standard selected. Unused I/O pins are disabled by Libero SoC software and include a weak pull-up resistor. During power-up, the used I/O pins are tristated with no pull-up or pull-down resistors until I/O enable (there is a delay after voltage stabilizes, and different I/O banks power up sequentially to avoid a surge of ICCI).

Unused I/Os are configured as follows:

- Output buffer is disabled (with tristate value of high impedance)
- Input buffer is disabled (with tristate value of high impedance)
- Weak pull-up is programmed

Some of these pins are also multiplexed with integrated peripherals in the MSS (Ethernet MAC and external memory controller).

All unused MSS I/Os are tristated by default (with output buffer disabled). However, you can configure it as weak pull-up or pull-down by using Libero SoC I/O attributor window. The Schmitt trigger is disabled. Essentially, I/Os have the reset values as defined in Table 19-25 IOMUX_n_CR, in the *SmartFusion Microcontroller Subsystem User's Guide*.

During programming, I/Os become tristated and weakly pulled up to VCCI. With the VCCI and VCC supplies continuously powered up, when the device transitions from programming to operating mode, the I/Os are instantly configured to the desired user configuration. For more information, see the SmartFusion FPGA User I/Os section in the *SmartFusion FPGA Fabric User’s Guide*.

Special Function Pins

Name	Type	Polarity/Bus Size	Description
NC			No connect This pin is not connected to circuitry within the device. These pins can be driven to any voltage or can be left floating with no effect on the operation of the device.
DC			Do not connect. This pin should not be connected to any signals on the PCB. These pins should be left unconnected.
LPXIN	In	1	Low power 32 KHz crystal oscillator. Input from the 32 KHz oscillator. Pin for connecting a low power 32 KHz watch crystal. If not used, the LPXIN pin can be left floating. For more information, see the PLLs, Clock Conditioning Circuitry, and On-Chip Crystal Oscillators section in the *SmartFusion Microcontroller Subsystem User's Guide*.
LPXOUT	In	1	Low power 32 KHz crystal oscillator. Output to the 32 KHz oscillator. Pin for connecting a low power 32 KHz watch crystal. If not used, the LPXOUT pin can be left floating. For more information, see the PLLs, Clock Conditioning Circuitry, and On-Chip Crystal Oscillators section in the *SmartFusion Microcontroller Subsystem User's Guide*.
MAINXIN	In	1	Main crystal oscillator circuit. Input to the crystal oscillator circuit. Pin for connecting an external crystal, ceramic resonator, or RC network. When using an external crystal or ceramic oscillator, external capacitors are also recommended. Refer to documentation from the crystal oscillator manufacturer for proper capacitor value. If using an external RC network or clock input, MAINXIN should be grounded for better noise immunity. For more information, see the PLLs, Clock Conditioning Circuitry, and On-Chip Crystal Oscillators section in the *SmartFusion Microcontroller Subsystem User's Guide*.
MAINXOUT	Out	1	Main crystal oscillator circuit. Output from the crystal oscillator circuit. Pin for connecting external crystal or ceramic resonator. When using an external crystal or ceramic oscillator, external capacitors are also recommended. Refer to documentation from the crystal oscillator manufacturer for proper capacitor value. If using external RC network or clock input, MAINXIN should be grounded and MAINXOUT left unconnected. For more information, see the PLLs, Clock Conditioning Circuitry, and On-Chip Crystal Oscillators section in the *SmartFusion Microcontroller Subsystem User's Guide*.
NCAP		1	Negative capacitor connection. This is the negative terminal of the charge pump. A capacitor, with a 2.2 µF recommended value, is required to connect between PCAP and NCAP. Analog charge pump capacitors are not needed if none of the analog SCB features are used and none of the SDDs are used. In that case it should be left unconnected.

Name	Type	Polarity/Bus Size	Description
PCAP		1	Positive Capacitor connection. This is the positive terminal of the charge pump. A capacitor, with a 2.2 μF recommended value, is required to connect between PCAP and NCAP. If this pin is not used, it must be left unconnected/floating. In this case, no capacitor is needed. Analog charge pump capacitors are not needed if none of the analog SCB features are used, and none of the SDDs are used.
PTBASE		1	Pass transistor base connection This is the control signal of the voltage regulator. This pin should be connected to the base of an external pass transistor used with the 1.5 V internal voltage regulator and can be floating if not used.
PTEM		1	Pass transistor emitter connection. This is the feedback input of the voltage regulator. This pin should be connected to the emitter of an external pass transistor used with the 1.5 V internal voltage regulator and can be floating if not used.
MSS_RESET_N		Low	Low Reset signal which can be used as an external reset and can also be used as a system level reset under control of the Cortex-M3 processor. MSS_RESET_N is an output asserted low after power-on reset. The direction of MSS_RESET_N changes during the execution of the Microsemi System Boot when chip-level reset is enabled. The Microsemi System Boot reconfigures MSS_RESET_N to become a reset input signal when chip-level reset is enabled. It has an internal pull-up so it can be left floating. In the current software, the MSS_RESET_N is modeled as an external input signal only.
PU_N	In	Low	Push-button is the connection for the external momentary switch used to turn on the 1.5 V voltage regulator and can be floating if not used.

JTAG Pins

SmartFusion cSoCs have a separate bank for the dedicated JTAG pins. The JTAG pins can be run at any voltage from 1.5 V to 3.3 V (nominal). VCC must also be powered for the JTAG state machine to operate, even if the device is in bypass mode; VJTAG alone is insufficient. Both VJTAG and VCC to the SmartFusion cSoC part must be supplied to allow JTAG signals to transition the SmartFusion cSoC. Isolating the JTAG power supply in a separate I/O bank gives greater flexibility with supply selection and simplifies power supply and PCB design. If the JTAG interface is neither used nor planned to be used, the VJTAG pin together with the TRSTB pin could be tied to GND.

Name	Type	Polarity/ Bus Size	Description
JTAGSEL	In	1	JTAG controller selection Depending on the state of the JTAGSEL pin, an external JTAG controller will either see the FPGA fabric TAP/auxiliary TAP (High) or the Cortex-M3 JTAG debug interface (Low). The JTAGSEL pin should be connected to an external pull-up resistor such that the default configuration selects the FPGA fabric TAP.
TCK	In	1	Test clock Serial input for JTAG boundary scan, ISP, and UJTAG. The TCK pin does not have an internal pull-up/-down resistor. If JTAG is not used, it is recommended to tie off TCK to GND or V_{JTAG} through a resistor placed close to the FPGA pin. This prevents JTAG operation in case TMS enters an undesired state. Note that to operate at all V_{JTAG} voltages, 500 Ω to 1 kΩ will satisfy the requirements. Refer to Table 5-1 on page 5-10 for more information. Can be left floating when unused.
TDI	In	1	Test data Serial input for JTAG boundary scan, ISP, and UJTAG usage. There is an internal weak pull-up resistor on the TDI pin.
TDO	Out	1	Test data Serial output for JTAG boundary scan, ISP, and UJTAG usage.
TMS	In	HIGH	Test mode select The TMS pin controls the use of the IEEE1532 boundary scan pins (TCK, TDI, TDO, TRST). There is an internal weak pull-up resistor on the TMS pin. Can be left floating when unused.
TRSTB	In	HIGH	Boundary scan reset pin The TRST pin functions as an active low input to asynchronously initialize (or reset) the boundary scan circuitry. There is an internal weak pull-up resistor on the TRST pin. If JTAG is not used, an external pull-down resistor could be included to ensure the TAP is held in reset mode. The resistor values must be chosen from Table 5-1 on page 5-10 and must satisfy the parallel resistance value requirement. The values in Table 5-1 on page 5-10 correspond to the resistor recommended when a single device is used. The values correspond to the equivalent parallel resistor when multiple devices are connected via a JTAG chain. In critical applications, an upset in the JTAG circuit could allow entering an undesired JTAG state. In such cases, it is recommended that you tie off TRST to GND through a resistor placed close to the FPGA pin. The TRSTB pin also resets the serial wire JTAG – debug port (SWJ-DP) circuitry within the Cortex-M3. Can be left floating when unused.

***Table 5-1* • Recommended Tie-Off Values for the TCK and TRST Pins**

VJTAG	Tie-Off Resistance[1, 2]
VJTAG at 3.3 V	200 Ω to 1 kΩ
VJTAG at 2.5 V	200 Ω to 1 kΩ
VJTAG at 1.8 V	500 Ω to 1 kΩ
VJTAG at 1.5 V	500 Ω to 1 kΩ

Notes:

1. *The TCK pin can be pulled up/down.*
2. *The TRST pin can only be pulled down.*
1. *Equivalent parallel resistance if more than one device is on JTAG chain.*

Microcontroller Subsystem (MSS)

Name	Type	Polarity/ Bus Size	Description
External Memory Controller			
EMC_ABx	Out	26	External memory controller address bus Can also be used as an FPGA user I/O (see "IO" on page 5-5).
EMC_BYTENx	Out	LOW/2	External memory controller byte enable Can also be used as an FPGA user I/O (see "IO" on page 5-5).
EMC_CLK	Out	Rise	External memory controller clock Can also be used as an FPGA user I/O (see "IO" on page 5-5).
EMC_CSx_N	Out	LOW/2	External memory controller chip selects Can also be used as an FPGA User IO (see "IO" on page 5-5).
EMC_DBx	In/out	16	External memory controller data bus Can also be used as an FPGA user I/O (see "IO" on page 5-5).
EMC_OENx_N	Out	LOW/2	External memory controller output enables Can also be used as an FPGA User IO (see "IO" on page 5-5).
EMC_RW_N	Out	Level	External memory controller read/write. Read = High, write = Low. Can also be used as an FPGA user I/O (see "IO" on page 5-5).
Inter-Integrated Circuit (I^2C) Peripherals			
I2C_0_SCL	In/out	1	I^2C bus serial clock output. First I^2C. Can also be used as an MSS GPIO (see "GPIO_x" on page 5-5).
I2C_0_SDA	In/out	1	I^2C bus serial data input/output. First I^2C. Can also be used as an MSS GPIO (see "GPIO_x" on page 5-5).
I2C_1_SCL	In/out	1	I^2C bus serial clock output. Second I^2C. Can also be used as an MSS GPIO (see "GPIO_x" on page 5-5).
I2C_1_SDA	In/out	1	I^2C bus serial data input/output. Second I^2C. Can also be used as an MSS GPIO (see "GPIO_x" on page 5-5).
Serial Peripheral Interface (SPI) Controllers			
SPI_0_CLK	Out	1	Clock. First SPI. Can also be used as an MSS GPIO (see "GPIO_x" on page 5-5).
SPI_0_DI	In	1	Data input. First SPI. Can also be used as an MSS GPIO (see "GPIO_x" on page 5-5).
SPI_0_DO	Out	1	Data output. First SPI. Can also be used as an MSS GPIO (see "GPIO_x" on page 5-5).
SPI_0_SS	Out	1	Slave select (chip select). First SPI. Can also be used as an MSS GPIO (see "GPIO_x" on page 5-5).
SPI_1_CLK	Out	1	Clock. Second SPI. Can also be used as an MSS GPIO (see "GPIO_x" on page 5-5).
SPI_1_DI	In	1	Data input. Second SPI. Can also be used as an MSS GPIO (see "GPIO_x" on page 5-5).

Name	Type	Polarity/ Bus Size	Description
SPI_1_DO	Out	1	Data output. Second SPI. Can also be used as an MSS GPIO (see "GPIO_x" on page 5-5).
SPI_1_SS	Out	1	Slave select (chip select). Second SPI. Can also be used as an MSS GPIO (see "GPIO_x" on page 5-5).
Universal Asynchronous Receiver/Transmitter (UART) Peripherals			
UART_0_RXD	In	1	Receive data. First UART. Can also be used as an MSS GPIO (see "GPIO_x" on page 5-5).
UART_0_TXD	Out	1	Transmit data. First UART. Can also be used as an MSS GPIO (see "GPIO_x" on page 5-5).
UART_1_RXD	In	1	Receive data. Second UART. Can also be used as an MSS GPIO (see "GPIO_x" on page 5-5).
UART_1_TXD	Out	1	Transmit data. Second UART. Can also be used as an MSS GPIO (see "GPIO_x" on page 5-5).
Ethernet MAC			
MAC_CLK	In	Rise	Receive clock. 50 MHz ± 50 ppm clock source received from RMII PHY. Can be left floating when unused.
MAC_CRSDV	In	High	Carrier sense/receive data valid for RMII PHY Can also be used as an FPGA User IO (see "IO" on page 5-5).
MAC_MDC	Out	Rise	RMII management clock Can also be used as an FPGA User IO (see "IO" on page 5-5).
MAC_MDIO	In/Out	1	RMII management data input/output Can also be used as an FPGA User IO (see "IO" on page 5-5).
MAC_RXDx	In	2	Ethernet MAC receive data. Data recovered and decoded by PHY. The RXD[0] signal is the least significant bit. Can also be used as an FPGA User I/O (see "IO" on page 5-5).
MAC_RXER	In	HIGH	Ethernet MAC receive error. If MACRX_ER is asserted during reception, the frame is received and status of the frame is updated with MACRX_ER. Can also be used as an FPGA user I/O (see "IO" on page 5-5).
MAC_TXDx	Out	2	Ethernet MAC transmit data. The TXD[0] signal is the least significant bit. Can also be used as an FPGA user I/O (see "IO" on page 5-5).
MAC_TXEN	Out	HIGH	Ethernet MAC transmit enable. When asserted, indicates valid data for the PHY on the TXD port. Can also be used as an FPGA User I/O (see "IO" on page 5-5).

Analog Front-End (AFE)

Name	Type	Description	Associated With	
			ADC/SDD	SCB
ABPS0	In	SCB 0 / active bipolar prescaler input 1. See the Active Bipolar Prescaler (ABPS) section in the *SmartFusion Programmable Analog User's Guide*.	ADC0	SCB0
ABPS1	In	SCB 0 / active bipolar prescaler Input 2	ADC0	SCB0
ABPS2	In	SCB 1 / active bipolar prescaler Input 1	ADC0	SCB1
ABPS3	In	SCB 1 / active bipolar prescaler Input 2	ADC0	SCB1
ABPS4	In	SCB 2 / active bipolar prescaler Input 1	ADC1	SCB2
ABPS5	In	SCB 2 / active bipolar prescaler Input 2	ADC1	SCB2
ABPS6	In	SCB 3 / active bipolar prescaler Input 1	ADC1	SCB3
ABPS7	In	SCB 3 / active bipolar prescaler input 2	ADC1	SCB3
ABPS8	In	SCB 4 / active bipolar prescaler input 1	ADC2	SCB4
ABPS9	In	SCB 4 / active bipolar prescaler input 2	ADC2	SCB4
ADC0	In	ADC 0 direct input 0 / FPGA Input. See the "Sigma-Delta Digital-to-Analog Converter (DAC)" section in the *SmartFusion Programmable Analog User's Guide*.	ADC0	SCB0
ADC1	In	ADC 0 direct input 1 / FPGA input	ADC0	SCB0
ADC2	In	ADC 0 direct input 2 / FPGA input	ADC0	SCB1
ADC3	In	ADC 0 direct input 3 / FPGA input	ADC0	SCB1
ADC4	In	ADC 1 direct input 0 / FPGA input	ADC1	SCB2
ADC5	In	ADC 1 direct input 1 / FPGA input	ADC1	SCB2
ADC6	In	ADC 1 direct input 2 / FPGA input	ADC1	SCB3
ADC7	In	ADC 1 direct input 3 / FPGA input	ADC1	SCB3
ADC8	In	ADC 2 direct input 0 / FPGA input	ADC2	SCB4
ADC9	In	ADC 2 direct input 1 / FPGA input	ADC2	SCB4
ADC10	In	ADC 2 direct input 2 / FPGA input	ADC2	N/A
ADC11	In	ADC 2 direct input 3 / FPGA input	ADC2	N/A
CM0	In	SCB 0 / high side of current monitor / comparator Positive input. See the Current Monitor section in the *SmartFusion Programmable Analog User's Guide*.	ADC0	SCB0
CM1	In	SCB 1 / high side of current monitor / comparator. Positive input.	ADC0	SCB1
CM2	In	SCB 2 / high side of current monitor / comparator. Positive input.	ADC1	SCB2
CM3	In	SCB 3 / high side of current monitor / comparator. Positive input.	ADC1	SCB3
CM4	In	SCB 4 / high side of current monitor / comparator. Positive input.	ADC2	SCB4

Note: Unused analog inputs should be grounded. This aids in shielding and prevents an undesired coupling path.

Name	Type	Description	Associated With	
			ADC/SDD	SCB
TM0	In	SCB 0 / low side of current monitor / comparator Negative input / high side of temperature monitor. See the Temperature Monitor section.	ADC0	SCB0
TM1	In	SCB 1 / low side of current monitor / comparator. Negative input / high side of temperature monitor.	ADC0	SCB1
TM2	In	SCB 2 / low side of current monitor / comparator. Negative input / high side of temperature monitor.	ADC1	SCB2
TM3	In	SCB 3 low side of current monitor / comparator. Negative input / high side of temperature monitor.	ADC1	SCB3
TM4	In	SCB 4 low side of current monitor / comparator. Negative input / high side of temperature monitor.	ADC2	SCB4
SDD0	Out	Output of SDD0 See the Sigma-Delta Digital-to-Analog Converter (DAC) section in the *SmartFusion Programmable Analog User's Guide*.	SDD0	N/A
SDD1	Out	Output of SDD1	SDD1	N/A
SDD2	Out	Output of SDD2	SDD2	N/A

Note: Unused analog inputs should be grounded. This aids in shielding and prevents an undesired coupling path.

Analog Front-End Pin-Level Function Multiplexing

Table 5-2 describes the relationships between the various internal signals found in the analog front-end (AFE) and how they are multiplexed onto the external package pins. Note that, in general, only one function is available for those pads that have numerous functions listed. The exclusion to this rule is when a comparator is used; the ADC can still convert either input side of the comparator.

***Table 5-2* • Relationships Between Signals in the Analog Front-End**

Pin	ADC Channel	Dir.-In Option	Prescaler	Current Mon.	Temp. Mon.	Compar.	LVTTL	SDD MUX	SDD
ABPS0	ADC0_CH1		ABPS0_IN						
ABPS1	ADC0_CH2		ABPS1_IN						
ABPS2	ADC0_CH5		ABPS2_IN						
ABPS3	ADC0_CH6		ABPS3_IN						
ABPS4	ADC1_CH1		ABPS4_IN						
ABPS5	ADC1_CH2		ABPS5_IN						
ABPS6	ADC1_CH5		ABPS6_IN						
ABPS7	ADC1_CH6		ABPS7_IN						
ABPS8	ADC2_CH1		ABPS8_IN						
ABPS9	ADC2_CH2		ABPS9_IN						
ADC0	ADC0_CH9	Yes				CMP1_P	LVTTL0_IN		
ADC1	ADC0_CH10	Yes				CMP1_N	LVTTL1_IN	SDDM0_OUT	
ADC2	ADC0_CH11	Yes				CMP3_P	LVTTL2_IN		
ADC3	ADC0_CH12	Yes				CMP3_N	LVTTL3_IN	SDDM1_OUT	
ADC4	ADC1_CH9	Yes				CMP5_P	LVTTL4_IN		
ADC5	ADC1_CH10	Yes				CMP5_N	LVTTL5_IN	SDDM2_OUT	
ADC6	ADC1_CH11	Yes				CMP7_P	LVTTL6_IN		
ADC7	ADC1_CH12	Yes				CMP7_N	LVTTL7_IN	SDDM3_OUT	
ADC8	ADC2_CH9	Yes				CMP9_P	LVTTL8_IN		
ADC9	ADC2_CH10	Yes				CMP9_N	LVTTL9_IN	SDDM4_OUT	
ADC10	ADC2_CH11	Yes					LVTTL10_IN		
ADC11	ADC2_CH12	Yes					LVTTL11_IN		
CM0	ADC0_CH3	Yes		CM0_H		CMP0_P			
CM1	ADC0_CH7	Yes		CM1_H		CMP2_P			
CM2	ADC1_CH3	Yes		CM2_H		CMP4_P			
CM3	ADC1_CH7	Yes		CM3_H		CMP6_P			
CM4	ADC2_CH3	Yes		CM4_H		CMP8_P			
SDD0	ADC0_CH15								SDD0_OUT
SDD1	ADC1_CH15								SDD1_OUT

Notes:

1. *ABPSx_IN: Input to active bipolar prescaler channel x.*
2. *CMx_H/L: Current monitor channel x, high/low side.*
3. *TMx_IO: Temperature monitor channel x.*
4. *CMPx_P/N: Comparator channel x, positive/negative input.*
5. *LVTTLx_IN: LVTTL I/O channel x.*
6. *SDDMx_OUT: Output from sigma-delta DAC MUX channel x.*
7. *SDDx_OUT: Direct output from sigma-delta DAC channel x.*

Table 5-2 • Relationships Between Signals in the Analog Front-End

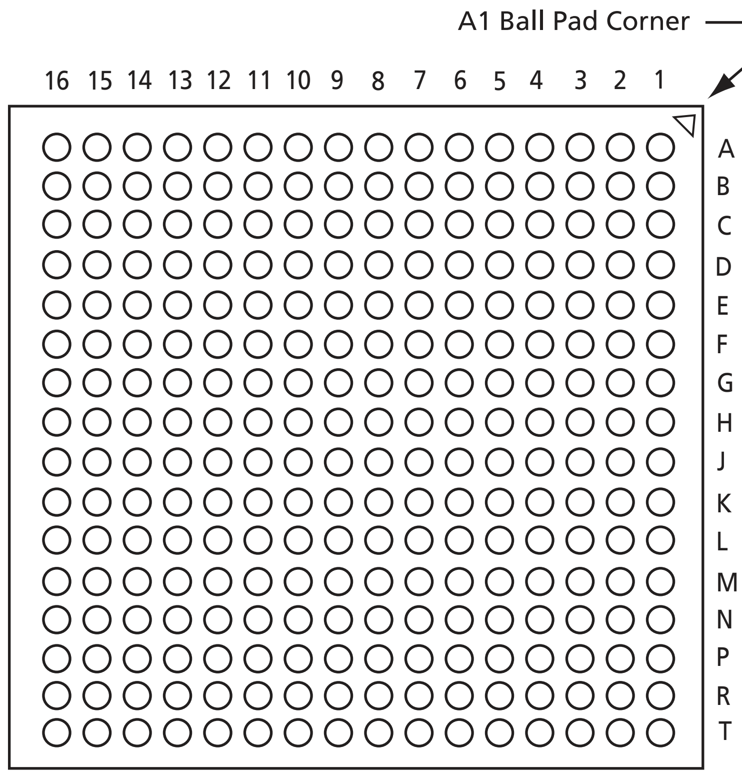
Pin	ADC Channel	Dir.-In Option	Prescaler	Current Mon.	Temp. Mon.	Compar.	LVTTL	SDD MUX	SDD
SDD2	ADC2_CH15								SDD2_OUT
TM0	ADC0_CH4	Yes		CM0_L	TM0_IO	CMP0_N			
TM1	ADC0_CH8	Yes		CM1_L	TM1_IO	CMP2_N			
TM2	ADC1_CH4	Yes		CM2_L	TM2_IO	CMP4_N			
TM3	ADC1_CH8	Yes		CM3_L	TM3_IO	CMP6_N			
TM4	ADC2_CH4	Yes		CM4_L	TM4_IO	CMP8_N			

Notes:

1. *ABPSx_IN: Input to active bipolar prescaler channel x.*
2. *CMx_H/L: Current monitor channel x, high/low side.*
3. *TMx_IO: Temperature monitor channel x.*
4. *CMPx_P/N: Comparator channel x, positive/negative input.*
5. *LVTTLx_IN: LVTTL I/O channel x.*
6. *SDDMx_OUT: Output from sigma-delta DAC MUX channel x.*
7. *SDDx_OUT: Direct output from sigma-delta DAC channel x.*

Pin Assignment Tables

FG256



Note

For Package Manufacturing and Environmental information, visit the Resource Center at http://www.microsemi.com/soc/products/solutions/package/docs.aspx.

Pin No.	FG256	
	A2F060 Function	A2F500 Function
A1	GND	GND
A2	VCCFPGAIOB0	VCCFPGAIOB0
A3	EMC_AB[0]/IO04NDB0V0	EMC_AB[0]/IO06NDB0V0
A4	EMC_AB[1]/IO04PDB0V0	EMC_AB[1]/IO06PDB0V0
A5	GND	GND
A6	EMC_AB[3]/IO05PDB0V0	EMC_AB[3]/IO09PDB0V0
A7	EMC_AB[5]/IO06PDB0V0	EMC_AB[5]/IO10PDB0V0
A8	VCCFPGAIOB0	VCCFPGAIOB0
A9	GND	GND
A10	EMC_AB[14]/IO11NDB0V0	EMC_AB[14]/IO15NDB0V0
A11	EMC_AB[15]/IO11PDB0V0	EMC_AB[15]/IO15PDB0V0
A12	GND	GND
A13	EMC_AB[20]/IO14NDB0V0	EMC_AB[20]/IO21NDB0V0
A14	EMC_AB[24]/IO16NDB0V0	EMC_AB[24]/IO20NDB0V0
A15	VCCFPGAIOB0	VCCFPGAIOB0
A16	GND	GND
B1	EMC_DB[15]/IO45PDB5V0	EMC_DB[15]/GAA2/IO88PDB5V0
B2	GND	GND
B3	EMC_BYTEN[1]/IO02PDB0V0	EMC_BYTEN[1]/GAC1/IO07PDB0V0
B4	EMC_OEN0_N/IO03NDB0V0	EMC_OEN0_N/IO08NDB0V0
B5	EMC_OEN1_N/IO03PDB0V0	EMC_OEN1_N/IO08PDB0V0
B6	EMC_AB[2]/IO05NDB0V0	EMC_AB[2]/IO09NDB0V0
B7	EMC_AB[4]/IO06NDB0V0	EMC_AB[4]/IO10NDB0V0
B8	EMC_AB[9]/IO08PDB0V0	EMC_AB[9]/IO13PDB0V0
B9	EMC_AB[12]/IO10NDB0V0	EMC_AB[12]/IO14NDB0V0
B10	EMC_AB[13]/IO10PDB0V0	EMC_AB[13]/IO14PDB0V0
B11	EMC_AB[16]/IO12NDB0V0	EMC_AB[16]/IO17NDB0V0
B12	EMC_AB[18]/IO13NDB0V0	EMC_AB[18]/IO18NDB0V0
B13	EMC_AB[21]/IO14PDB0V0	EMC_AB[21]/IO21PDB0V0
B14	EMC_AB[25]/IO16PDB0V0	EMC_AB[25]/IO20PDB0V0
B15	GND	GND
B16	GNDQ	GNDQ
C1	EMC_DB[14]/IO45NDB5V0	EMC_DB[14]/GAB2/IO88NDB5V0

Note: Shading denotes pins that do not have completely identical functions from density to density. For example, the bank assignment can be different for an I/O, or the function might be available only on a larger density device.

Pin No.	FG256	
	A2F060 Function	A2F500 Function
C2	VCCPLL0	VCCPLL0
C3	EMC_BYTEN[0]/IO02NDB0V0	EMC_BYTEN[0]/GAC0/IO07NDB0V0
C4	VCCFPGAIOB0	VCCFPGAIOB0
C5	EMC_CS0_N/IO01NDB0V0	EMC_CS0_N/GAB0/IO05NDB0V0
C6	EMC_CS1_N/IO01PDB0V0	EMC_CS1_N/GAB1/IO05PDB0V0
C7	GND	GND
C8	EMC_AB[8]/IO08NDB0V0	EMC_AB[8]/IO13NDB0V0
C9	EMC_AB[11]/IO09PDB0V0	EMC_AB[11]/IO11PDB0V0
C10	VCCFPGAIOB0	VCCFPGAIOB0
C11	EMC_AB[17]/IO12PDB0V0	EMC_AB[17]/IO17PDB0V0
C12	EMC_AB[19]/IO13PDB0V0	EMC_AB[19]/IO18PDB0V0
C13	GND	GND
C14	GCC0/IO18NPB0V0	GBA2/IO27PPB1V0
C15	GCB0/IO19NDB0V0	GCA2/IO28PDB1V0
C16	GCB1/IO19PDB0V0	IO28NDB1V0
D1	VCCFPGAIOB5	VCCFPGAIOB5
D2	VCOMPLA0	VCOMPLA0
D3	GND	GND
D4	GNDQ	GNDQ
D5	EMC_CLK/IO00NDB0V0	EMC_CLK/GAA0/IO02NDB0V0
D6	EMC_RW_N/IO00PDB0V0	EMC_RW_N/GAA1/IO02PDB0V0
D7	EMC_AB[6]/IO07NDB0V0	EMC_AB[6]/IO12NDB0V0
D8	EMC_AB[7]/IO07PDB0V0	EMC_AB[7]/IO12PDB0V0
D9	EMC_AB[10]/IO09NDB0V0	EMC_AB[10]/IO11NDB0V0
D10	EMC_AB[22]/IO15NDB0V0	EMC_AB[22]/IO19NDB0V0
D11	EMC_AB[23]/IO15PDB0V0	EMC_AB[23]/IO19PDB0V0
D12	GNDQ	GNDQ
D13	GCC1/IO18PPB0V0	GBB2/IO27NPB1V0
D14	GCA0/IO20NDB0V0	GCB2/IO33PDB1V0
D15	GCA1/IO20PDB0V0	IO33NDB1V0
D16	VCCFPGAIOB1	VCCFPGAIOB1
E1	EMC_DB[13]/IO44PDB5V0	EMC_DB[13]/GAC2/IO87PDB5V0
E2	EMC_DB[12]/IO44NDB5V0	EMC_DB[12]/IO87NDB5V0

Note: Shading denotes pins that do not have completely identical functions from density to density. For example, the bank assignment can be different for an I/O, or the function might be available only on a larger density device.

Pin No.	FG256	
	A2F060 Function	A2F500 Function
E3	GFA2/IO42PDB5V0	GFA2/IO85PDB5V0
E4	EMC_DB[10]/IO43NPB5V0	EMC_DB[10]/IO86NPB5V0
E5	GNDQ	GNDQ
E6	GND	GND
E7	VCCFPGAIOB0	VCCFPGAIOB0
E8	GND	GND
E9	VCCFPGAIOB0	VCCFPGAIOB0
E10	GND	GND
E11	VCCFPGAIOB0	VCCFPGAIOB0
E12	GCB2/IO22PDB1V0	GCA1/IO36PDB1V0
E13	VCCFPGAIOB1	VCCFPGAIOB1
E14	GCA2/IO21PDB1V0	GCB1/IO34PDB1V0
E15	GCC2/IO23PDB1V0	GDC1/IO38PDB1V0
E16	IO23NDB1V0	GDC0/IO38NDB1V0
F1	EMC_DB[9]/IO40PDB5V0	EMC_DB[9]/GEC1/IO80PDB5V0
F2	GND	GND
F3	GFB2/IO42NDB5V0	GFB2/IO85NDB5V0
F4	VCCFPGAIOB5	VCCFPGAIOB5
F5	EMC_DB[11]/IO43PPB5V0	EMC_DB[11]/IO86PPB5V0
F6	VCCFPGAIOB5	VCCFPGAIOB5
F7	GND	GND
F8	VCC	VCC
F9	GND	GND
F10	VCC	VCC
F11	GND	GND
F12	IO22NDB1V0	GCA0/IO36NDB1V0
F13	NC	GNDQ
F14	IO21NDB1V0	GCB0/IO34NDB1V0
F15	GND	GND
F16	VCCENVM	VCCENVM
G1	EMC_DB[8]/IO40NDB5V0	EMC_DB[8]/GEC0/IO80NDB5V0
G2	EMC_DB[7]/IO39PDB5V0	EMC_DB[7]/GEB1/IO79PDB5V0
G3	EMC_DB[6]/IO39NDB5V0	EMC_DB[6]/GEB0/IO79NDB5V0

Note: Shading denotes pins that do not have completely identical functions from density to density. For example, the bank assignment can be different for an I/O, or the function might be available only on a larger density device.

Pin No.	FG256	
	A2F060 Function	A2F500 Function
G4	GFC2/IO41PDB5V0	GFC2/IO84PDB5V0
G5	IO41NDB5V0	IO84NDB5V0
G6	GND	GND
G7	VCC	VCC
G8	GND	GND
G9	VCC	VCC
G10	GND	GND
G11	VCCFPGAIOB1	VCCFPGAIOB1
G12	VPP	VPP
G13	TRSTB	TRSTB
G14	TMS	TMS
G15	TCK	TCK
G16	GNDENVM	GNDENVM
H1	GND	GND
H2	EMC_DB[5]/IO38PPB5V0	EMC_DB[5]/GEA1/IO78PPB5V0
H3	VCCFPGAIOB5	VCCFPGAIOB5
H4	EMC_DB[1]/IO36PDB5V0	EMC_DB[1]/GEB2/IO76PDB5V0
H5	EMC_DB[0]/IO36NDB5V0	EMC_DB[0]/GEA2/IO76NDB5V0
H6	VCCFPGAIOB5	VCCFPGAIOB5
H7	GND	GND
H8	VCC	VCC
H9	GND	GND
H10	VCC	VCC
H11	GND	GND
H12	VJTAG	VJTAG
H13	TDO	TDO
H14	TDI	TDI
H15	JTAGSEL	JTAGSEL
H16	GND	GND
J1	EMC_DB[4]/IO38NPB5V0	EMC_DB[4]/GEA0/IO78NPB5V0
J2	EMC_DB[3]/IO37PDB5V0	EMC_DB[3]/GEC2/IO77PDB5V0
J3	EMC_DB[2]/IO37NDB5V0	EMC_DB[2]/IO77NDB5V0
J4	GNDRCOSC	GNDRCOSC

Note: Shading denotes pins that do not have completely identical functions from density to density. For example, the bank assignment can be different for an I/O, or the function might be available only on a larger density device.

Pin No.	FG256	
	A2F060 Function	A2F500 Function
J5	NC	GNDQ
J6	GND	GND
J7	VCC	VCC
J8	GND	GND
J9	VCC	VCC
J10	GND	GND
J11	VCCMSSIOB2	VCCMSSIOB2
J12	I2C_0_SCL/GPIO_23	I2C_0_SCL/GPIO_23
J13	I2C_0_SDA/GPIO_22	I2C_0_SDA/GPIO_22
J14	I2C_1_SCL/GPIO_31	I2C_1_SCL/GPIO_31
J15	VCCMSSIOB2	VCCMSSIOB2
J16	I2C_1_SDA/GPIO_30	I2C_1_SDA/GPIO_30
K1	GPIO_1/IO32RSB4V0	MAC_MDIO/IO58RSB4V0
K2	GPIO_0/IO33RSB4V0	MAC_MDC/IO57RSB4V0
K3	VCCMSSIOB4	VCCMSSIOB4
K4	MSS_RESET_N	MSS_RESET_N
K5	VCCRCOSC	VCCRCOSC
K6	VCCMSSIOB4	VCCMSSIOB4
K7	GND	GND
K8	VCC	VCC
K9	GND	GND
K10	VCC	VCC
K11	GND	GND
K12	UART_0_RXD/GPIO_21	UART_0_RXD/GPIO_21
K13	GND	GND
K14	UART_1_TXD/GPIO_28	UART_1_TXD/GPIO_28
K15	UART_1_RXD/GPIO_29	UART_1_RXD/GPIO_29
K16	UART_0_TXD/GPIO_20	UART_0_TXD/GPIO_20
L1	GND	GND
L2	GPIO_2/IO31RSB4V0	MAC_TXEN/IO61RSB4V0
L3	GPIO_3/IO30RSB4V0	MAC_CRSDV/IO60RSB4V0
L4	GPIO_4/IO29RSB4V0	MAC_RXER/IO59RSB4V0
L5	GPIO_9/IO24RSB4V0	MAC_CLK

Note: Shading denotes pins that do not have completely identical functions from density to density. For example, the bank assignment can be different for an I/O, or the function might be available only on a larger density device.

Pin No.	FG256	
	A2F060 Function	A2F500 Function
L6	GND	GND
L7	VCC	VCC
L8	GND	GND
L9	VCC	VCC
L10	GND	GND
L11	VCCMSSIOB2	VCCMSSIOB2
L12	SPI_1_DO/GPIO_24	SPI_1_DO/GPIO_24
L13	SPI_1_SS/GPIO_27	SPI_1_SS/GPIO_27
L14	SPI_1_CLK/GPIO_26	SPI_1_CLK/GPIO_26
L15	SPI_1_DI/GPIO_25	SPI_1_DI/GPIO_25
L16	GND	GND
M1	GPIO_5/IO28RSB4V0	MAC_TXD[0]/IO65RSB4V0
M2	GPIO_6/IO27RSB4V0	MAC_TXD[1]/IO64RSB4V0
M3	GPIO_7/IO26RSB4V0	MAC_RXD[0]/IO63RSB4V0
M4	GND	GND
M5	NC	ADC3
M6	NC	GND15ADC0
M7	GND33ADC0	GND33ADC1
M8	GND33ADC0	GND33ADC1
M9	ADC7	ADC4
M10	GNDTM0	GNDTM1
M11	ADC6	TM2
M12	ADC5	CM2
M13	SPI_0_SS/GPIO_19	SPI_0_SS/GPIO_19
M14	VCCMSSIOB2	VCCMSSIOB2
M15	SPI_0_CLK/GPIO_18	SPI_0_CLK/GPIO_18
M16	SPI_0_DI/GPIO_17	SPI_0_DI/GPIO_17
N1	GPIO_8/IO25RSB4V0	MAC_RXD[1]/IO62RSB4V0
N2	VCCMSSIOB4	VCCMSSIOB4
N3	VCC15A	VCC15A
N4	VCC33AP	VCC33AP
N5	NC	ABPS3
N6	ADC4	TM1

Note: Shading denotes pins that do not have completely identical functions from density to density. For example, the bank assignment can be different for an I/O, or the function might be available only on a larger density device.

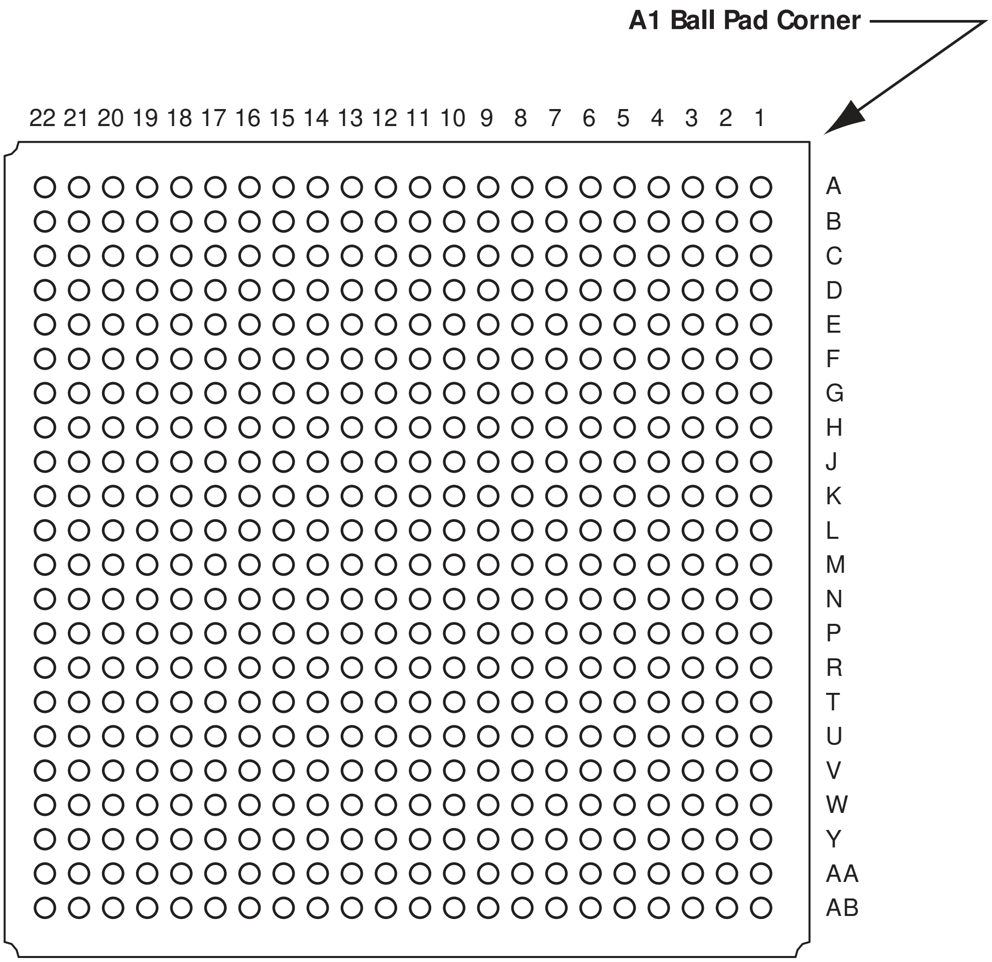
Pin No.	FG256	
	A2F060 Function	A2F500 Function
N7	NC	GND33ADC0
N8	VCC33ADC0	VCC33ADC1
N9	ADC8	ADC5
N10	CM0	CM3
N11	GNDAQ	GNDAQ
N12	VAREFOUT	VAREFOUT
N13	NC	GNDSDD1
N14	NC	VCC33SDD1
N15	GND	GND
N16	SPI_0_DO/GPIO_16	SPI_0_DO/GPIO_16
P1	GNDSDD0	GNDSDD0
P2	VCC33SDD0	VCC33SDD0
P3	VCC33N	VCC33N
P4	GNDA	GNDA
P5	GNDAQ	GNDAQ
P6	NC	CM1
P7	NC	ADC2
P8	NC	VCC15ADC0
P9	ADC9	ADC6
P10	TM0	TM3
P11	GNDA	GNDA
P12	VCCMAINXTAL	VCCMAINXTAL
P13	GNDLPXTAL	GNDLPXTAL
P14	VDDBAT	VDDBAT
P15	PTEM	PTEM
P16	PTBASE	PTBASE
R1	PCAP	PCAP
R2	SDD0	SDD0
R3	ADC0	ABPS0
R4	ADC3	TM0
R5	NC	ABPS2
R6	NC	ADC1
R7	NC	VCC33ADC0

Note: Shading denotes pins that do not have completely identical functions from density to density. For example, the bank assignment can be different for an I/O, or the function might be available only on a larger density device.

Pin No.	FG256	
	A2F060 Function	A2F500 Function
R8	VCC15ADC0	VCC15ADC1
R9	ADC10	ADC7
R10	ABPS1	ABPS7
R11	NC	ABPS4
R12	MAINXIN	MAINXIN
R13	MAINXOUT	MAINXOUT
R14	LPXIN	LPXIN
R15	LPXOUT	LPXOUT
R16	VCC33A	VCC33A
T1	NCAP	NCAP
T2	ADC1	ABPS1
T3	ADC2	CM0
T4	NC	GNDTM0
T5	NC	ADC0
T6	NC	VAREF0
T7	NC	GND33ADC0
T8	GND15ADC0	GND15ADC1
T9	VAREF0	VAREF1
T10	ABPS0	ABPS6
T11	NC	ABPS5
T12	NC	SDD1
T13	GNDVAREF	GNDVAREF
T14	GNDMAINXTAL	GNDMAINXTAL
T15	VCCLPXTAL	VCCLPXTAL
T16	PU_N	PU_N

Note: *Shading denotes pins that do not have completely identical functions from density to density. For example, the bank assignment can be different for an I/O, or the function might be available only on a larger density device.*

FG484



Note

For Package Manufacturing and Environmental information, visit the Resource Center at http://www.microsemi.com/soc/products/solutions/package/docs.aspx.

FG484	
Pin Number	**A2F500 Function**
A1	GND
A2	NC
A3	NC
A4	GND
A5	EMC_CS0_N/GAB0/IO05NDB0V0
A6	EMC_CS1_N/GAB1/IO05PDB0V0
A7	GND
A8	EMC_AB[0]/IO06NDB0V0
A9	EMC_AB[1]/IO06PDB0V0
A10	GND
A11	NC
A12	EMC_AB[7]/IO12PDB0V0
A13	GND
A14	EMC_AB[12]/IO14NDB0V0
A15	EMC_AB[13]/IO14PDB0V0
A16	GND
A17	IO16NDB0V0
A18	IO16PDB0V0
A19	GND
A20	NC
A21	NC
A22	GND
AA1	GPIO_4/IO52RSB4V0
AA2	GPIO_12/IO46RSB4V0
AA3	MAC_MDC/IO57RSB4V0
AA4	MAC_RXER/IO59RSB4V0
AA5	MAC_TXD[0]/IO65RSB4V0
AA6	ABPS0
AA7	TM1
AA8	ADC1
AA9	GND15ADC1
AA10	GND33ADC1
AA11	CM3
AA12	GNDTM1
AA13	ADC10
AA14	ADC9
AA15	GND15ADC2

FG484	
Pin Number	**A2F500 Function**
AA16	MAINXIN
AA17	MAINXOUT
AA18	LPXIN
AA19	LPXOUT
AA20	NC
AA21	NC
AA22	SPI_1_CLK/GPIO_26
AB1	GND
AB2	GPIO_13/IO45RSB4V0
AB3	GPIO_14/IO44RSB4V0
AB4	GND
AB5	PCAP
AB6	NCAP
AB7	ABPS3
AB8	ADC3
AB9	GND15ADC0
AB10	VCC33ADC1
AB11	VAREF1
AB12	TM2
AB13	CM2
AB14	ABPS4
AB15	GNDAQ
AB16	GNDMAINXTAL
AB17	GNDLPXTAL
AB18	VCCLPXTAL
AB19	VDDBAT
AB20	PTBASE
AB21	NC
AB22	GND
B1	EMC_DB[15]/GAA2/IO88PDB5V0
B2	GND
B3	NC
B4	NC
B5	VCCFPGAIOB0
B6	EMC_RW_N/GAA1/IO02PDB0V0
B7	IO04PPB0V0
B8	VCCFPGAIOB0

FG484	
Pin Number	A2F500 Function
B9	EMC_BYTEN[0]/GAC0/IO07NDB0V0
B10	EMC_AB[2]/IO09NDB0V0
B11	EMC_AB[3]/IO09PDB0V0
B12	EMC_AB[6]/IO12NDB0V0
B13	EMC_AB[14]/IO15NDB0V0
B14	EMC_AB[15]/IO15PDB0V0
B15	VCCFPGAIOB0
B16	EMC_AB[18]/IO18NDB0V0
B17	EMC_AB[19]/IO18PDB0V0
B18	VCCFPGAIOB0
B19	GBB0/IO24NDB0V0
B20	GBB1/IO24PDB0V0
B21	GND
B22	GBA2/IO27PDB1V0
C1	EMC_DB[14]/GAB2/IO88NDB5V0
C2	NC
C3	NC
C4	IO01NDB0V0
C5	IO01PDB0V0
C6	EMC_CLK/GAA0/IO02NDB0V0
C7	IO03PPB0V0
C8	IO04NPB0V0
C9	EMC_BYTEN[1]/GAC1/IO07PDB0V0
C10	EMC_OEN1_N/IO08PDB0V0
C11	GND
C12	VCCFPGAIOB0
C13	EMC_AB[8]/IO13NDB0V0
C14	EMC_AB[16]/IO17NDB0V0
C15	EMC_AB[17]/IO17PDB0V0
C16	EMC_AB[24]/IO20NDB0V0
C17	EMC_AB[22]/IO19NDB0V0
C18	EMC_AB[23]/IO19PDB0V0
C19	GBA0/IO23NPB0V0
C20	NC
C21	GBC2/IO30PDB1V0
C22	GBB2/IO27NDB1V0
D1	GND

FG484	
Pin Number	A2F500 Function
D2	EMC_DB[12]/IO87NDB5V0
D3	EMC_DB[13]/GAC2/IO87PDB5V0
D4	NC
D5	NC
D6	GND
D7	IO00NPB0V0
D8	IO03NPB0V0
D9	GND
D10	EMC_OEN0_N/IO08NDB0V0
D11	EMC_AB[10]/IO11NDB0V0
D12	EMC_AB[11]/IO11PDB0V0
D13	EMC_AB[9]/IO13PDB0V0
D14	GND
D15	GBC1/IO22PPB0V0
D16	EMC_AB[25]/IO20PDB0V0
D17	GND
D18	GBA1/IO23PPB0V0
D19	NC
D20	NC
D21	IO30NDB1V0
D22	GND
E1	GFC2/IO84PPB5V0
E2	VCCFPGAIOB5
E3	GFA2/IO85PDB5V0
E4	GND
E5	NC
E6	GNDQ
E7	VCCFPGAIOB0
E8	IO00PPB0V0
E9	NC
E10	VCCFPGAIOB0
E11	EMC_AB[4]/IO10NDB0V0
E12	EMC_AB[5]/IO10PDB0V0
E13	VCCFPGAIOB0
E14	GBC0/IO22NPB0V0
E15	NC
E16	VCCFPGAIOB0

FG484	
Pin Number	A2F500 Function
E17	VCOMPLA1
E18	IO25NPB1V0
E19	GND
E20	NC
E21	VCCFPGAIOB1
E22	IO32NDB1V0
F1	GFB1/IO82PPB5V0
F2	IO84NPB5V0
F3	GFB2/IO85NDB5V0
F4	EMC_DB[10]/IO86NPB5V0
F5	VCCFPGAIOB5
F6	VCCPLL0
F7	VCOMPLA0
F8	NC
F9	NC
F10	NC
F11	NC
F12	NC
F13	EMC_AB[20]/IO21NDB0V0
F14	EMC_AB[21]/IO21PDB0V0
F15	GNDQ
F16	VCCPLL1
F17	IO25PPB1V0
F18	VCCFPGAIOB1
F19	IO28NDB1V0
F20	IO31PDB1V0
F21	IO31NDB1V0
F22	IO32PDB1V0
G1	GND
G2	GFB0/IO82NPB5V0
G3	EMC_DB[9]/GEC1/IO80PDB5V0
G4	GFC1/IO83PPB5V0
G5	EMC_DB[11]/IO86PPB5V0
G6	GNDQ
G7	NC
G8	GND
G9	VCCFPGAIOB0

FG484	
Pin Number	A2F500 Function
G10	GND
G11	VCCFPGAIOB0
G12	GND
G13	VCCFPGAIOB0
G14	GND
G15	VCCFPGAIOB0
G16	GNDQ
G17	IO26PDB1V0
G18	IO26NDB1V0
G19	GCA2/IO28PDB1V0
G20	IO33NDB1V0
G21	GCB2/IO33PDB1V0
G22	GND
H1	EMC_DB[7]/GEB1/IO79PDB5V0
H2	VCCFPGAIOB5
H3	EMC_DB[8]/GEC0/IO80NDB5V0
H4	GND
H5	GFC0/IO83NPB5V0
H6	GFA1/IO81PDB5V0
H7	GND
H8	VCC
H9	GND
H10	VCC
H11	GND
H12	VCC
H13	GND
H14	VCC
H15	GND
H16	VCCFPGAIOB1
H17	IO29NDB1V0
H18	GCC2/IO29PDB1V0
H19	GND
H20	GCC0/IO35NPB1V0
H21	VCCFPGAIOB1
H22	GCB0/IO34NDB1V0
J1	EMC_DB[6]/GEB0/IO79NDB5V0
J2	EMC_DB[5]/GEA1/IO78PDB5V0

FG484	
Pin Number	A2F500 Function
J3	EMC_DB[4]/GEA0/IO78NDB5V0
J4	EMC_DB[3]/GEC2/IO77PPB5V0
J5	VCCFPGAIOB5
J6	GFA0/IO81NDB5V0
J7	VCCFPGAIOB5
J8	GND
J9	VCC
J10	GND
J11	VCC
J12	GND
J13	VCC
J14	GND
J15	VCC
J16	GND
J17	IO37PDB1V0
J18	VCCFPGAIOB1
J19	GCA0/IO36NDB1V0
J20	GCA1/IO36PDB1V0
J21	GCC1/IO35PPB1V0
J22	GCB1/IO34PDB1V0
K1	GND
K2	EMC_DB[0]/GEA2/IO76NDB5V0
K3	EMC_DB[1]/GEB2/IO76PDB5V0
K4	IO74PPB5V0
K5	EMC_DB[2]/IO77NPB5V0
K6	IO75PDB5V0
K7	GND
K8	VCC
K9	GND
K10	VCC
K11	GND
K12	VCC
K13	GND
K14	VCC
K15	GND
K16	VCCFPGAIOB1
K17	IO37NDB1V0

FG484	
Pin Number	A2F500 Function
K18	GDA1/IO40PDB1V0
K19	GDA0/IO40NDB1V0
K20	GDC1/IO38PDB1V0
K21	GDC0/IO38NDB1V0
K22	GND
L1	IO73PDB5V0
L2	IO73NDB5V0
L3	IO72PPB5V0
L4	GND
L5	IO74NPB5V0
L6	IO75NDB5V0
L7	VCCFPGAIOB5
L8	GND
L9	VCC
L10	GND
L11	VCC
L12	GND
L13	VCC
L14	GND
L15	VCC
L16	GND
L17	GNDQ
L18	GDA2/IO42NDB1V0
L19	VCCFPGAIOB1
L20	GDB1/IO39PDB1V0
L21	GDB0/IO39NDB1V0
L22	GDC2/IO41PDB1V0
M1	IO71PDB5V0
M2	IO71NDB5V0
M3	VCCFPGAIOB5
M4	IO72NPB5V0
M5	GNDQ
M6	IO68PDB5V0
M7	GND
M8	VCC
M9	GND
M10	VCC

FG484	
Pin Number	A2F500 Function
M11	GND
M12	VCC
M13	GND
M14	VCC
M15	GND
M16	VCCFPGAIOB1
M17	NC
M18	GDB2/IO42PDB1V0
M19	VJTAG
M20	GND
M21	VPP
M22	IO41NDB1V0
N1	GND
N2	IO70PDB5V0
N3	IO70NDB5V0
N4	VCCRCOSC
N5	VCCFPGAIOB5
N6	IO68NDB5V0
N7	VCCFPGAIOB5
N8	GND
N9	VCC
N10	GND
N11	VCC
N12	GND
N13	VCC
N14	GND
N15	VCC
N16	GND
N17	NC
N18	VCCFPGAIOB1
N19	VCCENVM
N20	GNDENVM
N21	NC
N22	GND
P1	IO69NDB5V0
P2	IO69PDB5V0
P3	GNDRCOSC

FG484	
Pin Number	A2F500 Function
P4	GND
P5	NC
P6	NC
P7	GND
P8	VCC
P9	GND
P10	VCC
P11	GND
P12	VCC
P13	GND
P14	VCC
P15	GND
P16	VCCFPGAIOB1
P17	TDI
P18	TCK
P19	GND
P20	TMS
P21	TDO
P22	TRSTB
R1	MSS_RESET_N
R2	VCCFPGAIOB5
R3	GPIO_1/IO55RSB4V0
R4	NC
R5	NC
R6	NC
R7	NC
R8	GND
R9	VCC
R10	GND
R11	VCC
R12	GND
R13	VCC
R14	GND
R15	VCC
R16	JTAGSEL
R17	NC
R18	NC

FG484	
Pin Number	A2F500 Function
R19	NC
R20	NC
R21	VCCFPGAIOB1
R22	NC
T1	GND
T2	VCCMSSIOB4
T3	GPIO_8/IO48RSB4V0
T4	GPIO_11/IO66RSB4V0
T5	GND
T6	MAC_CLK
T7	VCCMSSIOB4
T8	VCC33SDD0
T9	VCC15A
T10	GNDAQ
T11	GND33ADC0
T12	ADC7
T13	TM4
T14	VAREF2
T15	VAREFOUT
T16	VCCMSSIOB2
T17	SPI_1_DO/GPIO_24
T18	GND
T19	NC
T20	NC
T21	VCCMSSIOB2
T22	GND
U1	GND
U2	GPIO_5/IO51RSB4V0
U3	GPIO_10/IO67RSB4V0
U4	VCCMSSIOB4
U5	MAC_RXD[1]/IO62RSB4V0
U6	NC
U7	VCC33AP
U8	VCC33N
U9	CM1
U10	VAREF0
U11	GND33ADC1

FG484	
Pin Number	A2F500 Function
U12	ADC4
U13	GNDTM2
U14	ADC11
U15	GNDVAREF
U16	VCC33SDD1
U17	SPI_0_DO/GPIO_16
U18	UART_0_RXD/GPIO_21
U19	VCCMSSIOB2
U20	I2C_1_SCL/GPIO_31
U21	I2C_0_SCL/GPIO_23
U22	GND
V1	GPIO_0/IO56RSB4V0
V2	GPIO_6/IO50RSB4V0
V3	GPIO_9/IO47RSB4V0
V4	MAC_MDIO/IO58RSB4V0
V5	MAC_RXD[0]/IO63RSB4V0
V6	GND
V7	SDD0
V8	ABPS1
V9	ADC2
V10	VCC33ADC0
V11	ADC6
V12	ADC5
V13	ABPS5
V14	ADC8
V15	GND33ADC2
V16	NC
V17	GND
V18	SPI_0_DI/GPIO_17
V19	SPI_1_DI/GPIO_25
V20	UART_1_TXD/GPIO_28
V21	I2C_0_SDA/GPIO_22
V22	I2C_1_SDA/GPIO_30
W1	GPIO_2/IO54RSB4V0
W2	GPIO_7/IO49RSB4V0
W3	GND
W4	MAC_CRSDV/IO60RSB4V0

FG484	
Pin Number	A2F500 Function
W5	MAC_TXD[1]/IO64RSB4V0
W6	SDD2
W7	GNDA
W8	TM0
W9	ABPS2
W10	GND33ADC0
W11	VCC15ADC1
W12	ABPS6
W13	CM4
W14	ABPS9
W15	VCC33ADC2
W16	GNDA
W17	PU_N
W18	GNDSDD1
W19	SPI_0_CLK/GPIO_18
W20	GND
W21	SPI_1_SS/GPIO_27
W22	UART_1_RXD/GPIO_29
Y1	GPIO_3/IO53RSB4V0
Y2	VCCMSSIOB4
Y3	GPIO_15/IO43RSB4V0
Y4	MAC_TXEN/IO61RSB4V0
Y5	VCCMSSIOB4
Y6	GNDSDD0
Y7	CM0
Y8	GNDTM0
Y9	ADC0
Y10	VCC15ADC0
Y11	ABPS7
Y12	TM3
Y13	ABPS8
Y14	GND33ADC2
Y15	VCC15ADC2
Y16	VCCMAINXTAL
Y17	SDD1
Y18	PTEM
Y19	VCC33A

FG484	
Pin Number	A2F500 Function
Y20	SPI_0_SS/GPIO_19
Y21	VCCMSSIOB2
Y22	UART_0_TXD/GPIO_20

6 – Datasheet Information

List of Changes

The following table lists critical changes that were made in each revision of the SmartFusion datasheet.

Revision	Changes	Page
Revision 2 (March 2015)	Updated information about unused MSS I/O configuration in "User I/O Naming Conventions" (SAR 62994).	5-6
Revision 1 (September 2012)	The status was changed from Preliminary to Production for A2F060 and A2F500 in the "SmartFusion cSoC Device Status" table (SAR 41135).	III

Datasheet Categories

Categories

In order to provide the latest information to designers, some datasheet parameters are published before data has been fully characterized from silicon devices. The data provided for a given device, as highlighted in the "SmartFusion cSoC Device Status" table on page III, is designated as either "Product Brief," "Advance," "Preliminary," or "Production." The definitions of these categories are as follows:

Product Brief

The product brief is a summarized version of a datasheet (advance or production) and contains general product information. This document gives an overview of specific device and family information.

Advance

This version contains initial estimated information based on simulation, other products, devices, or speed grades. This information can be used as estimates, but not for production. This label only applies to the DC and Switching Characteristics chapter of the datasheet and will only be used when the data has not been fully characterized.

Preliminary

The datasheet contains information based on simulation and/or initial characterization. The information is believed to be correct, but changes are possible.

Production

This version contains information that is considered to be final.

Export Administration Regulations (EAR)

The products described in this document are subject to the Export Administration Regulations (EAR). They could require an approved export license prior to export from the United States. An export includes release of product or disclosure of technology to a foreign national inside or outside the United States.

Microsemi SoC Products Group Safety Critical, Life Support, and High-Reliability Applications Policy

The SoC Products Group products described in this advance status document may not have completed the SoC Products Group's qualification process. Products may be amended or enhanced during the product introduction and qualification process, resulting in changes in device functionality or performance. It is the responsibility of each customer to ensure the fitness of any product (but especially a new product) for a particular purpose, including appropriateness for safety-critical, life-support, and other high-reliability applications. Consult the SoC Products Group's Terms and Conditions for specific liability exclusions relating to life-support applications. A reliability report covering all of the SoC Products Group's products is available on the SoC Products Group website at http://www.microsemi.com/soc/documents/ORT_Report.pdf. Microsemi SoC Products Group also offers a variety of enhanced qualification and lot acceptance screening procedures. Contact your local SoC Products Group sales office for additional reliability information.

Microsemi Corporation (Nasdaq: MSCC) offers a comprehensive portfolio of semiconductor and system solutions for communications, defense & security, aerospace and industrial markets. Products include high-performance and radiation-hardened analog mixed-signal integrated circuits, FPGAs, SoCs and ASICs; power management products; timing and synchronization devices and precise time solutions, setting the world's standard for time; voice processing devices; RF solutions; discrete components; security technologies and scalable anti-tamper products; Power-over-Ethernet ICs and midspans; as well as custom design capabilities and services. Microsemi is headquartered in Aliso Viejo, Calif., and has approximately 3,400 employees globally. Learn more at **www.microsemi.com**.

Microsemi Corporate Headquarters
One Enterprise, Aliso Viejo,
CA 92656 USA

Within the USA: +1 (800) 713-4113
Outside the USA: +1 (949) 380-6100
Sales: +1 (949) 380-6136
Fax: +1 (949) 215-4996

E-mail: sales.support@microsemi.com

51700120-2/03.15