# PI3VDP3212

## 2-Lane DisplayPort™ Rev 1.2 Compliant Switch

## Features

➔ 2-lane, 1:2 mux/demux that will support RBR, HBR1, or HBR2

➔ 1-channel 1:2 mux/demux for DP_HPD signal

➔ 1-differential channel 1:2 mux/demux for DP_Aux signal with support up to 720Mbps

➔ Insertion Loss for high speed channels @ 2.7 GHz: -1.7dB

➔ -3dB Bandwidth for high speed channels:  4.7GHz

➔ Return loss for high speed channels @ 2.7GHz: -16dB

➔ Low Bit-to-Bit Skew , 7ps max (between '+' and '-' bits)

➔ Low Crosstalk for high speed channels: -25dB@5.4 Gbps

➔ Low Off Isolation for high speed channels:  -25dB@5.4 Gbps

➔ $V_{DD}$ Operating Range: 3.3V +/-10%

➔ ESD Tolerance: 2kV HBM

➔ Low channel-to-channel skew, 35ps max

➔ Packaging (Pb-free & Green):

  ▫ 32 TQFN (ZL)

## Description

Pericom Semiconductor's PI3VDP3212 mux/demux is targeted for next generation digital video signals. This device can be used to connect a DisplayPort™ Source to two Independent Display-Port Sinks or to connect two DisplayPort sources to a single DP display.

The newly released DisplayPort spec requires a data rate of 5.4 Gbps. Pericom's solution has been specifically designed around this standard and will support such signals.
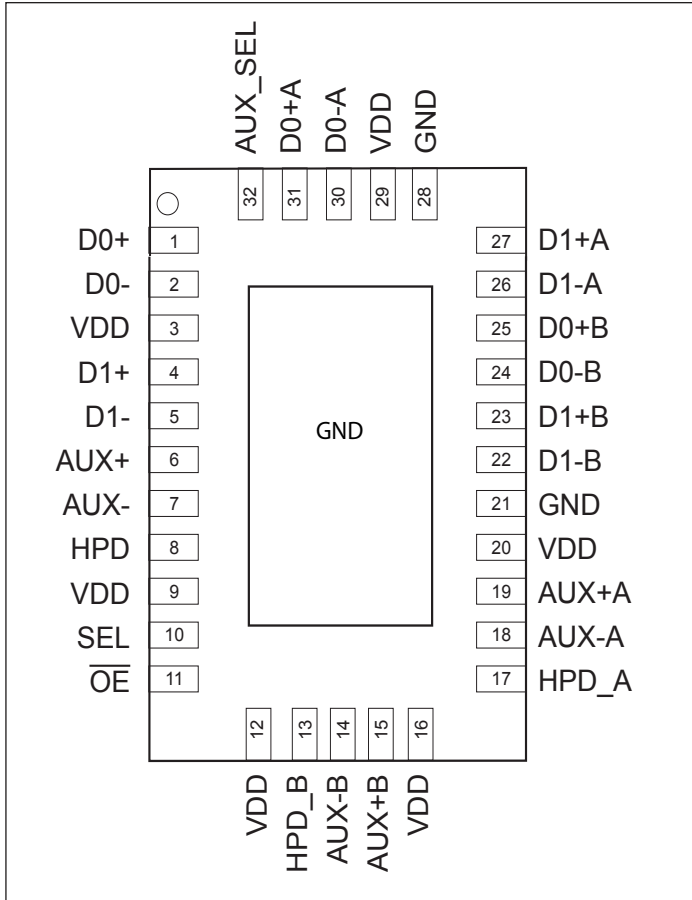
## Application

Routing of DisplayPort signals with low signal attenuation between source and sink.

## Block Diagram
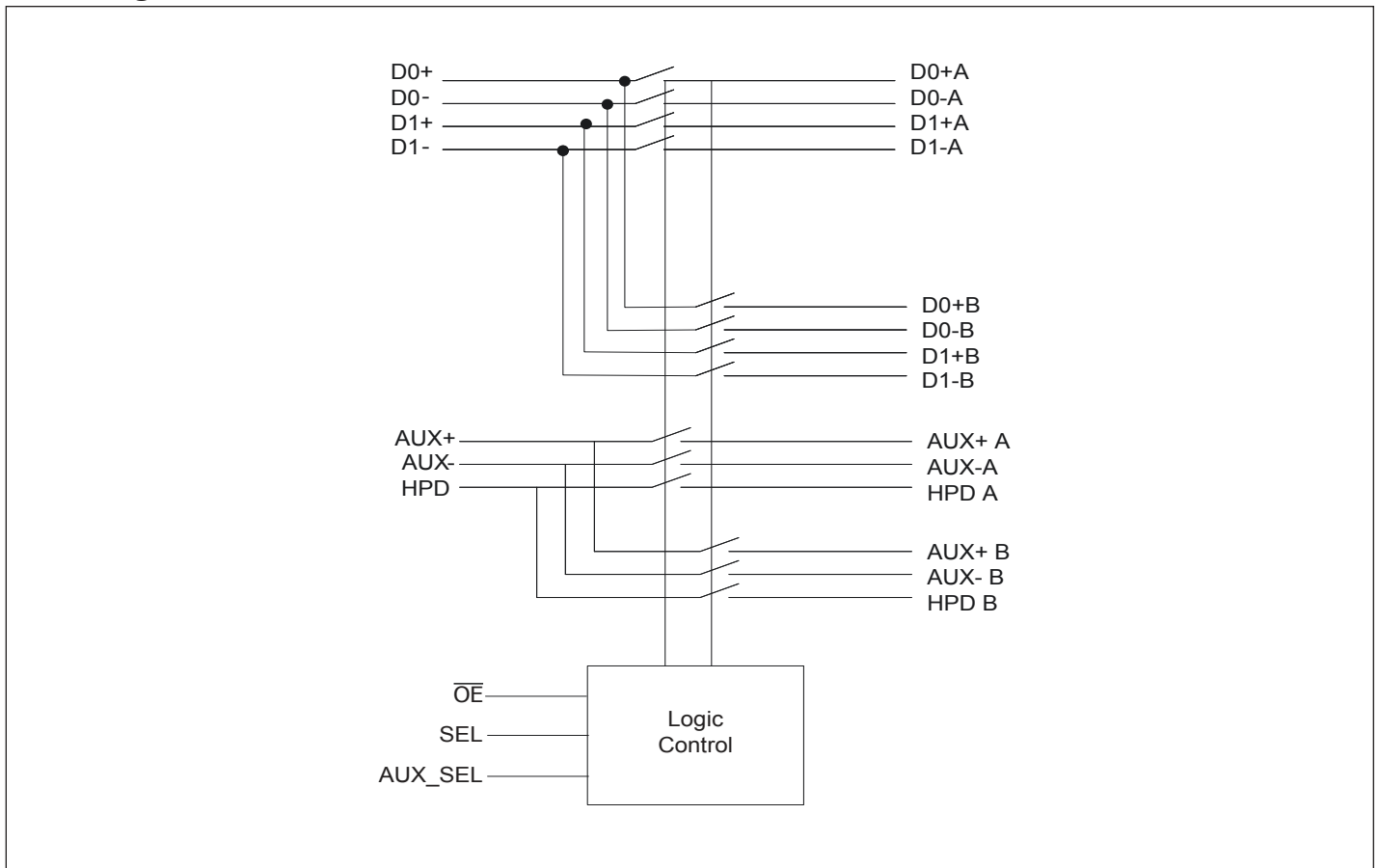
## Pin Assignment (TQFN-32)



## Truth Table

| $\overline{OE}$ | SEL | AUX_SEL | Function |
|---|---|---|---|
| Low | Low | Low | Port A active for all channels |
| Low | Low | High | Port A for HS, port B for HPD/AUX |
| Low | High | Low | Port B for HS, port A for HPD/AUX |
| Low | High | High | Port B active for all channels |
| High | x | x | All I/O's are hi-z and IC is power down |

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## Pin Description

| pin# | pin Name | Signal Type | Description |
|---|---|---|---|
| 1 | D0+ | I/O | positive differential signal 0 for COM port |
| 2 | D0- | I/O | negative differential signal 0 for COM port |
| 3 | VDD | Power | 3.3V +/-10% power supply |
| 4 | D1+ | I/O | positive differential signal 1 for COM port |
| 5 | D1- | I/O | negative differential signal 1 for COM port |
| 6 | AUX+ | I/O | positive differential signal for AUX COM port |
| 7 | AUX- | I/O | negative differential signal for AUX COM port |
| 8 | HPD | I/O | HPD for COM port |
| 9 | VDD | Power | 3.3V +/-10% power supply |
| 10 | SEL | I | switch logic control. If HIGH, then path B is selected for high speed channels only If LOW, then path A is selected for high speed channels only |
| 11 | $\overline{OE}$ | I | Output enable. if $\overline{OE}$ is low, IC is enabled. If $\overline{OE}$ is high, then IC is power down and all I/Os are hi-z |
| 12 | VDD | Power | 3.3V +/-10% power supply |
| 13 | HPD_B | I/O | HPD for port B |
| 14 | AUX-B | I/O | negative differential signal for AUX, port B |
| 15 | AUX+B | I/O | positive differential signal for AUX, port B |
| 16 | VDD | Power | 3.3V +/-10% power supply |
| 17 | HPD_A | I/O | HPD for port A |
| 18 | AUX-A | I/O | negative differential signal for AUX, port A |
| 19 | AUX+A | I/O | positive differential signal for AUX, port A |
| 20 | VDD | Power | 3.3V +/-10% power supply |
| 21 | GND | Ground | Ground |
| 22 | D1-B | I/O | negative differential signal 1 for port B |
| 23 | D1+B | I/O | positive differential signal 1 for port B |
| 24 | D0-B | I/O | negative differential signal 0 for port B |
| 25 | D0+B | I/O | positive differential signal 0 for port B |
| 26 | D1-A | I/O | negative differential signal 1 for port A |
| 27 | D1+A | I/O | positive differential signal 1 for port A |
| 28 | GND | Ground | Ground |
| 29 | VDD | Power | 3.3V +/-10% power supply |
| 30 | D0-A | I/O | negative differential signal 0 for port A |
| 31 | D0+A | I/O | positive differential signal 0 for port A |
| 32 | AUX_SEL | I | switches only the AUX and HPD channels from port A vs. port B If High, path B is selected If LOW, path A is selected |

## Maximum Ratings

(Above which useful life may be impaired.  For user guidelines, not tested.)

Storage Temperature ............................................. −65°C to +150°C
Supply Voltage to Ground Potential .................................... −0.5V to +4.2V
DC Input Voltage ........................................................ −0.5V to $V_{DD}$
DC Output Current ............................................................ 120mA
Power Dissipation ................................................................ 0.5W

**Note:** Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

## DC Electrical Characteristics for Switching over Operating Range (TA = −40°C to +85°C, VDD = 3.3V ±10%)

| Parameter | Description | Test Conditions[1] | Min | Typ[1] | Max | Units |
|---|---|---|---|---|---|---|
| $V_{IH}$ | Input HIGH Voltage | Guaranteed HIGH level | 1.5 | | | V |
| $V_{IL}$ | Input LOW Voltage | Guaranteed LOW level | | | 0.75 | |
| $V_{IK}$ | Clamp Diode Voltage, Dx | $V_{DD}$ = Max., $I_{IN}$ = −18mA | | −1.6 | −1.8 | |
| $I_{IH}$ | Input HIGH Current | $V_{DD}$ = Max., $V_{IN}$ = $V_{DD}$ | | | ±5 | |
| $I_{IL}$ | Input LOW Current | $V_{DD}$ = Max., $V_{IN}$ = GND | | | ±5 | μA |
| $I_{OFF\_SB}$ | I/O leakage when part is off for side band signals only (DDC, AUX, HPD) | $V_{DD}$ = 0V, $V_{INPUT}$ = 0V to 3.6V | | | 20 | |
| $R_{ON\_HS}$ | On resistance between input to output for high speed signals | $V_{DD}$ = 3.3V, Vinput = 0V to 2V, $I_{INPUT}$ = 20mA | | 10 | | Ohm |
| $R_{ON\_AUX}$ | On resistance between input to output for side-band signals (AUX) | $V_{DD}$ = 3.3V, Vinput = 0 to 3.3V, $I_{INPUT}$ = 20mA | | 7 | | Ohm |
| Aux_ss | Signal Swing Tolerance in Aux path | $V_{DD}$ = 3.0V | −0.5 | | 3.6 | V |
| HPD_I | Input voltage tolerance on HPD path | | | | 5.5 | V |
| HPD_O | Output voltage on HPD path | HPD input from 0V to 5.25V | | | 3.6 | V |

## Power Supply Characteristics (TA = −40°C to +85°C)

| Parameter | Description | Test Conditions[1] | Min | Typ[1] | Max | Units |
|---|---|---|---|---|---|---|
| $I_{CC}$ | Quiescent Power  Supply Current | $V_{DD}$ = 3.3V., $V_{IN}$ = GND or $V_{DD}$ | | 320 | 500 | uA |

## Dynamic Electrical Characteristics over Operating Range (TA = -40° to +85°C, VDD = 3.3V ±10%)

| Parameter | Description | Test Conditions | | Typ. | Max | Units |
|---|---|---|---|---|---|---|
| $X_{TALK}$ | Crosstalk on High Speed Channels | See Fig. 1 for Measurement Setup | f= 2.7 GHz | -25dB | | dB |
| | | | f = 1.35 GHz | -32dB | | |
| $O_{IRR}$ | OFF Isolation on High Speed Channels | See Fig. 2 for Measurement Setup, | f= 2.7 GHz | -22dB | | |
| | | | f = 1.35 GHz | -30dB | | |
| $I_{LOSS}$ | Differential Insertion Loss on High Speed Channels | @5.4Gbps (see figure 3) | | -1.7 | | dB |
| $R_{loss}$ | Differential Return Loss on high speed channels | @ 2.7GHz | | -16 | | dB |
| BW_Dx± | Bandwidth -3dB for Main high speed path (Dx±) | See figure 3 | | 4.7 | | GHz |
| BW_AUX/ HPD | -3dB BW for AUX and HPD signals | See figure 3 | | 1.5 | | GHz |
| Tsw a-b | time it takes to switch from port A to port B | | | | 1 | us |
| Tsw b-a | time it takes to switch from port B to port A | | | | 1 | us |
| Tstartup | Vdd valid to channel enable | | | | 10 | us |
| Twakeup | Enabling output by changing $\overline{OE}$ from low to High | | | | 10 | us |

1.  For Max. or Min. conditions, use appropriate value specified under Electrical Characteristics for the applicable device type.

2.  Typical values are at $V_{DD}$ = 3.3V, $T_A$ = 25°C ambient and maximum loading.

## Switching Characteristics (TA= -40° to +85°C, V_DD = 3.3V±10%)

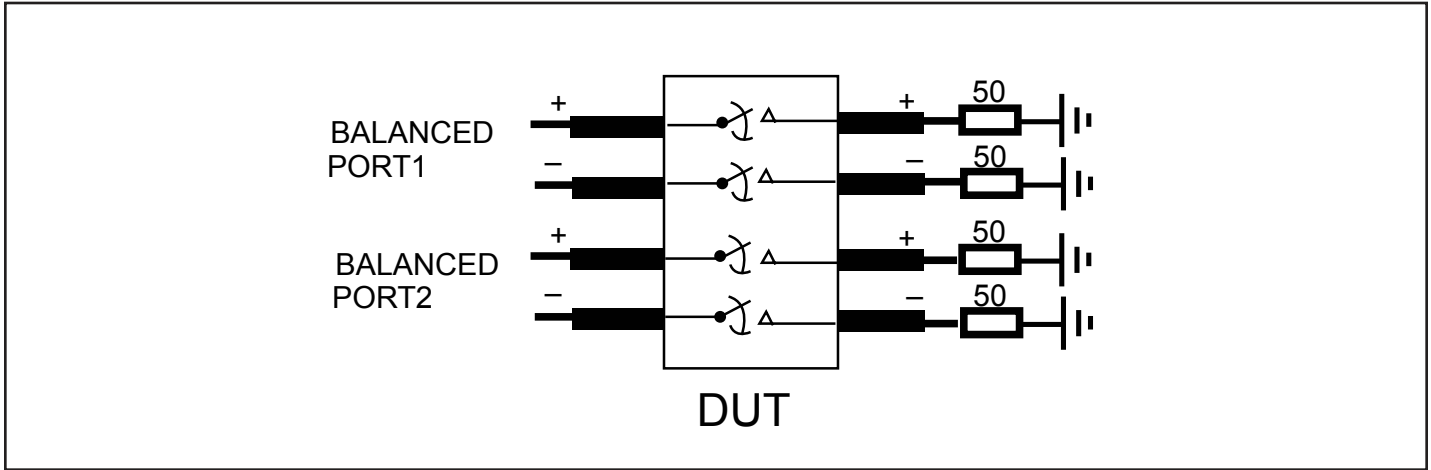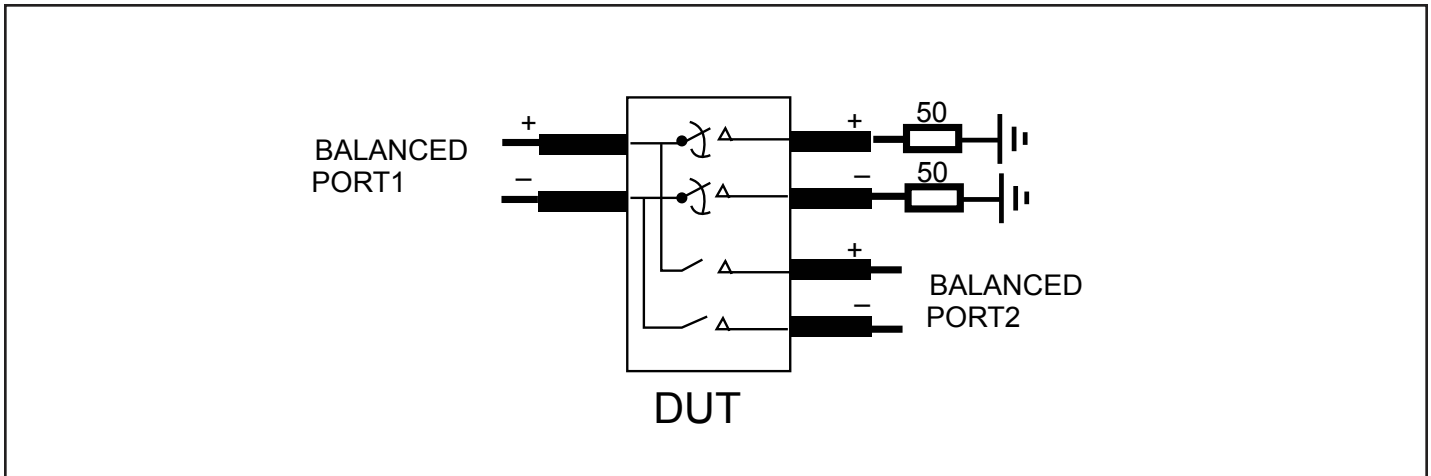| Parameter | Description | Min. | Typ. | Max. | Units |
|---|---|---|---|---|---|
| $T_{pd}$ | Propagation delay (input pin to output pin) | | 80 | | ps |
| $t_{b-b}$ | Bit-to-bit skew within the same differential pair | | 5 | | ps |
| $t_{ch-ch}$ | Channel-to-channel skew | | | 50 | ps |

**Fig 1. Crosstalk Setup**
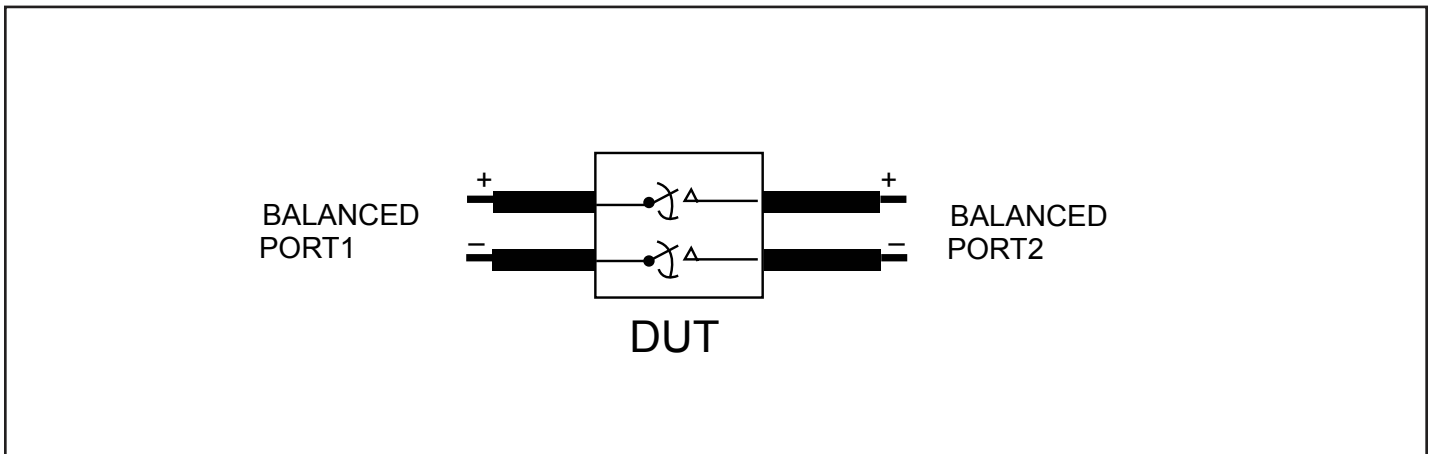


**Fig 2. Off-isolation setup**



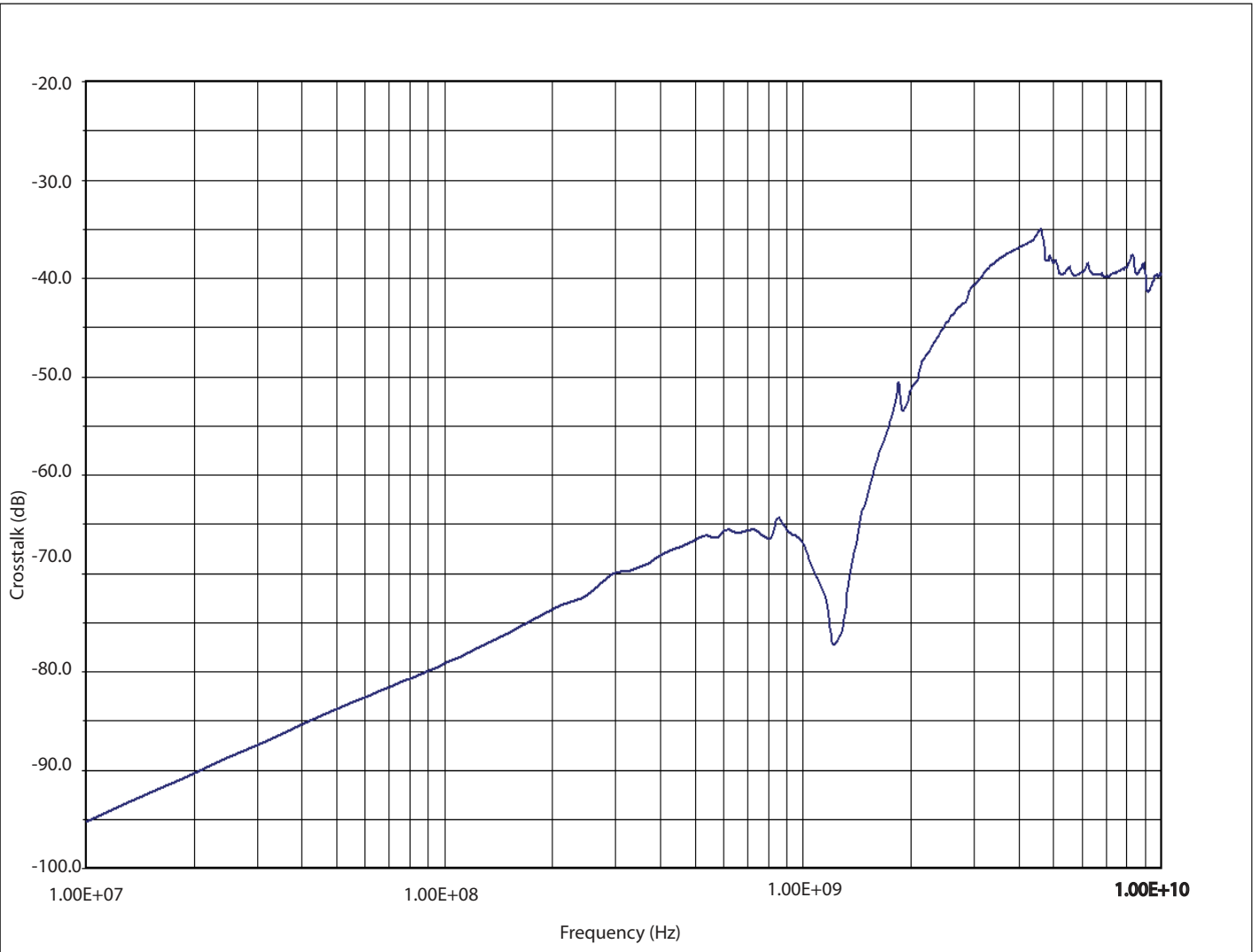**Fig 3. Differential Insertion Loss set up**

**Fig 4. Xtalk for high speed channels (D0 and D1)**
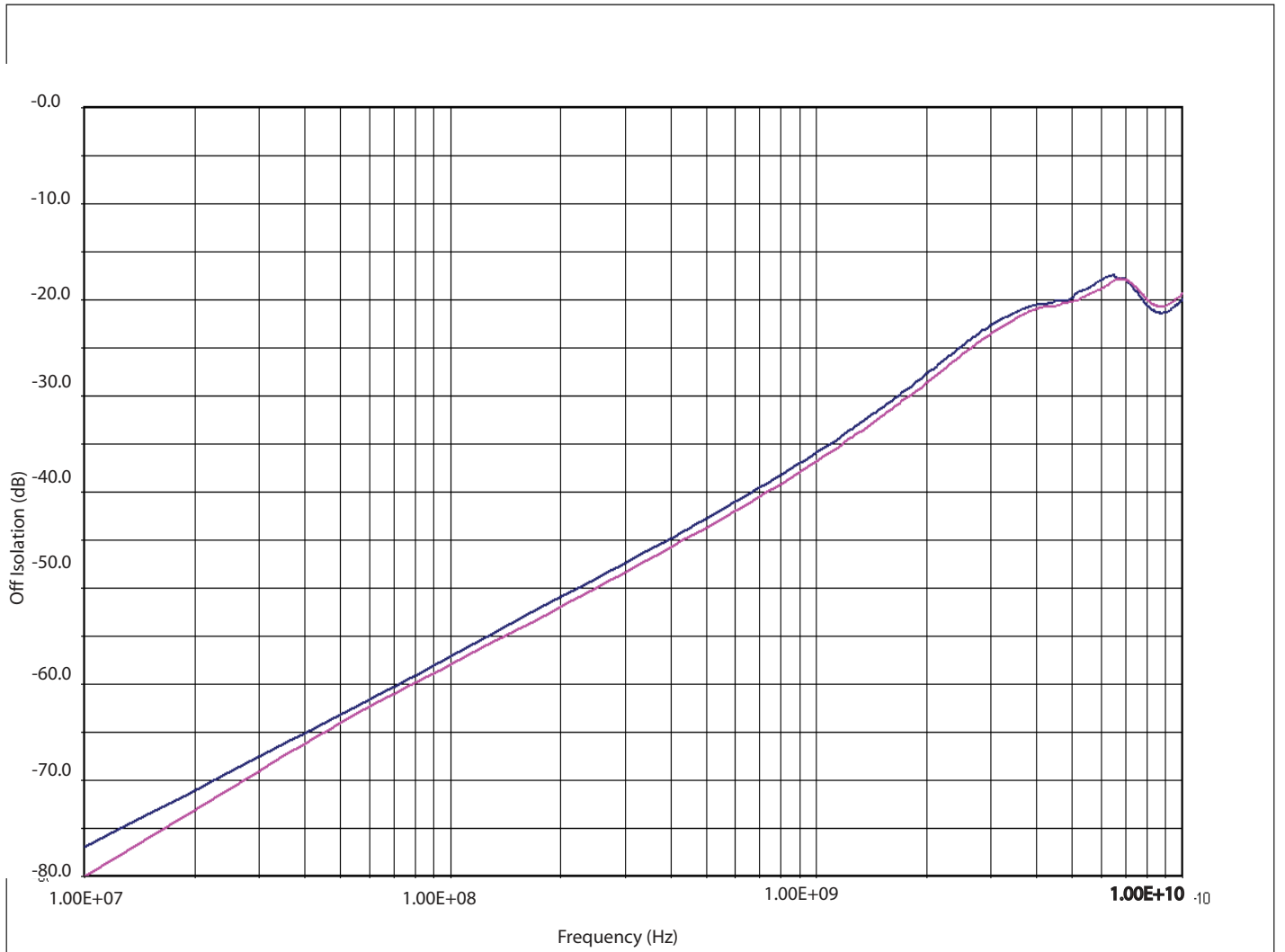
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**Fig 5. Off Isolation for high speed channels (D0 an D1). Red is for path B and Blue is for path A**
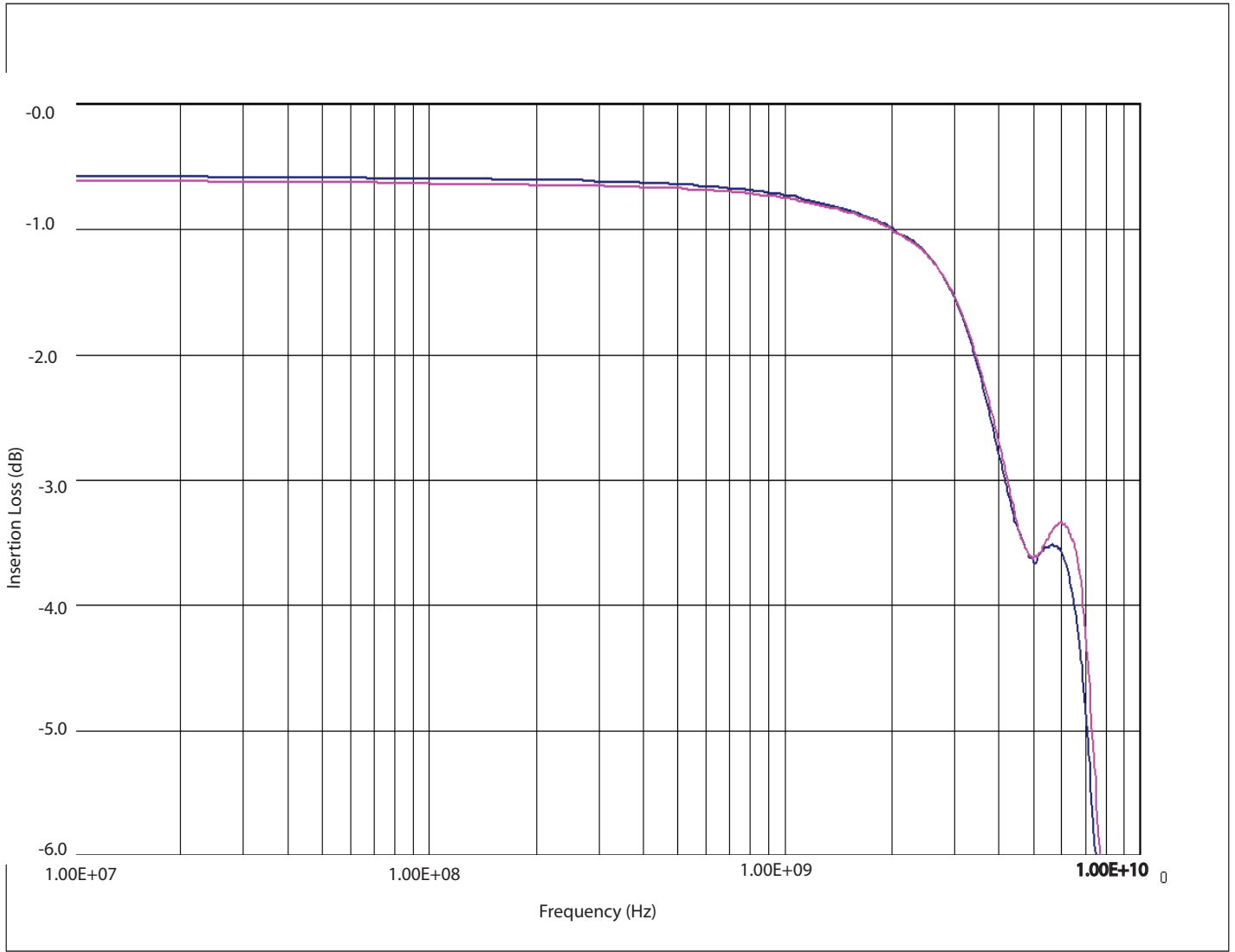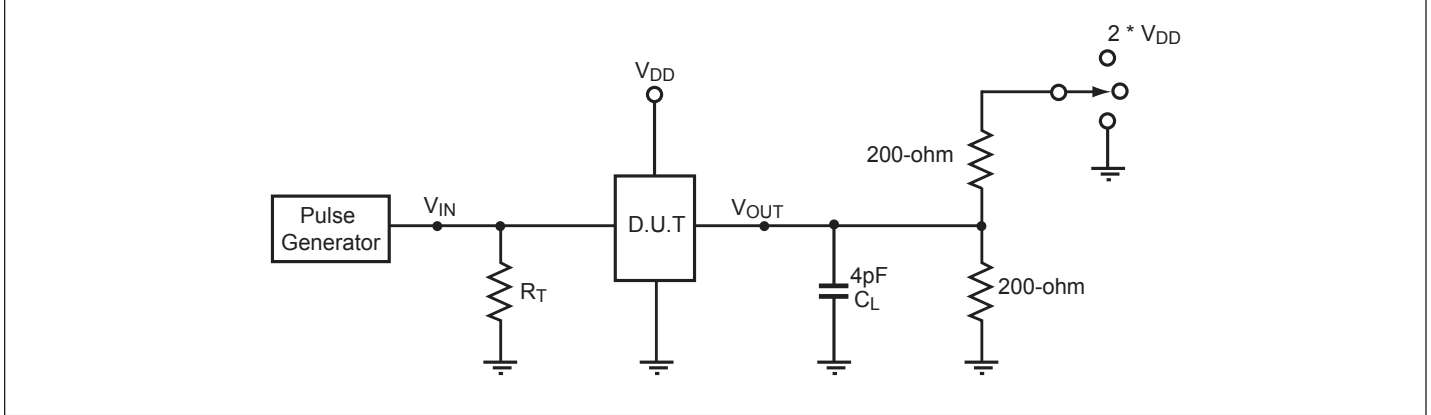
**Fig 6. Insertion Loss for high speed channels, D0 and D1. Red is for path B and Blue is for path A**
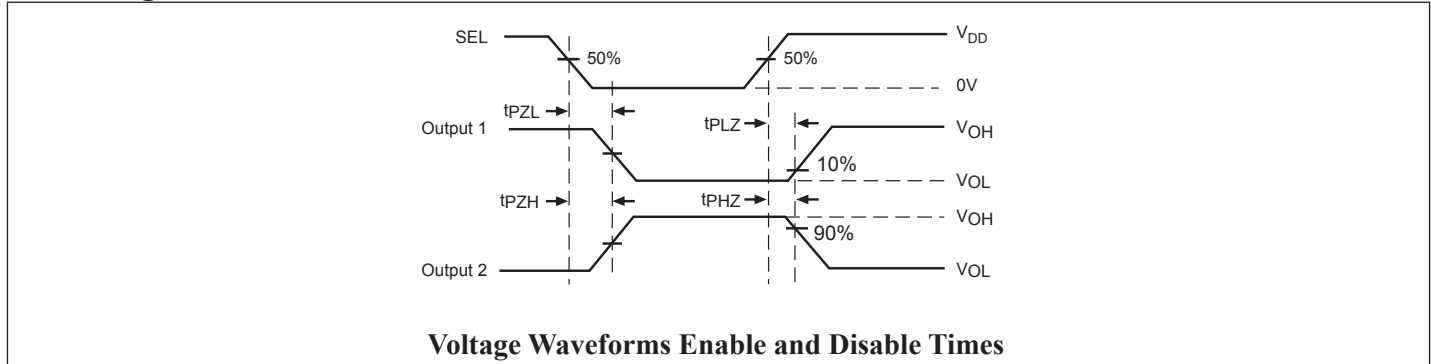
## Test Circuit for Electrical Characteristics(1-5)



**Notes:**

1.  $C_L$ = Load capacitance: includes jig and probe capacitance.

2.  $R_T$ = Termination resistance: should be equal to $Z_{OUT}$ of the Pulse Generator

3.  Output 1 is for an output with internal conditions such that the output is low except when disabled by the output control.

4.  Output 2 is for an output with internal conditions such that the output is high except when disabled by the output control.

5.  All input impulses are supplied by generators having the following characteristics: PRR ≤ MHz, $Z_O$ = 50Ω, $t_R$ ≤ 2.5ns, $t_F$ ≤ 2.5ns.

6.  The outputs are measured one at a time with one transition per measurement.

## Switching Waveforms



**Voltage Waveforms Enable and Disable Times**

## Switch Positions

| Test | Switch |
|------|--------|
| $t_{PLZ}$, $t_{PZL}$  (output on B-side) | 2 * Vdd |
| $t_{PHZ}$, $t_{PZH}$  (output on B-side) | GND |
| Prop Delay | Open |

## Test Circuit for Dynamic Electrical Characteristics

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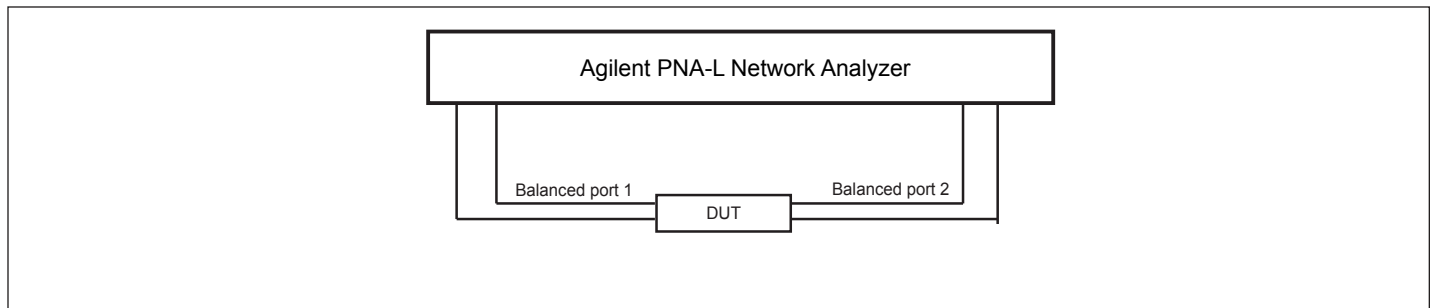
## Packaging Mechanical: 32-Contact TQFN (ZL)



NOTE :

1. ALL DIMENSIONS ARE IN mm. ANGLES IN DEGREES.
2. COPLANARITY APPLIES TO THE EXPOSED THERMAL PAD AS WELL AS THE TERMINALS.
3. REFER JEDEC MO−220.
4. RECOMMENDED LAND PATTERN IS FOR REFERENCE ONLY.
5. THERMAL PAD SOLDERING AREA

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*Enabling Serial Connectivity*

**DATE: 10/09/09**

**DESCRIPTION: 32-contact, Thin Fine Pitch Quad Flat No-Lead (TQFN)**

**PACKAGE CODE: ZL (ZL32)**

**DOCUMENT CONTROL #: PD-2044**          **REVISION: A**

09-0125

NOTE :
1. ALL DIMENSIONS ARE IN mm.
2. COPLANARITY APPLIES TO THE EXPOSED THERMAL PAD AS WELL AS THE TERMINALS.
3. REFER JEDEC MO-220.
4. RECOMMENDED LAND PATTERN IS FOR REFERENCE ONLY.
5. THERMAL PAD SOLDERING AREA (MESH STENCIL DESIGN IS RECOMMENDED.)

| SYMBOLS | MIN. | NOM. | MAX. |
|---|---|---|---|
| A | 0.70 | 0.75 | 0.80 |
| A1 | 0.00 | 0.02 | 0.05 |
| A3 | | 0.203 REF. | |
| b | 0.15 | 0.20 | 0.25 |
| D | 2.90 | 3.00 | 3.10 |
| E | 5.90 | 6.00 | 6.10 |
| D2 | 1.55 | 1.60 | 1.65 |
| E2 | 4.55 | 4.60 | 4.65 |
| L | 0.25 | 0.30 | 0.35 |
| e | | 0.40 BSC. | |
| K | | 0.40 REF. | |

**DATE: 11/11/13**

DESCRIPTION: 32-contact, Thin Fine Pitch Quad Flat No-Lead (TQFN)
PACKAGE CODE: ZLS (ZLS32)
DOCUMENT CONTROL #: PD-2175    REVISION: --

**Note:**

For latest package info, please check: http://www.pericom.com/products/packaging/mechanicals.php

## Ordering Information

| Ordering Code | Package Code | Package Description |
|---|---|---|
| PI3VDP3212ZLE | ZL | Pb-free & Green, 32-contact TQFN |
| PI3VDP3212ZLSE | ZLS | Pb-free & Green, 32-contact TQFN |

**Notes:**
- Thermal characteristics can be found on the company web site at www.pericom.com/packaging/
- "E" denotes Pb-free and Green
- Adding an "X" at the end of the ordering code denotes tape and reel packaging