DS3184DK
Quad ATM/Packet PHYs for DS3/E3/STS-1 with Built-In LIU Demo Kit

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GENERAL DESCRIPTION

The DS3184DK is an easy-to-use demo kit for the DS3184. A surface-mounted DS3184 and careful layout of the analog signal traces provide maximum signal integrity to demonstrate the transmit and receive capabilities of the DS3184. On-board Dallas 8051-compatible microcontroller and included software give point-and-click access to configuration and status registers from a personal computer. General-purpose LEDs on the board can easily be configured to indicate various alarm conditions for all four ports. The board provides eight BNC connectors for the line-side transmit and receive differential pairs, two 140-pin connectors for system interface signals, and two FPGAs to support overhead functions. All LEDs and connectors are clearly labeled with silkscreening to identify associated signals.

DEMO KIT CONTENTS

DS3184DK Board
CD-ROM
- ChipView Software
- DS3184 Definition Files
- DS3184DK Data Sheet
- DS3184 Data Sheet

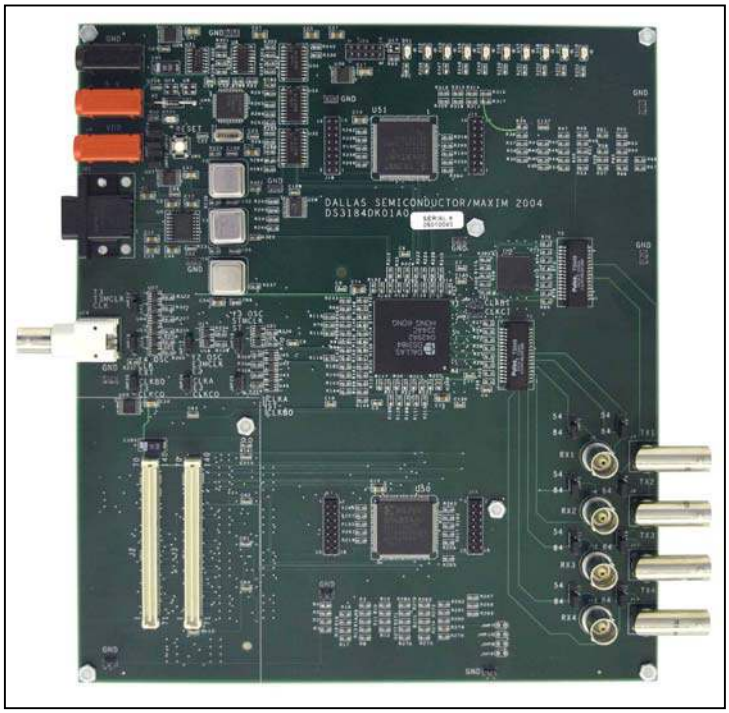
ORDERING INFORMATION

PART	DESCRIPTION
DS3184DK	Demo Kit for the DS3184

FEATURES

- Soldered DS3184 for Best Signal Integrity
- BNC Connectors, Transformers, and Termination Passives for All Four LIUs
- Careful Layout for Analog Signal Paths
- Equipment-Side Connector for External Data Source/Sink or System Side Loopback
- On-Board DS3, E3, and STS-1 Crystal Oscillators
- DS3184 Configured for CPU Bus Operation for Complete Control Over the Device
- On-Board Dallas Microcontroller and Included Software Provide Point-and-Click Access to the DS3184 Register Set
- General-Purpose LEDs can be Configured for Various Alarm Conditions
- Banana Jack Connectors for V_{DD} and GND Support Use of Lab Power Supplies
- Separate DS3184 V_{DD} to Allow I_{DD} Measurements
- Easy-to-Read Silkscreen Labels Identify the Signals Associated with All Connectors, Jumpers, and LEDs

DS3184 DEMO KIT BOARD



COMPONENT LIST

DESIGNATION	QTY	DESCRIPTION	MANUFACTURER	PART
C1, C2, C12, C13, C14, C18, C19, C44, C54, C57, C65, C69, C70, C74, C75	15	10µF ±20%, 10V ceramic capacitors (1206)	Panasonic	ECJ-3YB1A106M
C3–C7, C9, C10, C11, C20, C21, C24–C38, C46, C47, C58–C64, C66, C67, C68, C76–C87, C95, C98, C100, C102, C109–C137	82	0.1µF ±20%, 16V X7R ceramic capacitors	AVX	0603YC104MAT
C8, C15, C39, C40	4	4.7µF ±10%, 25V X5R ceramic capacitors	Panasonic	ECJ-3YB1E475K
C16, C17, C41, C42	4	6.8µF 10%, 6.3V X5R ceramic capacitors (1206)	Panasonic	ECJ-3YB0J685K
C22, C23	2	22pF ±5%, 25V NPO ceramic capacitors	AVX	06033A220JAT
C43, C103	2	68µF ±20%, 16V tantalum capacitors (D case)	Panasonic	ECS-T1CD686R
D1	1	Diode, 1A, 50V, general-purpose silicon	General Semiconductor	1N4001
DS1, DS10	2	Green SMD LEDs	Panasonic	LN1351C
DS2–DS9	8	Red SMD LEDs	Panasonic	LN1251C
DS21	1	Red SMD LED	Panasonic	LN1251C
J1, J4	2	Sockets, banana plug, horizontal, red	Mouser (distributor)	164-6219
J2, J3	2	Plugs, SMD, 140-pin, 0.8mm, 2-row vertical	AMP	179031-6
J5	1	Socket, banana plug, horizontal, black	Mouser (distributor)	164-6218
J6, J8, J10, J12	4	BNC connectors 75Ω, vertical, 5-pin	Cambridge	CP-BNCPC-004
J7, J9, J11, J13	4	Connector, BNC, 75 ohm, right angle, 5-pin	Trompeter	UCBJR220
J14	1	Amphenol, right-angle BNC	Amphenol	31-5431
J15–J18	4	Terminal strip, 16-pin, dual-row, vertical	Samtec	TSW-108-07-T-D
J21	1	Connector, DB9, right-angle, long case	AMP	747459-1
J25	1	Terminal strip, 10-pin, dual-row, vertical	—	—
JMP1, JMP2, JMP15	3	2-pin header, 0.100 centers, vertical	Samtec	TSW-102-07-T-S
JMP3–JMP6, JMP11–JMP14, JMP16, JMP17, JMP18, JMP23–JMP26	15	3-pin header, 0.100 centers, vertical	Samtec	TSW-103-07-T-S
JMP7–JMP10, JMP19–JMP22	8	Do not place, open 2 pin TH jumper	—	—
R1, R2, R3, R16–R19, R36–R39, R41–R51, R53–R59, R61–R68, R229–R231, R244	41	0Ω ±1%, 1/16W resistors (0603)	AVX	CJ10-000F
R4, R146, R147, R148, R158, R159, R160	7	Resistors (0603) Do not populate	—	—
R5, R8–15, R92, R93, R95, R161, R270–R285, R313–R320	37	10kΩ ±5%, 1/16W resistors (0603)	Panasonic	ERJ-3GEYJ103V

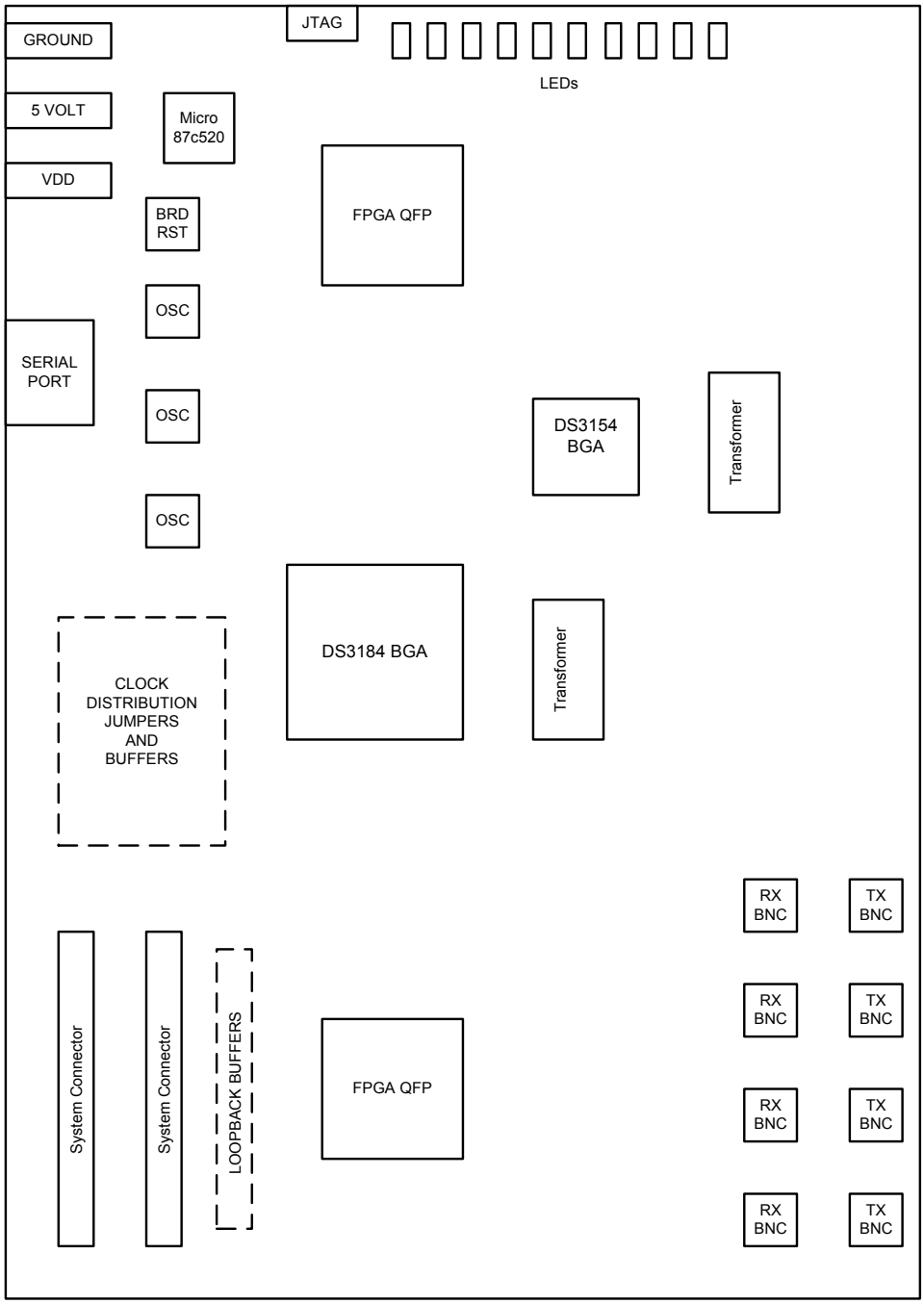
DESIGNATION	QTY	DESCRIPTION	MANUFACTURER	PART
R6, R7, R28–R35, R77–R91, R94, R96–R145, R149–R157, R162–R228, R233–R240, R255–R266, R305–R312, R321–R329	189	33Ω ±5%, 1/16W resistors (0603)	Panasonic	ERJ-3GEYJ330V
R20–R27, R69–R76	16	332Ω ±1%, 1/16W resistors (0603)	Panasonic	ERJ-3EKF3320V
R52, R246–R254	10	330Ω ±5%, 1/16W resistors (0603)	Panasonic	ERJ-3GEYJ331V
R232	1	51.1Ω ±1%, 1/16W resistor (0603)	Panasonic	ERJ-3EKF51R1V
R241	1	3.3kΩ ±5%, 1/16W resistor (0603)	Panasonic	ERJ-3GEYJ332V
R242, R243, R245, R267, R268, R269	6	4.7kΩ ±5%, 1/16W resistors (0603)	Panasonic	ERJ-3GEYJ472V
R286–R304, R330	20	100Ω ±5%, 1/16W resistors (0603)	Panasonic	ERJ-3GEYJ101V
SW5	1	Switch, momentary, 4-pin, single pole	Panasonic	EVQPAE04M
T1, T2	2	Octal T3/E3 transformers, 1 to 2, SMD 32-pin	Pulse Engineering	T3049
TP3–TP10, TP17, TP21–TP32, TP70	22	Test points, 1 plated hole, do not stuff	—	—
U1	1	Quad ATM/Packet PHYs for DS3\E3\STS1 with built-in LIU (400-pin CSBGA)	Dallas Semiconductor	DS3184
U2	1	Quad DS3/E3/STS1 LIU (144-pin CSBGA)	Dallas Semiconductor	DS3154
U3	1	Dual RS-232 transmitter/receiver (16-pin SO, 300 mils)	Dallas Semiconductor	DS232AS
U4, U5, U6, U10, U11, U12	6	IC, 3.3V octal buffer/driver (20-pin narrow SOP)	Texas Instruments	SN74ALVC244NSR
U8	1	IC, 3-line to 8-line decoder/demultiplexer (16-pin SOIC)	Texas Instruments	SN74HC138NSR
U9	1	Microprocessor voltage monitor, 3.08V reset (4-pin SOT143)	Maxim	MAX811TEUS-T
U13	1	IC, TinyLogic ultra-high-speed 2-input exclusive-OR gate (5-pin SOT23)	Fairchild	NC7SZ86M5
U14	1	Microprocessor voltage monitor, 4.38V reset (4-pin SOT143)	Maxim	MAX812MEUS-T
U17	1	Microprocessor reset circuit, 3.08V reset (3-pin SC70)	Maxim	MAX803TEXR-T
U18–U25, U41–U46	14	IC, TinyLogic ultra-high-speed 2-input OR gate (5-pin SOT23)	Fairchild	NC7SZ32M5
U26, U27, U29	3	3.3V linear regulator (16-pin TSSOP-EP)	Maxim	MAX1793EUE-33
U28	1	IC, Xilinx platform flash in-system-programmable config PROM (20-pin TSSOP)	Xilinx	XCF04SVO20C
U30	1	1.8V linear regulator (16-pin TSSOP-EP)	Maxim	MAX1793EUE-18
U31	1	IC, hex inverter, SOIC	Toshiba	TC74HC04AFN

DESIGNATION	QTY	DESCRIPTION	MANUFACTURER	PART
U32, U33, U34	3	IC, 5.0V octal buffer/driver (20-pin narrow SOIC)	Texas Instruments	SN74HC244NSR
U40	1	High-speed microcontroller (44-pin TQFP)	Dallas Semiconductor	DS87C520-ECL
U50, U51	2	IC, Xilinx Spartan 100k gate, 1.8V FPGA (144-pin TQFP)	Xilinx	XC2S100E-6TQ144C
Y1	1	11.0592MHz low-profile crystal	Pletronics	LP49-33-11.0592M
Y2	1	3.3V, 34.368MHz oscillator	Saronix	NTH089AA3-34.368
Y4	1	3.3V, 44.736MHz oscillator	Saronix	NTH089AA3-44.736
Y3	1	3.3V, 51.840MHz oscillator	Saronix	NTH089AA3-51.840

BOARD FLOOR PLAN

Figure 1 shows the floor plan of the DS3184DK. The DS3184 is near the center of the board. The analog circuitry is on the right side of the board, which includes transformers and BNC connectors. There is an optional external LIU (DS3154) that can be used in certain configurations. Located one above and one below of the DS3184 are two FPGAs that, along with headers, provide access to the overhead signals. The microprocessor is on the left top of the board, clock distribution is in the left center, and system interface is at the left bottom. General-purpose LEDs, which are driven by configurable outputs, are located at the top of the board. In the upper-left corner are banana jacks for ground, 5V (regulated to provide board V_{DD}), and a separate DS3184 V_{DD} (useful for DS3184 I_{DD} measurements). There are connectors provided for the serial interface to the microprocessor and the JTAG chain. The board also contains DS3, E3, and STS1 oscillators and the necessary jumpers to configure both the DS3184 and the DS3154 clocking.

Figure 1. Board Floor Plan



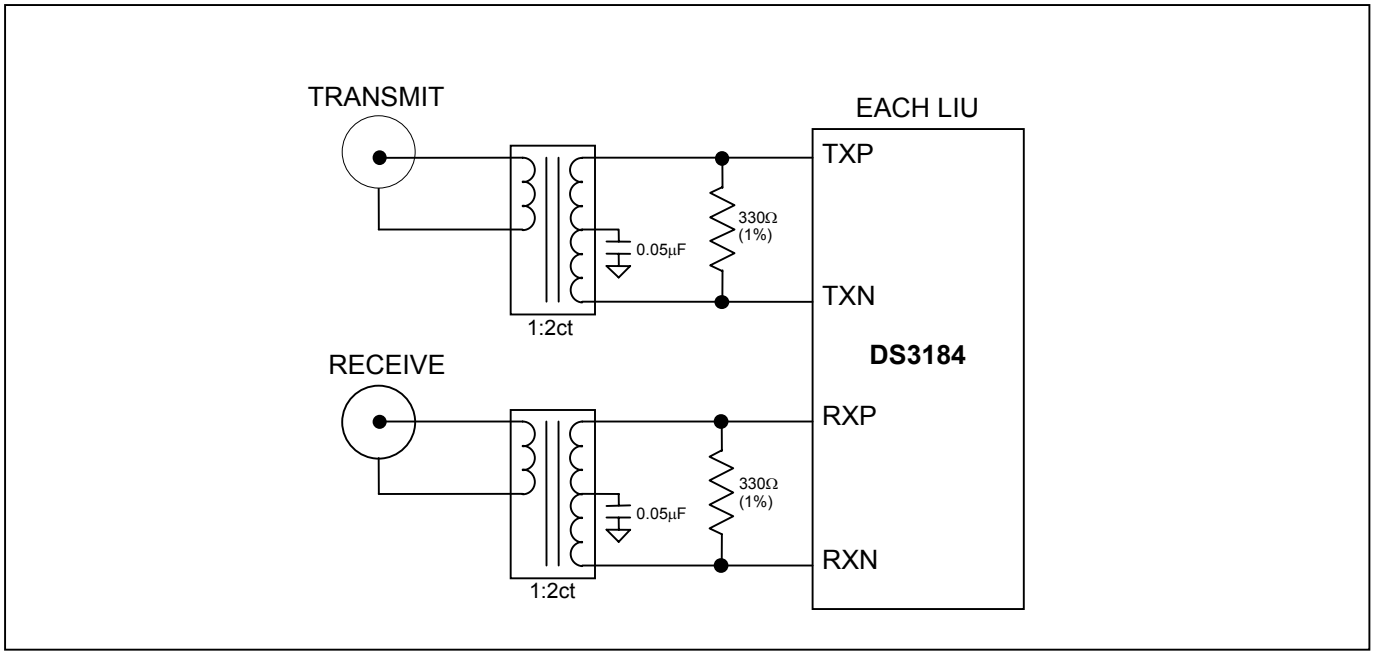
CLOCK JUMPERS

Jumper JMP16 (middle left of board) selects the clock source (external BNC or on-board oscillator) for both CLKA and the system clocks on the DS3184. Jumpers JMP17, JMP18, and JMP23 select the source of the clocks to the external LIU (DS3154), which can be on-board oscillators or a CLAD output of the DS3184. Jumpers JMP24, JMP25, and JMP26 select the specific CLAD output to be connected to the LIU clock inputs on the DS3154.

LINE-SIDE CONNECTIONS

The DS3184DK implements the transmit (Tx) and receive (Rx) line interface networks recommended in the DS3184 data sheet and shown in Figure 2. The BNC connectors for LIU1 are labeled TX1 and RX1. The BNC connectors for LIU2 are labeled TX2 and RX2. The BNC connectors for LIU3 are labeled TX3 and RX3. The BNC connectors for LIU4 are labeled TX4 and RX4.

Figure 2. Line-Side Circuitry



SYSTEM CONNECTOR

Two 140-pin connectors at the lower left of the board provide access to the DS3184 system interface pins. The connector labeled J2 supports the receive signals and J3 supports the transmit. There are ground pins spread over both connectors to maintain a low-impedance connection to interface boards. All the interface pins that are driven by the DK are series terminated at the driver to maintain signal integrity. Receive pins are looped back to transmit pins automatically when no interface board is connected via high-speed buffers. When an interface board is attached to the DK, the buffers are tri-stated.

MICROCONTROLLER

The DS87C520 microcontroller has factory-installed firmware in on-chip nonvolatile memory. This firmware translates memory access requests from the RS-232 serial port into register accesses on the DS3184. When the microcontroller starts up it turns on DS1, a green LED, to indicate that the controller is working correctly.

POWER-SUPPLY CONNECTORS

Connect a 5.0V power supply with a current rating of at least 1 amp across the red J1 and black J5 (GND) banana jacks for normal operation. Banana jack J4 accommodates DS3184 IDD measurements. This is accomplished by disconnecting the DS3184 VDD connections from the board VDD by removing jumpers 19, 20, 21, and 22. Diode

D1 provides protection against power connection reversal. The LED DS21 provides indications that a 5V supply is connected properly. The 5V supply is regulated to supply proper voltages to various circuits on the board.

CONNECTING TO A COMPUTER

Connect a standard DB-9 serial cable between the serial port on the DS3184DK and an available serial port on the host computer. The host computer must be a Windows®-based PC. Be sure the cable is a standard straight-through cable rather than a null-modem cable. Null-modem cables prevent proper operation.

INSTALLING AND RUNNING THE SOFTWARE

ChipView is a general-purpose program that supports a number of Dallas Semiconductor demo kits. To install the ChipView software, run SETUP.EXE from the disk included in the DS3184DK box or from the zip file downloadable on our website at www.maxim-ic.com/DS3184DK.

After installation, run the ChipView program with the DS3184DK board powered up and connected to the PC. If the default installation options were used, one easy way to run ChipView is to click the **Start** button on the Windows toolbar and select Programs→ChipView→ChipView. In the opening screen, click the **Register View** button. (The **Demo** and **Terminal** buttons are not supported for the DS3184DK.) Select the correct serial port in the *Port Selection* dialog box, then click OK.

Next, the *Definition File Assignment* window appears. This window has subwindows to select definition files for up to four separate boards on other Dallas evaluation platforms. Because ChipView is communicating with the DS3184DK, only one subwindow is active. In the active subwindow, select the **DS3184.DEF** definition file from the list shown, or browse to find it in another directory. Press the **Continue** button.

After selecting the definition file, the main part of the ChipView window displays the DS3184's register map (described in the DS3184 data sheet). To select a register, click on it in the register map. When a register is selected, the full name of the register and its bit map are displayed at the bottom of the ChipView window. Bits that are logic 0 are displayed in white, while bits that are logic 1 are displayed in green.

The ChipView software supports the following actions:

- **Toggle a bit.** Select the register in the register map and then click the bit in the bit map.
- **Write a register.** Select the register, click the **Write** button, and enter the value to be written.
- **Write all registers.** Click the **Write All** button and enter the value to be written.
- **Read a register.** Select the register in the register map and click the **Read** button.
- **Read all registers.** Click the **Read All** button.

Windows is a registered trademark of Microsoft Corp.

BASIC DS3184DK CONFIGURATION

The following example DS3 configuration provides a quick start to using the DS3184DK. The DS3184 and the DS3184DK can be configured in many other ways. To set up other configurations, refer to Section 9 of the DS3184 data sheet and other sections of this data sheet.

The following configuration supports port 1 only. The same directions apply for additional ports using the DEF files that support the specific port.

- Connect 5V between J1 and J5 and verify that jumpers 19 through 22 are installed. Verify LEDs DS1 and DS21 are on. Connect 75Ω coaxial cables to connectors J6 (Rx) and J7 (Tx). Verify J3 and J4 jumpers are set to the 84 position.
- Connect the serial port of a computer to J21. Run the ChipView application and load the definition file named ds3184.def provided with the kit.

The following registers in the DS3184 need to be configured. For ChipView-specific help, review the ChipView manual.

Select “ds3184.def slot_0” from the “DEF File Selection” Menu

Click Read All

Put DS3184 in known condition with all registers set to their default value by initiating a Global Reset

SET	GCR1L.RST	
CLEAR	GCR1L.RST	
CLEAR	GCR1L.RSTDP	clear data path resets

Note: To configure all 4 ports simultaneously, set GCR1U.GWRM.

SET	GCR1U.SIW[1:0]	=	01	16 bit system interface
SET	GCR1U.SIM[1:0]	=	11	POS PHY L3

Note: UTOPIA L2 is the default setting: GCR1U.SIM[1:0] = 00

Configure internal CLAD

Note: The following CLAD configuration requires a DS3 clock applied to CLKA (CLKB and CLKC are driven low).

See CLAD table in DS318x data sheet for other configurations

CLEAR	GCR2L.CLAD3
SET	GCR2L.CLAD2
CLEAR	GCR2L.CLAD1
CLEAR	GCR2L.CLAD0

Select “ports.def slot_0” from the “DEF File Selection” Menu

Click Read All

CLEAR	PCR1L.RSTDP	normal operation
CLEAR	PCR1L.PD	
SET	PCR1U.PAIS2	disable payload AIS
SET	PCR1U.PAIS1	
SET	PCR1U.PAIS0	
SET	PCR1U.LAIS1	disable line AIS
SET	PCR1U.LAIS0	

Configure the Framer and LIU

For DS3 C-bit format (default mode)

CLEAR	PCR2L.FM5
CLEAR	PCR2L.FM4
CLEAR	PCR2L.FM3
CLEAR	PCR2L.FM2
CLEAR	PCR2L.FM1
CLEAR	PCR2L.FM0

SET	PCR2U.LM0	LIU on, No JA
SET	PCR2U.LM1	JA on in RX path

Select “FIFO_ALL.def slot_0” from the “DEF File Selection” Menu

Click Read All

CLEAR TCR.TFRST – do this for all 4 ports
CLEAR RCR.RFRST – do this for all 4 ports

SET TPACL of Port 1 = 0x00 (default setting)
SET RPACL of Port 1 = 0x00 (default setting)

SET TPACL of Port 2 = 0x01
SET RPACL of Port 2 = 0x01

SET TPACL of Port 3 = 0x02
SET RPACL of Port 3 = 0x02

SET TPACL of Port 4 = 0x03
SET RPACL of Port 4 = 0x03

SET RLCRU of Port 1 = 0x08 – set receive FIFO almost empty level
SET TLCRU of Port 1 = 0x10 (default) – set transmit FIFO almost empty level

PC BOARD LAYOUT RECOMMENDATIONS

Standard high-speed layout guidelines should be observed when designing a PC board to support the DS3184. The DS3184 should have a low-impedance power supply path that is accomplished with an appropriate decoupling scheme. Decoupling capacitors should be connected directly to the planes with minimal trace length. Surface-mount ceramic capacitors should be used with one 0.1μF per power pin to provide adequate decoupling. Bulk capacitors of the higher capacitance tantalum type should be used near the power-supply connections to provide low-frequency decoupling. All high-speed connections to the DS3184 should be designed with controlled impedance and proper terminations to prevent reflections. The differential connections to the primary or system side of the transformer should be short traces from the DS3184 run together with respect to differential pairs. The connections on the secondary or network side of the transformers should be 75Ω controlled impedance traces.

DS3184 INFORMATION

The DS3184 Quick View page on our website has the latest DS3184 data sheet, application notes, and downloads. Go to www.maxim-ic.com/DS3184.

DS3184DK INFORMATION

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TECHNICAL SUPPORT

For additional technical support, please email your questions to telecom.support@dalsemi.com.

SCHEMATICS

The following 13 pages provide the schematic diagram of the DS3184DK.

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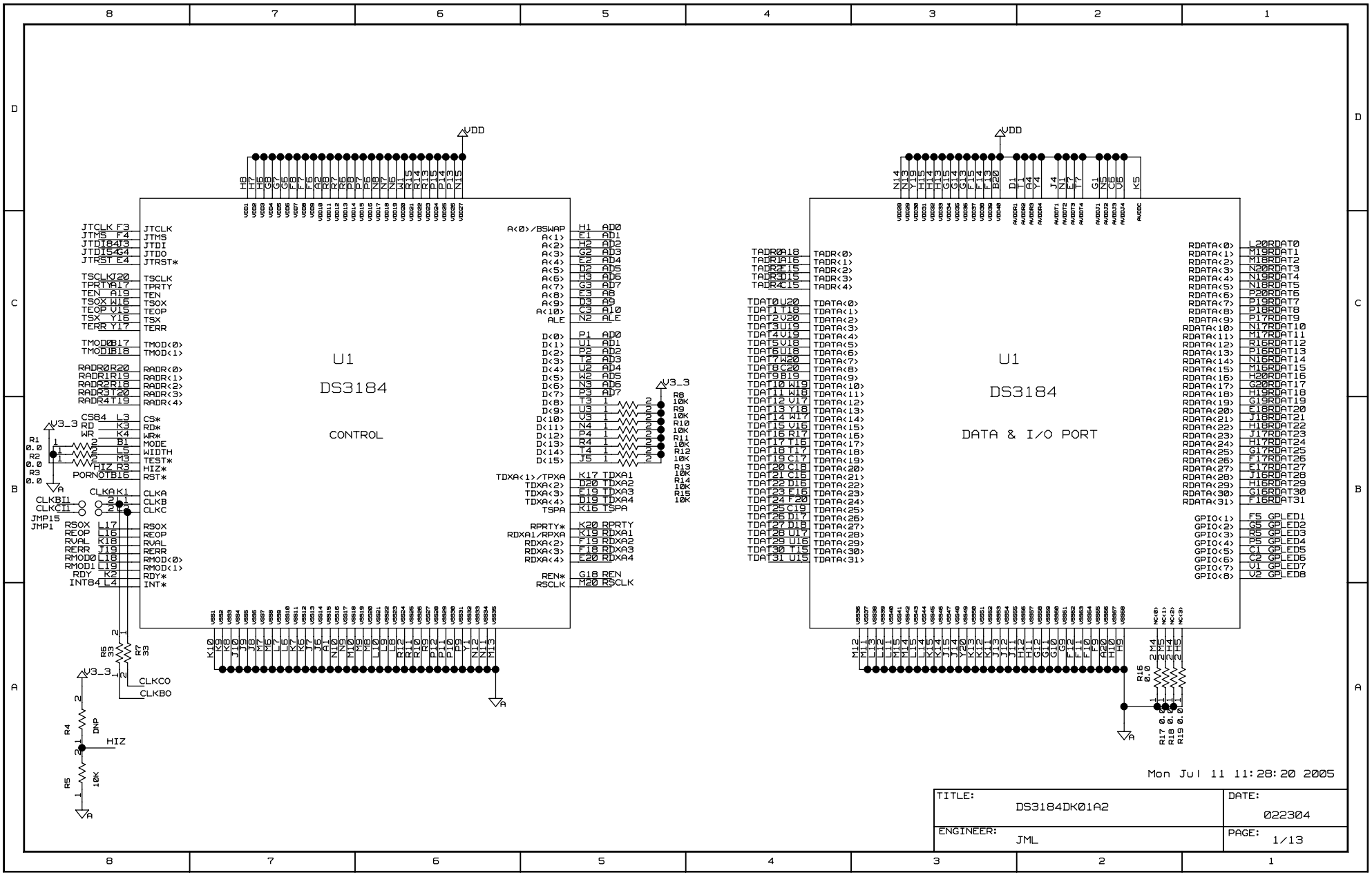
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DS3184
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U1
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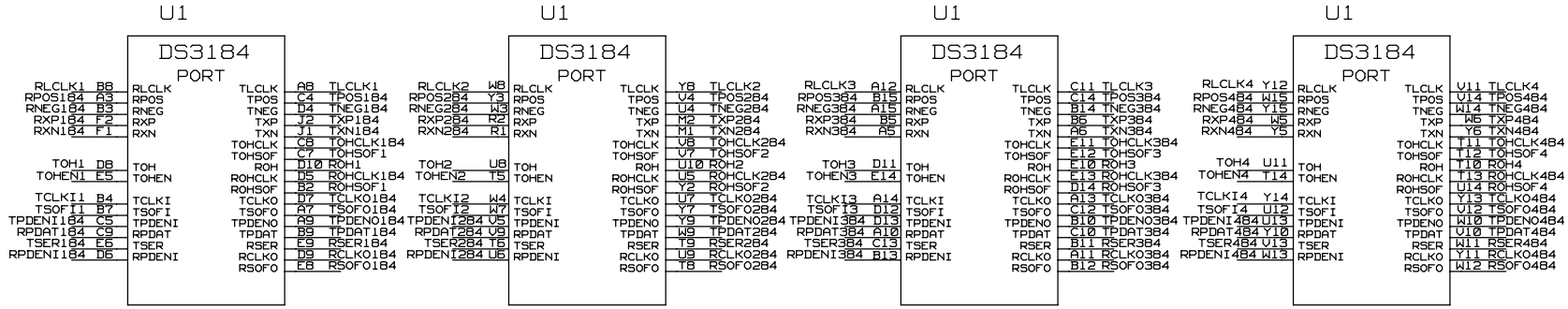

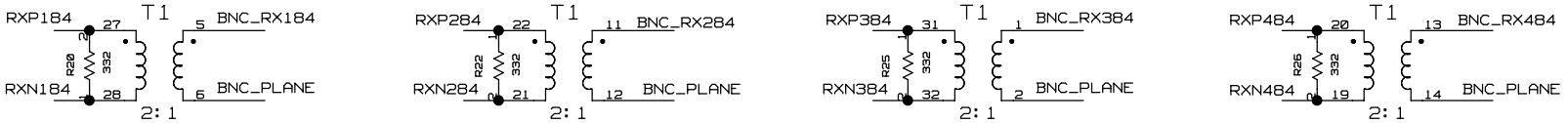

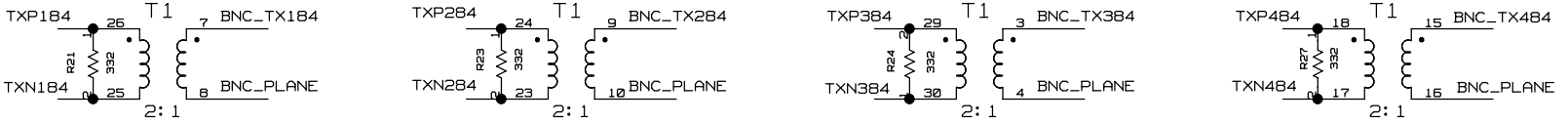

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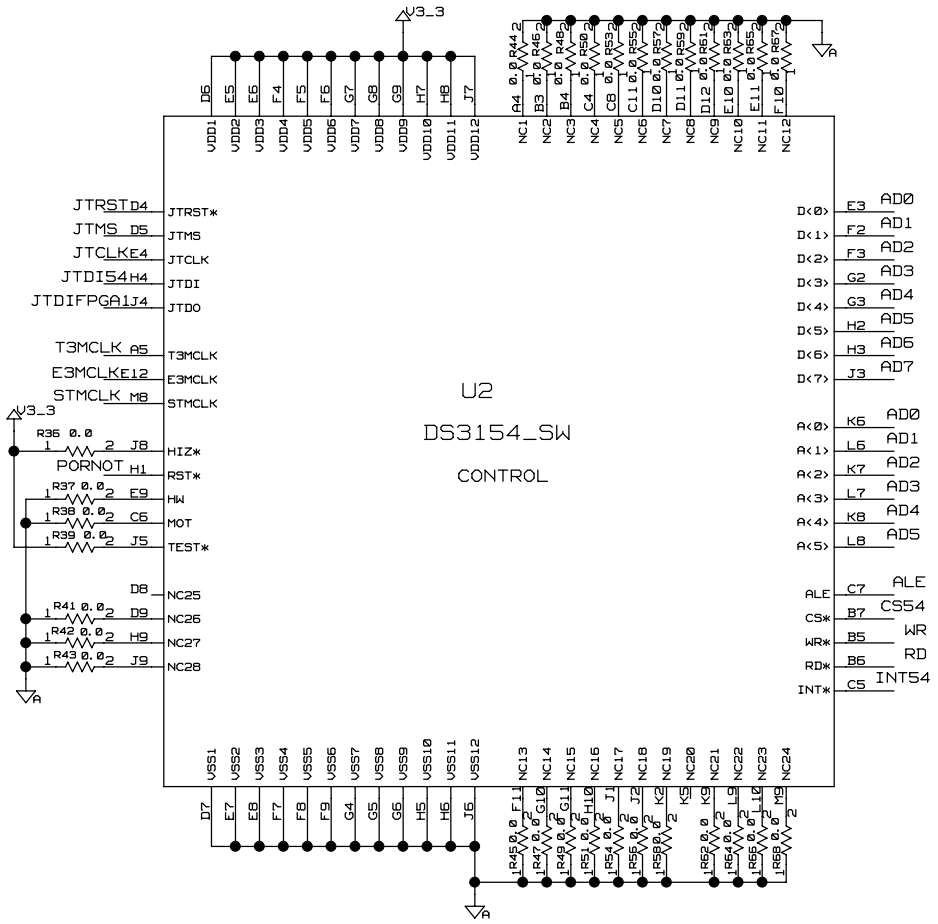

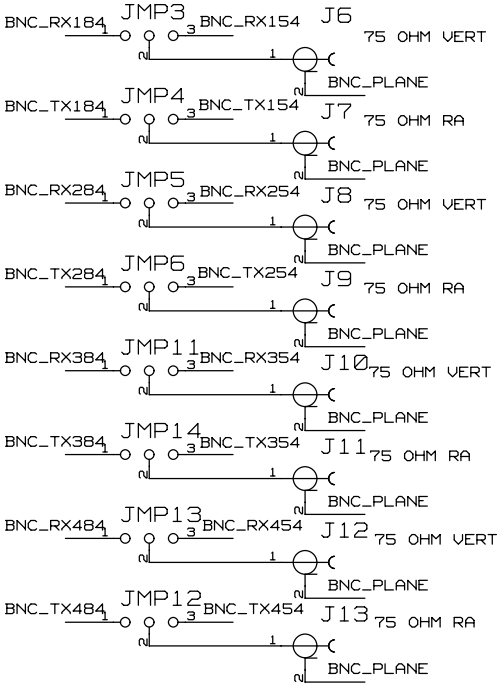

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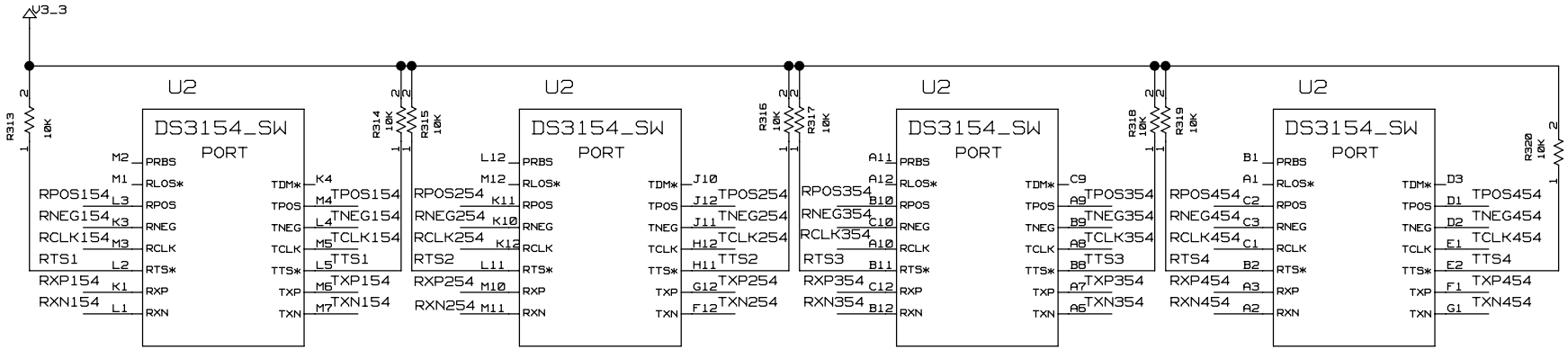

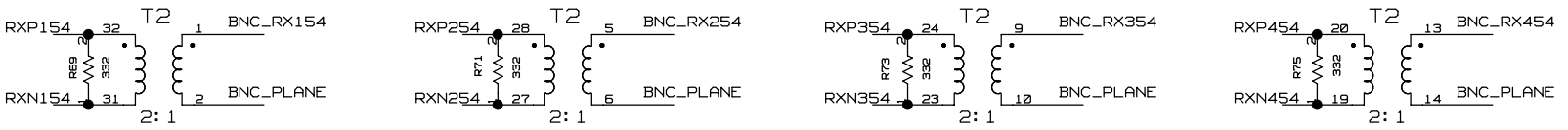

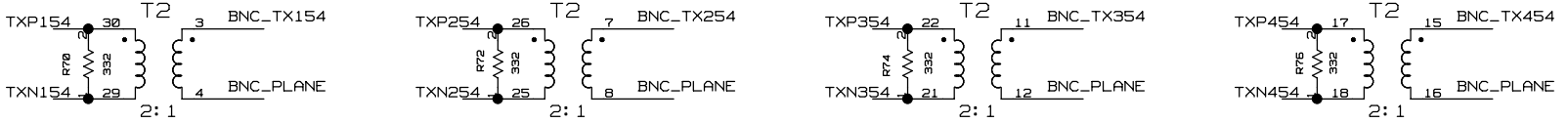

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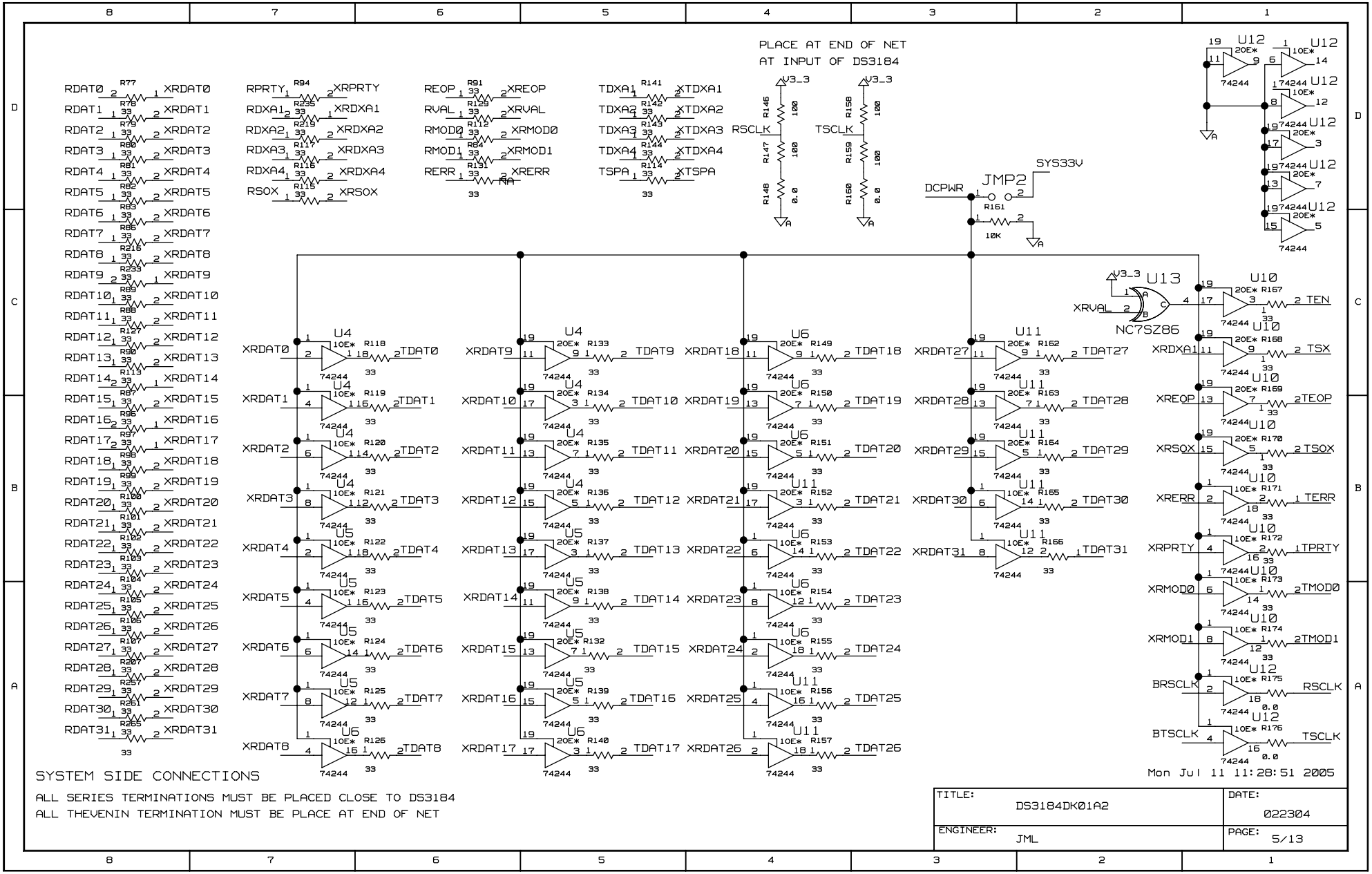

SYSTEM SIDE CONNECTIONS

ALL SERIES TERMINATIONS MUST BE PLACED CLOSE TO DS3184

ALL THEVENIN TERMINATION MUST BE PLACE AT END OF NET

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PLUG

P1

J3

	1	1	71	71	
TDAT0	2	2	72	72	GNDA
TDAT2	3	3	73	73	TDAT1
GNDA	4	4	74	74	TDAT3
TDAT4	5	5	75	75	GNDA
TDAT6	6	6	76	76	TDAT5
GNDA	7	7	77	77	TDAT7
	8	8	78	78	SYS33V
TDAT9	9	9	79	79	TDAT8
GNDA	10	10	80	80	TDAT10
TDAT11	11	11	81	81	GNDA
TDAT13	12	12	82	82	TDAT12
	13	13	83	83	
TDAT14	14	14	84	84	GNDA
TDAT16	15	15	85	85	TDAT15
GNDA	16	16	86	86	TDAT17
TDAT18	17	17	87	87	GNDA
TDAT20	18	18	88	88	TDAT19
GNDA	19	19	89	89	TDAT21
	20	20	90	90	SYS33V
TDAT23	21	21	91	91	TDAT22
GNDA	22	22	92	92	TDAT24
TDAT25	23	23	93	93	GNDA
TDAT27	24	24	94	94	TDAT26
	25	25	95	95	
TDAT28	26	26	96	96	GNDA
TDAT30	27	27	97	97	TDAT29
GNDA	28	28	98	98	TDAT31
TPRTY	29	29	99	99	GNDA
TADR0	30	30	100	100	TSOX
GNDA	31	31	101	101	TADR1
	32	32	102	102	SYS33V
TADR3	33	33	103	103	TADR2
GNDA	34	34	104	104	TADR4
XTDXA1	35	35	105	105	GNDA
XTDXA3	36	36	106	106	XTDXA2
	37	37	107	107	
XTDXA4	38	38	108	108	GNDA
	39	39	109	109	
GNDA	40	40	110	110	
	41	41	111	111	GNDA
	42	42	112	112	
GNDA	43	43	113	113	
	44	44	114	114	SYS33V
TEN	45	45	115	115	
GNDA	46	46	116	116	TEOP
TERR	47	47	117	117	GNDA
TMOD1	48	48	118	118	TMOD0
	49	49	119	119	
TSX	50	50	120	120	GNDA
TSCLK	51	51	121	121	XTSPA
GNDA	52	52	122	122	
	53	53	123	123	GNDA
	54	54	124	124	
GNDA	55	55	125	125	
	56	56	126	126	SYS33V
	57	57	127	127	
GNDA	58	58	128	128	
	59	59	129	129	GNDA
AD0	60	60	130	130	
	61	61	131	131	
AD1	62	62	132	132	GNDA
AD3	63	63	133	133	AD2
GNDA	64	64	134	134	AD4
AD5	65	65	135	135	GNDA
AD7	66	66	136	136	AD6
GNDA	67	67	137	137	CSA
	68	68	138	138	SYS33V
RD	69	69	139	139	CSB
GNDA	70	70	140	140	WR

PLUG

P2

J2

	1	1	71	71	
XRDAT0	2	2	72	72	GNDA
XRDAT2	3	3	73	73	XRDAT1
GNDA	4	4	74	74	XRDAT3
XRDAT4	5	5	75	75	GNDA
XRDAT6	6	6	76	76	XRDAT5
GNDA	7	7	77	77	XRDAT7
	8	8	78	78	SYS33V
XRDAT9	9	9	79	79	XRDAT8
GNDA	10	10	80	80	XRDAT10
XRDAT11	11	11	81	81	GNDA
XRDAT13	12	12	82	82	XRDAT12
	13	13	83	83	
XRDAT14	14	14	84	84	GNDA
XRDAT16	15	15	85	85	XRDAT15
GNDA	16	16	86	86	XRDAT17
XRDAT18	17	17	87	87	GNDA
XRDAT20	18	18	88	88	XRDAT19
GNDA	19	19	89	89	XRDAT21
	20	20	90	90	SYS33V
XRDAT23	21	21	91	91	XRDAT22
GNDA	22	22	92	92	XRDAT24
XRDAT25	23	23	93	93	GNDA
XRDAT27	24	24	94	94	XRDAT26
	25	25	95	95	
XRDAT28	26	26	96	96	GNDA
XRDAT30	27	27	97	97	XRDAT29
GNDA	28	28	98	98	XRDAT31
XRPRTY	29	29	99	99	GNDA
XRSOX	30	30	100	100	XRVAL
GNDA	31	31	101	101	XRDXA1
	32	32	102	102	SYS33V
XRMOD1	33	33	103	103	XRMOD0
GNDA	34	34	104	104	XRERR
XREOP	35	35	105	105	GNDA
RADR1	36	36	106	106	RADR0
	37	37	107	107	
RADR2	38	38	108	108	GNDA
RADR4	39	39	109	109	RADR3
GNDA	40	40	110	110	XRDXA2
XRDXA3	41	41	111	111	GNDA
	42	42	112	112	XRDXA4
GNDA	43	43	113	113	
	44	44	114	114	SYS33V
	45	45	115	115	
GNDA	46	46	116	116	
	47	47	117	117	GNDA
	48	48	118	118	
	49	49	119	119	
REN	50	50	120	120	GNDA
	51	51	121	121	RSCLK
GNDA	52	52	122	122	
	53	53	123	123	GNDA
	54	54	124	124	
GNDA	55	55	125	125	
	56	56	126	126	SYS33V
A1	57	57	127	127	A0
GNDA	58	58	128	128	A2
A3	59	59	129	129	GNDA
A5	60	60	130	130	A4
	61	61	131	131	
A6	62	62	132	132	GNDA
A8	63	63	133	133	A7
GNDA	64	64	134	134	A9
A10	65	65	135	135	GNDA
	66	66	136	136	A11
GNDA	67	67	137	137	
	68	68	138	138	DCPWR
	69	69	139	139	
GNDA	70	70	140	140	

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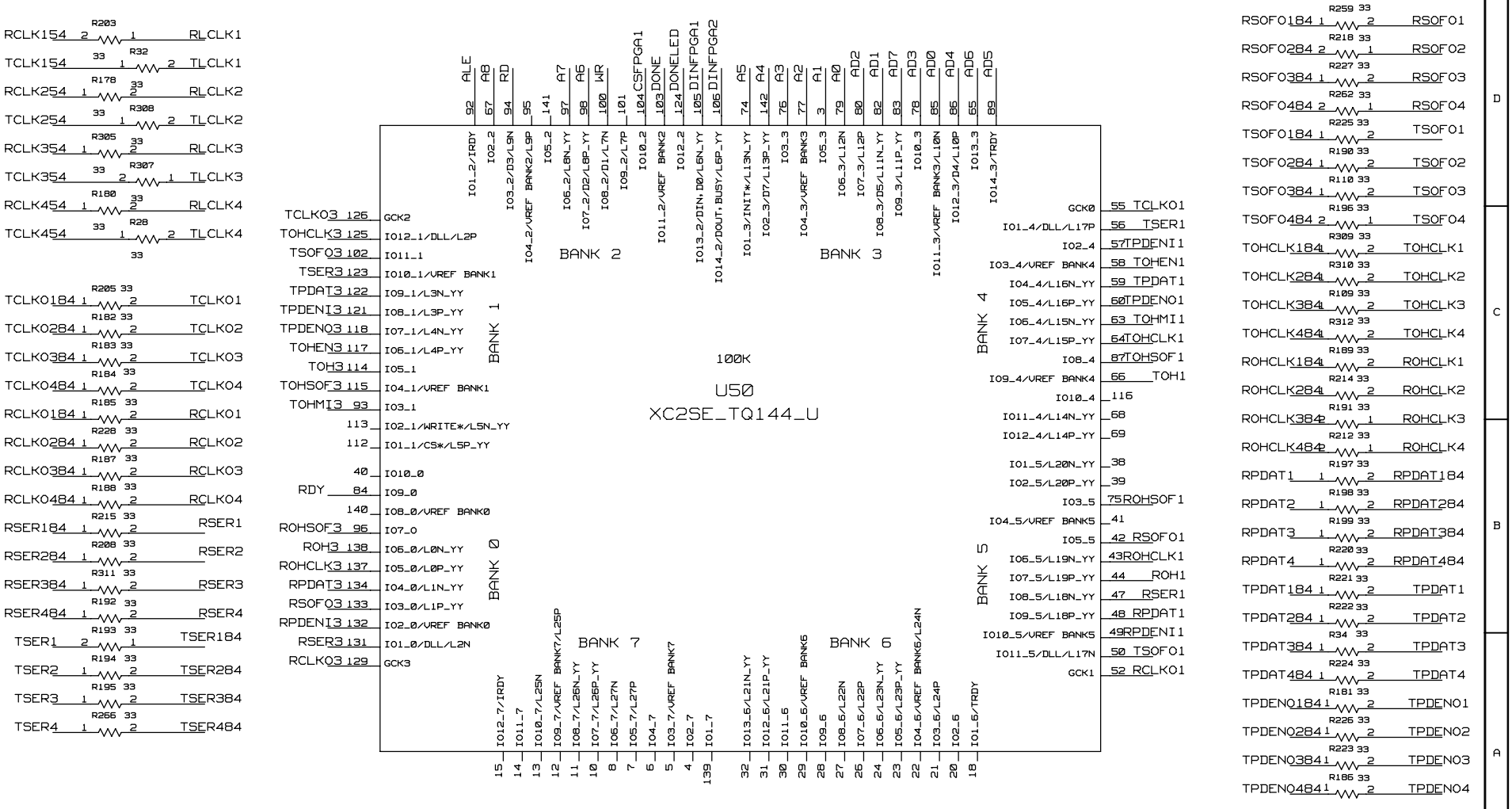

OVERHEAD CONNECTIONS

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TITLE: DS3184DK01A2	DATE: 022304
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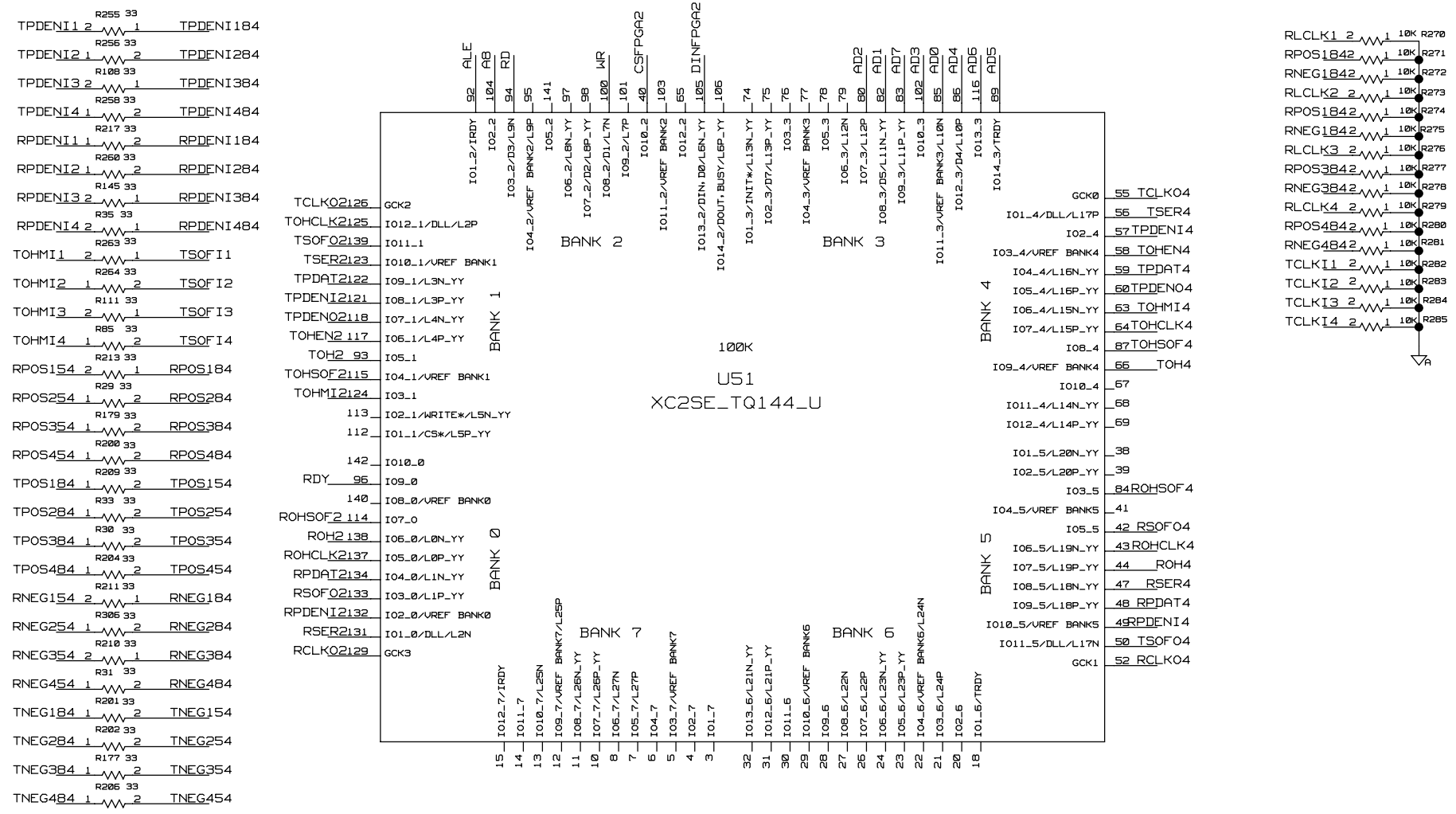

OVERHEAD CONNECTIONS

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TITLE: DS3184DK01A2	DATE: 022304
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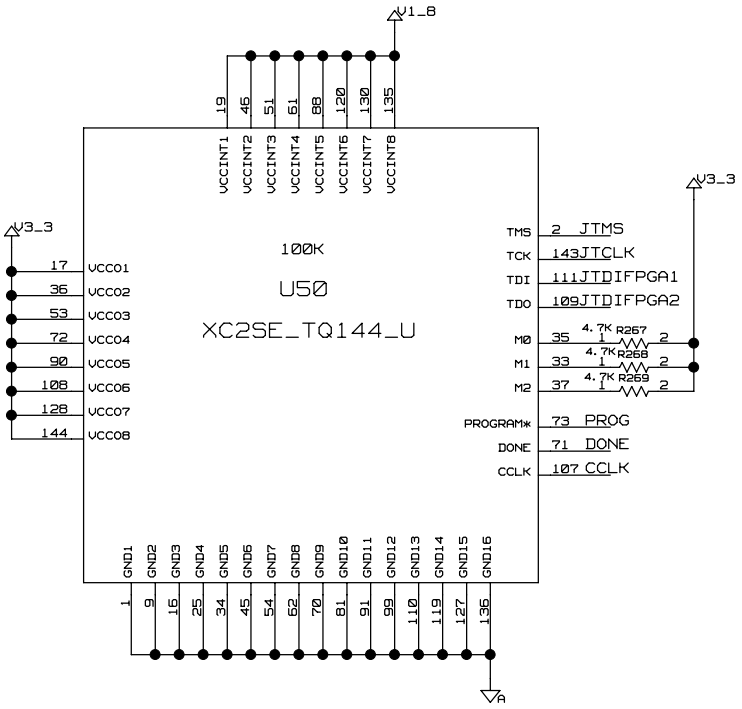

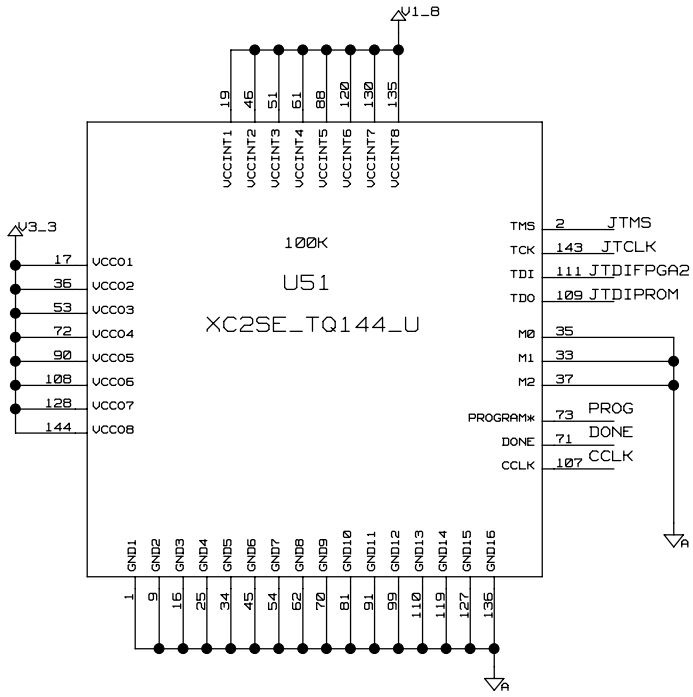

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OVERHEAD CONNECTIONS

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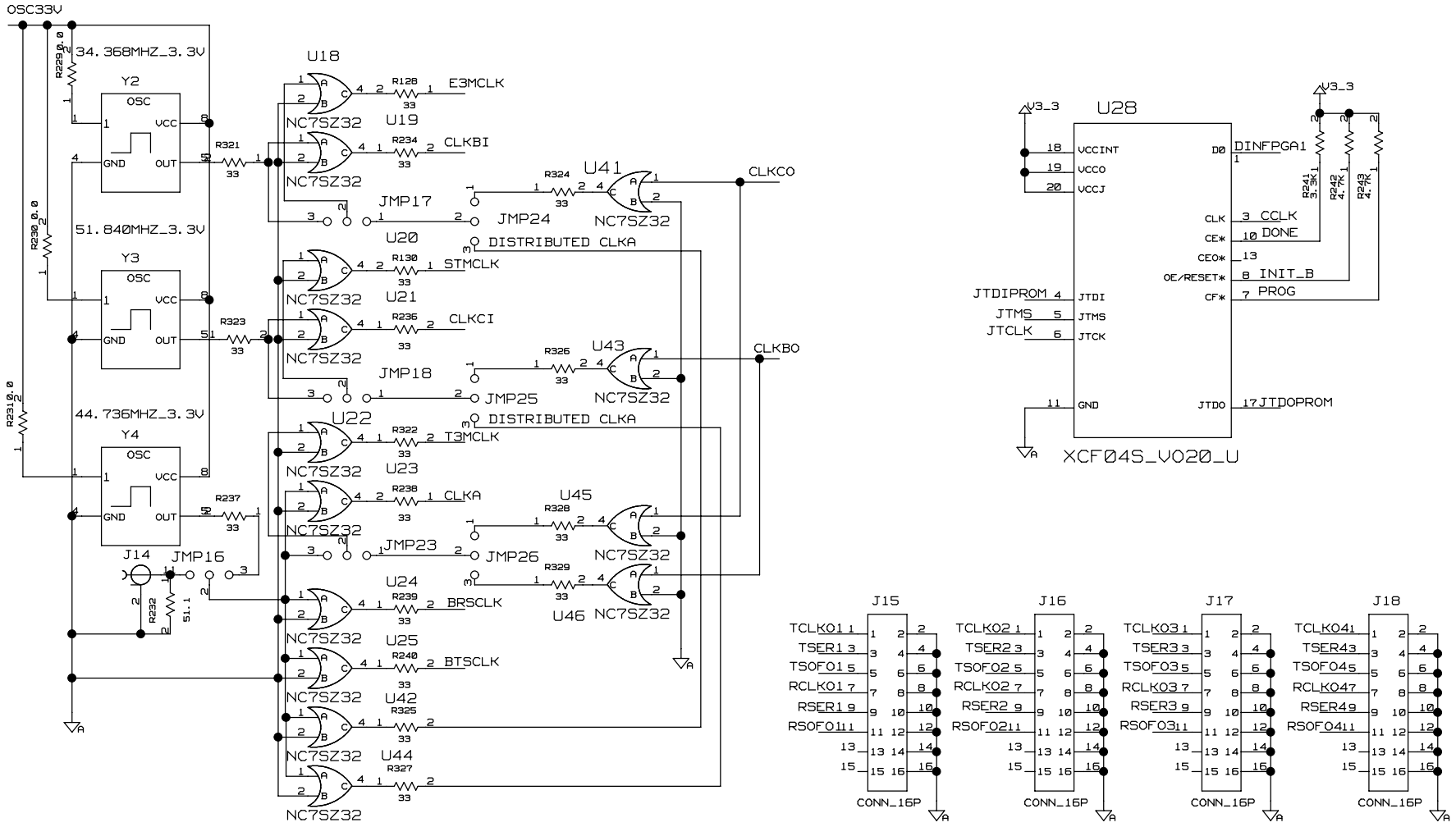

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CLOCK DISTRIBUTION

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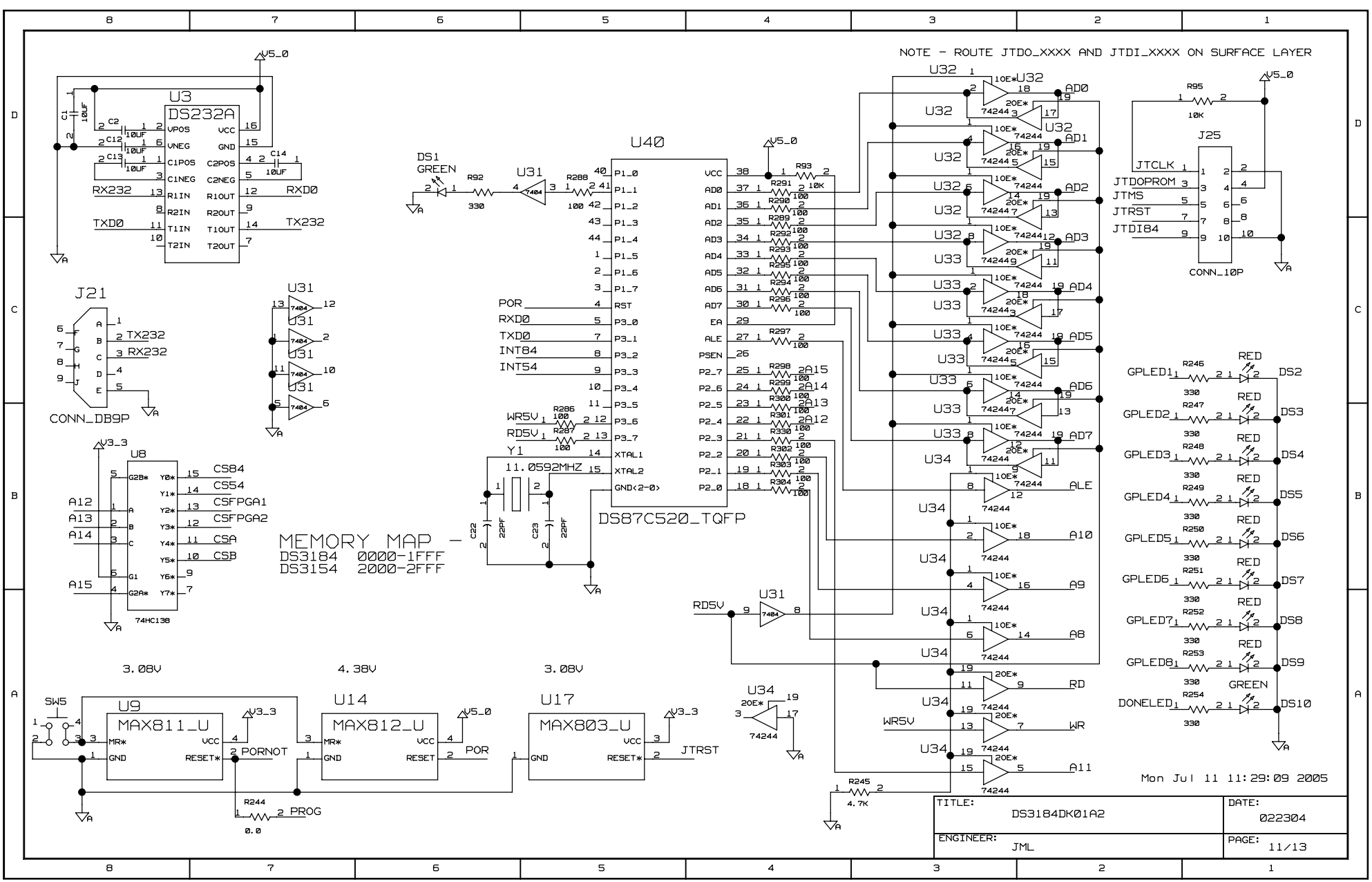
NOTE - ROUTE JTDO_XXXX AND JTDI_XXXX ON SURFACE LAYER
U3
DS232A
U40
DS87C520_TQFP
J21
CONN_DB9P
J25
CONN_10P
U8
74HC138
MEMORY MAP -
DS3184 0000-1FFF
DS3154 2000-2FFF
Y1
11.0592MHZ
U9
MAX811_U
U14
MAX812_U
U17
MAX803_U
3.08V
4.38V
3.08V
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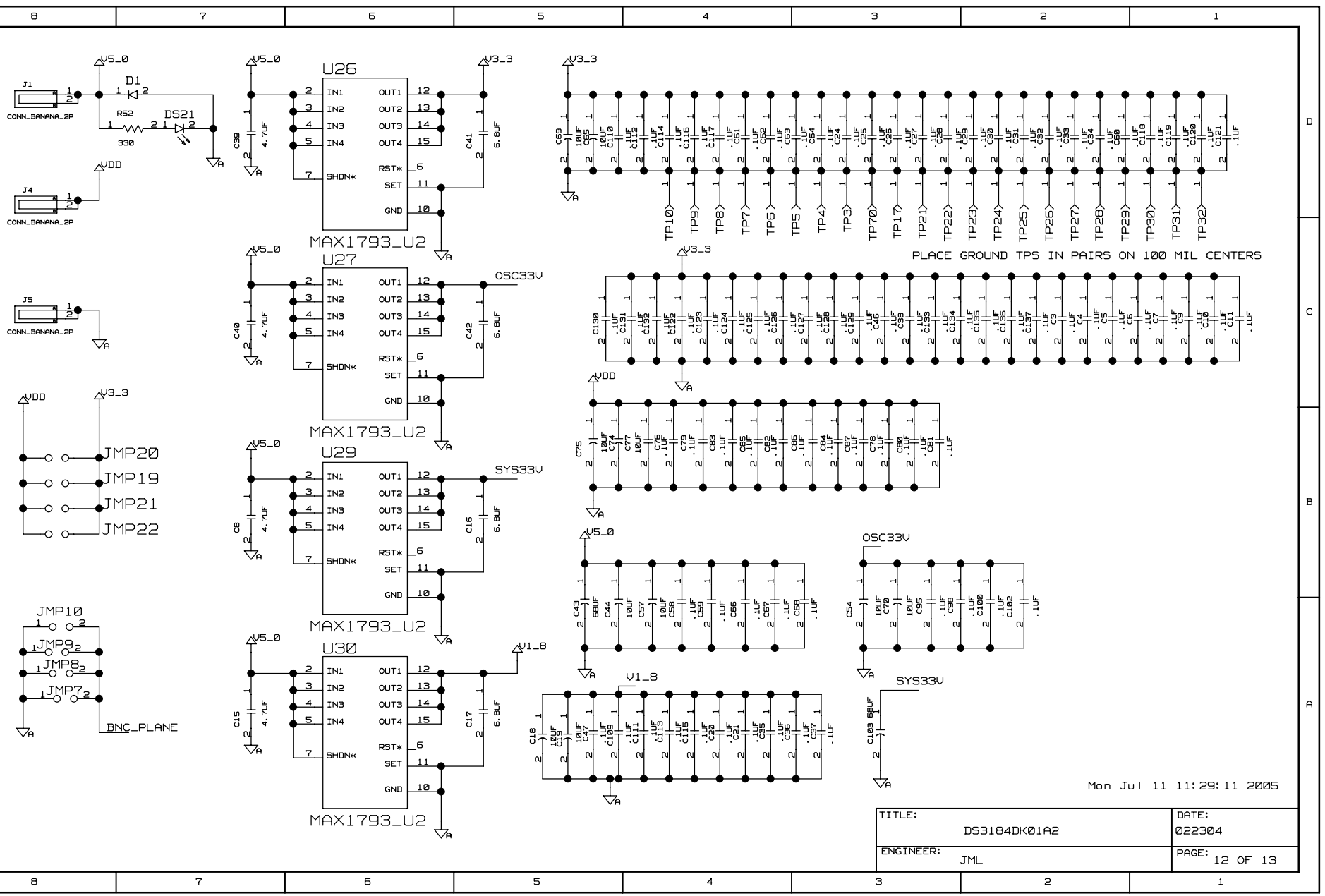
J1
CONN_BANANA_2P
D1
R52
330
DS21
J4
CONN_BANANA_2P
J5
CONN_BANANA_2P
JMP20
JMP19
JMP21
JMP22
JMP10
JMP9
JMP8
JMP7
BNC_PLANE
U26
U27
U29
U30
MAX1793_U2
IN1
IN2
IN3
IN4
SHDN*
RST*
SET
GND
OUT1
OUT2
OUT3
OUT4
V5_0
V3_3
VDD
V1_8
OSC33V
SYS33V
TP10
TP9
TP8
TP7
TP6
TP5
TP4
TP3
TP70
TP17
TP21
TP22
TP23
TP24
TP25
TP26
TP27
TP28
TP29
TP30
TP31
TP32
PLACE GROUND TPS IN PAIRS ON 100 MIL CENTERS
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REVISION HISTORY -

062904 - A0 - INITIAL RELEASE

040805 - A1 - ADDED MISSING SIGNAL NAMES ON PAGE 12 & CLEANED-UP TEXT ON VARIOUS PAGES.

070705 - A2 - ADDED VDD CONNECTION TO TTS/RTS NET
FIXED XRMOD1/RVAL CONNECTIONS
FIXED ALE SHORT ACROSS U34
CHANGED R92 VALUE TO 330 OHMS
CHANGED R175 AND R176 TO 33 OHMS FROM 0
CHANGED R148 AND R160 FROM DNP TO 0
CHANGED R146, R147, R158, R159 FROM DNP TO 100 OHMS
CHANGED JMP19 TO JMP22 FROM DNP TO PLACE
ALL A2 CHANGES ARE DOCUMENT CHANGES TO MATCH MODIFIED BOARDS WITH SCHEMATIC

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