TPS61022EVM-034 Evaluation module

The TPS61022EVM-034 evaluates the performance of the TPS61022, which is a 8-A boost converter with 0.5-V ultra-low input voltage. This user's guide describes the input and output ranges, EVM setup, bill of materials (BOM), schematic, and the PCB layout.

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Trademarks

1 Introduction

1.1 Performance

Table 1 provides a summary of the TPS61022EVM performance characteristics, tested at 25°C ambient temperature.

Table 1. EVM Characteristics

	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input voltage			3.6		V
Output voltage	TPS61022EVM, V_{IN} = 3.6 V, I_O ≤ 3A		5.1		V
Output current	V_{IN} = 2.7 V			3	A
	V_{IN} = 1.8 V			2	

1.2 Modification

The EVM is designed to support some modifications by the user. The external component can be changed according to the real application.

1.3 Input Capacitor

A 150-µF tantalum capacitor, C1, is added as the input capacitor in the EVM. The ESR of the tantalum capacitor is 0.1 Ω, to damp the ringing of the input voltage when the EVM is powered by a power supply with a long cable. The capacitor is not required for proper operation and can be removed in a real application.

1.4 Feedforward Capacitor

A feedforward capacitor C8 in parallel with R1 induces a pair of zero and pole in the loop transfer function. By setting the proper zero frequency, the feedforward capacitor can increase the phase margin to improve the loop stability. The C8 is not populated in the TPS61022EVM. The phase margin of the TPS61022EVM is good enough when the input voltage is from 2.5 V to 4.4 V. In the applications that input voltage is below 2 V or output effective capacitance is larger than 40 µF, TI suggests to add the feedforward capacitor. The calculation of the feedforward capacitor can be found in the TPS61022 data sheet and in TI application report *Feedforward Capacitor Makes Boost Converter Fast and Stable*.

For example, TI suggests a 10-pF feedforward capacitor for C8 if input voltage of the EVM is 1.8 V. Figure 1 is the Bode plot with and without the feedforward capacitor. The phase margin is 63° with the feedforward capacitor, while the phase margin is only 44° without feedforward capacitor. Test conditions are VIN = 1.8 V, V_{OUT} = 5 V, and I_{OUT} = 1 A,

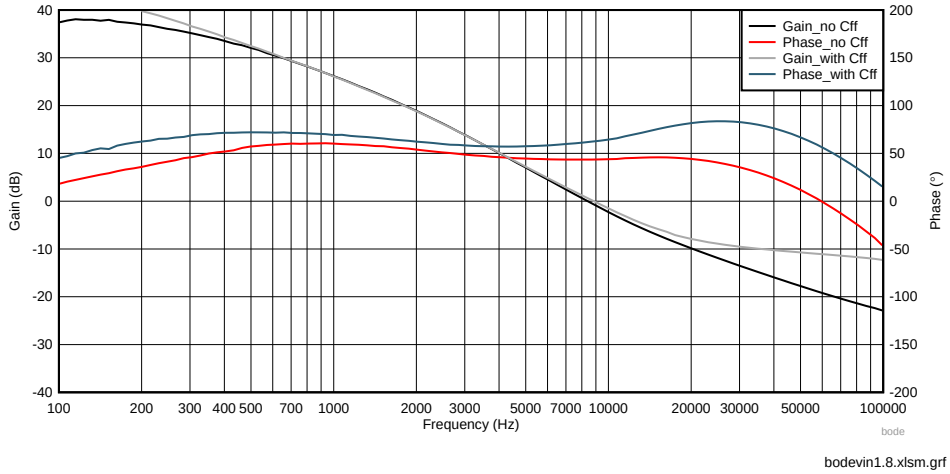

Figure 1. Bode Plot Comparison With and Without Feedforward Capacitor

2 Setup

This section describes the setup of the TPS61022EVM-034.

2.1 Input/Output Connector Descriptions

See the following :

J1-VIN	Positive input connection from the input supply for the EVM
J2-VOUT	Positive connection for the output voltage
J3-GND	Return connection from the input supply for the EVM
J4-GND	Return connection for the output voltage
J5-MODE	MODE pin input jumper. Place a jumper across MODE and pin 1 (GND) to set in auto PFM mode, place a jumper across MODE and pin 3 (VIN) to set in forced PWM mode
J6-EN	EN pin input jumper. Place a jumper across EN and pin 3 (VIN) to turn on the IC, place a jumper across EN and pin 1 (GND) to turn off the IC
J7-VIN_S	Input voltage sensing for measuring efficiency. VIN_S+ is for positive input and VIN_S- is for negative input.
J8-VOUT_S	Output voltage sensing for measuring efficiency. VOUT_S+ is for output positive node and VOUT_S- is for output negative node

3 Schematic and Bill of Materials

This section provides the TPS61022EVM-034 schematic, bill of materials (BOM), and board layout.

3.1 Schematic

Figure 2 is the EVM schematic.

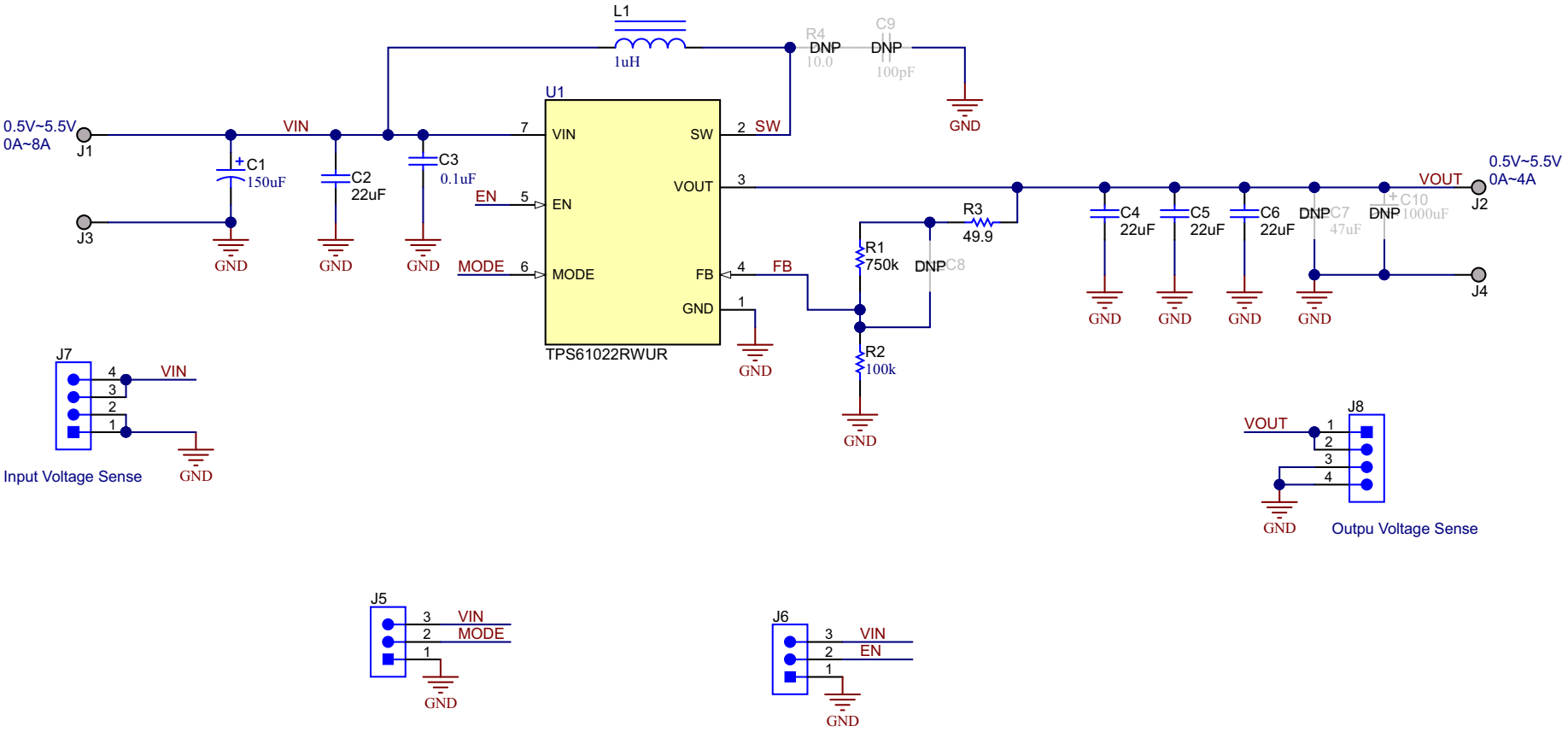

Figure 2. TPS61022EVM-034 Schematic

3.2 Bill of Materials

Table 2 displays the EVM bill of materials.

Table 2. TPS61022EVM-034 Bill of Materials

Designator	Qty	Value	Description	PackageReference	PartNumber	Manufacturer
C1	1	150uF	CAP, TA, 150 uF, 10 V, +/- 10%, 0.1 ohm, SMD	7343-31	T495D157K010ATE100	Kemet
C2, C4, C5, C6	4	22uF	CAP, CERM, 22 uF, 10 V, +/- 20%, X5R, 0805	0805	GRM21BR61A226ME44L	MuRata
C3	1	0.1uF	CAP, CERM, 0.1 uF, 10 V, +/- 10%, X5R, 0402	0402	GRM155R61A104KA01D	MuRata
J1, J2, J3, J4	4		Terminal, Turret, TH, Double	Keystone1502-2	1502-2	Keystone
J5, J6	2		Header, 100mil, 3x1, Gold, TH	3x1 Header	TSW-103-07-G-S	Samtec
J7, J8	2		Header, 100mil, 4x1, Gold, TH	4x1 Header	TSW-104-07-G-S	Samtec
L1	1	1uH	Inductor, Shielded, Composite, 1 uH, 21.8 A, 0.00455 ohm, SMD	XAL7030	XAL7030-102MEB	Coilcraft
R3	1	49.9	RES, 49.9, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	CRCW060349R9FKEA	Vishay-Dale
R1	1	750k	RES, 750 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	CRCW0603750KFKEA	Vishay-Dale
R2	1	100k	RES, 100 k, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	CRCW0603100KFKEA	Vishay-Dale
U1	1		8-A boost converter with 0.5-v ultra-low input voltage, RWU0007A (VQFN-HR-7)	RWU0007A	TPS61022	Texas Instruments
C7	0	47uF	CAP, CERM, 47 uF, 10 V, +/- 10%, X5R, 1206	1206	GRM31CR61A476KE15L	MuRata
C9	0	100pF	CAP, CERM, 100 pF, 50 V, +/- 5%, C0G/NP0, 0603	0603	GRM1885C1H101JA01D	MuRata
C10	0	1000uF	CAP, AL, 1000 uF, 10 V, +/- 20%, 0.15 ohm, SMD	SMT Radial G	EEE-FC1A102P	Panasonic
C8	0	10pF	CAP, CERM, 10 pF, 10 V, +/- 10%, X7R, 0603	0603	0603ZC100KAT2A	AVX
R4	0	10.0	RES, 10.0, 1%, 0.1 W, AEC-Q200 Grade 0, 0603	0603	CRCW060310R0FKEA	Vishay-Dale

4 Board Layout

The PCB of the TPS61022EVM has four layers. Figure 3 and Figure 4 show the top side and bottom side of the PCB layout, respectively. The two internal layers are ground panel helping to improve the thermal performance.

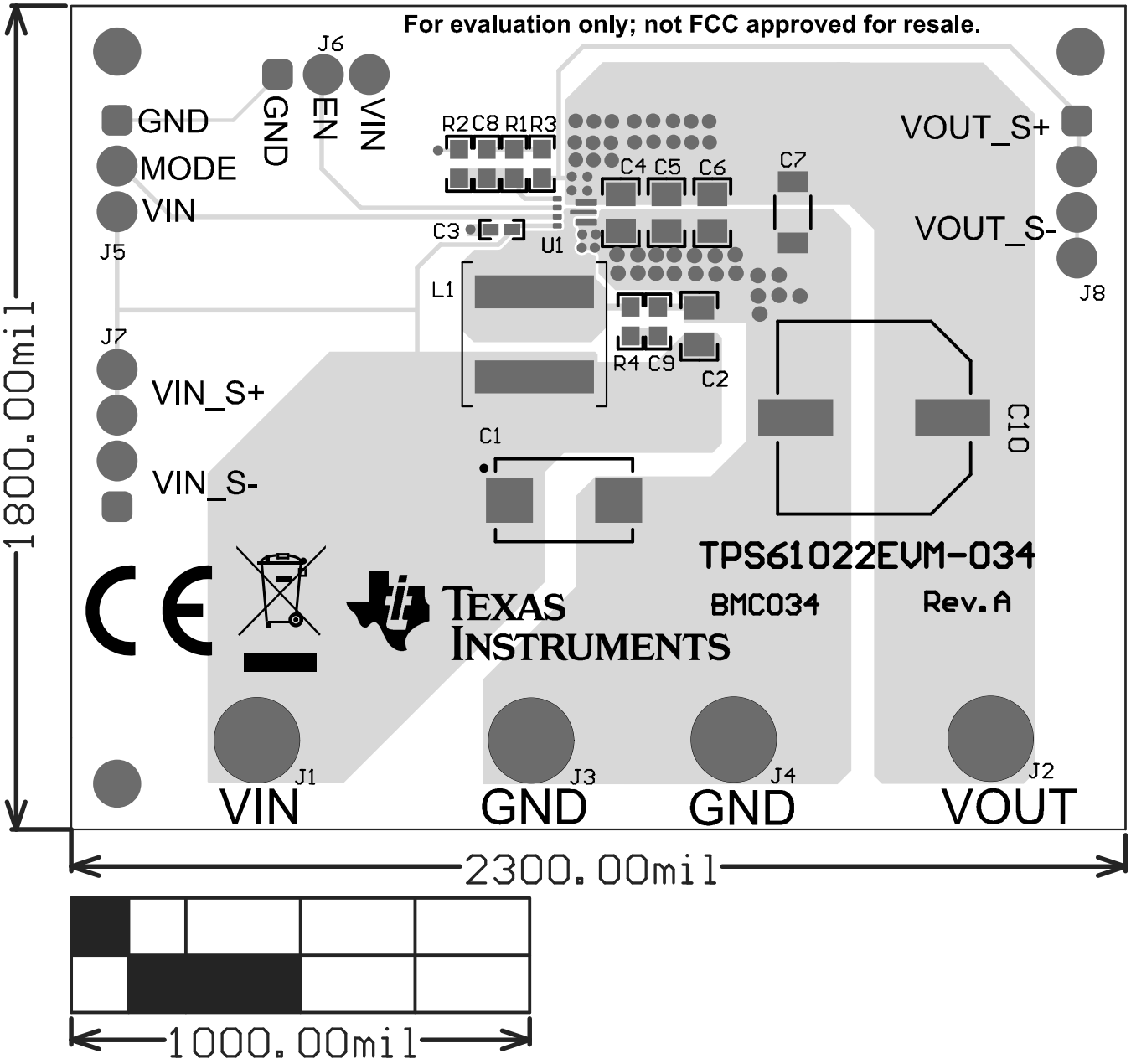

Figure 3. TPS61022EVM-034 Top-Side Layout

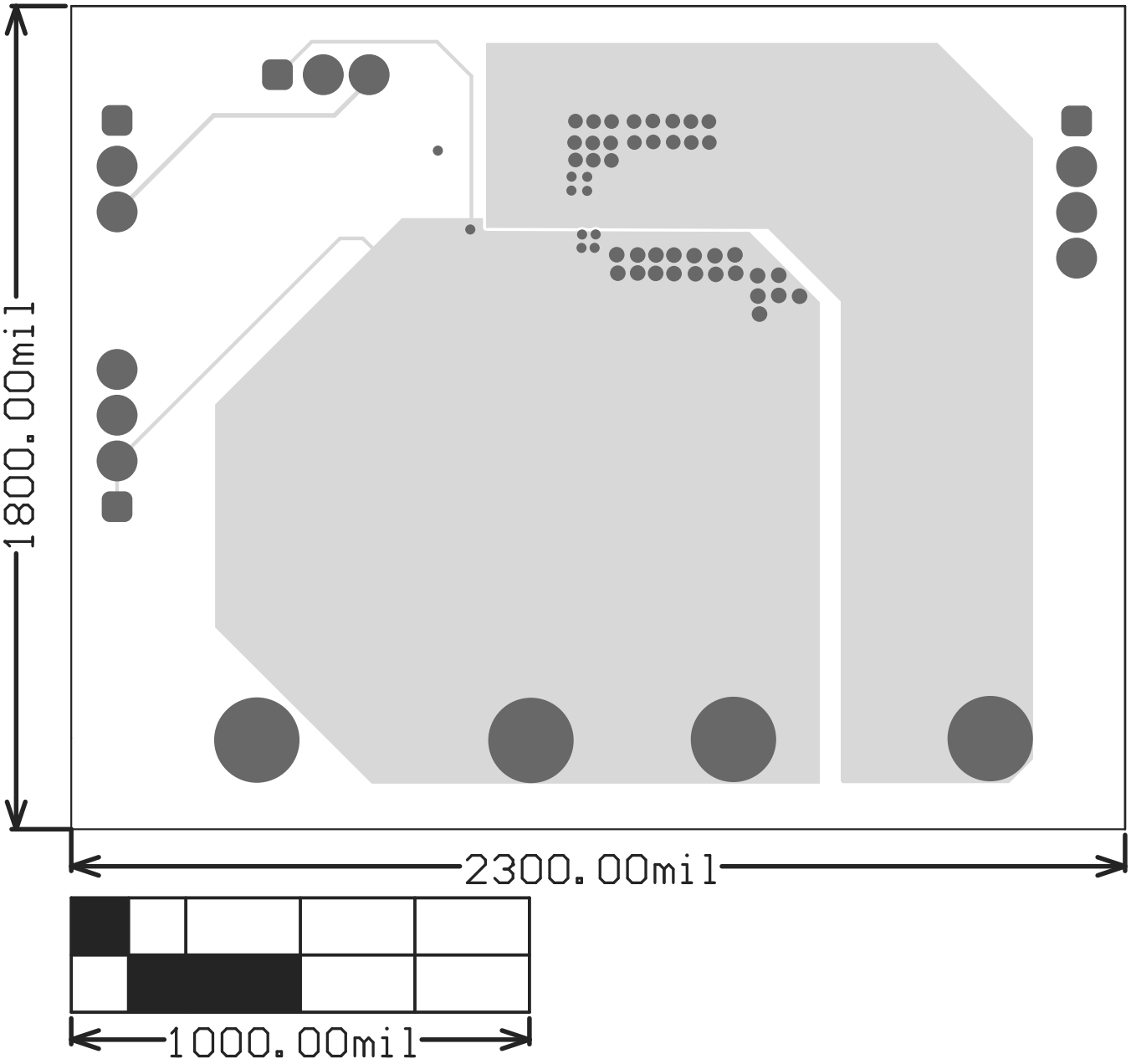

Figure 4. TPS61022EVM-034 Bottom-Side Layout

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