

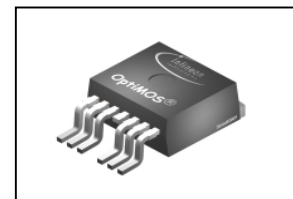
OptiMOS™ -T2 Power-Transistor

Features

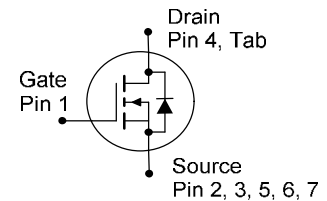
- N-channel - Enhancement mode
- AEC qualified
- MSL1 up to 260°C peak reflow
- 175°C operating temperature
- Green product (RoHS compliant)
- Ultra low Rds(on)
- 100% Avalanche tested

Product Summary

| | | |
|--------------|-----|----|
| V_{DS} | 40 | V |
| $R_{DS(on)}$ | 1.0 | mΩ |
| I_D | 240 | A |

PG-TO263-7-3


| Type | Package | Marking |
|-----------------|--------------|---------|
| IPB240N04S4-1R0 | PG-TO263-7-3 | 4N041R0 |


Maximum ratings, at $T_j=25\text{ °C}$, unless otherwise specified

| Parameter | Symbol | Conditions | Value | Unit |
|--|----------------|--|--------------|------|
| Continuous drain current | I_D | $T_C=25\text{ °C}$, $V_{GS}=10\text{ V}^{1)}$ | 240 | A |
| | | $T_C=100\text{ °C}$, $V_{GS}=10\text{ V}^{2)}$ | 240 | |
| Pulsed drain current ²⁾ | $I_{D,pulse}$ | $T_C=25\text{ °C}$ | 960 | |
| Avalanche energy, single pulse ²⁾ | E_{AS} | $I_D=120\text{ A}$ | 750 | mJ |
| Avalanche current, single pulse | I_{AS} | - | 190 | A |
| Gate source voltage | V_{GS} | - | ±20 | V |
| Power dissipation | P_{tot} | $T_C=25\text{ °C}$ | 231 | W |
| Operating and storage temperature | T_j, T_{stg} | - | -55 ... +175 | °C |
| IEC climatic category; DIN IEC 68-1 | - | - | 55/175/56 | |

| Parameter | Symbol | Conditions | Values | | | Unit |
|---|------------|--|--------|------|------|------|
| | | | min. | typ. | max. | |
| Thermal characteristics²⁾ | | | | | | |
| Thermal resistance, junction - case | R_{thJC} | - | - | - | 0.65 | K/W |
| SMD version, device on PCB | R_{thJA} | minimal footprint | - | - | 62 | |
| | | 6 cm ² cooling area ³⁾ | - | - | 40 | |

Electrical characteristics, at $T_j=25\text{ °C}$, unless otherwise specified

Static characteristics

| | | | | | | |
|----------------------------------|---------------|---|-----|------|------|---------------|
| Drain-source breakdown voltage | $V_{(BR)DSS}$ | $V_{GS}=0\text{ V}$, $I_D=1\text{ mA}$ | 40 | - | - | V |
| Gate threshold voltage | $V_{GS(th)}$ | $V_{DS}=V_{GS}$, $I_D=180\text{ }\mu\text{A}$ | 2.0 | 3.0 | 4.0 | |
| Zero gate voltage drain current | I_{DSS} | $V_{DS}=40\text{ V}$, $V_{GS}=0\text{ V}$, $T_j=25\text{ °C}$ | - | 0.1 | 1 | μA |
| | | $V_{DS}=18\text{ V}$, $V_{GS}=0\text{ V}$, $T_j=85\text{ °C}^{2)}$ | - | 1 | 20 | |
| Gate-source leakage current | I_{GSS} | $V_{GS}=20\text{ V}$, $V_{DS}=0\text{ V}$ | - | - | 100 | nA |
| Drain-source on-state resistance | $R_{DS(on)}$ | $V_{GS}=10\text{ V}$, $I_D=100\text{ A}$ | - | 0.85 | 1.00 | m Ω |

| Parameter | Symbol | Conditions | Values | | | Unit |
|-----------|--------|------------|--------|------|------|------|
| | | | min. | typ. | max. | |

Dynamic characteristics²⁾

| | | | | | | |
|------------------------------|--------------|--|---|-------|-------|----|
| Input capacitance | C_{iss} | $V_{GS}=0\text{ V}, V_{DS}=25\text{ V},$ $f=1\text{ MHz}$ | - | 13601 | 17682 | pF |
| Output capacitance | C_{oss} | | - | 2969 | 3860 | |
| Reverse transfer capacitance | C_{rss} | | - | 104 | 238 | |
| Turn-on delay time | $t_{d(on)}$ | $V_{DD}=20\text{ V}, V_{GS}=10\text{ V},$ $I_D=240\text{ A}, R_G=3.5\ \Omega$ | - | 42 | - | ns |
| Rise time | t_r | | - | 28 | - | |
| Turn-off delay time | $t_{d(off)}$ | | - | 44 | - | |
| Fall time | t_f | | - | 47 | - | |

Gate Charge Characteristics²⁾

| | | | | | | |
|-----------------------|---------------|---|---|-----|-----|----|
| Gate to source charge | Q_{gs} | $V_{DD}=32\text{ V}, I_D=240\text{ A},$ $V_{GS}=0\text{ to }10\text{ V}$ | - | 77 | 100 | nC |
| Gate to drain charge | Q_{gd} | | - | 24 | 54 | |
| Gate charge total | Q_g | | - | 170 | 221 | |
| Gate plateau voltage | $V_{plateau}$ | | - | 5.5 | - | V |

Reverse Diode

| | | | | | | |
|--|---------------|---|---|-----|-----|----|
| Diode continuous forward current ²⁾ | I_S | $T_C=25\text{ }^\circ\text{C}$ | - | - | 240 | A |
| Diode pulse current ²⁾ | $I_{S,pulse}$ | | - | - | 960 | |
| Diode forward voltage | V_{SD} | $V_{GS}=0\text{ V}, I_F=100\text{ A},$ $T_j=25\text{ }^\circ\text{C}$ | - | 0.9 | 1.3 | V |
| Reverse recovery time ²⁾ | t_{rr} | $V_R=20\text{ V}, I_F=50\text{ A},$ $di_F/dt=100\text{ A}/\mu\text{s}$ | - | 80 | - | ns |
| Reverse recovery charge ²⁾ | Q_{rr} | | - | 130 | - | nC |

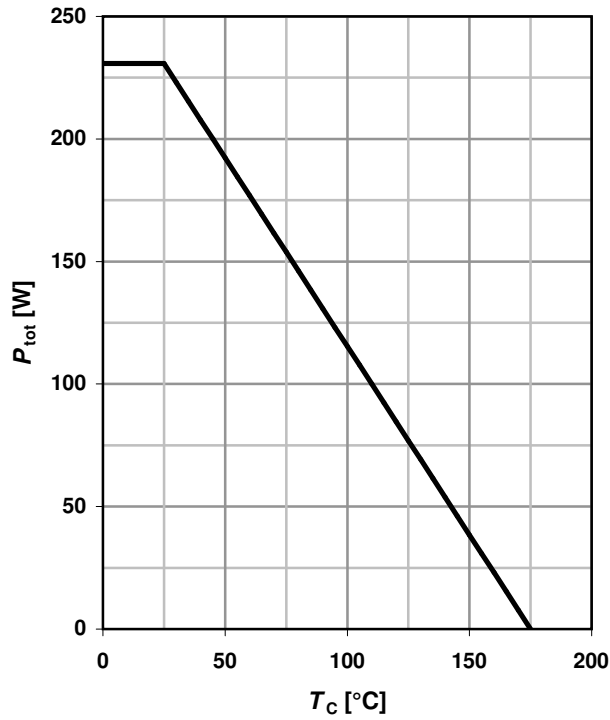
¹⁾ Current is limited by bondwire; with an $R_{thJC} = 0.65\text{ K/W}$ the chip is able to carry 367A at 25°C.

²⁾ Defined by design. Not subject to production test.

³⁾ Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm² (one layer, 70 μm thick) copper area for drain connection. PCB is vertical in still air.

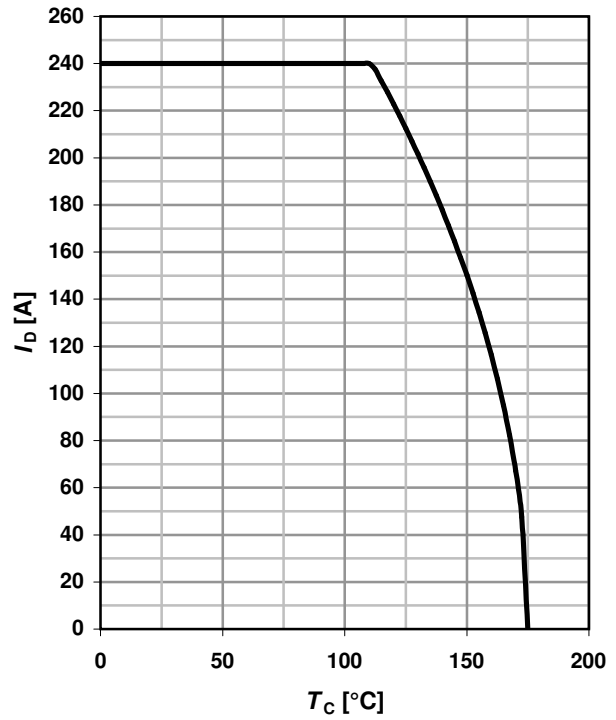
1 Power dissipation

$P_{tot} = f(T_C); V_{GS} \geq 6 V$



2 Drain current

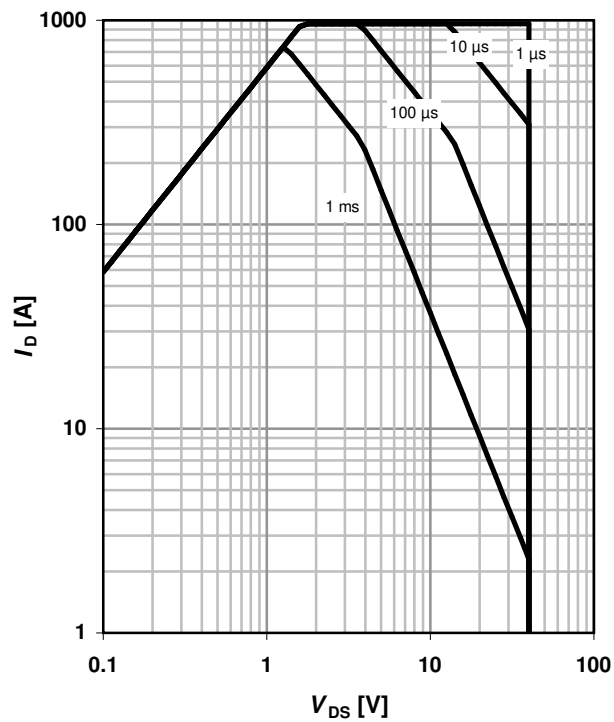
$I_D = f(T_C); V_{GS} \geq 6 V$



3 Safe operating area

$I_D = f(V_{DS}); T_C = 25\text{ °C}; D = 0$

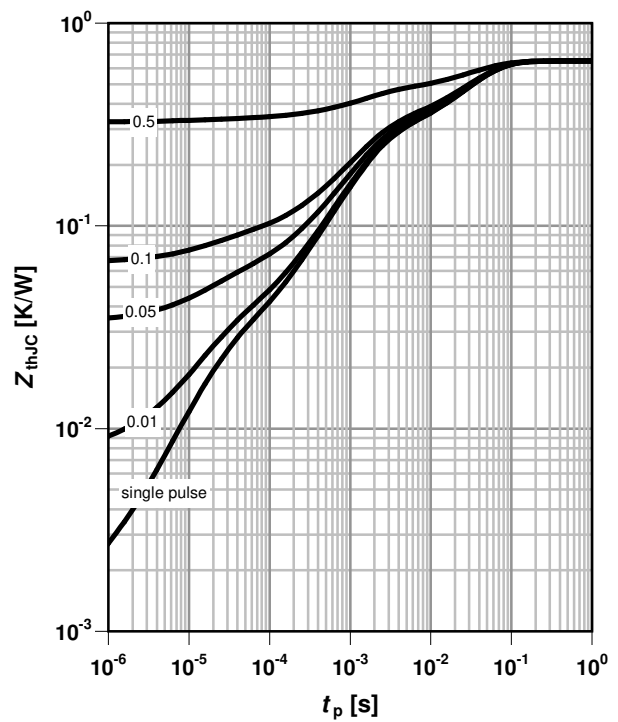
parameter: t_p



4 Max. transient thermal impedance

$Z_{thJC} = f(t_p)$

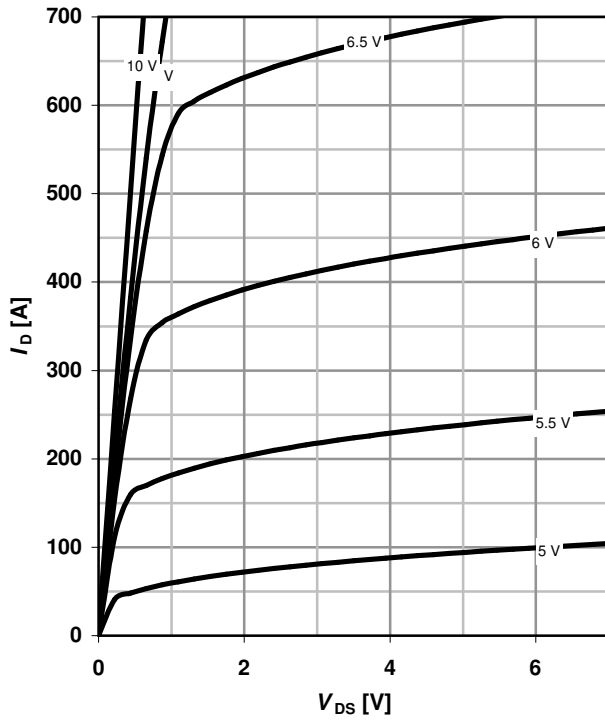
parameter: $D = t_p/T$



5 Typ. output characteristics

$I_D = f(V_{DS}); T_j = 25\text{ }^\circ\text{C}$

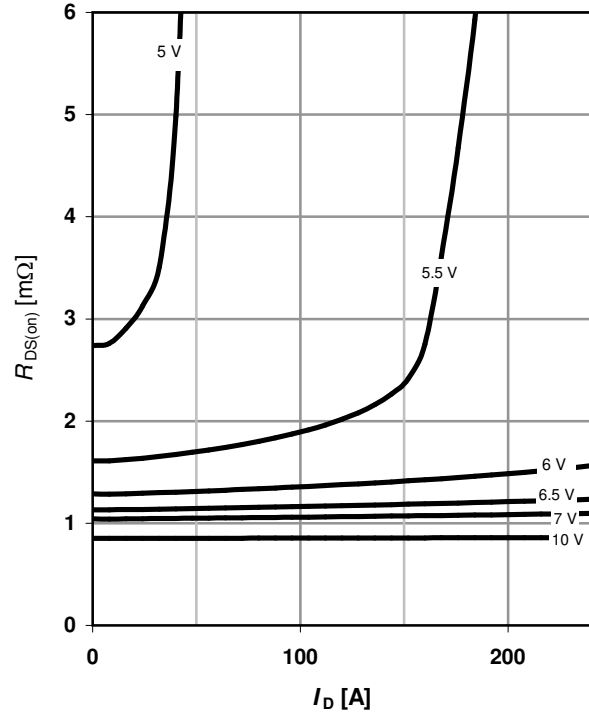
parameter: V_{GS}



6 Typ. drain-source on-state resistance

$R_{DS(on)} = f(I_D); T_j = 25\text{ }^\circ\text{C}$

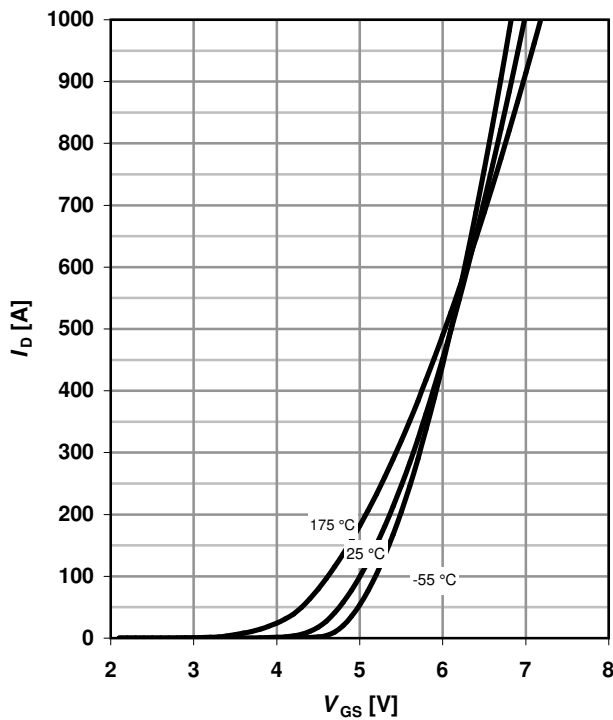
parameter: V_{GS}



7 Typ. transfer characteristics

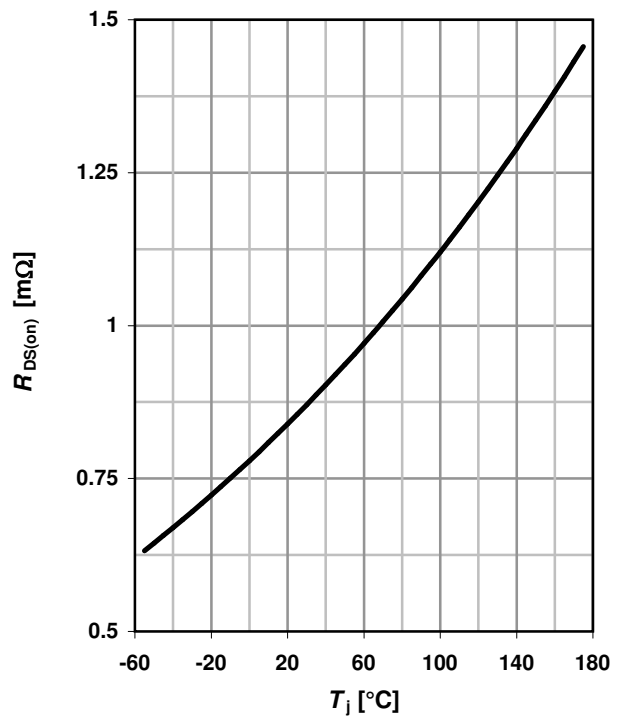
$I_D = f(V_{GS}); V_{DS} = 6\text{ V}$

parameter: T_j



8 Typ. drain-source on-state resistance

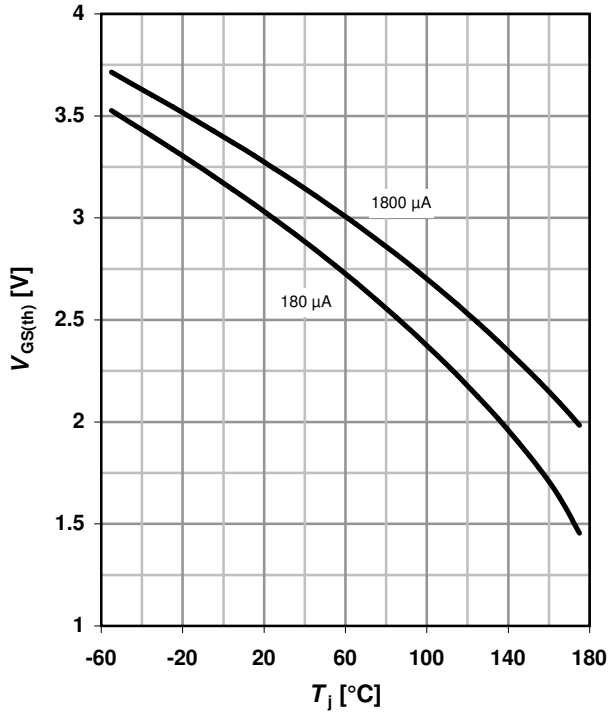
$R_{DS(on)} = f(T_j); I_D = 100\text{ A}; V_{GS} = 10\text{ V}$



9 Typ. gate threshold voltage

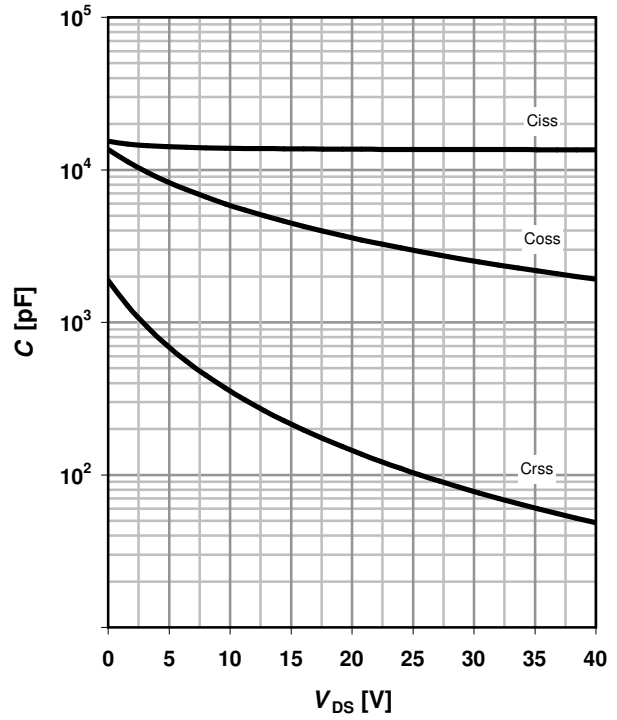
$V_{GS(th)} = f(T_j); V_{GS} = V_{DS}$

parameter: I_D



10 Typ. capacitances

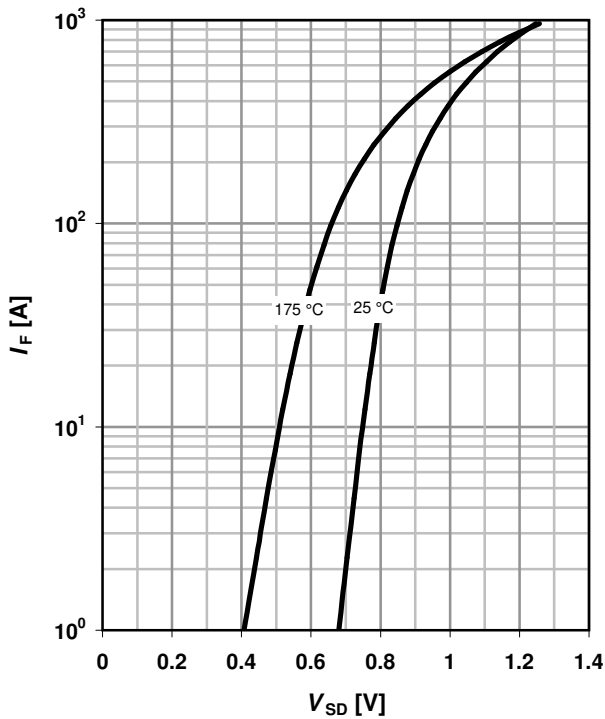
$C = f(V_{DS}); V_{GS} = 0 V; f = 1 MHz$



11 Typical forward diode characteristics

$I_F = f(V_{SD})$

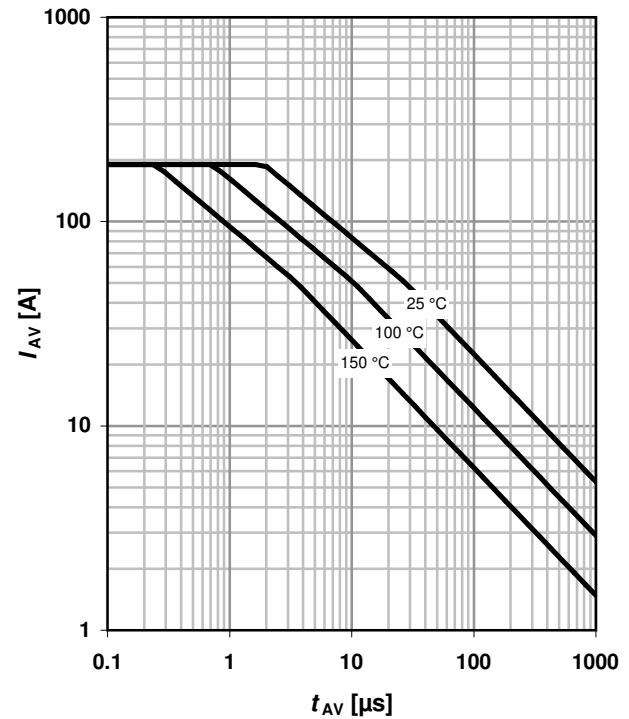
parameter: T_j



12 Typ. avalanche characteristics

$I_{AS} = f(t_{AV})$

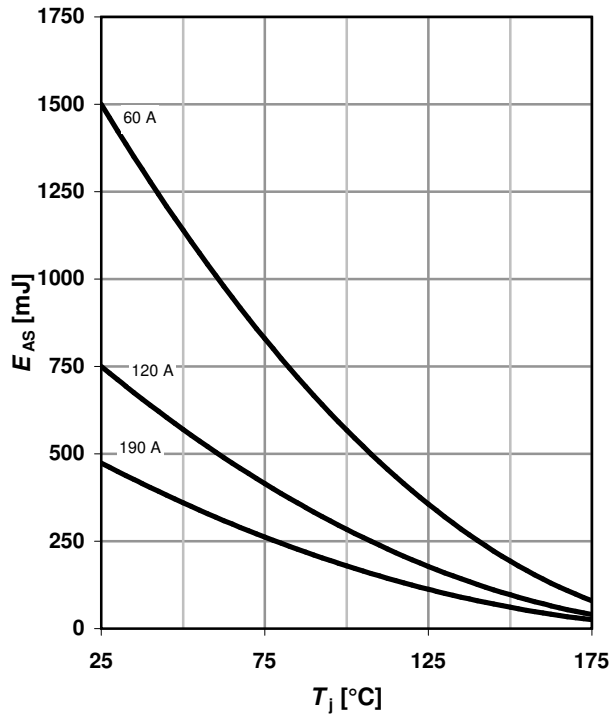
parameter: $T_{j(start)}$



13 Typical avalanche energy

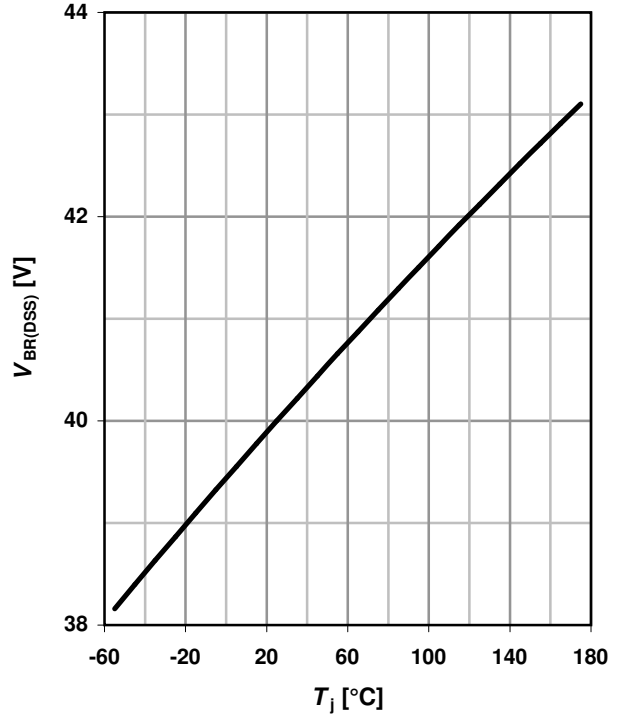
$$E_{AS} = f(T_j)$$

parameter: I_D



14 Drain-source breakdown voltage

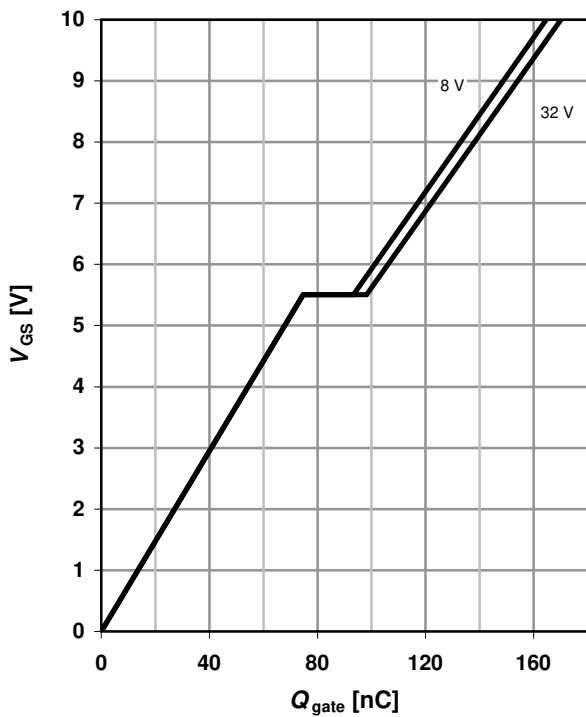
$$V_{BR(DSS)} = f(T_j); I_D = 1 \text{ mA}$$



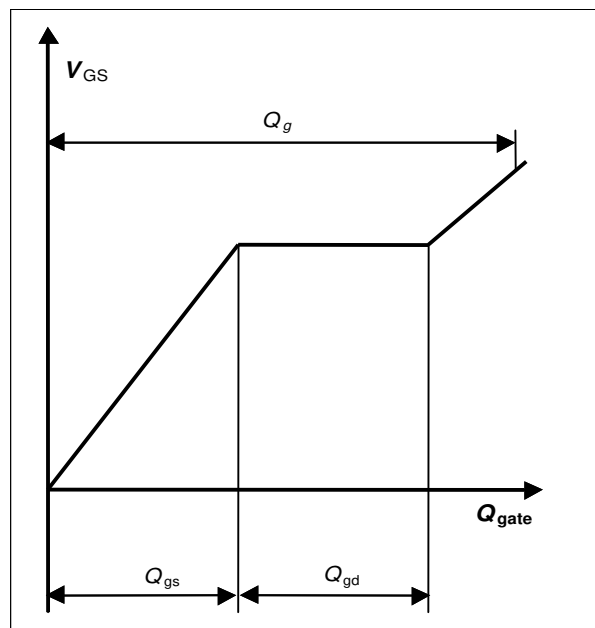
15 Typ. gate charge

$$V_{GS} = f(Q_{gate}); I_D = 180 \text{ A pulsed}$$

parameter: V_{DD}



16 Gate charge waveforms



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Revision History

| Version | Date | Changes |
|---------|------------|------------------|
| 1.0 | 22.08.2013 | Final Data Sheet |