

N-channel 1700 V, 7 Ω typ., 2.6 A PowerMESH™ Power MOSFETs in TO-247 and TO-247 long leads packages

Datasheet - production data

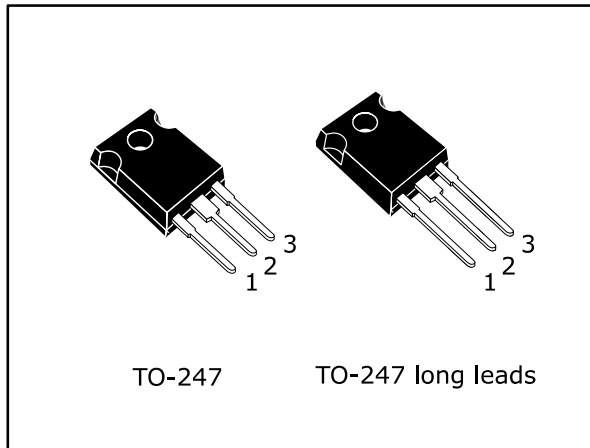


Figure 1: Internal schematic diagram

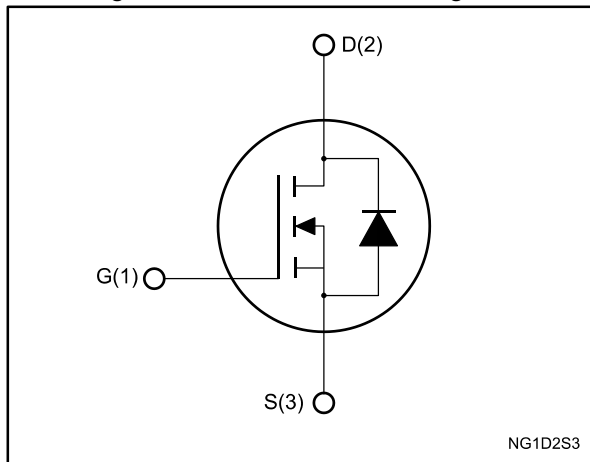


Table 1: Device summary

Order code	Marking	Package	Packing
STW3N170	3N170	TO-247	Tube
STWA3N170		TO-247 long leads	

Features

Order code	V _{DS}	R _{DS(on)} max.	I _D	P _{TOT}
STW3N170	1700 V	13 Ω	2.6 A	160 W
STWA3N170				

- Intrinsic capacitances and Q_g minimized
- High speed switching
- 100% avalanche tested

Applications

- Switching applications

Description

This Power MOSFET is designed using the STMicroelectronics consolidated strip-layout-based MESH OVERLAY™ process. The result is a product that matches or improves on the performance of comparable standard parts from other manufacturers.

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1 Electrical ratings

Table 2: Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	1700	V
V_{GS}	Gate-source voltage	± 30	V
I_D	Drain current (continuous) at $T_{case} = 25\text{ }^\circ\text{C}$	2.6	A
	Drain current (continuous) at $T_{case} = 100\text{ }^\circ\text{C}$	1.6	
$I_{DM}^{(1)}$	Drain current (pulsed)	10.4	A
P_{TOT}	Total dissipation at $T_{case} = 25\text{ }^\circ\text{C}$	160	W
I_{AR}	Avalanche current, repetitive or not repetitive	0.8	A
$E_{AS}^{(2)}$	Single pulse avalanche energy	2	mJ
T_{stg}	Storage temperature	-55 to 150	$^\circ\text{C}$
T_j	Operating junction temperature		

Notes:

⁽¹⁾ Pulse width limited by T_{jmax} .

⁽²⁾ starting $T_j = 25\text{ }^\circ\text{C}$, $I_D = I_{AR}$, $V_{DD} = 50\text{ V}$.

Table 3: Thermal data

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case	0.78	$^\circ\text{C/W}$
$R_{thj-amb}$	Thermal resistance junction-ambient	50	

2 Electrical characteristics

($T_{\text{case}} = 25\text{ °C}$ unless otherwise specified)

Table 4: Static

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(\text{BR})\text{DSS}}$	Drain-source breakdown voltage	$V_{\text{GS}} = 0\text{ V}$, $I_{\text{D}} = 1\text{ mA}$	1700			V
I_{DSS}	Zero gate voltage drain current	$V_{\text{GS}} = 0\text{ V}$, $V_{\text{DS}} = 1700\text{ V}$			10	μA
		$V_{\text{GS}} = 0\text{ V}$, $V_{\text{DS}} = 1700\text{ V}$, $T_{\text{case}} = 125\text{ °C}$			500	
I_{GSS}	Gate-body leakage current	$V_{\text{DS}} = 0\text{ V}$, $V_{\text{GS}} = \pm 30\text{ V}$			± 100	nA
$V_{\text{GS}(\text{th})}$	Gate threshold voltage	$V_{\text{DS}} = V_{\text{GS}}$, $I_{\text{D}} = 250\text{ }\mu\text{A}$	3	4	5	V
$R_{\text{DS}(\text{on})}$	Static drain-source on-resistance	$V_{\text{GS}} = 10\text{ V}$, $I_{\text{D}} = 1.3\text{ A}$		7	13	Ω

Table 5: Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{\text{DS}} = 100\text{ V}$, $f = 1\text{ MHz}$, $V_{\text{GS}} = 0\text{ V}$	-	1100	-	pF
C_{oss}	Output capacitance		-	50	-	
C_{riss}	Reverse transfer capacitance		-	7	-	
R_{G}	Intrinsic gate resistance	$f = 1\text{ MHz}$, $I_{\text{D}} = 0\text{ A}$	-	3.6	-	Ω
Q_{g}	Total gate charge	$V_{\text{DD}} = 1360\text{ V}$, $I_{\text{D}} = 2.6\text{ A}$, $V_{\text{GS}} = 10\text{ V}$ (see Figure 15: "Test circuit for gate charge behavior")	-	44	-	nC
Q_{gs}	Gate-source charge		-	7	-	
Q_{gd}	Gate-drain charge		-	25	-	

Table 6: Switching times

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{\text{d}(\text{on})}$	Turn-on delay time	$V_{\text{DD}} = 850\text{ V}$, $I_{\text{D}} = 1.3\text{ A}$ $R_{\text{G}} = 4.7\text{ }\Omega$, $V_{\text{GS}} = 10\text{ V}$ (see Figure 14: "Test circuit for resistive load switching times" and Figure 19: "Switching time waveform")	-	25	-	ns
t_{r}	Rise time		-	9	-	
$t_{\text{d}(\text{off})}$	Turn-off delay time		-	51	-	
t_{f}	Fall time		-	53	-	

Table 7: Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current	$T_j = 25\text{ °C}$	-		2.6	A
I_{SDM}	Source-drain current (pulsed)	$T_j = 25\text{ °C}$	-		10.4	A
$V_{SD}^{(1)}$	Forward on voltage	$V_{GS} = 0\text{ V}$, $I_{SD} = 2.6\text{ A}$	-		1.5	V
t_{rr}	Reverse recovery time	$I_{SD} = 2.6\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $V_{DD} = 60\text{ V}$ (see <i>Figure 16: "Test circuit for inductive load switching and diode recovery times")</i>)	-	1.58		μs
Q_{rr}	Reverse recovery charge		-	6		μC
I_{RRM}	Reverse recovery current		-	7.9		A
t_{rr}	Reverse recovery time	$I_{SD} = 2.6\text{ A}$, $di/dt = 100\text{ A}/\mu\text{s}$, $V_{DD} = 60\text{ V}$, $T_j = 150\text{ °C}$ (see <i>Figure 16: "Test circuit for inductive load switching and diode recovery times")</i>)	-	2.12		μs
Q_{rr}	Reverse recovery charge		-	8.8		μC
I_{RRM}	Reverse recovery current		-	8.3		A

Notes:

⁽¹⁾ Pulse test: pulse duration = 300 μs , duty cycle 1.5%.

2.1 Electrical characteristics (curves)

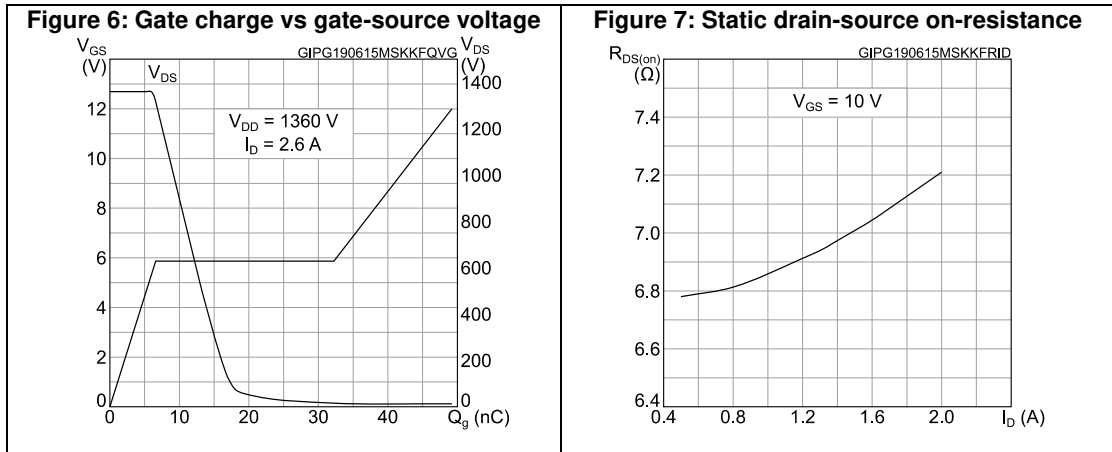
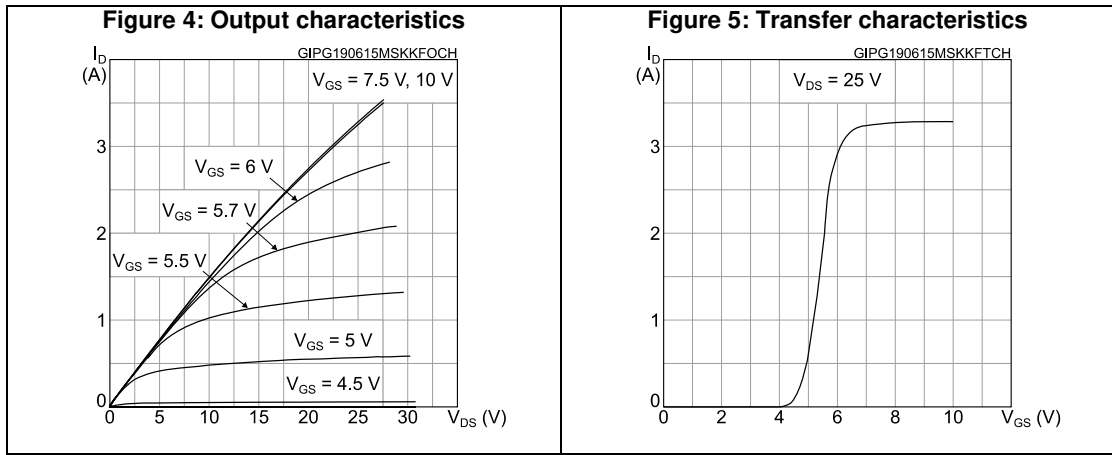
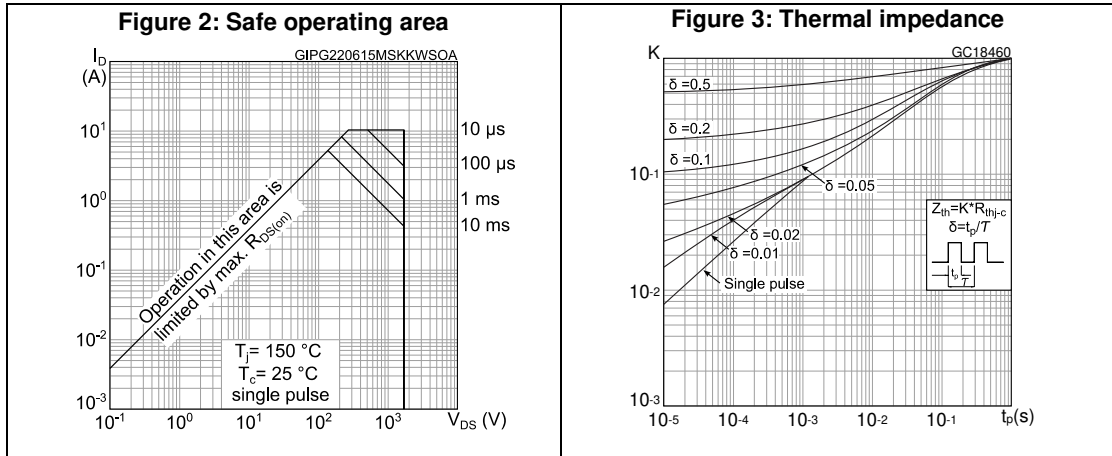


Figure 8: Capacitance variations

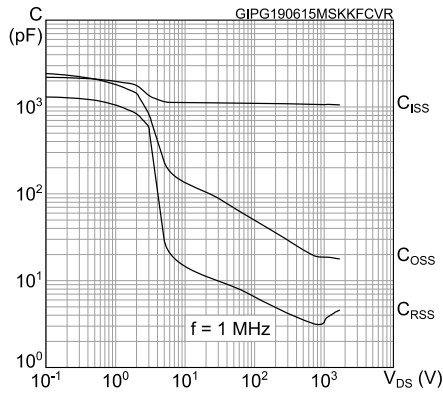


Figure 9: Normalized gate threshold voltage vs temperature

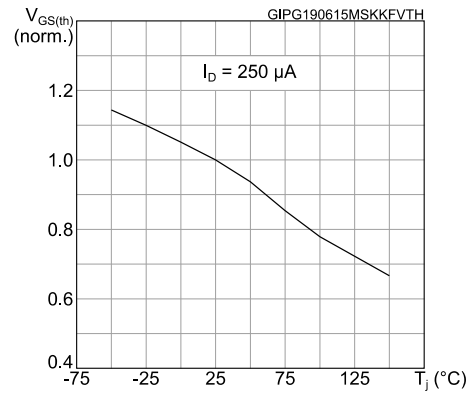


Figure 10: Normalized on-resistance vs temperature

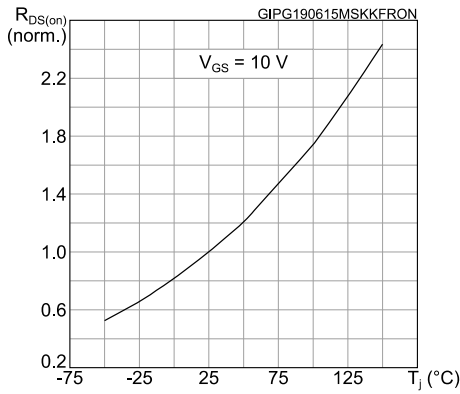


Figure 11: Normalized V(BR)DSS vs temperature

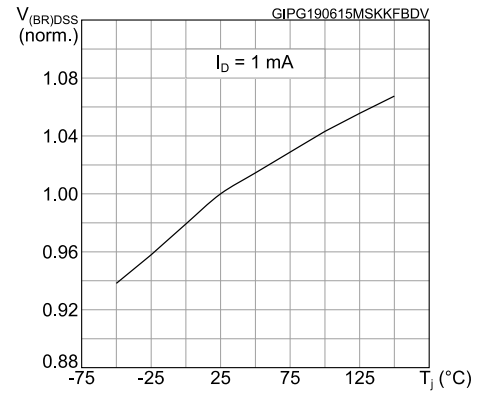


Figure 12: Output capacitance stored energy

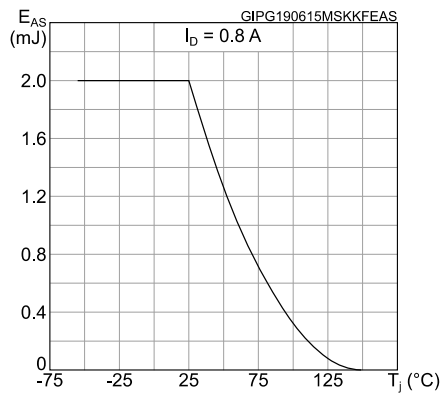
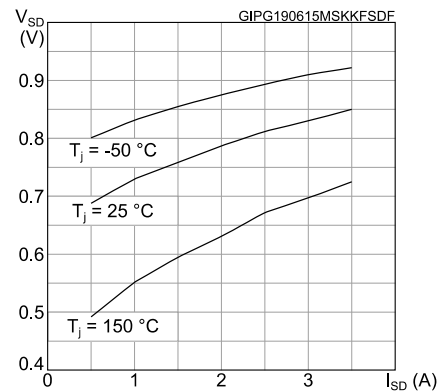
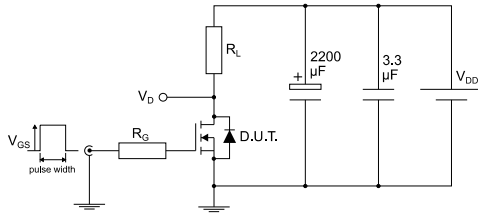


Figure 13: Source-drain diode forward characteristics



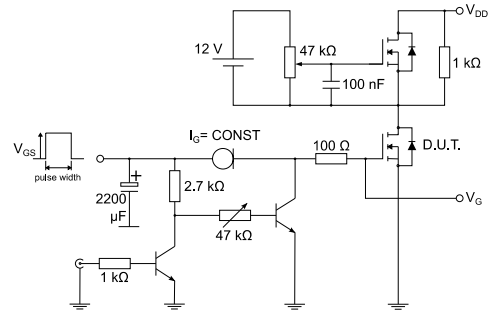
3 Test circuits

Figure 14: Test circuit for resistive load switching times



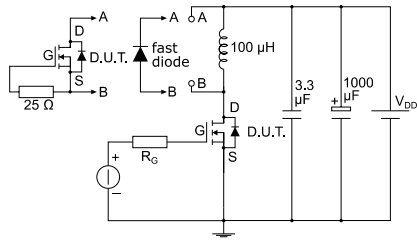
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Figure 15: Test circuit for gate charge behavior



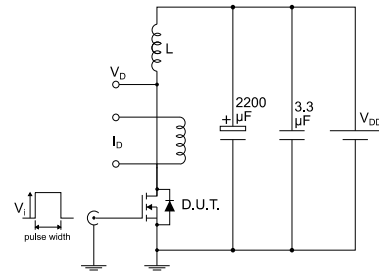
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Figure 16: Test circuit for inductive load switching and diode recovery times



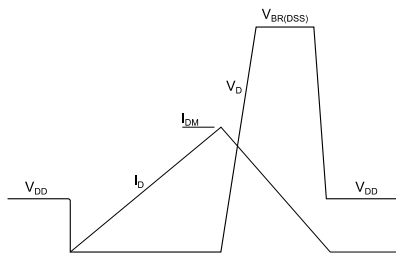
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Figure 17: Unclamped inductive load test circuit



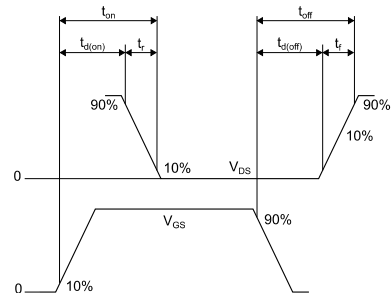
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Figure 18: Unclamped inductive waveform



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Figure 19: Switching time waveform



AM01473v1

4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

4.1 TO-247 package information

Figure 20: TO-247 package outline

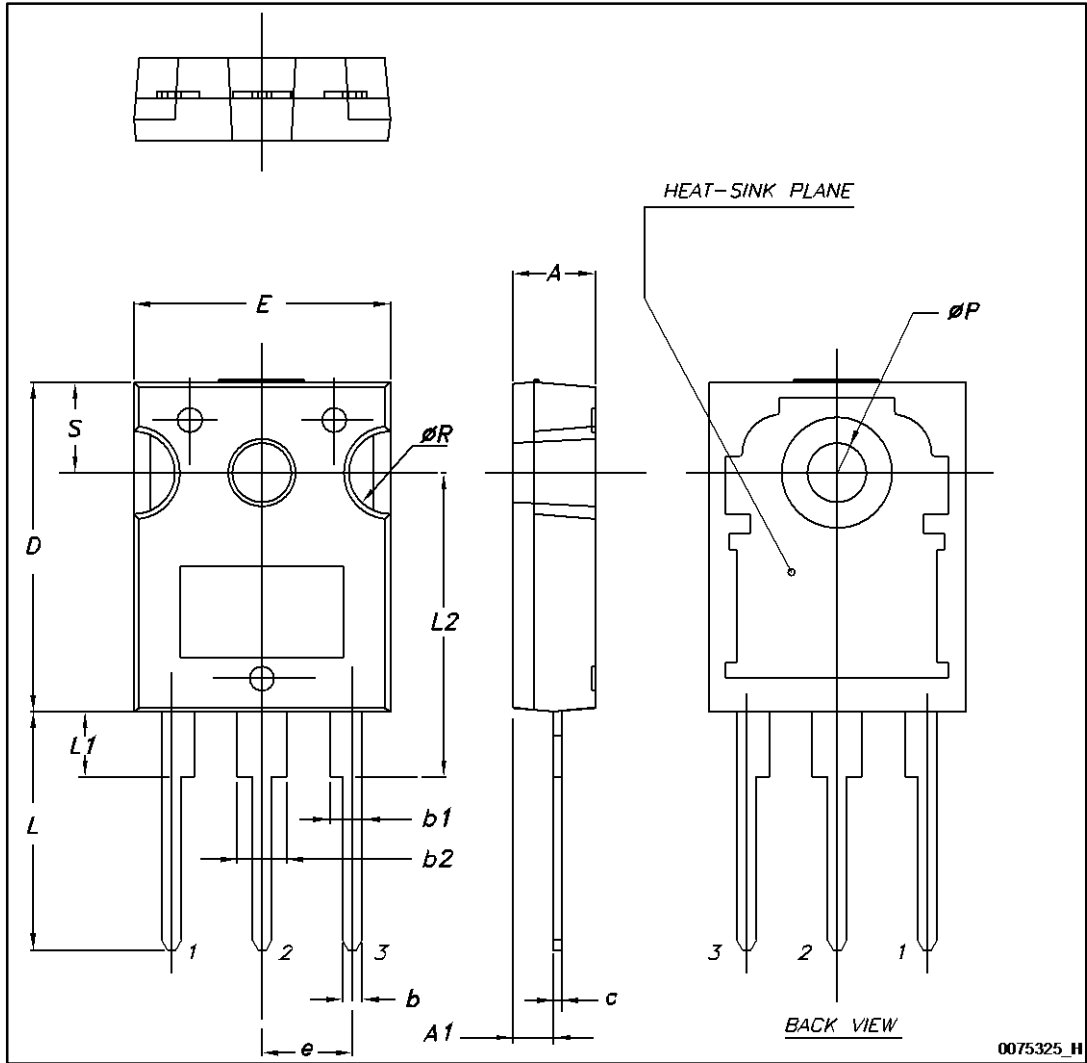
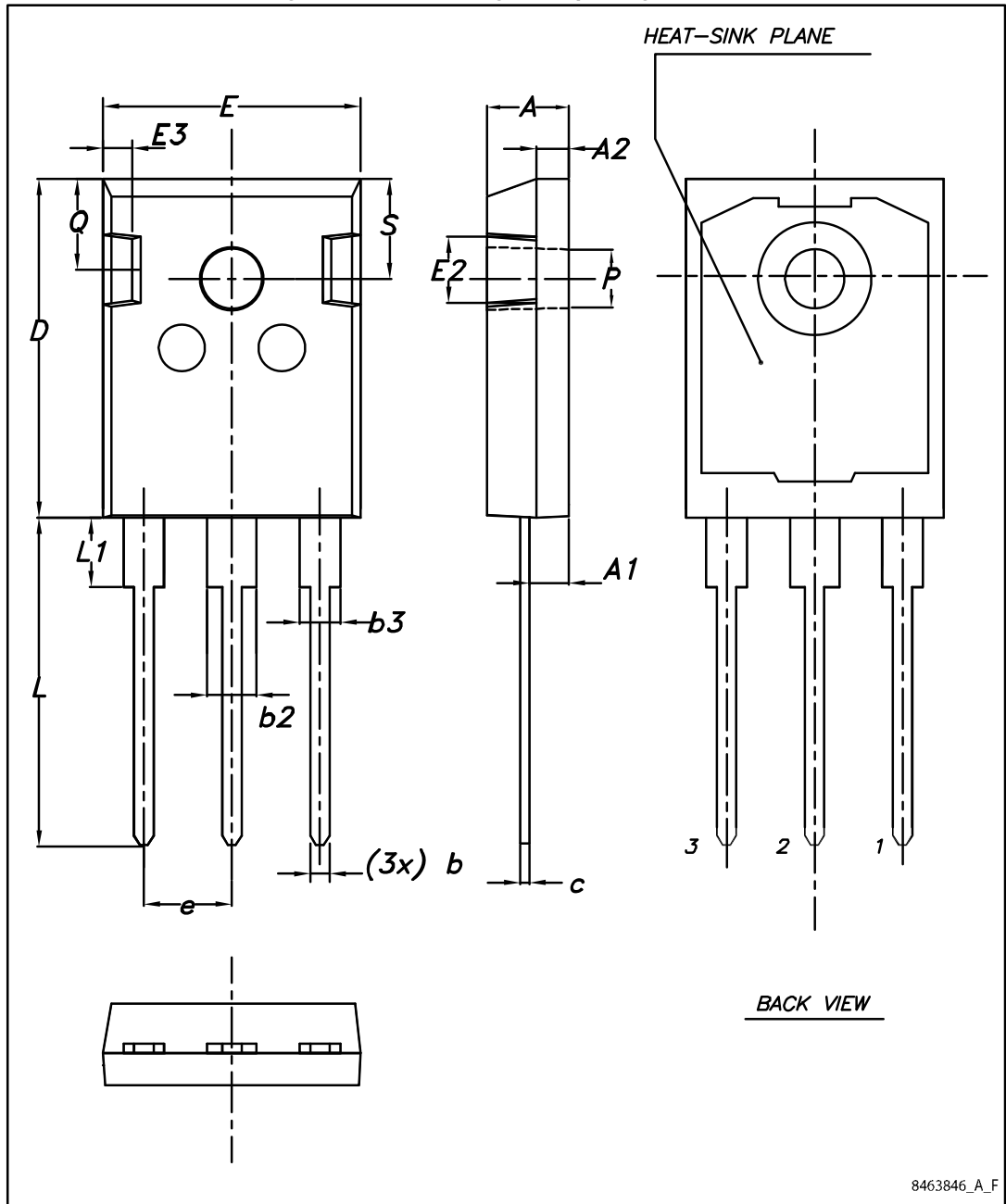


Table 8: TO-247 package mechanical data

Dim.	mm.		
	Min.	Typ.	Max.
A	4.85		5.15
A1	2.20		2.60
b	1.0		1.40
b1	2.0		2.40
b2	3.0		3.40
c	0.40		0.80
D	19.85		20.15
E	15.45		15.75
e	5.30	5.45	5.60
L	14.20		14.80
L1	3.70		4.30
L2		18.50	
ØP	3.55		3.65
ØR	4.50		5.50
S	5.30	5.50	5.70

4.2 TO-247 long leads package information

Figure 21: TO-247 long leads package outline



8463846_A_F

Table 9: TO-247 long leads package mechanical data

Dim.	mm.		
	Min.	Typ.	Max.
A	4.90	5.00	5.10
A1	2.31	2.41	2.51
A2	1.90	2.00	2.10
b	1.16		1.26
b2			3.25
b3			2.25
c	0.59		0.66
D	20.90	21.00	21.10
E	15.70	15.80	15.90
E2	4.90	5.00	5.10
E3	2.40	2.50	2.60
e	5.34	5.44	5.54
L	19.80	19.92	20.10
L1			4.30
P	3.50	3.60	3.70
Q	5.60		6.00
S	6.05	6.15	6.25

5 Revision history

Table 10: Document revision history

Date	Revision	Changes
14-Sep-2015	1	First release.

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