



# PESD18VF1BL-Q

Ultra low capacitance bidirectional ESD protection diode

18 January 2022

Product data sheet

## 1. General description

Ultra low capacitance bidirectional ElectroStatic Discharge (ESD) protection diode in a DFN1006-2 (SOD882) leadless ultra small Surface-Mounted Device (SMD) plastic package designed to protect one signal line from the damage caused by ESD and other transients.

## 2. Features and benefits

- Ultra low diode capacitance  $C_d = 0.35$  pF
- High reverse standoff voltage  $V_{RWM} = 18$  V
- Very small voltage dependency of the capacitance
- ESD protection up to  $\pm 10$  kV according to IEC 61000-4-2, level 4
- Qualified according to AEC-Q101 and recommended for use in automotive applications

## 3. Applications

- NFC antenna protection
- Protection of high-speed data lines

## 4. Quick reference data

Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$V_{RWM}$	reverse standoff voltage	$T_{amb} = 25$ °C	-	-	18	V
$C_d$	diode capacitance	$f = 1$ MHz; $V_R = 0$ V; $T_{amb} = 25$ °C	0.28	0.35	0.5	pF

## 5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	K1	cathode (diode 1)	<p>Transparent top view DFN1006-2 (SOD882)</p>	<p>sym045</p>
2	K2	cathode (diode 2)		

## 6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PESD18VF1BL-Q	DFN1006-2	plastic, leadless ultra small package; 2 terminals; 0.65 mm pitch; 1 mm x 0.6 mm x 0.48 mm body	SOD882

## 7. Marking

Table 4. Marking codes

Type number	Marking code
PESD18VF1BL-Q	WM

## 8. Limiting values

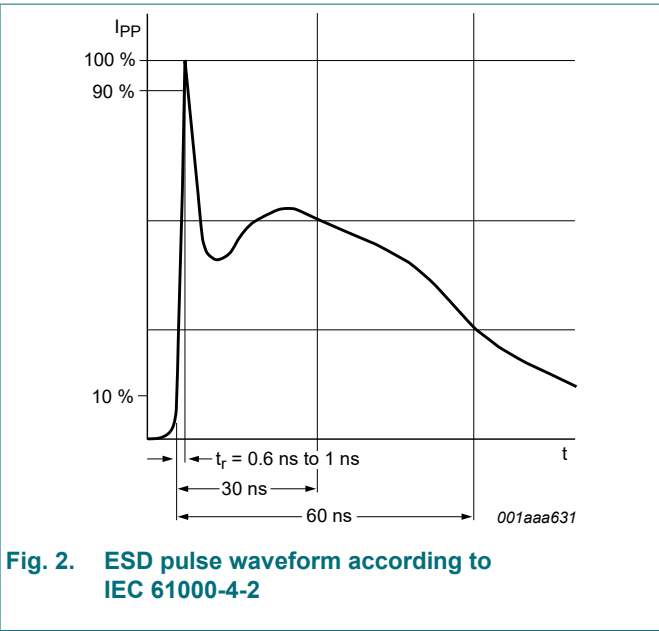
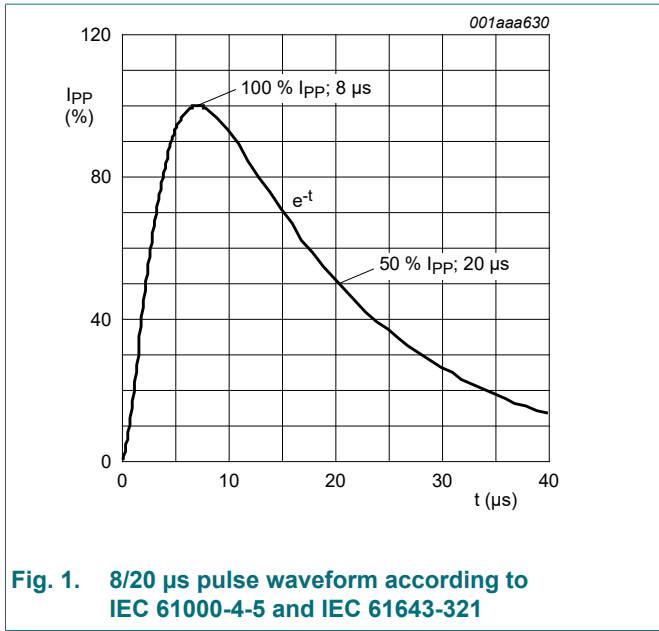
Table 5. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
$I_{PPM}$	rated peak pulse current	$t_p = 8/20 \mu s$ ; IEC 61000-4-5; IEC 61643-321	[1]	-	1	A
$T_j$	junction temperature			-	150	°C
$T_{amb}$	ambient temperature			-55	150	°C
$T_{stg}$	storage temperature			-65	150	°C
<b>ESD maximum ratings</b>						
$V_{ESD}$	electrostatic discharge voltage	IEC 61000-4-2; contact discharge	[1] [2]	-	10	kV
		IEC 61000-4-2; air discharge	[1] [2]	-	15	kV
		MIL-STD-883; human body model; HBM	[1]	-	10	kV
		machine model; MM	[1]	-	400	V

[1] Measured from pin 1 to pin 2.

[2] Device stressed with ten non-repetitive ESD pulses.



## 9. Characteristics

Table 6. Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
V <sub>RWM</sub>	reverse standoff voltage	T <sub>amb</sub> = 25 °C		-	-	18	V
V <sub>BR</sub>	breakdown voltage	I <sub>R</sub> = 10 mA; T <sub>amb</sub> = 25 °C		19	22	24	V
I <sub>RM</sub>	reverse leakage current	V <sub>R</sub> = 18 V; T <sub>amb</sub> = 25 °C		-	1	30	nA
C <sub>d</sub>	diode capacitance	f = 1 MHz; V <sub>R</sub> = 0 V; T <sub>amb</sub> = 25 °C		0.28	0.35	0.5	pF
V <sub>CL</sub>	clamping voltage	I <sub>PP</sub> = 1 A; t <sub>p</sub> = 8/20 μs; IEC 61000-4-5; IEC 61643-321; T <sub>amb</sub> = 25 °C	[1]	-	-	17	V
R <sub>dyn</sub>	dynamic resistance	I <sub>R</sub> = 10 A; T <sub>amb</sub> = 25 °C	[2]	-	0.8	-	Ω

[1] Measured from pin 1 to pin 2.

[2] Non-repetitive current pulse, Transmission Line Pulse (TLP) t<sub>p</sub> = 100 ns; square pulse; ANSI / ESD STM5.5.1-2008.

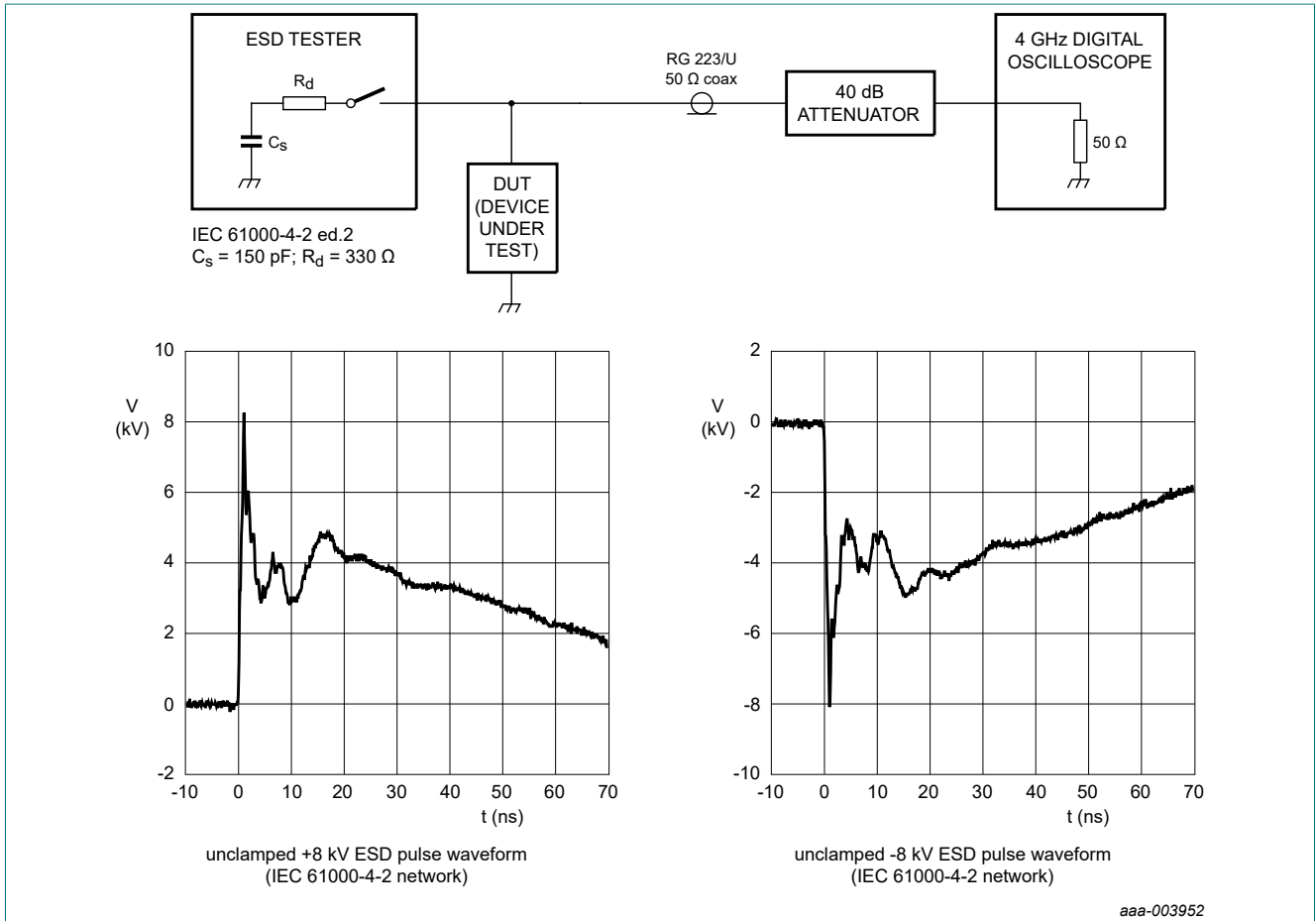


Fig. 3. ESD clamping test setup and waveforms

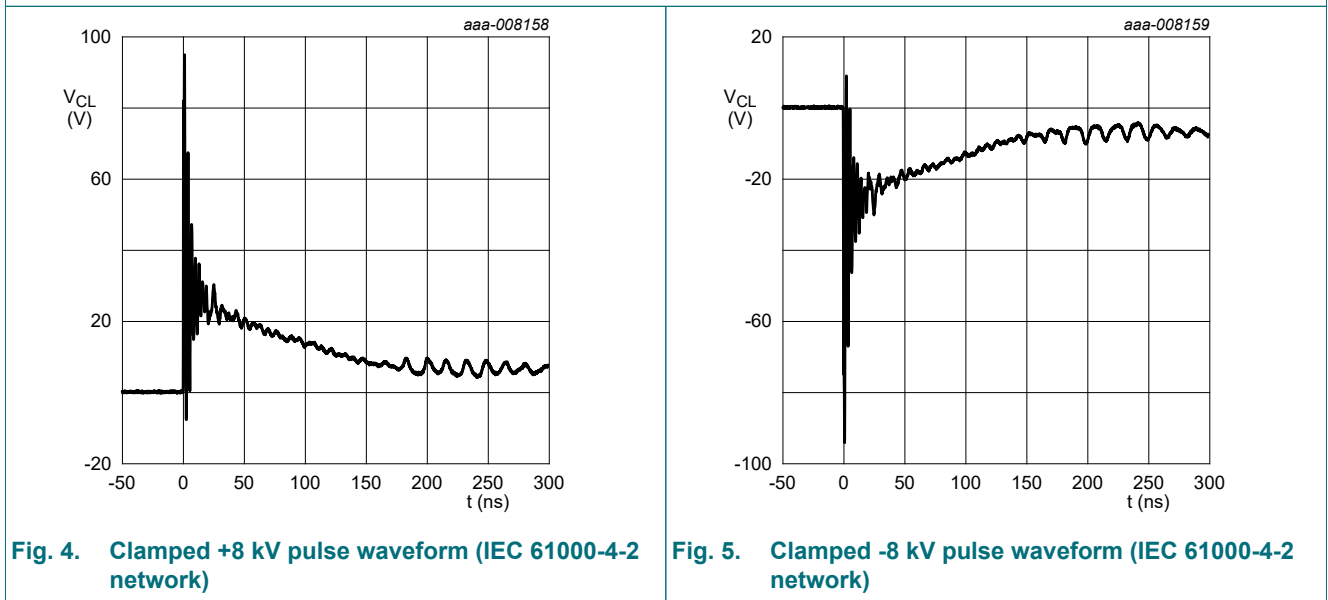
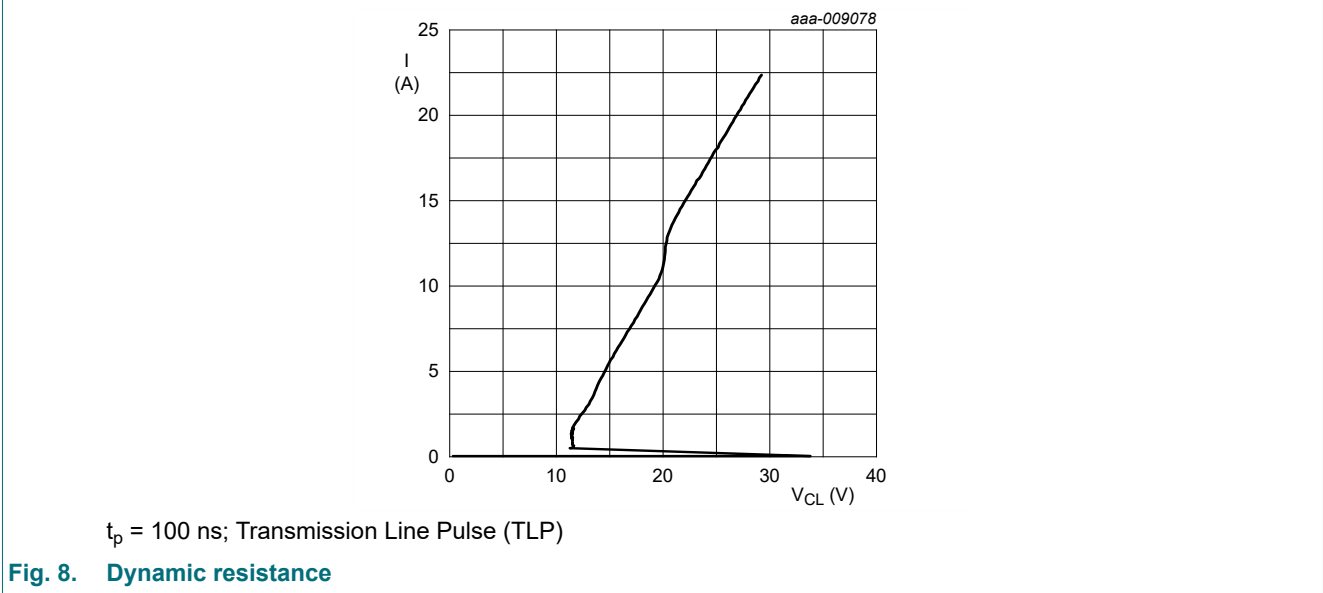
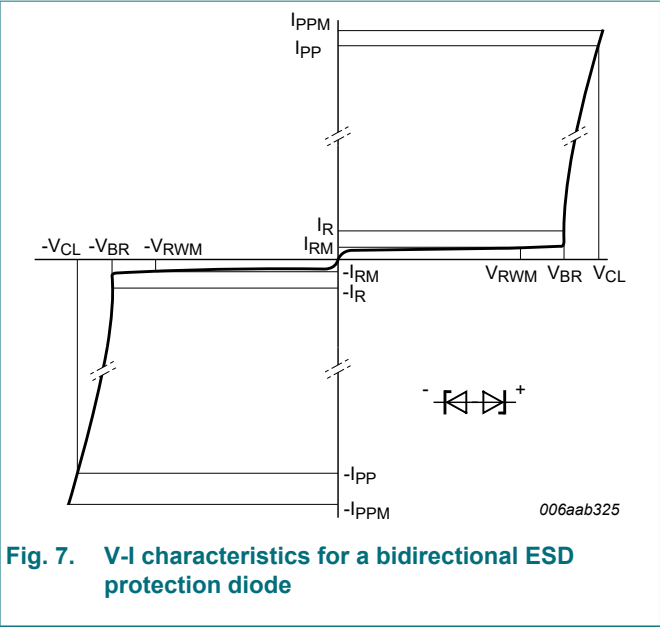
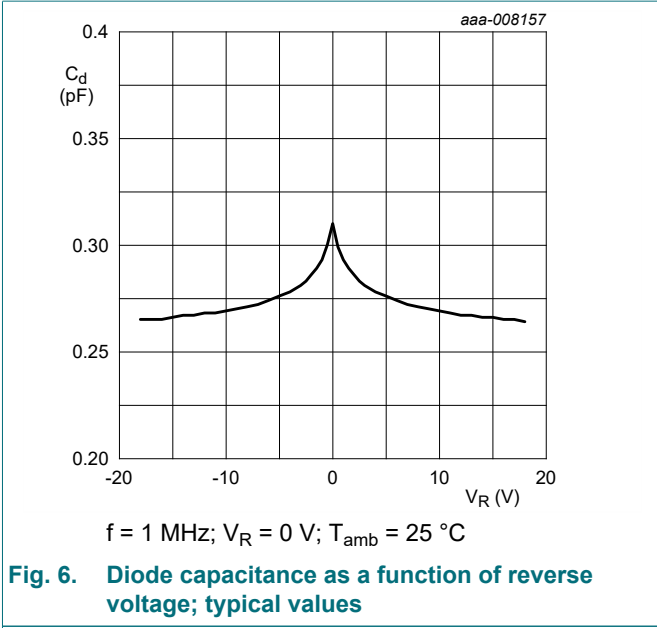


Fig. 4. Clamped +8 kV pulse waveform (IEC 61000-4-2 network)

Fig. 5. Clamped -8 kV pulse waveform (IEC 61000-4-2 network)



## 10. Application information

The device is designed for the protection of one bidirectional data line from surge pulses and ESD damage. The device is suitable on lines where the signal polarities are both positive and negative with respect to ground.

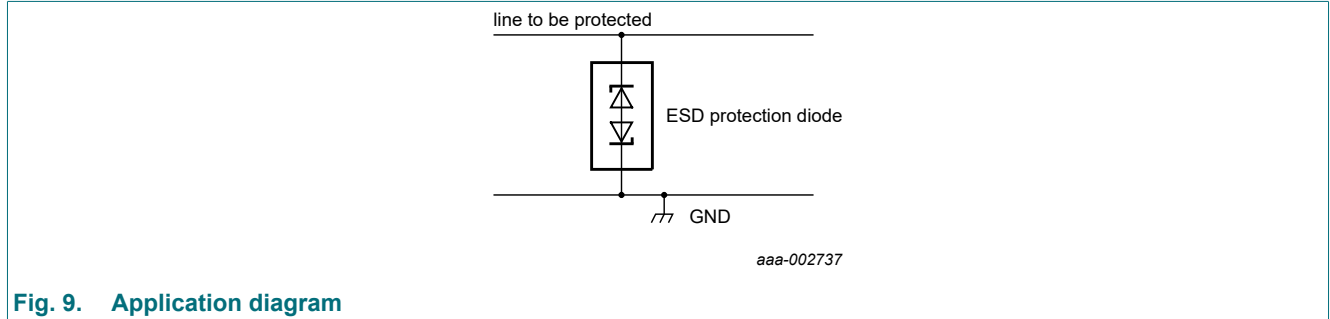


Fig. 9. Application diagram

### Circuit board layout and protection device placement

Circuit board layout is critical for the suppression of ESD, Electrical Fast Transient (EFT) and surge transients. The following guidelines are recommended:

1. Place the device as close to the input terminal or connector as possible.
2. Minimize the path length between the device and the protected line.
3. Keep parallel signal paths to a minimum.
4. Avoid running protected conductors in parallel with unprotected conductors.
5. Minimize all Printed-Circuit Board (PCB) conductive loops including power and ground loops.
6. Minimize the length of the transient return path to ground.
7. Avoid using shared transient return paths to a common ground point.
8. Use ground planes whenever possible. For multilayer PCBs, use ground vias.

## 11. Test information

### Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard Q101 - *Stress test qualification for discrete semiconductors*, and is suitable for use in automotive applications.

## 12. Package outline

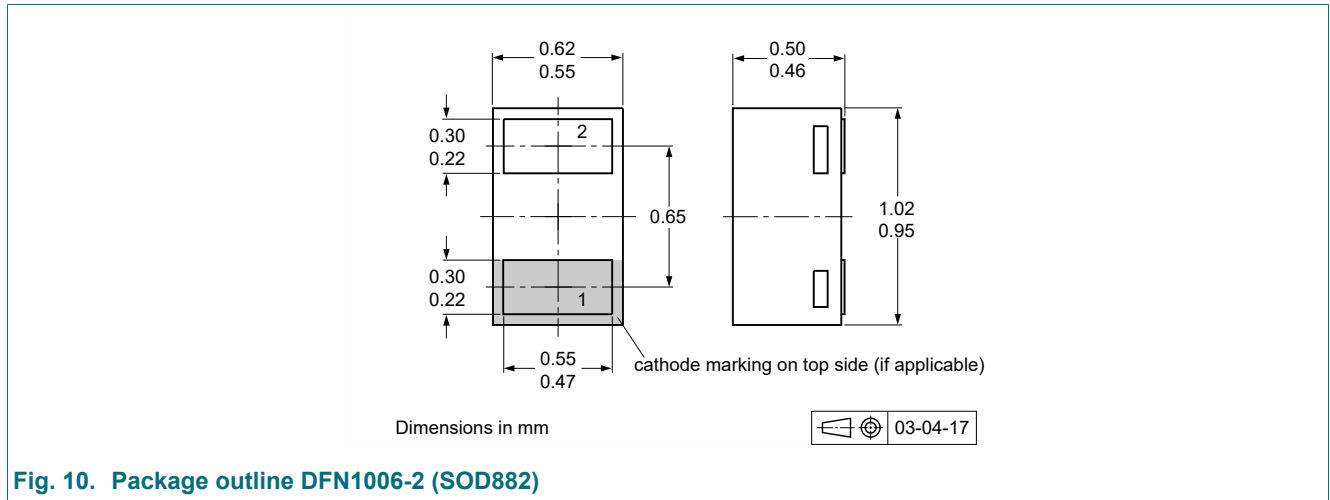


Fig. 10. Package outline DFN1006-2 (SOD882)

## 13. Soldering

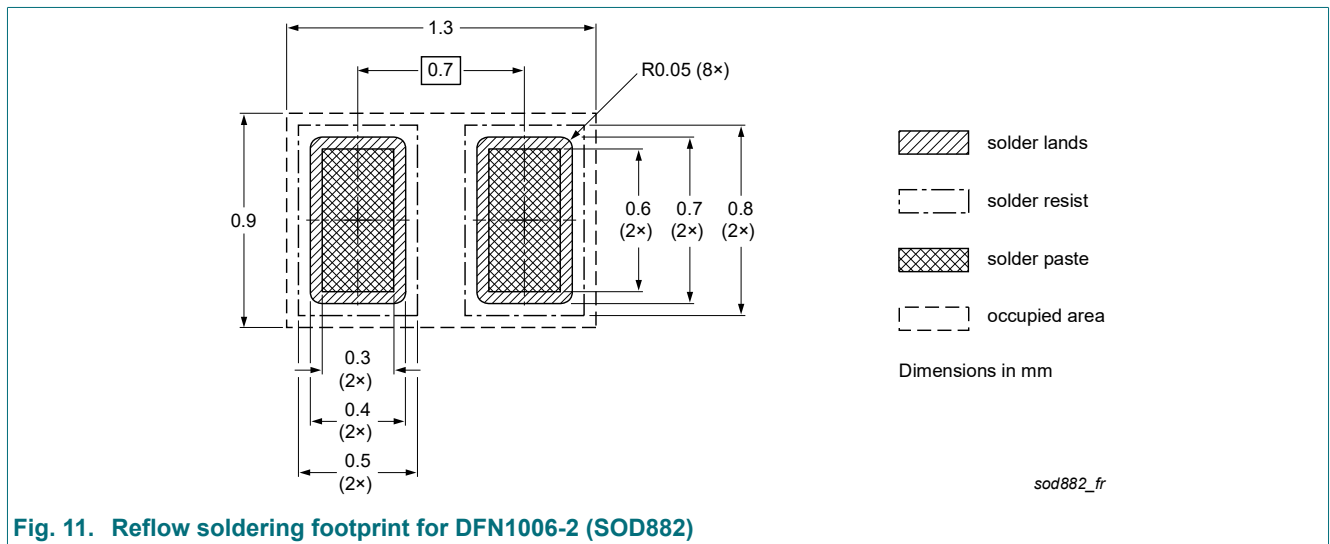


Fig. 11. Reflow soldering footprint for DFN1006-2 (SOD882)

## 14. Revision history

Table 7. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
PESD18VF1BL-Q v.1	20220118	Product data sheet	-	-



## 15. Legal information

### Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
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