

# FAB3102

## 2.0 Watt Class-D Audio Amplifier with Integrated Boost Regulator and Automatic Gain Control

### Features

- High Output, High-Efficiency, Class-D Mono Speaker Amplifier
- Low EMI Design Allows Filterless Operation
- High Noise Rejection Using Differential Audio Inputs
- High-Efficiency Boost Regulator Provides Higher Output Power Over Battery Voltages
- Boost Shutdown at Lower Output Power Increases Efficiency and Reduces Quiescent Current Consumption
- Automatic Gain Control (AGC) Monitors Battery Voltage and Dynamically Adjusts Gain, Extending Battery Runtime
- Short-Circuit Protection
- Low-Voltage Shutdown
- Click and Pop Suppression
- Available in 12-Bump WLCSP

### Description

The FAB3102 is a mono, Class-D, boosted audio amplifier with differential audio inputs.

An integrated boost regulator allows for high output power over a power supply range of 2.5V to 5.2V. At low output power, the boost regulator automatically shuts down for greater efficiency and lower quiescent current consumption.

Automatic Gain Control (AGC) reduces gain when the power supply voltage is low to limit maximum current consumption.

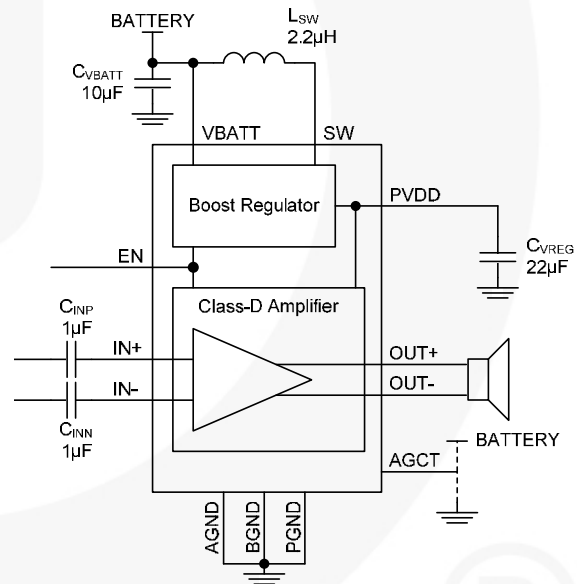


Figure 1. Typical Application Circuit

### Ordering Information

Part Number	Operating Temperature Range	Package	Packing Method
FAB3102UCX	-40°C to +85°C	12-Bump, 0.5mm Pitch, Wafer-Level Chip-Scale Package (WLCSP)	3000 Units on Tape & Reel

## Pin Configuration

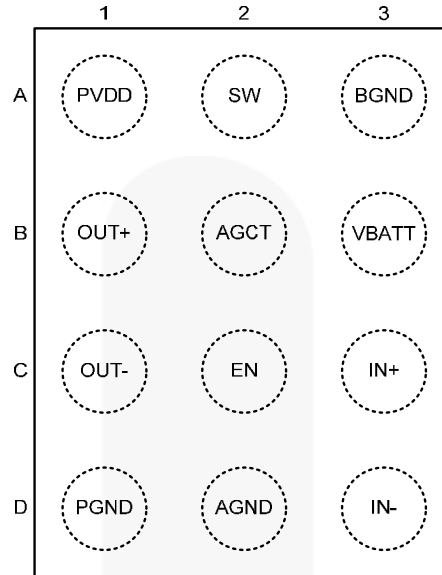


Figure 2. 12-Bump, 0.5mm Pitch WLCSP, Top View

## Pin Definitions

WLCSP	Name	Type	Description
B1	OUT+	Output	Positive audio output
C1	OUT-	Output	Negative audio output
C3	IN+	Analog input	Positive audio input
D3	IN-	Analog input	Negative audio input
C2	EN	CMOS input	Shutdown signal for boost regulator and amplifier: VBATT=enabled, PGND=shutdown (internal 300KΩ pull-down)
B2	AGCT	Analog input	AGC trip point setting
B3	VBATT	Power	Supply voltage
A2	SW	Power	Boost regulator switching node
A1	PVDD	Power	Boost regulator output
A3	BGND	Ground	Boost regulator ground – connect to PGND and AGND with a ground plane.
D1	PGND	Ground	Power ground – connect to BGND and AGND with a ground plane.
D2	AGND	Ground	Analog ground – connect to BGND and PGND with a ground plane.

## Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Min.	Max.	Unit
V <sub>BATT</sub>	Voltage on VBATT Pin	-0.3	6.0	V
V <sub>OUT</sub>	Voltage on OUT-, OUT+ Pin	-0.3	V <sub>BSTOUT</sub> + 0.3	V
V <sub>IN</sub>	Voltage on SW, IN-, IN+, EN, AGCT Pin	-0.3	V <sub>BATT</sub> + 0.3	V
P <sub>D</sub>	Power Dissipation		Internally Limited	

## Dissipation Ratings

Symbol	Parameter	Min.	Typ.	Max.	Unit
T <sub>J</sub>	Junction Temperature			150	°C
T <sub>STG</sub>	Storage Temperature Range	-65		150	°C
T <sub>L</sub>	Lead Temperature (Soldering, 10s)			300	°C
θ <sub>JA</sub>	Thermal Resistance, JEDEC Standard, Multilayer Test Boards, Still Air		77		°C/W

## Electrostatic Discharge Protection

Symbol	Parameter	Condition	Level	Unit
ESD	Human Body Model (HBM)	EIA/JESD22-A114	±3	KV
	Charged Device Model (CDM)	According to "EIA/JESD22-C101 Level III" Compatible with "IEC61340-3-3 Level C4" or "ESD-STM5.3.1-1999 Level C4"	±1	KV

## Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Min.	Typ.	Max.	Unit
T <sub>A</sub>	Operating Temperature Range	-40		85	°C
V <sub>BATT</sub>	V <sub>BATT</sub> Supply Voltage Range	2.5		5.2	V
L <sub>SW</sub>	Inductor (at Peak Inductor Current: 1.5A) <sup>(1)</sup>	1.4	2.2		μH
C <sub>VBATT</sub>	VBATT Capacitor <sup>(1)</sup>	2.0	10.0		μF
C <sub>PVDD</sub>	PVDD Capacitor <sup>(1)</sup>	6.8	22.0		μF
C <sub>AGCT</sub>	Capacitive Load on AGCT			10	pF
R <sub>L</sub>	Load Resistance	3.5			Ω

**Note:**

1. Minimum passive component values include temperature, tolerance, and aging.

## Electrical Characteristics

Unless otherwise noted: AGCT=GND,  $R_L=8\Omega + 33\mu\text{H}$ ,  $f=1\text{KHz}$ , and audio measurement bandwidth=22Hz to 20KHz (AES17). Typical values are at  $V_{\text{BATT}}=3.6\text{V}$ ,  $T_A=25^\circ\text{C}$ , with typical external component values. Minimum and maximum values are at  $V_{\text{BATT}}=2.5\text{V}$  to  $5.2\text{V}$ ,  $T_A=-40^\circ\text{C}$  to  $85^\circ\text{C}$ , with minimum external component values.

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Unit
$I_{\text{DD}}$	Quiescent Current	Inputs AC Grounded, $R_L=\text{Open}$ , EN=HIGH	With Class-D Edge Rate Control		3.1		mA
			Without Class-D Edge Rate Control		2.7		
$I_{\text{SD}}$	Shutdown Current	EN=PGND, Inputs AC Grounded, $V_{\text{BATT}}=3.6\text{V}$ , $T_A=25^\circ\text{C}$			0.1	2	$\mu\text{A}$
$t_{\text{WU}}$	Wake-Up Time	From LOW to HIGH EN Transition to Full Operation			5	12	ms
$f_{\text{SW(AMP)}}$	Class D Switching Frequency				300		KHz
$V_{\text{OS}}$	Differential Output Offset Voltage	Inputs AC Grounded			1.67	5.00	mV
$A_v$	Gain	AGC Inactive		9.5	10	10.5	V/V
$R_{\text{IN}}$	Input Resistance	Gain=10V/V (AGC Inactive)	Differential	24	30	36	K $\Omega$
			Single-Ended	12	15	18	
$R_{\text{STD}}$	Single-Ended Input Impedance During Shutdown	EN=PGND, AC-Coupled Inputs, $V_{\text{INx}} < 2V_{\text{rms}}$ per Input		80			K $\Omega$
$V_{\text{STD}}$	Maximum Single-Ended Input Voltage Swing During Shutdown	EN=PGND, AC-Coupled Inputs		2			$V_{\text{rms}}$
	THD+N Added to Audio Signal at Inputs During Shutdown	EN=PGND, AC-Coupled Inputs, Source Impedance $< 1\Omega$				0.02	%
THD+N	Total Harmonic Distortion Plus Noise	f=300Hz, $P_{\text{OUT}}=100\text{mW}$			0.03		%
		f=1KHz, $P_{\text{OUT}}=100\text{mW}$			0.03		
		f=10KHz, $P_{\text{OUT}}=100\text{mW}$			0.20		
		f=300Hz, $P_{\text{OUT}}=1\text{W}$			0.03		
		f=1KHz, $P_{\text{OUT}}=1\text{W}$			0.03		
		f=10KHz, $P_{\text{OUT}}=1\text{W}$			0.20		
		f=300Hz to 10KHz, $P_{\text{OUT}}=10\text{mW}$ to $1.7\text{W}$ , $V_{\text{BATT}}=3.6\text{V}$ , $T_A=25^\circ\text{C}$				1.00	
$P_{\text{O}}$	Output Power	THD+N $\leq 1\%$ , f=300Hz to 10KHz, $V_{\text{BATT}} \geq 3.6\text{V}$	$R_L=8\Omega+33\mu\text{H}$ , $T_A=25^\circ\text{C}$	1.7			W
			$R_L=4\Omega+33\mu\text{H}$ , $T_A=25^\circ\text{C}$	2.0			
			$R_L=8\Omega+33\mu\text{H}$ , $T_A=-40^\circ\text{C}$ to $85^\circ\text{C}$	1.7			
			$R_L=4\Omega+33\mu\text{H}$ , $T_A=-40^\circ\text{C}$ to $75^\circ\text{C}$	1.9			
$I_{\text{DLMT}}$	Class-D Output Current Limit				1.4		A

Continued on the following page...

## Electrical Characteristics

Unless otherwise noted: AGCT=GND,  $R_L=8\Omega + 33\mu\text{H}$ ,  $f=1\text{KHz}$ , and audio measurement bandwidth=22Hz to 20KHz (AES17). Typical values are at  $V_{\text{BATT}}=3.6\text{V}$ ,  $T_A=25^\circ\text{C}$ , with typical external component values. Minimum and maximum values are at  $V_{\text{BATT}}=2.5\text{V}$  to  $5.2\text{V}$ ,  $T_A=-40^\circ\text{C}$  to  $85^\circ\text{C}$ , with minimum external component values.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
PSRR	Power Supply Rejection Ratio	Inputs Shorted, AC Grounded, Input Referred; $V_{\text{RIPPLE}}=200\text{mV}_{\text{P-P}}$ Square Centered Around $V_{\text{BATT}}=3.8\text{V}$ , 50% Duty Cycle, 10 $\mu\text{s}$ Rise/Fall Time	$f_{\text{RIPPLE}}=1\text{KHz}$ , Boost Enabled		85	dB
			$f_{\text{RIPPLE}}=217\text{Hz}$ , Boost Enabled		88	
			$f_{\text{RIPPLE}}=1\text{KHz}$ , Boost Bypassed		77	
			$f_{\text{RIPPLE}}=217\text{Hz}$ , Boost Bypassed		70	
CMRR	Common Mode Rejection Ratio	$V_{\text{RIPPLE}}=200\text{mV}_{\text{P-P}}$ Square, 50% Duty Cycle, 10 $\mu\text{s}$ Rise/Fall Time, Inputs Shorted and AC-Coupled to $V_{\text{RIPPLE}}$	$f_{\text{RIPPLE}}=1\text{KHz}$		55	dB
			$f_{\text{RIPPLE}}=217\text{Hz}$		51	
$V_{\text{BIAS}}$	IN+, IN- Bias Voltage			1.2		V
$\eta$	Efficiency with Class-D Edge Rate Control	$R_L=8\Omega+33\mu\text{H}$ , $P_{\text{OUT}}=1.7\text{W}$		73	%	
		$R_L=4\Omega+33\mu\text{H}$ , $P_{\text{OUT}}=2.4\text{W}$		67		
	Efficiency without Class-D Edge Rate Control	$R_L=8\Omega+33\mu\text{H}$ , $P_{\text{OUT}}=1.7\text{W}$		74		
		$R_L=4\Omega+33\mu\text{H}$ , $P_{\text{OUT}}=2.4\text{W}$		68		
SNR	Signal-To-Noise Ratio	$P_{\text{OUT}}=1.7\text{W}$ , $R_L=8\Omega+33\mu\text{H}$ , A-Weighted		96	dB	
		$P_{\text{OUT}}=1.7\text{W}$ , $R_L=8\Omega + 33\mu\text{H}$ , Unweighted		94		
		$P_{\text{OUT}}=2.0\text{W}$ , $R_L=4\Omega + 33\mu\text{H}$ , A-Weighted		94		
		$P_{\text{OUT}}=2.0\text{W}$ , $R_L=4\Omega + 33\mu\text{H}$ , Unweighted		91		
$e_n$	Output Noise	A-Weighted		59	$\mu\text{V}_{\text{rms}}$	
		Unweighted		76		
$T_{\text{STD}}$	Thermal Shutdown	Junction Temperature		165		$^\circ\text{C}$
$T_{\text{HYS}}$	Thermal Shutdown Hysteresis	Junction Temperature		25		$^\circ\text{C}$
$V_{\text{ULVO}}$	$V_{\text{BATT}}$ Under-Voltage Shutdown		1.8	2.1	2.3	V
$V_{\text{HYS}}$	$V_{\text{BATT}}$ Under-Voltage Hysteresis	$T_A=25^\circ\text{C}$		120	300	mV
$f_{\text{SW(REG)}}$	Boost Converter Switching Frequency	$P_{\text{OUT}}=1.7\text{W}$		1.2		MHz
$I_{\text{LIMIT(SU)}}$	Boost Converter Inrush Current Limit	$PV_{\text{DD}}$ Rising from 0V to $V_{\text{BATT}}$ , $C_{\text{PVDD}}=22\mu\text{F}$			600	mA
$t_{\text{INRUSH}}$	Boost Converter Inrush Time	$PV_{\text{DD}}$ Rising from 0V to $V_{\text{BATT}}$ , $C_{\text{PVDD}}=22\mu\text{F}$			1000	$\mu\text{s}$

Continued on the following page...

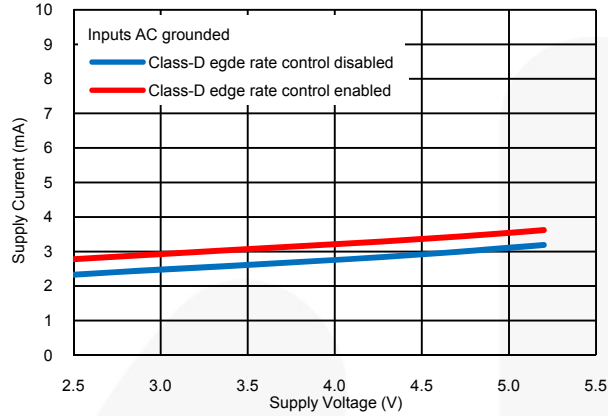
## Electrical Characteristics

Unless otherwise noted: AGCT=GND,  $R_L=8\Omega + 33\mu\text{H}$ ,  $f=1\text{KHz}$ , and audio measurement bandwidth=22Hz to 20KHz (AES17). Typical values are at  $V_{\text{BATT}}=3.6\text{V}$ ,  $T_A=25^\circ\text{C}$ , with typical external component values. Minimum and maximum values are at  $V_{\text{BATT}}=2.5\text{V}$  to  $5.2\text{V}$ ,  $T_A=-40^\circ\text{C}$  to  $85^\circ\text{C}$ , with minimum external component values.

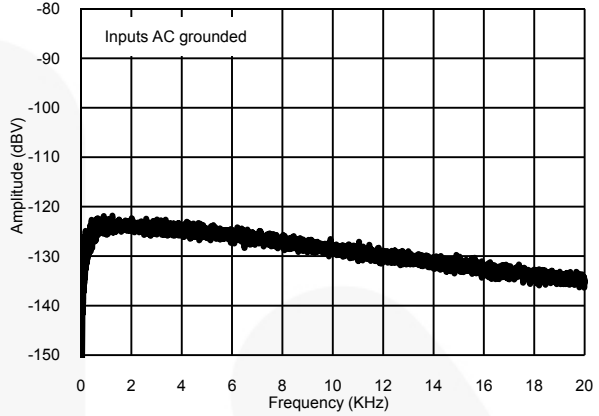
Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$I_{\text{BST}}$	Auto Boost Startup Current Limit	$PV_{\text{DD}}$ Rising from $V_{\text{BATT}}$ to 5.6V, $C_{\text{PVDD}}=22\mu\text{F}$			2000	mA
$t_{\text{BSTSRT}}$	Auto Boost Startup Time	$PV_{\text{DD}}$ Rising from $V_{\text{BATT}}$ to 5.6V, $C_{\text{PVDD}}=22\mu\text{F}$ , $V_{\text{BATT}}=3.6\text{V}$ , $T_A=25^\circ\text{C}$			200	$\mu\text{s}$
	Auto Boost Startup Current Ramp Rate	$PV_{\text{DD}}$ Rising from $V_{\text{BATT}}$ to 5.6V, $C_{\text{PVDD}}=22\mu\text{F}$ , $V_{\text{BATT}}=3.6\text{V}$ , $T_A=25^\circ\text{C}$		15		mA/ $\mu\text{s}$
$I_{\text{BOOST}}$	Boost Converter Peak Input Current Limit	Open-Loop Limit, $V_{\text{BATT}}=3.6\text{V}$ , $T_A=25^\circ\text{C}$	1100	1600	2100	mA
$V_{\text{BSTOUT}}$	Boost Converter Output Voltage	$V_{\text{BATT}}=3.6\text{V}$ , $T_A=25^\circ\text{C}$	5.55	5.65	5.75	V
$V_{\text{BSTSTD}}$	Auto Boost Shutdown Threshold Voltage			2		$V_{\text{pk}}$
$t_{\text{HOLD}}$	Auto Boost Shutdown Hold Time			125		ms
$V_{\text{AGC}}$	AGC Trip Point	AGCT=Floating	3.190	3.250	3.283	V
		AGCT=GND	3.480	3.550	3.586	
		AGCT= $V_{\text{BATT}}$	3.680	3.750	3.788	
	Output Power with AGC	AGCT=GND, $V_{\text{IN}}=0.4V_{\text{pk}}$ , 1KHz Sine Wave	$V_{\text{BATT}}=3.4\text{V}$	0.79		W
		$V_{\text{BATT}}=3.0\text{V}$	0.45			
$t_{\text{A}}$	AGC Attack Time			20		$\mu\text{s}/\text{dB}$
$t_{\text{R}}$	AGC Release Time			1600		ms/dB
	AGC Step Size			0.5		dB
	AGC Maximum Attenuation			10		dB
$V_{\text{IH}}$	EN Logic Input High Voltage		1.1			V
$V_{\text{IL}}$	EN Logic Input Low Voltage				0.45	V
$C_{\text{IN}}$	EN Capacitance			10		pF
$R_{\text{PD}}$	EN Pull-Down Resistance			300		K $\Omega$

## Typical Performance Characteristics

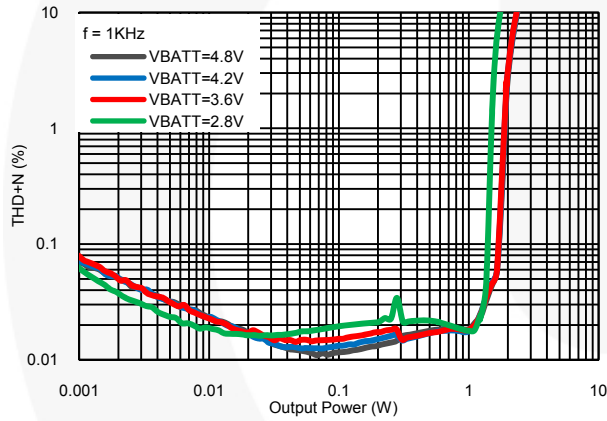
Unless otherwise noted: AGCT = GND,  $R_L = 8\Omega + 33\mu\text{H}$ ,  $f = 1\text{KHz}$ , audio measurement bandwidth 22Hz to 20KHz (AES17),  $V_{\text{BATT}} = 3.6\text{V}$ ,  $T_A = 25^\circ\text{C}$ , typical external component values.



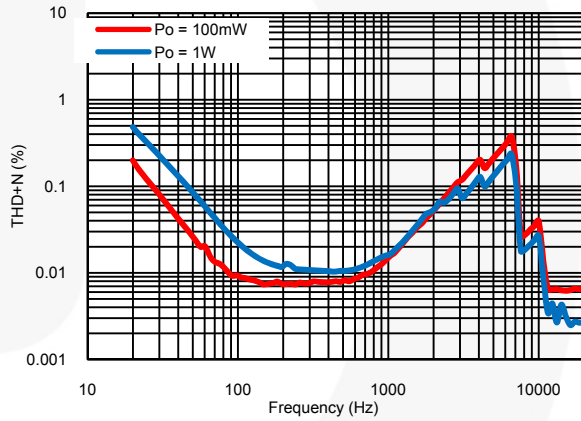
**Figure 3. Quiescent Supply Current vs. Supply Voltage**



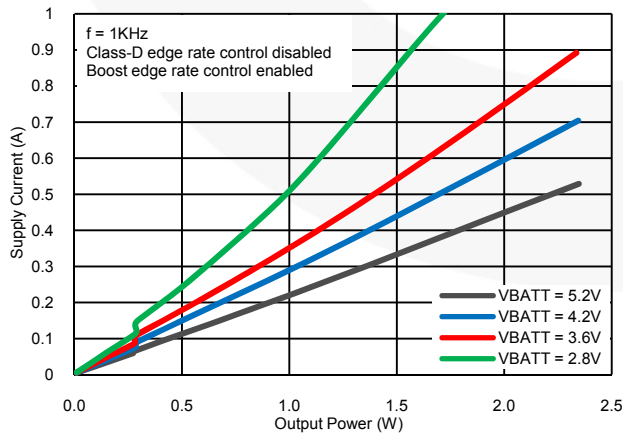
**Figure 4. A-Weighted Output Noise vs. Frequency**



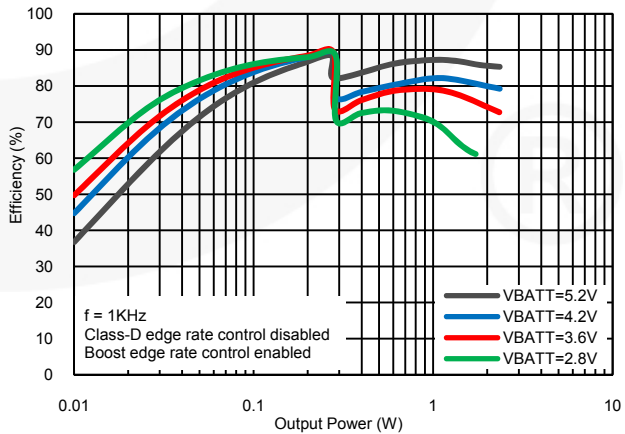
**Figure 5. Total Harmonic Distortion + Noise vs. Output Power**



**Figure 6. Total Harmonic Distortion + Noise vs. Frequency**



**Figure 7. Supply Current vs. Output Power**



**Figure 8. Efficiency vs. Output Power**

## Typical Performance Characteristics

Unless otherwise noted: AGCT = GND,  $R_L = 8\Omega + 33\mu\text{H}$ ,  $f = 1\text{KHz}$ , audio measurement bandwidth 22Hz to 20KHz (AES17),  $V_{\text{BATT}} = 3.6\text{V}$ ,  $T_A = 25^\circ\text{C}$ , typical external component values.

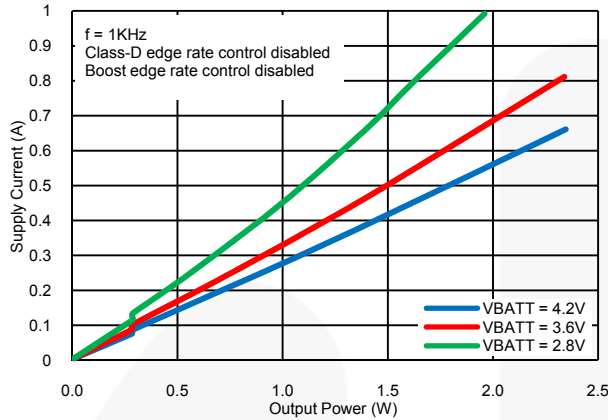


Figure 9. Supply Current vs. Output Power

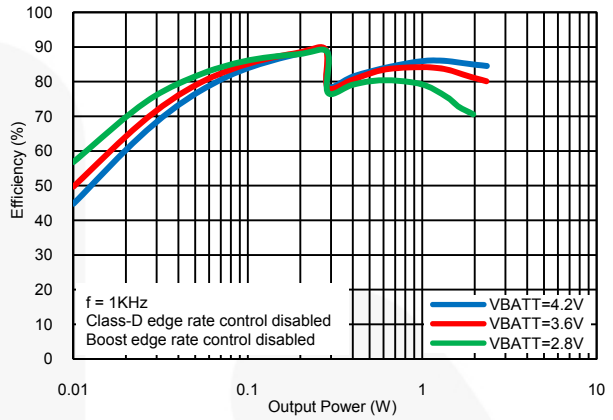


Figure 10. Efficiency vs. Output Power

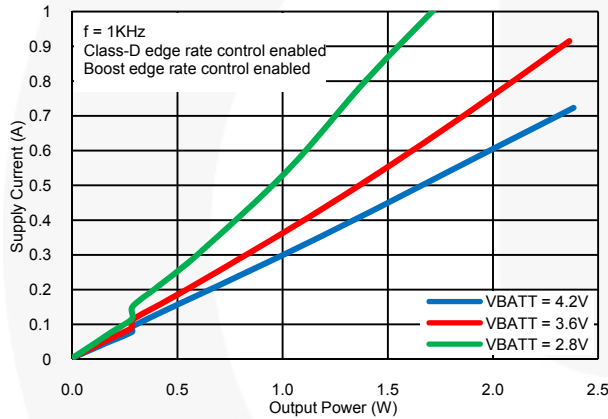


Figure 11. Supply Current vs. Output Power

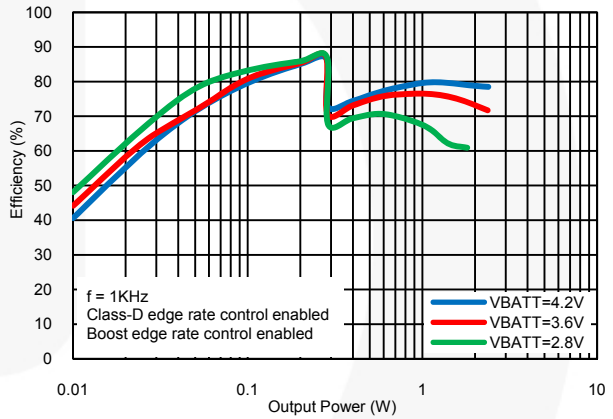


Figure 12. Efficiency vs. Output Power

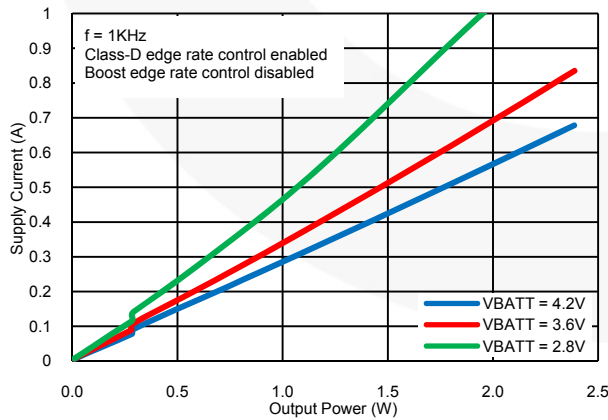


Figure 13. Supply Current vs. Output Power

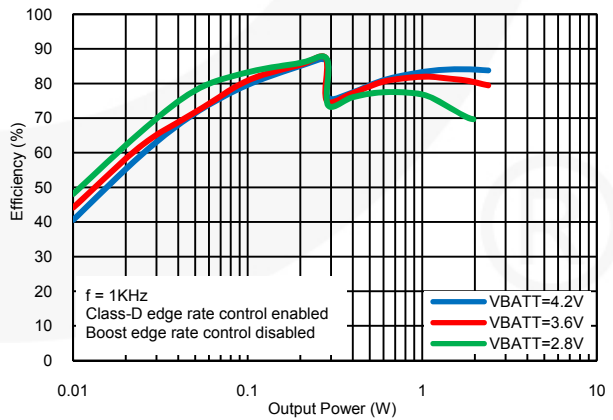


Figure 14. Efficiency vs. Output Power



## Typical Performance Characteristics

Unless otherwise noted: AGCT = GND,  $R_L = 8\Omega + 33\mu\text{H}$ ,  $f = 1\text{KHz}$ , audio measurement bandwidth 22Hz to 20KHz (AES17),  $V_{\text{BATT}} = 3.6\text{V}$ ,  $T_A = 25^\circ\text{C}$ , typical external component values.

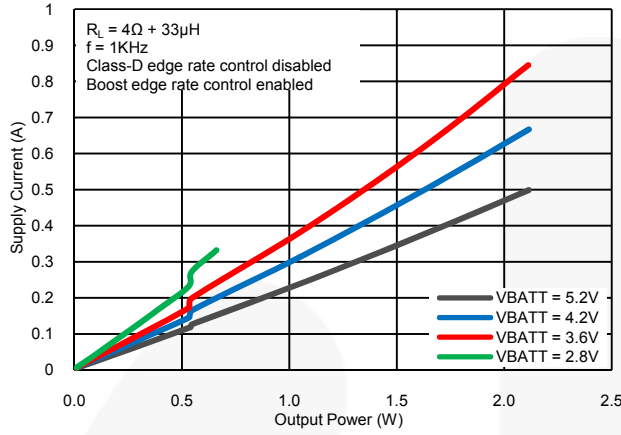


Figure 15. Supply Current vs. Output Power

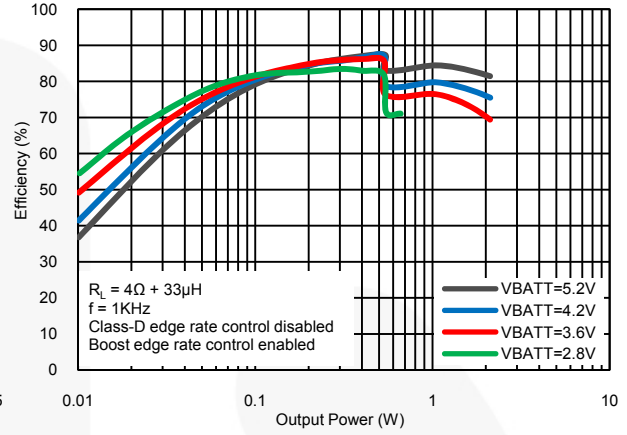


Figure 16. Efficiency vs. Output Power

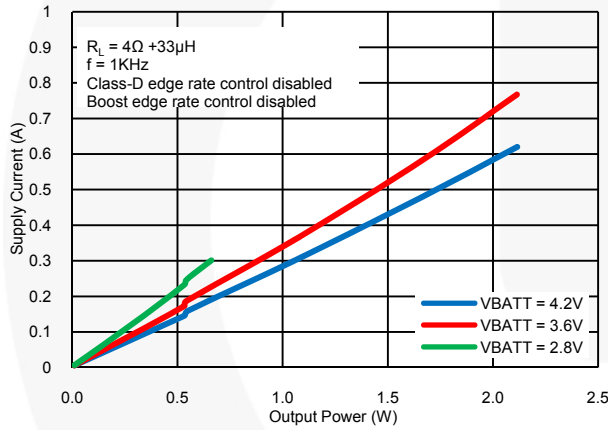


Figure 17. Supply Current vs. Output Power

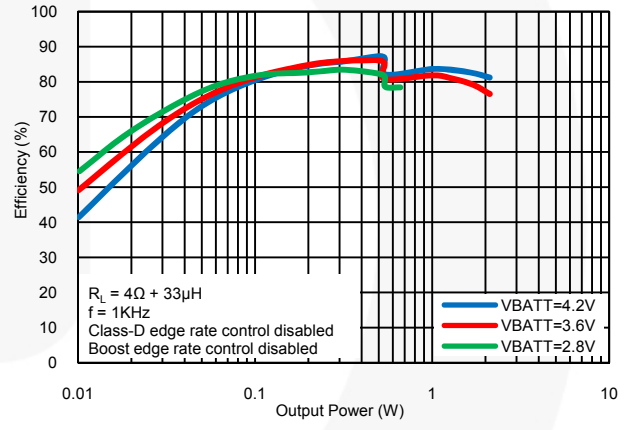


Figure 18. Efficiency vs. Output Power

## Detailed Description

### Signal Path

The FAB3102 features a fully differential signal path for noise rejection. The low-EMI design allows the OUT+ and OUT- pins to be connected directly to a speaker without an output filter.

The input section includes an 80KHz low-pass filter for removing out-of-band noise from audio sources, such as sigma delta DACs.

### Shutdown

If EN is grounded, the Class-D amplifier and the boost regulator are turned off. IN+ and IN- are high impedance. Audio signals present at IN+ and IN- with amplitude less than the maximum differential input voltage swing are not distorted by the FAB3102 (see *electrical characteristics*).

When EN transitions from LOW to HIGH, during the wake-up time (see *Electrical Characteristics*) the FAB3102 charges the input DC blocking capacitors to the Common Mode voltage before enabling the Class-D amplifier. To minimize click and pop during turn-on, audio signals should not be present during the wake-up period. Other devices that are connected to the same input signal, if not muted, may experience a pop due to this capacitor charging.

There is no limitation on the length of shutdown. Remaining charge on the PVDD capacitor at startup (for example, if EN is LOW for only a short period) does not affect startup behavior.

The EN pin has an internal 300K $\Omega$  pull-down resistor.

EN must be LOW when  $V_{BATT}$  is lower than the  $V_{BATT}$  under-voltage shutdown voltage (see *Electrical Characteristics*). EN must remain LOW for at least 100 $\mu$ s after  $V_{BATT}$  rises above the  $V_{BATT}$  under-voltage shutdown voltage.

### Class-D Amplifier Over-Current Protection

If the output current of the Class-D amplifier exceeds limits (see *the Electrical Characteristics*), the amplifier is disabled for approximately one second. (Other systems, such as the boost regulator and AGC, remain active.) After one second, the amplifier is re-enabled. If the fault condition still exists, the amplifier is disabled again. This cycle repeats until the fault condition is removed.

### Low EMI

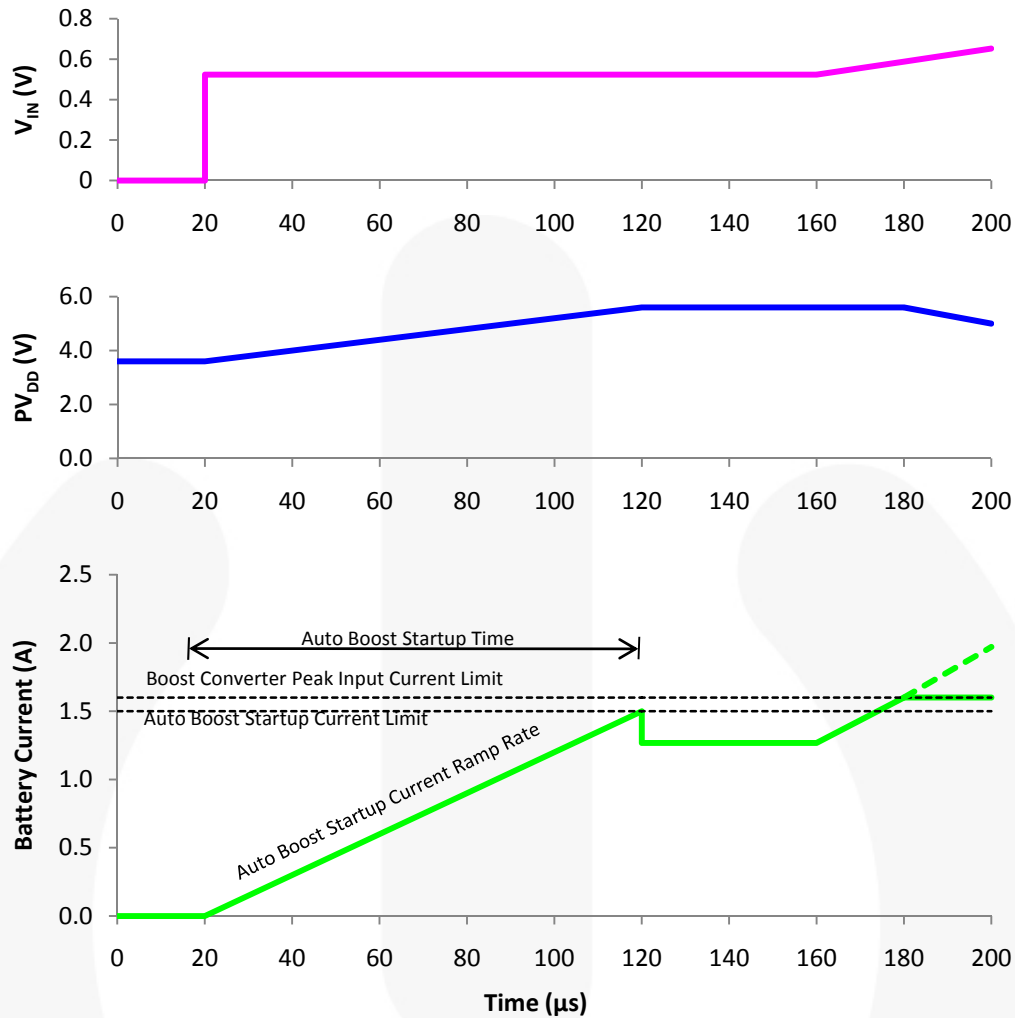
To minimize EMI, edge rate control for the boost regulator and Class-D amplifier can be employed.

The boost regulator's rise and fall times are set to 20ns per transition by default. For devices with 10ns boost edge rates or disabled boost regulator edge-rate control, contact a Fairchild Representative. This is a factory option that cannot be changed in the application.

The Class-D amplifier's edge rate control is disabled by default. For devices with 20ns Class-D edge rates, contact a Fairchild Representative. This is a factory option that cannot be changed in the application.

### Automatic Boost Shutdown

Automatic boost shutdown changes the Class-D amplifier supply voltage as a function of audio output level. At audio output levels above  $2V_{pk}$ , the boost converter generates 5.65V from the input battery voltage. If the output level is below  $2V_{pk}$  for more than 125ms, the boost converter is switched off and the Class-D amplifier is supplied directly from the battery. As a result, efficiency is improved at low audio output levels and quiescent current consumption is reduced.



**Figure 19. Auto Boost Startup**

Figure 19 shows an example of an auto boost startup event. At first, the boost converter is off and PV<sub>DD</sub> is the same voltage as VBATT. At 20μs, a large audio signal is presented at the inputs, which causes the boost converter to start up. From 20μs to 120μs, battery current is ramped up from 0A to the auto boost startup current Limit of 1.5A for the duration of the auto boost startup time. The auto boost startup current ramp rate is 15mA/μs. These limits are enforced to avoid sudden current draw spikes from the battery.

At 120μs, after the auto boost startup time, the ramp is released and battery current falls to a level capable of sustaining the speaker amplifier's outputs. At 160μs, the input signal begins to rise, which increases battery current. At 180μs, the boost converter peak input current limit is enforced and battery current levels off, which causes PV<sub>DD</sub> to droop.

The boost regulator should not be used to drive any loads other than the Class-D amplifier.

### Automatic Gain Control

Due to constant output power, the amount of VBATT current needed to maintain a given output amplitude is inversely proportional to VBATT voltage. This produces very large current requirements at low VBATT. The AGC eases low-VBATT current demands by reducing the gain when VBATT voltage drops below a trip point. One of three different trip points may be selected by shorting AGCT to VBATT, shorting AGCT to PGND, or floating AGCT (see *Electrical Characteristics*).

The trip point is determined upon power-on and when EN transitions from LOW to HIGH. If AGCT is changed during operation, the new value is not read until power or EN is cycled.

When VBATT is above the trip point, the AGC has no effect on the signal path.

When VBATT is at or below the trip point, target gain is reduced in 0.5dB steps according to the equation:

$$G_{target} = G_I - S_L G_I \left( \frac{V_T - V_{batt}}{V_{out\ max}} \right) \quad (1)$$

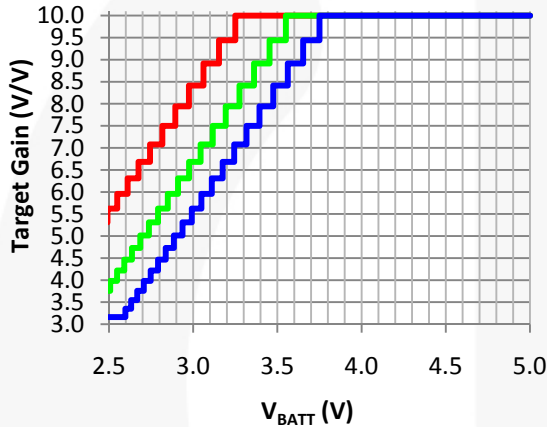
where:

- $G_I$  = Initial Gain (10V/V);
- $S_L$  = 3V/V Slope;
- $V_{OUTMAX}$  = 5.2V;
- $V_T$  = AGC Trip Point Set by the AGCT Pin; and
- $V_{BATT}$  = Voltage at the VBATT Pin.

Target gain can be reduced by as much as 10dB.

Note that the state of auto boost shutdown has no effect on the AGC.

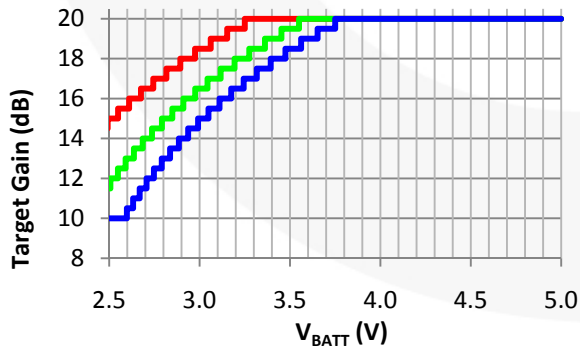
Figure 20 shows target gain vs. battery voltage.



Line Color	AGCT Configuration	AGC Trip Point (V)
Red	Float	3.25
Green	Ground	3.55
Blue	V <sub>BATT</sub>	3.75

Figure 20. Target Gain vs. Battery Voltage

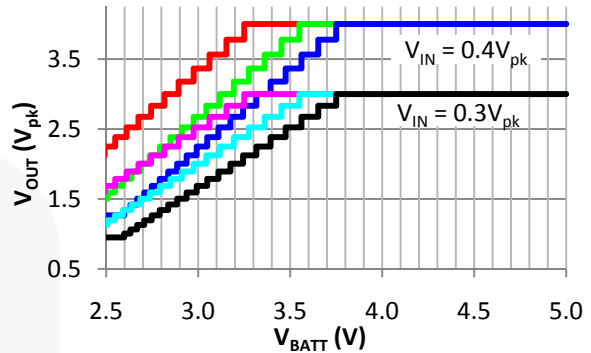
Figure 21 is similar to Figure 20 except that the target gain is expressed in dB rather than V/V.



Line Color	AGCT Configuration	AGC Trip Point (V)
Red	Float	3.25
Green	Ground	3.55
Blue	V <sub>BATT</sub>	3.75

Figure 21. Target Gain vs. Battery Voltage

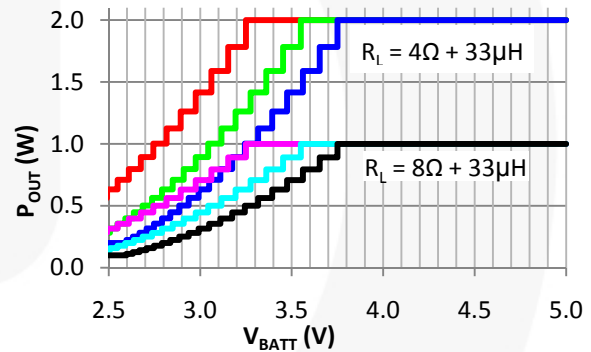
Figure 22 shows examples of peak output voltage vs. battery voltage.



Line Color	AGCT Configuration	AGC Trip Point (V)	Input Voltage (V <sub>pk</sub> )
Red	Float	3.25	0.4
Green	Ground	3.55	0.4
Blue	V <sub>BATT</sub>	3.75	0.4
Magenta	Float	3.25	0.3
Cyan	Ground	3.55	0.3
Black	V <sub>BATT</sub>	3.75	0.3

Figure 22. Output Voltage vs. Battery Voltage

Figure 23 shows examples of output power vs. battery voltage with a 0.4V<sub>pk</sub> sinusoidal input signal.



Line Color	AGCT Configuration	AGC Trip Point (V)	Input Voltage (V <sub>pk</sub> )
Red	Float	3.25	0.4
Green	Ground	3.55	0.4
Blue	V <sub>BATT</sub>	3.75	0.4
Magenta	Float	3.25	0.3
Cyan	Ground	3.55	0.3
Black	V <sub>BATT</sub>	3.75	0.3

Figure 23. Output Power vs. Battery Voltage Examples (V<sub>IN</sub>=0.4V<sub>pk</sub> Sine)

The speed at which gain can change is limited (see *Electrical Characteristics*); therefore, the actual gain may lag the target gain if  $V_{BATT}$  voltage changes quickly.

Figure 24 and Figure 25 show examples of AGC changes over time. In these examples, AGCT is grounded, so the AGC trip point is 3.55V.

- Initially,  $V_{BATT}$  is 3.6V and gain is 10V/V (20dB).
- A narrow  $V_{BATT}$  drop of less than  $2\mu\text{s}$  is ignored by the AGC.
- The next  $V_{BATT}$  drop lasts longer and the AGC is tripped. The initial 0.5dB gain reduction occurs  $3.9\mu\text{s}$  after  $V_{BATT}$  crosses below the 3.55V trip point.

- $V_{BATT}$  is now 3.1V, so target gain is  $10\text{V/V} - 3\text{V/V} \times 10\text{V/V} \times [(3.55\text{V} - 3.1\text{V}) / 5.2\text{V}] = 7.40\text{V/V} = 17.4\text{dB}$ .
- Gain continues to drop by 0.5dB every  $10\mu\text{s}$  until it is below the target gain, where it settles at 17.0dB.
- When  $V_{BATT}$  rises above the trip point, gain increases by 0.5dB. If more than 800ms has passed since the last gain change, gain does not rise until after 800ms has passed, as shown in Figure 25.
- While  $V_{BATT}$  remains above the trip point, gain continues to increase by 0.5dB every 800ms until it returns to 20dB.

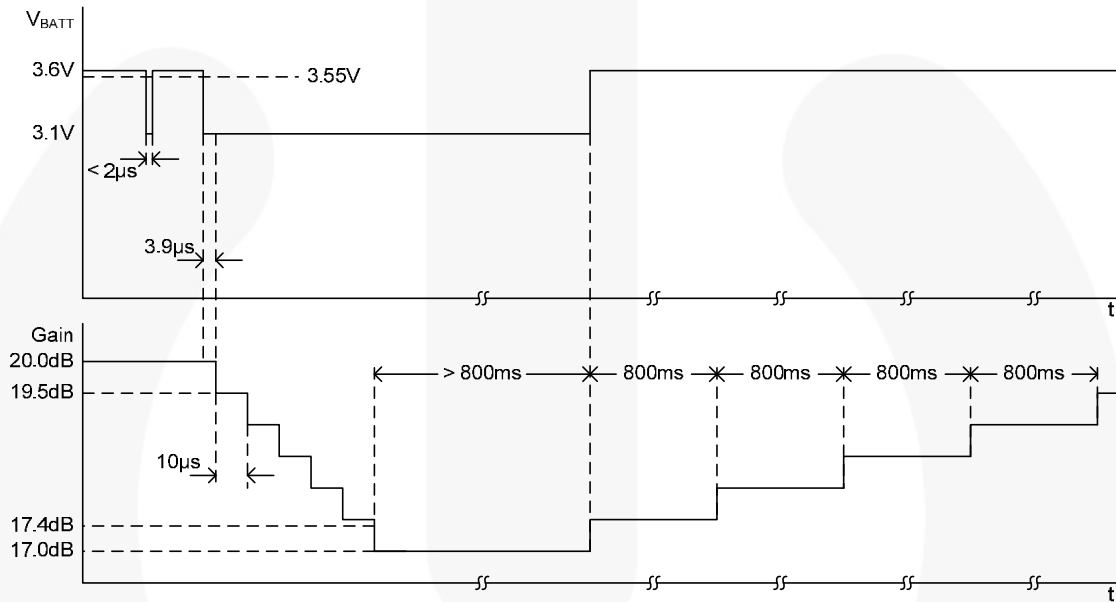


Figure 24. AGC Changes vs. Time, Example 1

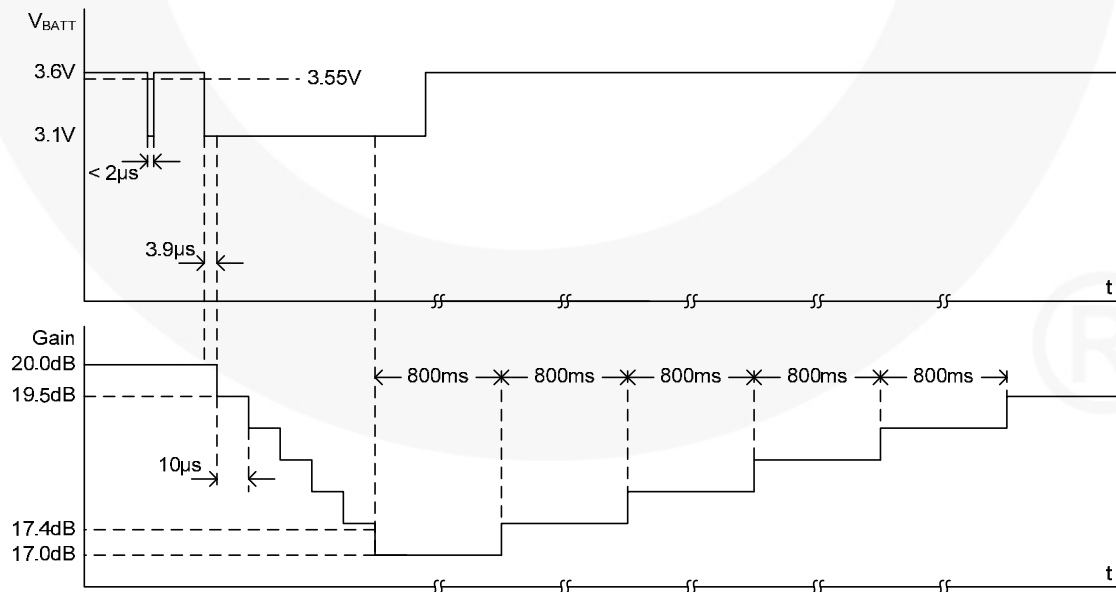


Figure 25. AGC Changes vs. Time, Example 2

The intent of the AGC circuitry is to limit current draw from the battery to extend runtime. This is particularly important for handsets that incorporate advanced shutdown algorithms that measure battery voltage. The AGC circuit dynamically adjusts the amplifier gain depending on the trip point used. Even though the amplifier gain is reduced in response to lower battery

voltages, two conditions result in continued higher current draw: 1) the handset volume is turned up in an attempt to maintain the same loudness, or 2) the input signal is increased. If one or both of these conditions exist, even though the amplifier gain is reduced in response to lower battery voltage, current draw remains elevated, eventually resulting in handset shutdown.

## Applications Information

### Layout Considerations

General layout and supply bypassing play a major role in analog performance and thermal characteristics. Fairchild offers an evaluation board to guide layout and aid device evaluation. Following this layout configuration provides optimum performance for the device. For best results, follow the steps and recommended routing rules listed below.

### Recommended Routing/Layout Rules

- Do not run analog and digital signals in parallel.
- Traces must run on top of the ground plane.
- Avoid routing at 90° angles.
- Place bypass capacitors within 2.54mm (0.1 inches) of the device power pin.
- Minimize all trace lengths to reduce series inductance.
- Connect BGND, PGND, and AGND together using a single ground plane.

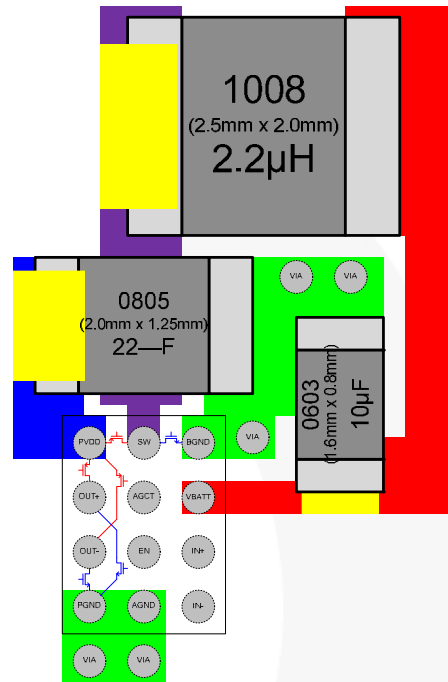


Figure 26. Recommended PCB Layout

Table 1 – Recommended Passive Components

Component	Vendor	Part Number	Value
L <sub>SW</sub>	Murata	LQM2HPN2R2NJCL	2.2µH
C <sub>PVDD</sub>	Murata	GRM21AR60J226UE80K	22µF
C <sub>VBATT</sub>	Murata	GRM188R60J106UE82J	10µF

### Physical Dimensions

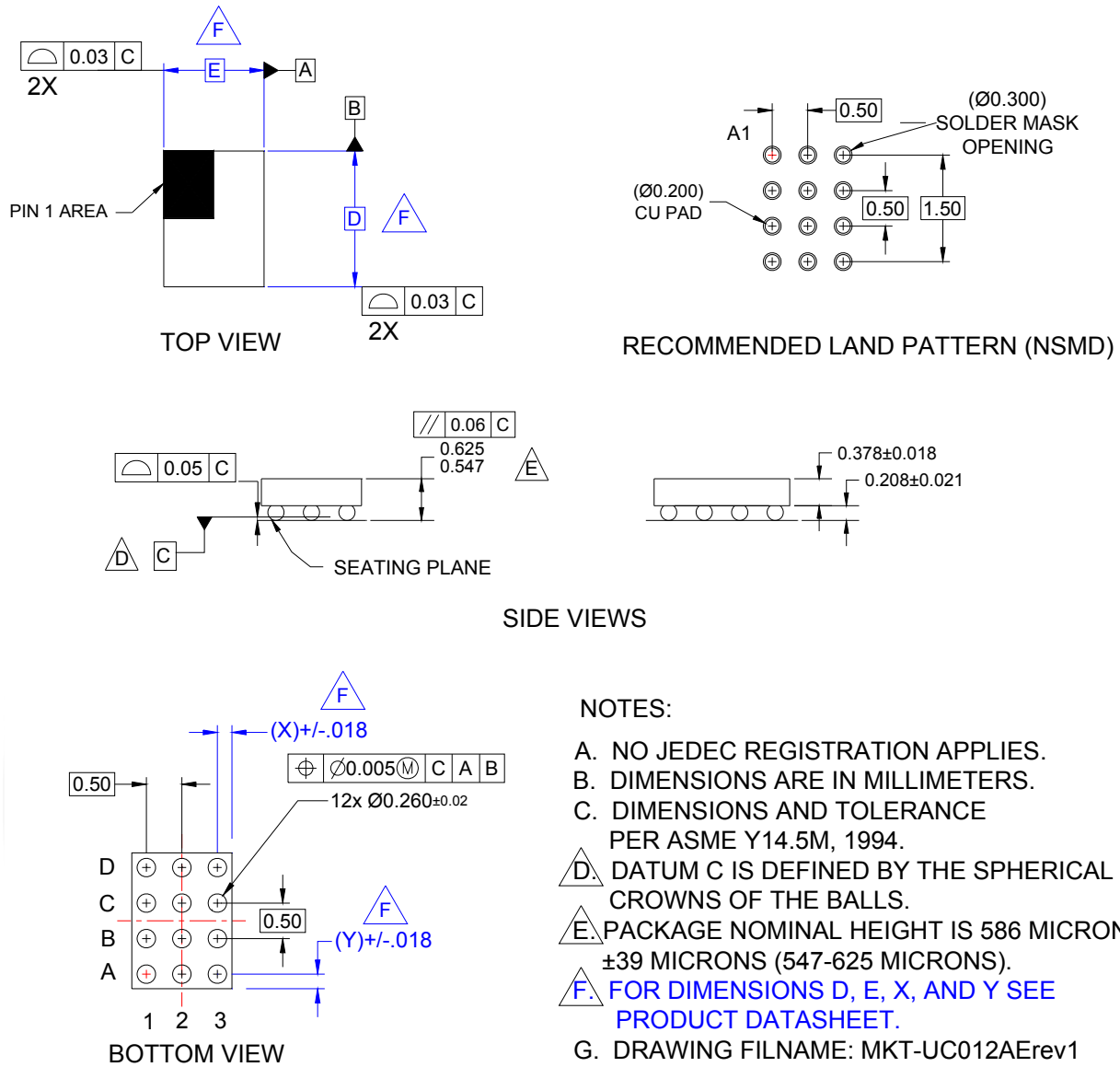


Figure 27. 12-Ball WLCSP, 3x4 Array, 0.5mm Pitch, 250µm Ball

### Product Dimensions

Product	D	E	X	Y
FAB3102UCX	1.86mm	1.44mm	0.22mm	0.18mm




Package drawings are provided as a service to customers considering Fairchild components. Drawings may change in any manner without notice. Please note the revision and/or date on the drawing and contact a Fairchild Semiconductor representative to verify or obtain the most recent version. Package specifications do not expand Fairchild's worldwide terms and conditions, specifically the warranty therein, which covers Fairchild products.

Always visit Fairchild Semiconductors online packaging area for the most recent packaging drawings and tape and reel specifications. <http://www.fairchildsemi.com/packaging/>.



**TRADEMARKS**

The following includes registered and unregistered trademarks and service marks, owned by Fairchild Semiconductor and/or its global subsidiaries, and is not intended to be an exhaustive list of all such trademarks.

- |   |  |   |   |
|---|--|---|---|
| 2Cool™  | FPS™   | PDP SPM™  | The Power Franchise®  |
| AccuPower™  | F-PFS™   | Power-SPM™  | <b>the power franchise</b>  |
| Auto-SPM™   | FRFET®   | PowerTrench®  | TinyBoost™  |
| AX-CAP™*  | Global Power Resource™                         | PowerXS™  | TinyBuck™   |
| BitSiC®   | Green FPS™                                     | Programmable Active Droop™  | TinyCalc™   |
| Build it Now™   | Green FPST™ e-Series™                          | QFET®   | TinyLogic®  |
| CorePLUS™   | Gmax™  | QS™   | TINYOPTO™   |
| CorePOWER™  | GTO™   | Quiet Series™   | TinyPower™  |
| CROSSVOLT™  | IntelliMAX™                                    | RapidConfigure™   | TinyPWM™  |
| CTL™  | ISOPLANAR™                                     |  ™ | TinyWire™   |
| Current Transfer Logic™   | Making Small Speakers Sound Louder and Better™ | Saving our world, 1mW/W/kW at a time™   | TranSiC®  |
| DEUXPEED®   | MegaBuck™                                      | SignalWise™   | TriFault Detect™  |
| Dual Cool™  | MICROCOUPLER™                                  | SmartMax™   | TRUECURRENT®*   |
| EcoSPARK®   | MicroFET™                                      | SMART START™  | μSerDes™  |
| EfficientMax™   | MicroPak™                                      | SPM®  |  ™ |
| ESBCT™  | MicroPak2™                                     | STEALTH™  | UHC®  |
|  ™ | MillerDrive™                                   | SuperFET®   | Ultra FRFET™  |
| Fairchild®  | MotionMax™                                     | SuperSOT™-3   | UniFET™   |
| Fairchild Semiconductor®  | Motion-SPM™                                    | SuperSOT™-6   | VCX™  |
| FACT Quiet Series™  | mWSaver™                                       | SuperSOT™-8   | VisualMax™  |
| FACT®   | OptoHiT™                                       | SupreMOS®   | VoltagePlus™  |
| FAST®   | OPTOLOGIC®                                     | SyncFET™  | XS™   |
| FastvCore™  | OPTOPLANAR®                                    | Sync-Lock™  |   |
| FETBench™   |  |  ™ |   |
| FlashWriter®*   |  |   |   |

\* Trademarks of System General Corporation, used under license by Fairchild Semiconductor.

**DISCLAIMER**

FAIRCHILD SEMICONDUCTOR RESERVES THE RIGHT TO MAKE CHANGES WITHOUT FURTHER NOTICE TO ANY PRODUCTS HEREIN TO IMPROVE RELIABILITY, FUNCTION, OR DESIGN. FAIRCHILD DOES NOT ASSUME ANY LIABILITY ARISING OUT OF THE APPLICATION OR USE OF ANY PRODUCT OR CIRCUIT DESCRIBED HEREIN; NEITHER DOES IT CONVEY ANY LICENSE UNDER ITS PATENT RIGHTS, NOR THE RIGHTS OF OTHERS. THESE SPECIFICATIONS DO NOT EXPAND THE TERMS OF FAIRCHILD'S WORLDWIDE TERMS AND CONDITIONS, SPECIFICALLY THE WARRANTY THEREIN, WHICH COVERS THESE PRODUCTS.

**LIFE SUPPORT POLICY**

FAIRCHILD'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF FAIRCHILD SEMICONDUCTOR CORPORATION.

As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body or (b) support or sustain life, and (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury of the user.
2. A critical component in any component of a life support, device, or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

**ANTI-COUNTERFEITING POLICY**

Fairchild Semiconductor Corporation's Anti-Counterfeiting Policy. Fairchild's Anti-Counterfeiting Policy is also stated on our external website, [www.fairchildsemi.com](http://www.fairchildsemi.com), under Sales Support.

Counterfeiting of semiconductor parts is a growing problem in the industry. All manufacturers of semiconductor products are experiencing counterfeiting of their parts. Customers who inadvertently purchase counterfeit parts experience many problems such as loss of brand reputation, substandard performance, failed applications, and increased cost of production and manufacturing delays. Fairchild is taking strong measures to protect ourselves and our customers from the proliferation of counterfeit parts. Fairchild strongly encourages customers to purchase Fairchild parts either directly from Fairchild or from Authorized Fairchild Distributors who are listed by country on our web page cited above. Products customers buy either from Fairchild directly or from Authorized Fairchild Distributors are genuine parts, have full traceability, meet Fairchild's quality standards for handling and storage and provide access to Fairchild's full range of up-to-date technical and product information. Fairchild and our Authorized Distributors will stand behind all warranties and will appropriately address any warranty issues that may arise. Fairchild will not provide any warranty coverage or other assistance for parts bought from Unauthorized Sources. Fairchild is committed to combat this global problem and encourage our customers to do their part in stopping this practice by buying direct or from authorized distributors.

**PRODUCT STATUS DEFINITIONS**

**Definition of Terms**

Datasheet Identification	Product Status	Definition
Advance Information	Formative / In Design	Datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
Obsolete	Not In Production	Datasheet contains specifications on a product that is discontinued by Fairchild Semiconductor. The datasheet is for reference information only.

Rev. I57