

Level Translating I2C-Bus/SMBus Repeater with Tiny Package

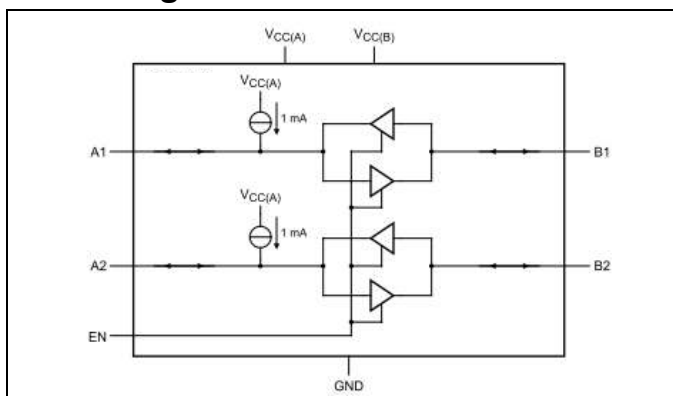
Features

- ➔ Bidirectional buffer isolates capacitance and allows 400 pF on port B of the device
- ➔ Port A operating supply voltage range of 1.1 V to $V_{CC(B)} - 1.0V$
- ➔ Port B operating supply voltage range of 2.5 V to 5.5 V
- ➔ Voltage level translation from 1.1V to $V_{CC(B)} - 1.0V$ and from 2.5 V to 5.5 V
- ➔ Requires no external pull-up resistors on lower voltage port A
- ➔ Open-drain port B inputs/outputs
- ➔ Lock-up free operation
- ➔ Supports arbitration and clock stretching across the repeater
- ➔ Accommodates Standard-mode and Fast-mode I²C-bus devices and multiple masters
- ➔ Powered-off high-impedance I²C-bus pins
- ➔ 5 V tolerant B SCL, SDA and enable pins
- ➔ 0 Hz to 400 kHz clock frequency (Remark: The maximum system operating frequency may be less than 400 kHz because of the delays added by the repeater.)
- ➔ ESD protection exceeds 8KV HBM per JESD22-A114
- ➔ Totally Lead-Free & Fully RoHS Compliant (Notes 1 & 2)
- ➔ Halogen and Antimony Free. “Green” Device (Note 3)
- ➔ For automotive applications requiring specific change control (i.e. parts qualified to AEC-Q100/101/200, PPAP capable, and manufactured in IATF 16949 certified facilities), please [contact us](mailto:contact_us) or your local Diodes representative.

<https://www.diodes.com/quality/product-definitions/>

- ➔ Package: MSOP-8

Block Diagram



Notes:
 1. No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
 2. See <https://www.diodes.com/quality/lead-free/> for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
 3. Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.

Description

The PI6ULS5V9509 is a level translating I²C-bus/SMBus repeater. It can provide bidirectional level translation between low voltage (down to 1.1V) and higher voltage (2.5V to 5.5V) in mixed-mode applications. And it enables I²C and similar bus system to be extended, without degradation of performance even during level shifting.

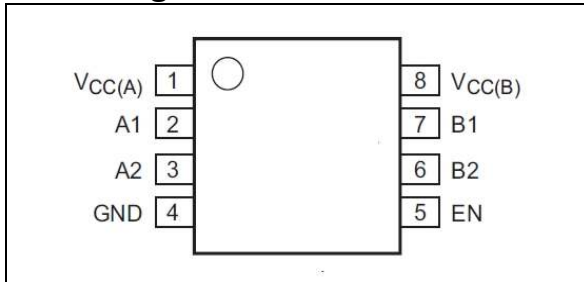
The PI6ULS5V9509 enables the system designer to isolate two halves of a bus for both voltage and capacitance, accommodating more I²C devices or longer trace length. It also permits extension of the I²C-bus by providing bidirectional buffering for both the data (SDA) and the clock (SCL) lines, thus allowing two buses of 400 pF to be connected in an I²C application.

The bus port B drivers are compliant with SMBus I/O levels, while port A uses a current sensing mechanism to detect the input or output LOW signal which prevents bus lock-up. Port A uses a 1 mA current source for pull-up and a 200Ω pull-down driver. This result in a LOW on the port A accommodating smaller voltage swings. The output pull-down on the port A internal buffer LOW is set for approximately 0.2V, while the input threshold of the internal buffer is set about 50 mV lower than that of the output voltage LOW. When the port A I/O is driven LOW internally, the LOW is not recognized as a LOW by the input. This prevents a lock-up condition from occurring. The output pull-down on the port B drives a hard LOW and the input level is set at 0.3 of SMBus or I²C-bus voltage level which enables port B to connect to any other I²C-bus devices or buffer.

The PI6ULS5V9509 drivers are not enabled unless $V_{CC(A)}$ is above 0.8 V and $V_{CC(B)}$ is above 2.5 V. The enable (EN) pin can also be used to turn the drivers on and off under system control. Caution should be observed to only change the state of the EN pin when the bus is idle.

EN	Function
H	A1 = B1; A2 = B2;
L	disabled

Pin Configuration



Pin Description

Pin No	Pin Name	Description
1	V _{CC(A)}	port A supply voltage
2	A1	port A (lower voltage side)
3	A2	port A (lower voltage side)
4	GND	supply ground (0 V)
5	EN	active HIGH repeater enable input
6	B2	port B (SMBus/I ² C-bus side)
7	B1	port B (SMBus/I ² C-bus side)
8	V _{CC(B)}	port B supply voltage

Maximum Ratings

Storage Temperature	-55°C to +125°C
Supply Voltage port B.....	-0.5V to +6.0V
Supply Voltage port A	-0.5V to +6.0V
DC Input Voltage	-0.5V to +6.0V
Control Input Voltage(EN).....	-0.5V to +6.0V
Total Power Dissipation.....	100mA
Input/Output Current (portA&B).....	20mA
Input Current (EN, V _{CC(A)} , V _{CC(B)} , GND).....	20mA
ESD: HBM Mode.....	8000V

Note:

Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended Operation Conditions

GND = 0 V; T_{amb} = -40 °C to +85 °C; unless otherwise specified

Symbol	Parameter	Test Conditions	Min	Typ ^[1]	Max	Unit
V _{CC(B)}	supply voltage port B	-	2.5	-	5.5	V
V _{CC(A)}	supply voltage port A	-	1.1	-	V _{CC(B)} - 1.0	V
I _{CC(A)}	supply current on pin V _{CC(A)}	all port A static HIGH	0.25	0.45	0.9	mA
		all port A static LOW	1.25	3.0	5	
I _{CC(B)}	supply current on pin V _{CC(B)}	all port B static HIGH	0.5	0.9	1.1	mA

Note:

[1] Typical values with V_{CC(A)} = 1.1 V, V_{CC(B)} = 5 V.

DC Electrical Characteristics

 GND = 0 V; T_{amb} = -40 °C to +85 °C; unless otherwise specified

Parameter	Description	Test Conditions	Min	Typ ^[1]	Max	Unit
Input and output of port A (A1&A2)						
V _{IH}	HIGH-level input voltage	-	0.7V _{CC(A)}	-	V _{CC(A)}	V
V _{IL} ^[2]	LOW-level input voltage	-	-0.5	-	+0.3	
V _{ILc}	contention LOW-level input voltage	-	-0.5	+0.15	-	V
V _{IK}	input clamping voltage	I _I = -18 mA	-1.5	-	-0.5	V
I _{LI}	input leakage current	V _I = V _{CC(A)}	-	-	±1	μA
I _{IL}	LOW-level input current	SDA, SCL; V _I = 0.2 V	-1.5	-1.0	-0.45	mA
V _{OL}	LOW-level output voltage	V _{CC(A)} = 0.95 V to 1.2V	-	0.18	0.25	V
		V _{CC(A)} = > 1.2V to (V _{CC(B)} - 1 V)	-	0.2	0.3	
V _{OL} -V _{ILc}	difference between LOW-level output and LOW-level input voltage contention	guaranteed by design	-	50	-	mV
I _{LOH}	HIGH-level output leakage current	V _O = V _{CC(A)}	-	-	10	μA
C _{io}	input/output capacitance	-	-	6	-	pF
Input and output of port B (B1&B2)						
V _{IH}	HIGH-level input voltage	-	0.7V _{CC(B)}	-	V _{CC(B)}	V
V _{IL}	LOW-level input voltage	-	-0.5	-	+0.3 V _{CC(B)}	
V _{IK}	input clamping voltage	I _I = -18 mA	-1.5	-	-0.5	V
I _{LI}	input leakage current	V _I = 3.6 V	-1	-	1	μA
I _{IL}	LOW-level input current	V _I = 0.2 V	-	-	10	μA
V _{OL}	LOW-level output voltage	I _{OL} = 6 mA	-	0.1	0.2	V
I _{LOH}	HIGH-level output leakage current	V _O = 3.6 V	-	-	10	μA
C _{io}	input/output capacitance	-	-	3	-	pF
Enable						
V _{IH}	HIGH-level input voltage	-	0.9V _{CC(A)}	-	V _{CC(B)}	V
V _{IL}	LOW-level input voltage	-	-0.5	-	+0.1 V _{CC(A)}	V
I _{IL}	LOW-level input current	V _I = 0.2 V, EN; V _{CC} = 3.6 V	-1	-	+1	μA
I _{LI}	input leakage current	V _I = V _{CC}	-1	-	+1	μA
C _i	input capacitance	V _I = 3.0 V or 0V	-	2	-	pF

Note:

1. Typical values with V_{CC(A)} = 1.1 V, V_{CC(B)} = 5 V.
2. V_{IL} specification is for the falling edge seen by the port A input. V_{ILc} is for the static LOW levels seen by the port A input resulting in port B output staying LOW.

Dynamic Characteristics
 $V_{CC(A)} = 1.1 \text{ V}; V_{CC(B)} = 3.3 \text{ V}^{[1]}$

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
t_{PLH}	LOW-to-HIGH propagation delay	port B to port A	-	65	216	ns
t_{PHL}	HIGH-to-LOW propagation delay	port B to port A	-	25	140	ns
t_{TLH}	LOW to HIGH output transition time	port A	14	22	96	ns
t_{THL}	HIGH to LOW output transition time	port A	-	20	-	ns
t_{PLH}	LOW to HIGH propagation delay	port A to port B	-	-69	-139	ns
t_{PLH2}	LOW to HIGH propagation delay	port A to port B; measured from the 50 % of initial LOW on port A to 1.5 V rising on port B	-	100	226	ns
t_{PHL}	HIGH to LOW propagation delay	port A to port B	20	50	183	ns
$t_{TLH}^{[2]}$	LOW to HIGH output transition time	port B	-	61	-	ns
t_{THL}	HIGH to LOW output transition time	port B	1	2	40	ns
t_{su}	set-up time	EN HIGH before START condition	100	-	-	ns
t_h	hold time	EN HIGH after STOP condition	100	-	-	ns

 $V_{CC(A)} = 1.9 \text{ V}; V_{CC(B)} = 5.0 \text{ V}^{[1]}$

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
t_{PLH}	LOW-to-HIGH propagation delay	port B to port A	-	75	216	ns
t_{PHL}	HIGH-to-LOW propagation delay	port B to port A	-	20	140	ns
t_{TLH}	LOW to HIGH output transition time	port A	14	27	96	ns
t_{THL}	HIGH to LOW output transition time	port A	-	20	-	ns
t_{PLH}	LOW to HIGH propagation delay	port A to port B	-	-69	-139	ns
t_{PLH2}	LOW to HIGH propagation delay	port A to port B; measured from the 50 % of initial LOW on port A to 1.5 V rising on port B	-	91	226	ns
t_{PHL}	HIGH to LOW propagation delay	port A to port B	20	50	183	ns
$t_{TLH}^{[2]}$	LOW to HIGH output transition time	port B	-	65	-	ns
t_{THL}	HIGH to LOW output transition time	port B	1	2	40	ns
t_{su}	set-up time	EN HIGH before START condition	100	-	-	ns
t_h	hold time	EN HIGH after STOP condition	100	-	-	ns

Note:

[1] Load capacitance = 50 pF; load resistance on port B = 1.35 k

[2] Value is determined by RC time constant of bus line

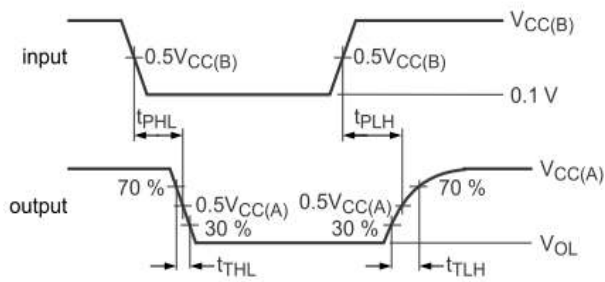


Figure 2: Propagation Delay and Transition Times B→A

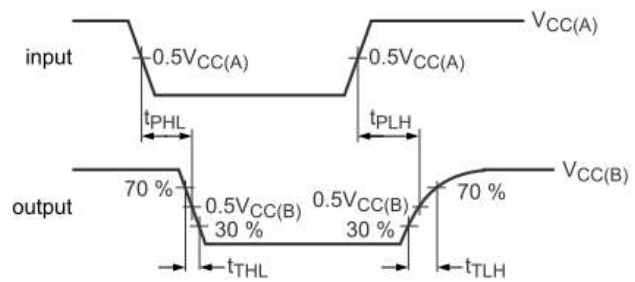


Figure 3: Propagation Delay and Transition Times A→B

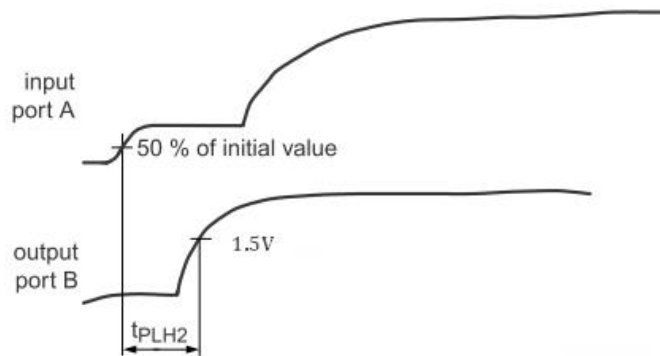
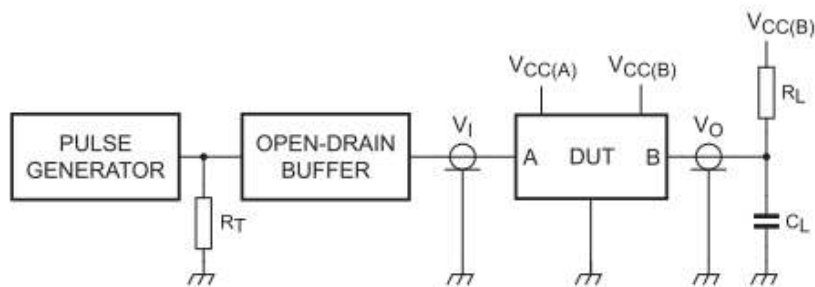


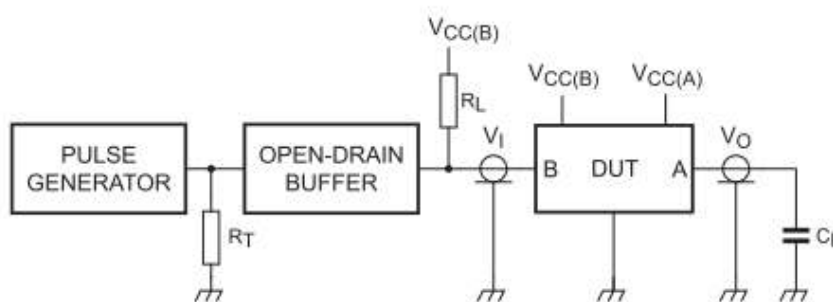
Figure 4: Propagation delay from the port A's external driver switching off to port B LOW-to-HIGH transition; (A→B)



R_L = load resistor; 1.35 k Ω on port B

C_L = load capacitance includes jig and probe capacitance; 50 pF

R_T = termination resistance should be equal to Z_o of pulse generators



R_L = load resistor; 1.35 k Ω on port B

C_L = load capacitance includes jig and probe capacitance; 50 pF

R_T = termination resistance should be equal to Z_o of pulse generators

Figure 5: Test Circuit

Functional Description

The PI6ULS5V9509 is a level translating I²C-bus/SMBus repeater. It can provide bidirectional level translation between low voltage (down to 1.1V) and higher voltage (2.5V to 5.5V) in mixed-mode applications. And it enables I²C and similar bus system to be extended, without degradation of performance even during level shifting.

The PI6ULS5V9509 enables the system designer to isolate two halves of a bus for both voltage and capacitance, accommodating more I²C devices or longer trace length. It also permits extension of the I²C-bus by providing bidirectional buffering for both the data (SDA) and the clock (SCL) lines, thus allowing two buses of 400 pF to be connected in an I²C application.

The bus port B drivers are compliant with SMBus I/O levels, while port A uses a current sensing mechanism to detect the input or output LOW signal which prevents bus lock-up. Port A uses a 1 mA current source for pull-up and a 200 Ω pull-down driver. This result in a LOW on the port A accommodating smaller voltage swings. The output pull-down on the port A internal buffer LOW is set for approximately 0.2 V, while the input threshold of the internal buffer is set about 50 mV lower than that of the output voltage LOW. When the port A I/O is driven LOW internally, the LOW is not recognized as a LOW by the input. This prevents a lock-up condition from occurring. The output pull-down on the port B drives a hard LOW and the input level is set at 0.3 of SMBus or I²C-bus voltage level which enables port B to connect to any other I²C-bus devices or buffer.

The PI6ULS5V9509 drivers are not enabled unless $V_{CC(A)}$ is above 0.8 V and $V_{CC(B)}$ is above 2.5 V. The enable (EN) pin can also be used to turn the drivers on and off under system control. Caution should be observed to only change the state of the EN pin when the bus is idle.

Application Information

A typical application is shown in Figure 6. In this example, the system master is running on a 1.1 V I²C-bus while the slave is connected to a 3.3 V bus. Both buses run at 400 kHz. Master devices can be placed on either bus.

When port B of the PI6ULS5V9509 is pulled LOW by a driver on the I²C-bus, a CMOS hysteresis detects the falling edge when it goes below $0.3V_{CC(B)}$ and causes the internal driver on port A to turn on, causing port A to pull down to about 0.2 V. When port A of the PI6ULS5V9509 falls, first a comparator detects the falling edge and causes the internal driver on port B to turn on and pull the port B pin down to ground. In order to illustrate what would be seen in a typical application, refer to Figure 7 and Figure 8. If the bus master in Figure 6 were to write to the slave through the PI6ULS5V9509, waveforms shown in Figure 7 would be observed on the B bus. This looks like a normal I²C-bus transmission.

On the A bus side of the PI6ULS5V9509, the clock and data lines would have a positive offset from ground equal to the V_{OL} of the PI6ULS5V9509. After the eighth clock pulse, the data line will be pulled to the V_{OL} of the master device, which is very close to ground in this example. At the end of the acknowledge, the level rises only to the LOW level set by the driver in the PI6ULS5V9509 for a short delay while the B bus side rises above $0.5 V_{CC(B)}$, then it continues HIGH. It is important to note that any arbitration or clock stretching events require that the LOW level on the A bus side at the input of the PI6ULS5V9509 (V_{IL}) is below V_{ILC} to be recognized by the PI6ULS5V9509 and then transmitted to the B bus side.

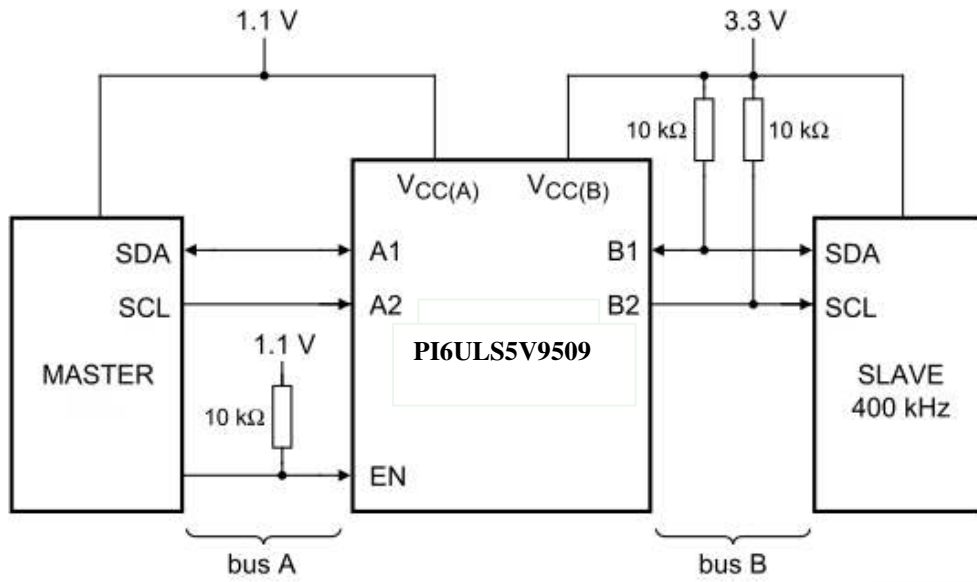


Figure 6: Typical Application

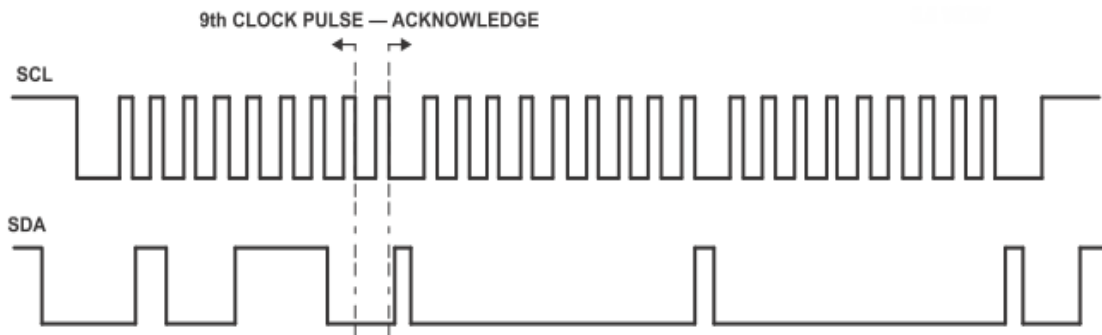


Figure 7: Bus B I²C/SMBus Waveform

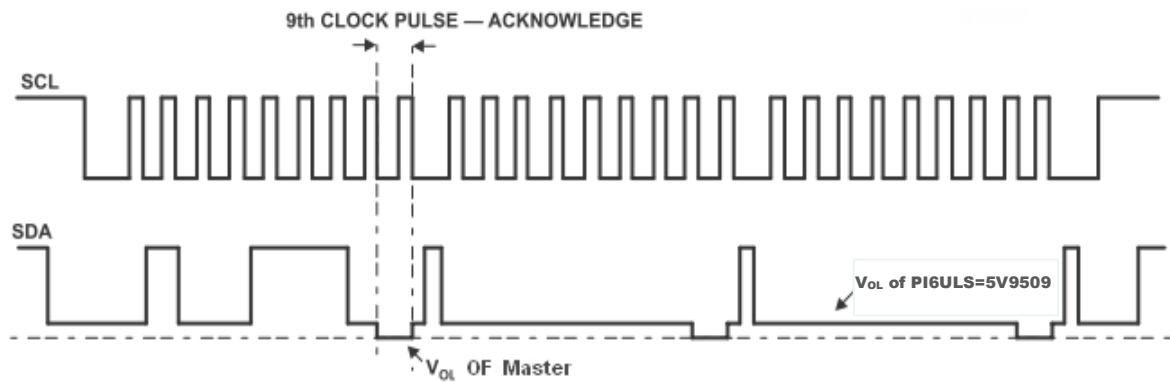


Figure 8: Bus A Lower Voltage Waveform

Part Marking



Y: Date Code (Year)

W: Date Code (Workweek)

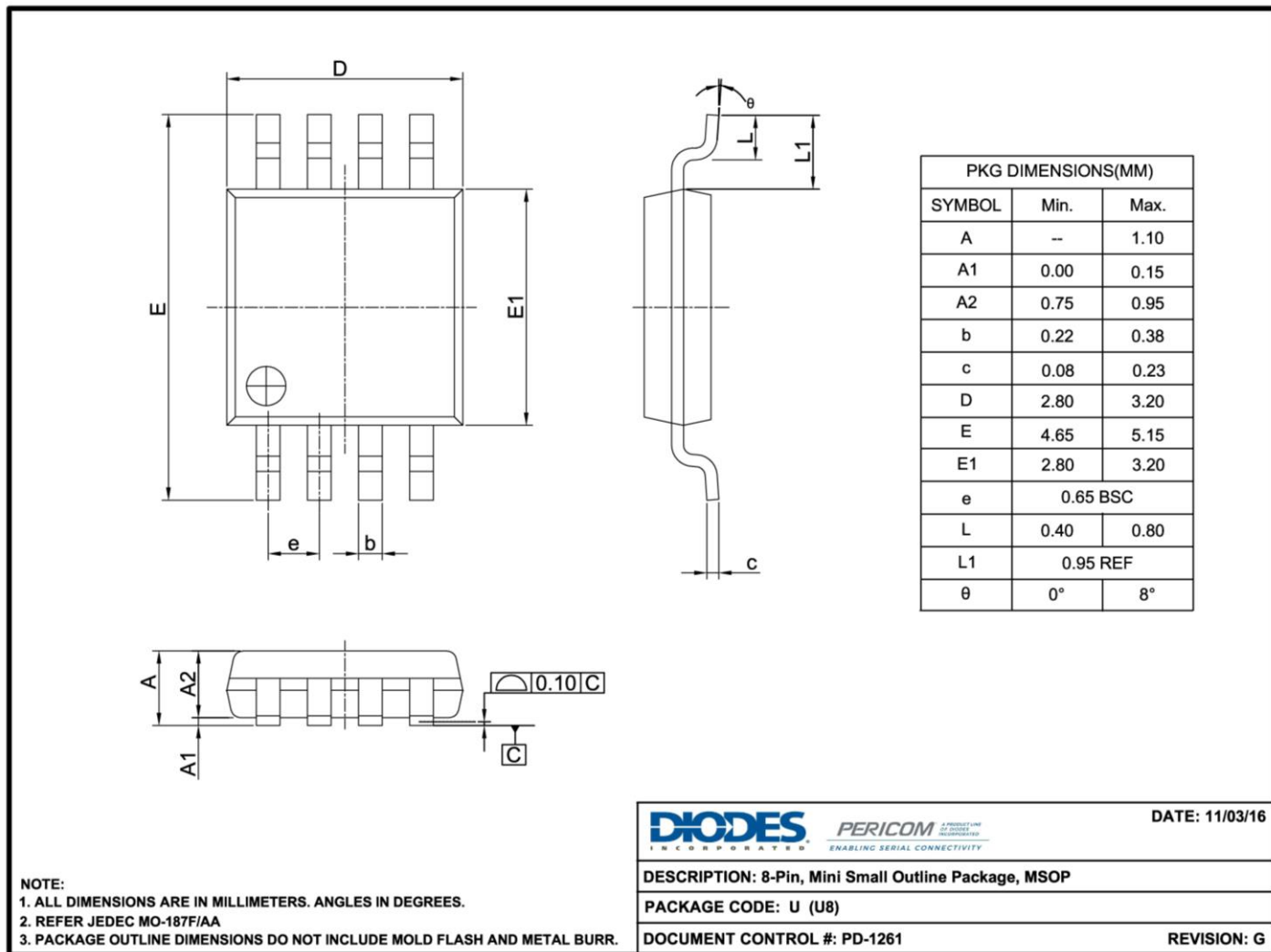
1st X: Assembly Site Code

2nd X: Wafer Fab Site Code

Bar above "L" means Fab3 of MGN

Bar above fab code means Cu wire

Packaging Mechanical
8-MSOP (U)



16-0242

For latest package info.

please check: <http://www.diodes.com/design/support/packaging/pericom-packaging/packaging-mechanicals-and-thermal-characteristics/>

Ordering Information

Part Number	Package Code	Package Description
PI6ULS5V9509UEX	U	8-Pin, Mini Small Outline Package (MSOP)

Notes:

- No purposely added lead. Fully EU Directive 2002/95/EC (RoHS), 2011/65/EU (RoHS 2) & 2015/863/EU (RoHS 3) compliant.
- See <https://www.diodes.com/quality/lead-free/> for more information about Diodes Incorporated's definitions of Halogen- and Antimony-free, "Green" and Lead-free.
- Halogen- and Antimony-free "Green" products are defined as those which contain <900ppm bromine, <900ppm chlorine (<1500ppm total Br + Cl) and <1000ppm antimony compounds.
- E = Pb-free and Green
- X suffix = Tape/Reel

IMPORTANT NOTICE

DIODES INCORPORATED MAKES NO WARRANTY OF ANY KIND, EXPRESS OR IMPLIED, WITH REGARDS TO THIS DOCUMENT, INCLUDING, BUT NOT LIMITED TO, THE IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE (AND THEIR EQUIVALENTS UNDER THE LAWS OF ANY JURISDICTION).

Diodes Incorporated and its subsidiaries reserve the right to make modifications, enhancements, improvements, corrections or other changes without further notice to this document and any product described herein. Diodes Incorporated does not assume any liability arising out of the application or use of this document or any product described herein; neither does Diodes Incorporated convey any license under its patent or trademark rights, nor the rights of others. Any Customer or user of this document or products described herein in such applications shall assume all risks of such use and will agree to hold Diodes Incorporated and all the companies whose products are represented on Diodes Incorporated website, harmless against all damages.

Diodes Incorporated does not warrant or accept any liability whatsoever in respect of any products purchased through unauthorized sales channel.

Should Customers purchase or use Diodes Incorporated products for any unintended or unauthorized application, Customers shall indemnify and hold Diodes Incorporated and its representatives harmless against all claims, damages, expenses, and attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized application.

Products described herein may be covered by one or more United States, international or foreign patents pending. Product names and markings noted herein may also be covered by one or more United States, international or foreign trademarks.

This document is written in English but may be translated into multiple languages for reference. Only the English version of this document is the final and determinative format released by Diodes Incorporated.

LIFE SUPPORT

Diodes Incorporated products are specifically not authorized for use as critical components in life support devices or systems without the express written approval of the Chief Executive Officer of Diodes Incorporated. As used herein:

A. Life support devices or systems are devices or systems which:

1. are intended to implant into the body, or
2. support or sustain life and whose failure to perform when properly used in accordance with instructions for use provided in the labeling can be reasonably expected to result in significant injury to the user.

B. A critical component is any component in a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or to affect its safety or effectiveness.

Customers represent that they have all necessary expertise in the safety and regulatory ramifications of their life support devices or systems, and acknowledge and agree that they are solely responsible for all legal, regulatory and safety-related requirements concerning their products and any use of Diodes Incorporated products in such safety-critical, life support devices or systems, notwithstanding any devices- or systems-related information or support that may be provided by Diodes Incorporated. Further, Customers must fully indemnify Diodes Incorporated and its representatives against any damages arising out of the use of Diodes Incorporated products in such safety-critical, life support devices or systems.

Copyright © 2016, Diodes Incorporated
www.diodes.com