

N-channel 600 V, 1.06 Ω typ., 4.5 A MDmesh™ M2 Power MOSFETs in D²PAK and DPAK packages

Datasheet - production data

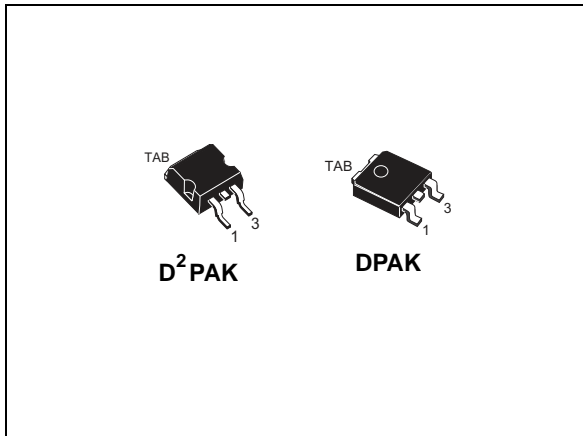
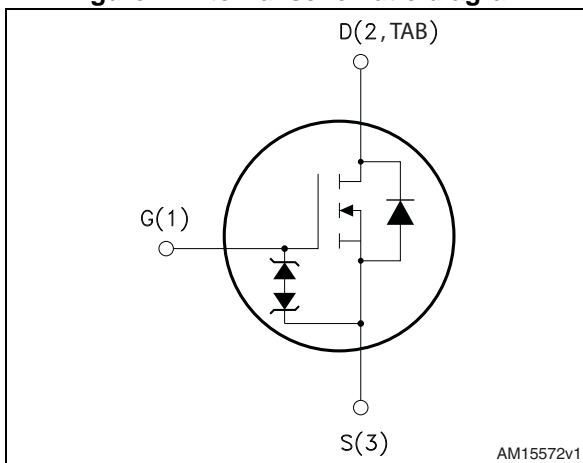


Figure 1. Internal schematic diagram



Features

Order code	$V_{DS} @ T_{Jmax}$	$R_{DS(on) max}$	I_D
STB6N60M2	650 V	1.2 Ω	4.5 A
STD6N60M2			

- Extremely low gate charge
- Excellent output capacitance (C_{oss}) profile
- 100% avalanche tested
- Zener-protected

Applications

- Switching applications

Description

These devices are N-channel Power MOSFETs developed using MDmesh™ M2 technology. Thanks to their strip layout and improved vertical structure, the devices exhibit low on-resistance and optimized switching characteristics, rendering them suitable for the most demanding high efficiency converters.

Table 1. Device summary

Order code	Marking	Package	Packing
STB6N60M2	6N60M2	D ² PAK	Tape and reel
STD6N60M2		DPAK	

Contents

- 1 Electrical ratings 3**
- 2 Electrical characteristics 4**
 - 2.1 Electrical characteristics (curves) 6
- 3 Test circuits 9**
- 4 Package information 10**
 - 4.1 D²PAK(TO-263) package information11
 - 4.2 DPAK(TO-252) package information 14
- 5 Packing information 17**
- 6 Revision history 20**

1 Electrical ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{GS}	Gate-source voltage	± 25	V
I_D	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	4.5	A
I_D	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	2.9	A
$I_{DM}^{(1)}$	Drain current (pulsed)	18	A
P_{TOT}	Total dissipation at $T_C = 25\text{ }^\circ\text{C}$	60	W
$dv/dt^{(2)}$	Peak diode recovery voltage slope	15	V/ns
$dv/dt^{(3)}$	MOSFET dv/dt ruggedness	50	
T_{stg}	Storage temperature range	-55 to 150	$^\circ\text{C}$
T_j	Operating junction temperature range		

1. Pulse width limited by safe operating area
2. $I_{SD} \leq 4.5\text{ A}$, $di/dt \leq 400\text{ A}/\mu\text{s}$; $V_{DS\text{ peak}} < V_{(BR)DSS}$, $V_{DD}=400\text{ V}$
3. $V_{DS} \leq 480\text{ V}$

Table 3. Thermal data

Symbol	Parameter	Value		Unit
		D ² PAK	DPAK	
$R_{thj-case}$	Thermal resistance junction-case max	2.08		$^\circ\text{C}/\text{W}$
$R_{thj-pcb}$	Thermal resistance junction-pcb max ⁽¹⁾	30	50	$^\circ\text{C}/\text{W}$

1. When mounted on 1 inch² FR-4, 2 Oz copper board

Table 4. Avalanche characteristics

Symbol	Parameter	Value	Unit
I_{AR}	Avalanche current, repetitive or not repetitive (pulse width limited by T_{jmax})	1	A
E_{AS}	Single pulse avalanche energy (starting $T_j=25\text{ }^\circ\text{C}$, $I_D=I_{AR}$; $V_{DD}=50\text{ V}$)	86	mJ

2 Electrical characteristics

($T_C = 25\text{ °C}$ unless otherwise specified)

Table 5. On /off states

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 1\text{ mA}$, $V_{GS} = 0$	600			V
I_{DSS}	Zero gate voltage drain current ($V_{GS} = 0$)	$V_{DS} = 600\text{ V}$			1	μA
		$V_{DS} = 600\text{ V}$, $T_C = 125\text{ °C}^{(1)}$			100	μA
I_{GSS}	Gate-body leakage current ($V_{DS} = 0$)	$V_{GS} = \pm 25\text{ V}$			± 10	μA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 250\text{ }\mu\text{A}$	2	3	4	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}$, $I_D = 2.25\text{ A}$		1.06	1.2	Ω

1. Defined by design, not subject to production test

Table 6. Dynamic

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
C_{iss}	Input capacitance	$V_{DS} = 100\text{ V}$, $f = 1\text{ MHz}$, $V_{GS} = 0$	-	232	-	pF
C_{oss}	Output capacitance		-	14	-	pF
C_{riss}	Reverse transfer capacitance		-	0.7	-	pF
$C_{oss\text{ eq.}(1)}$	Equivalent output capacitance	$V_{DS} = 0\text{ to }480\text{ V}$, $V_{GS} = 0$	-	71	-	pF
R_G	Intrinsic gate resistance	$f = 1\text{ MHz}$ open drain	-	6.5	-	Ω
Q_g	Total gate charge	$V_{DD} = 480\text{ V}$, $I_D = 4.5\text{ A}$, $V_{GS} = 10\text{ V}$ (see Figure 16)	-	8.2	-	nC
Q_{gs}	Gate-source charge		-	1.7	-	nC
Q_{gd}	Gate-drain charge		-	4.2	-	nC

1. $C_{oss\text{ eq.}}$ is defined as a constant equivalent capacitance giving the same charging time as C_{oss} when VDS increases from 0 to 80% VDS

Table 7. Switching times

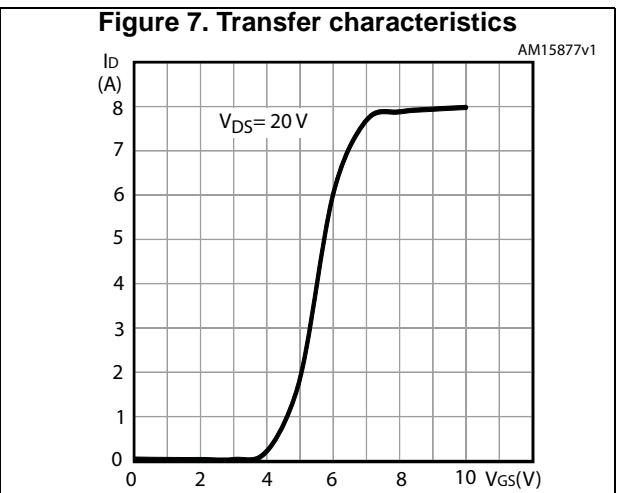
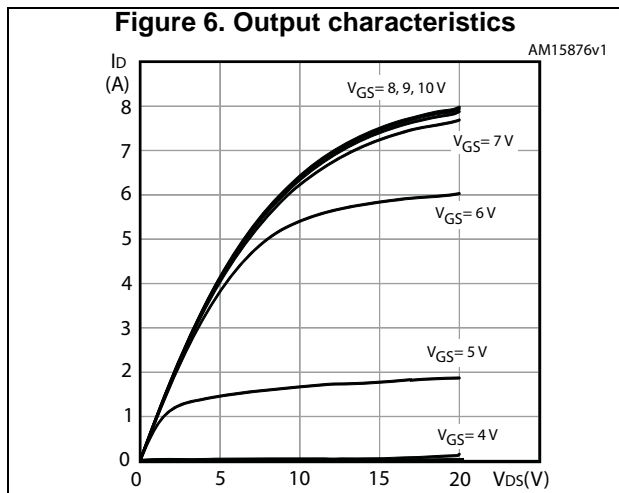
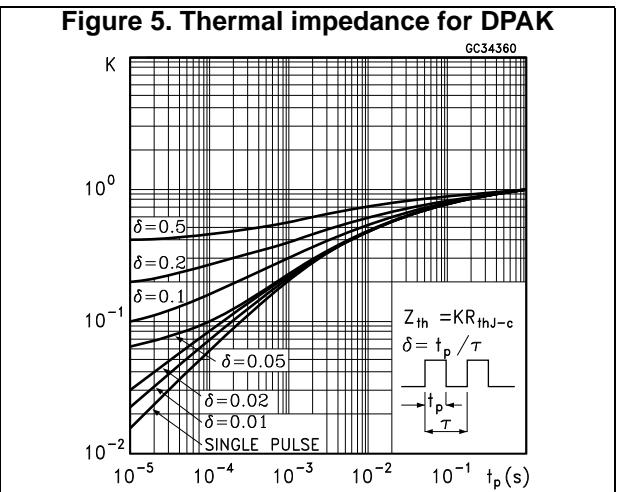
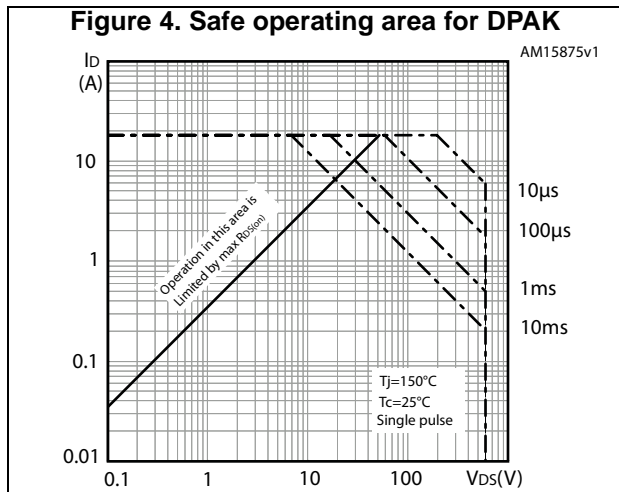
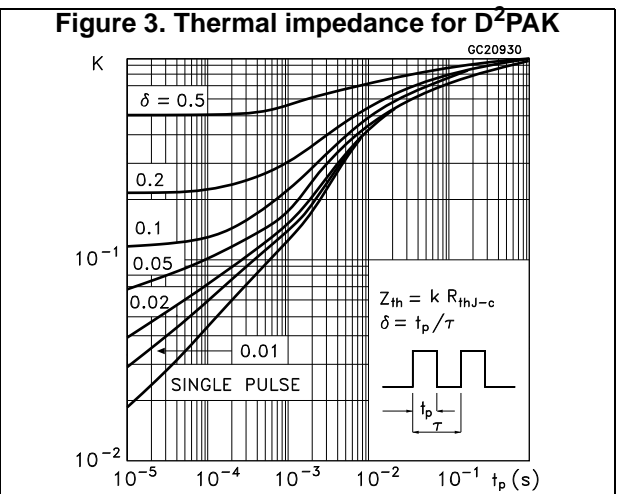
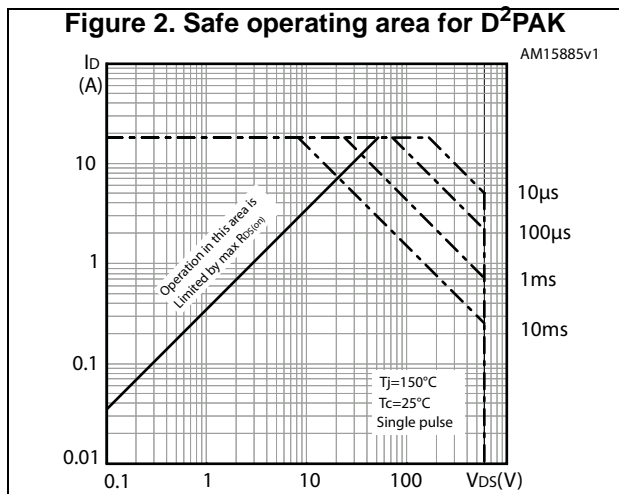
Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 300\text{ V}$, $I_D = 1.65\text{ A}$, $R_G = 4.7\text{ }\Omega$, $V_{GS} = 10\text{ V}$ (see Figure 15 and Figure 20)	-	9.5	-	ns
t_r	Rise time		-	7.4	-	ns
$t_{d(off)}$	Turn-off delay time		-	24	-	ns
t_f	Fall time		-	22.5	-	ns

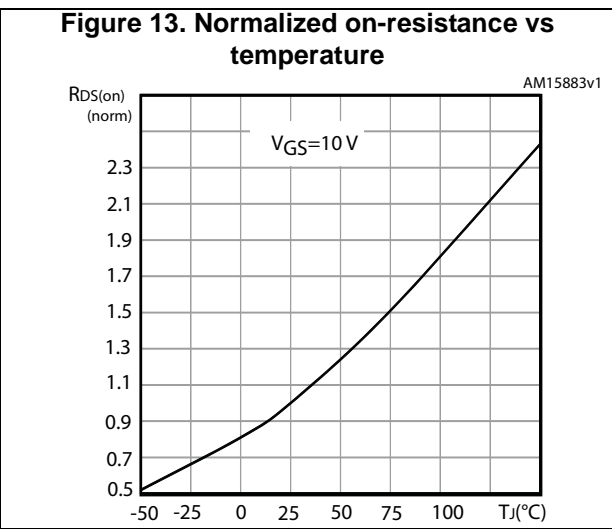
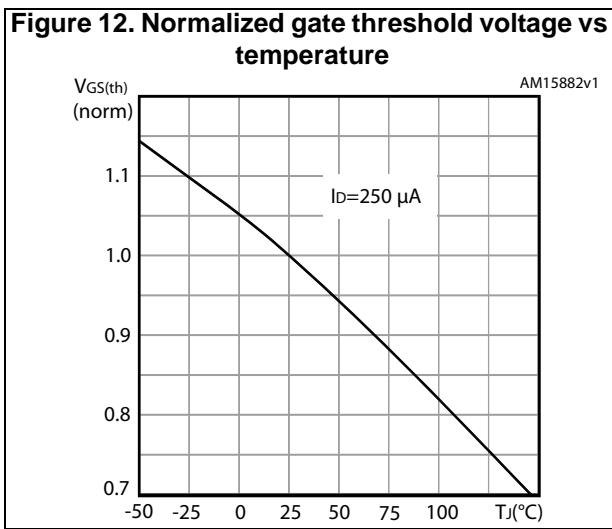
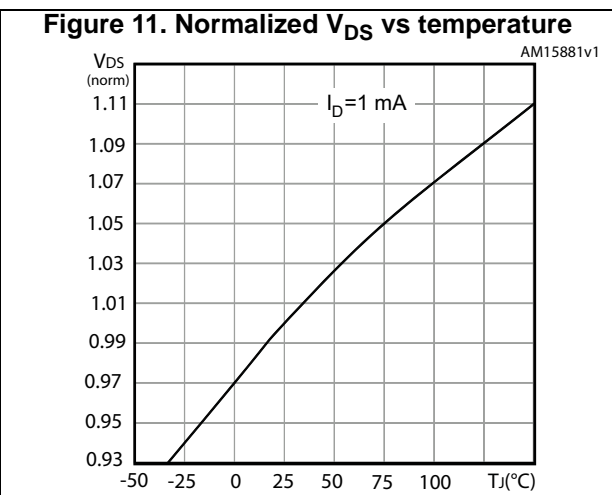
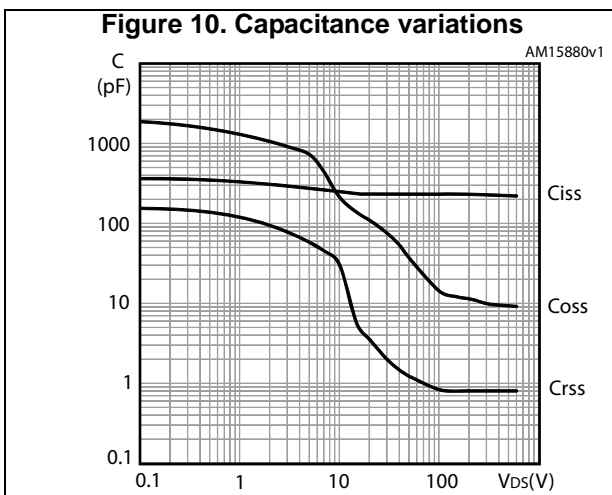
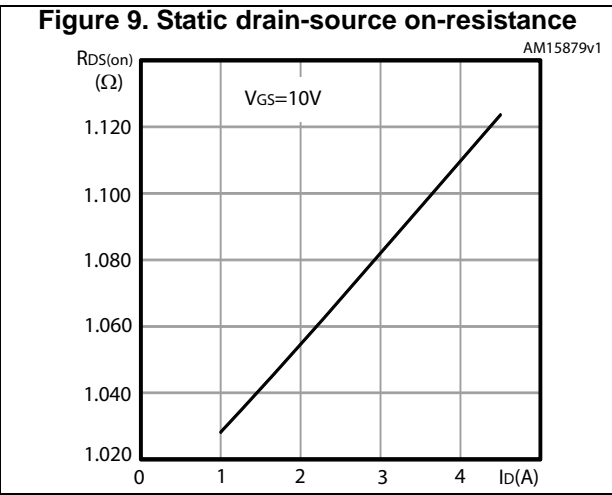
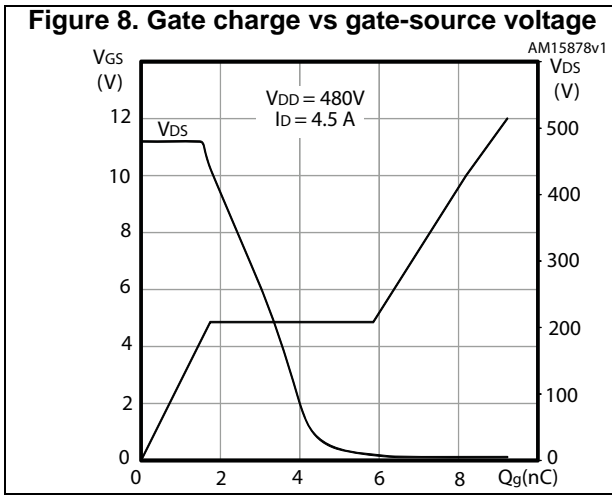
Table 8. Source drain diode

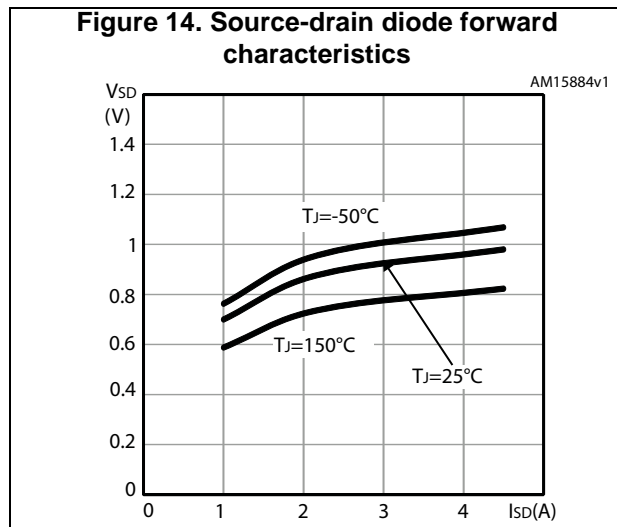
Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{SD}	Source-drain current		-		4.5	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		18	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 4.5 \text{ A}$, $V_{GS} = 0$	-		1.6	V
t_{rr}	Reverse recovery time	$I_{SD} = 4.5 \text{ A}$, $di/dt = 100 \text{ A}/\mu\text{s}$ $V_{DD} = 60 \text{ V}$ (see Figure 17)	-	274		ns
Q_{rr}	Reverse recovery charge		-	1.47		μC
I_{RRM}	Reverse recovery current		-	10.7		A
t_{rr}	Reverse recovery time	$I_{SD} = 4.5 \text{ A}$, $di/dt = 100 \text{ A}/\mu\text{s}$ $V_{DD} = 60 \text{ V}$, $T_j = 150 \text{ }^\circ\text{C}$ (see Figure 17)	-	376		ns
Q_{rr}	Reverse recovery charge		-	1.96		μC
I_{RRM}	Reverse recovery current		-	10.5		A

1. Pulse width limited by safe operating area.
2. Pulsed: pulse duration = 300 μs , duty cycle 1.5%

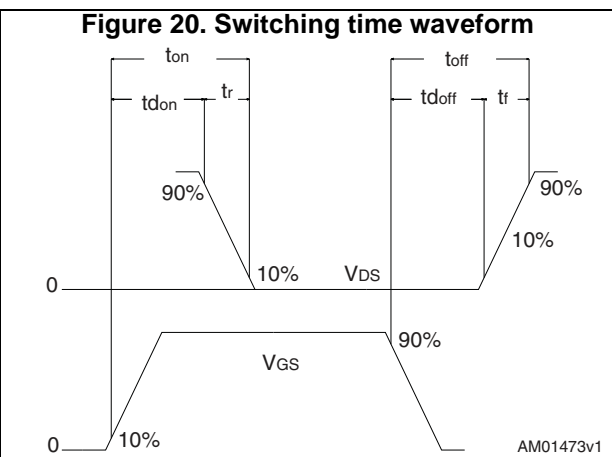
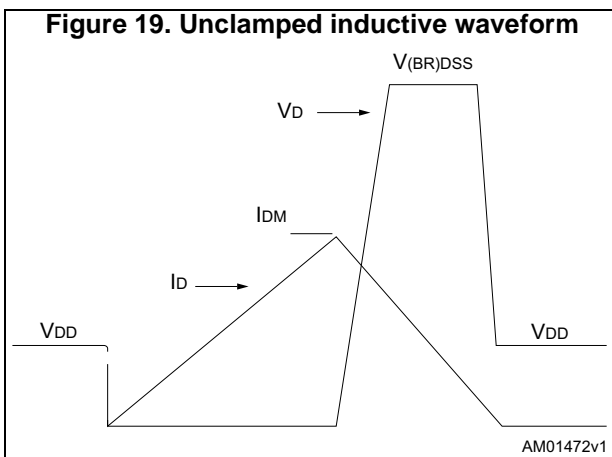
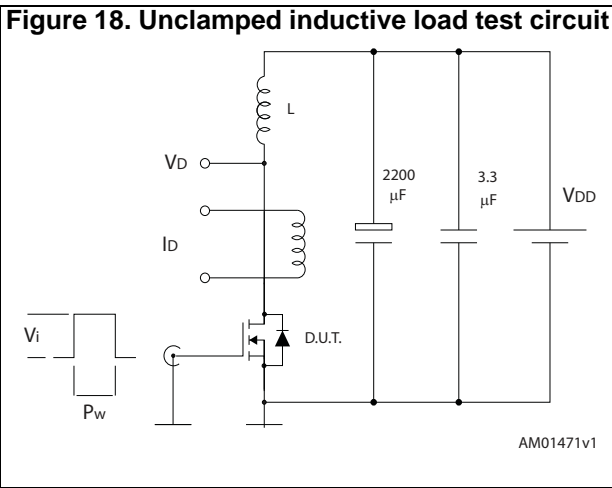
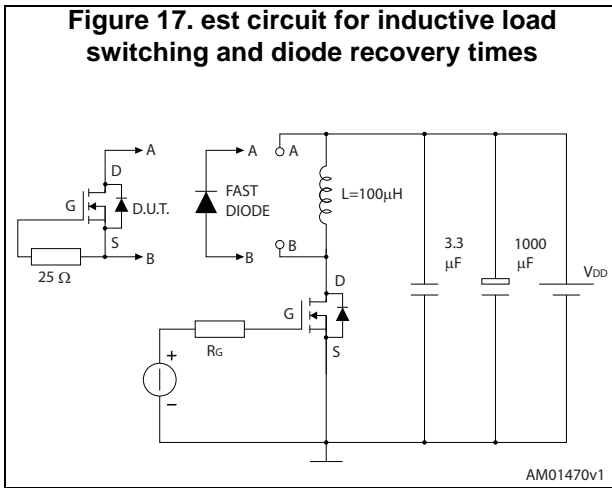
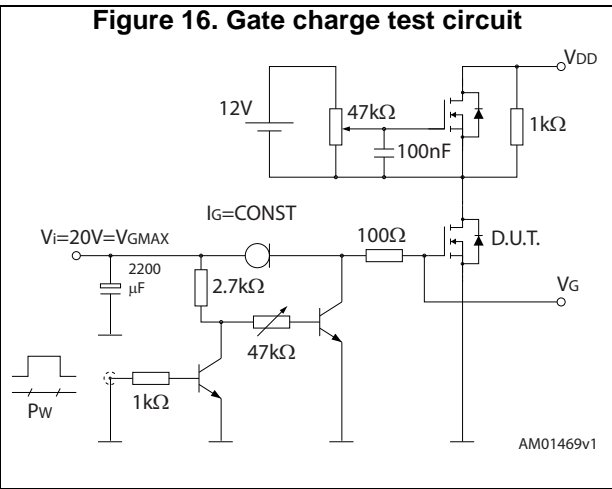
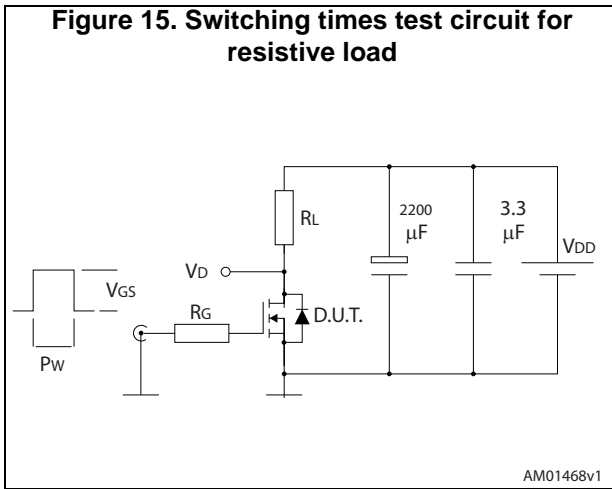
2.1 Electrical characteristics (curves)







3 Test circuits



4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK[®] packages, depending on their level of environmental compliance. ECOPACK[®] specifications, grade definitions and product status are available at: www.st.com. ECOPACK[®] is an ST trademark.

4.1 D²PAK(TO-263) package information

Figure 21. D²PAK (TO-263) type A package outline

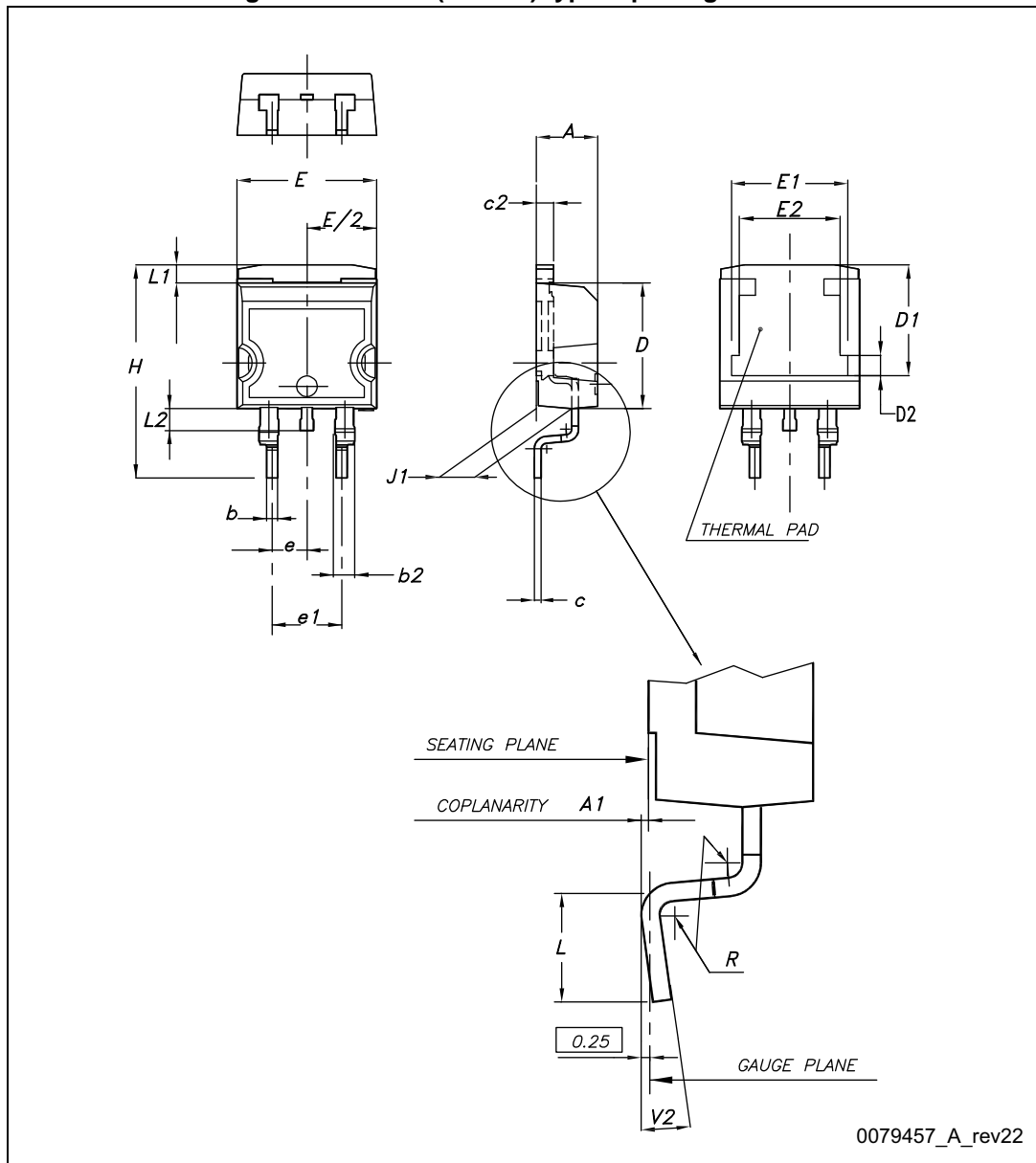
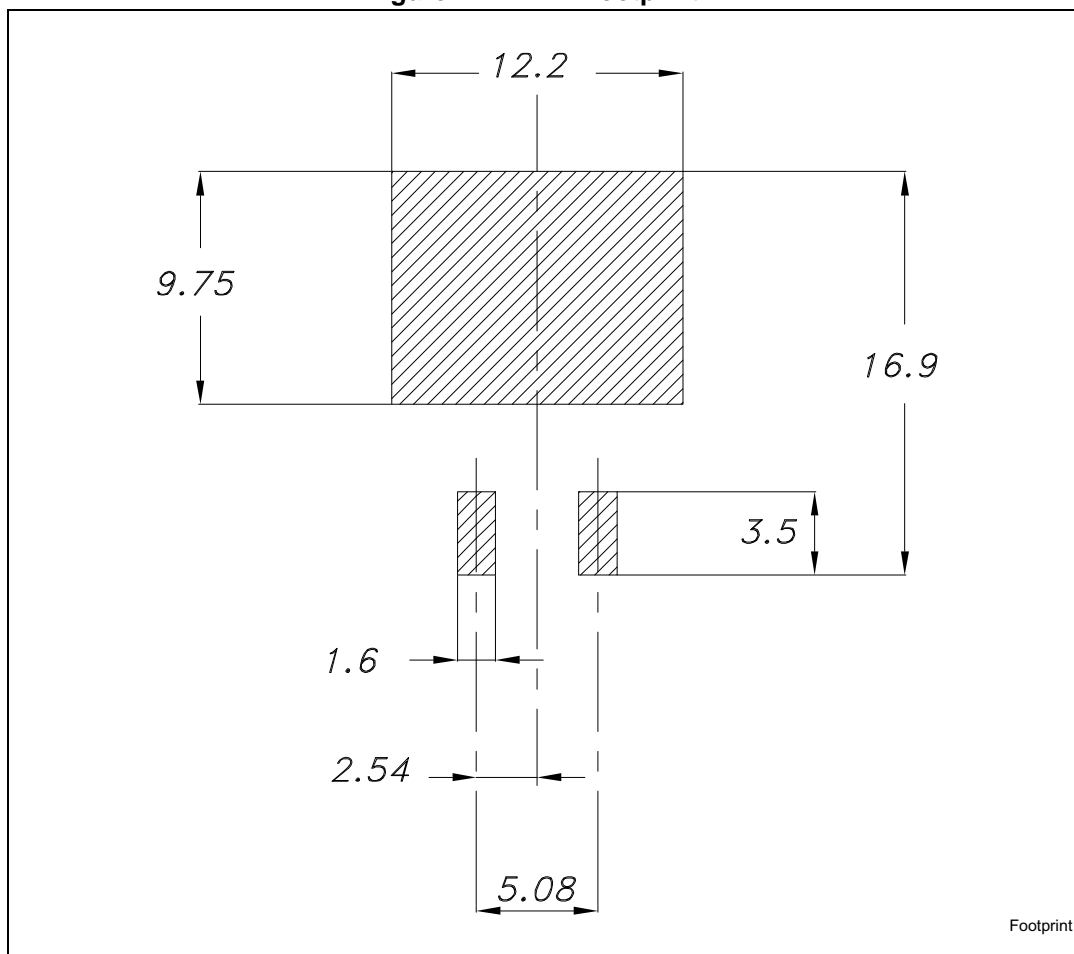


Table 9. D²PAK (TO-263) type A mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
A1	0.03		0.23
b	0.70		0.93
b2	1.14		1.70
c	0.45		0.60
c2	1.23		1.36
D	8.95		9.35
D1	7.50	7.75	8.00
D2	1.10	1.30	1.50
E	10		10.40
E1	8.50	8.70	8.90
E2	6.85	7.05	7.25
e		2.54	
e1	4.88		5.28
H	15		15.85
J1	2.49		2.69
L	2.29		2.79
L1	1.27		1.40
L2	1.30		1.75
R		0.4	
V2	0°		8°

Figure 22. D²PAK footprint^(a)



a. All dimension are in millimeters

4.2 DPAK(TO-252) package information

Figure 23. DPAK (TO-252) type C outline

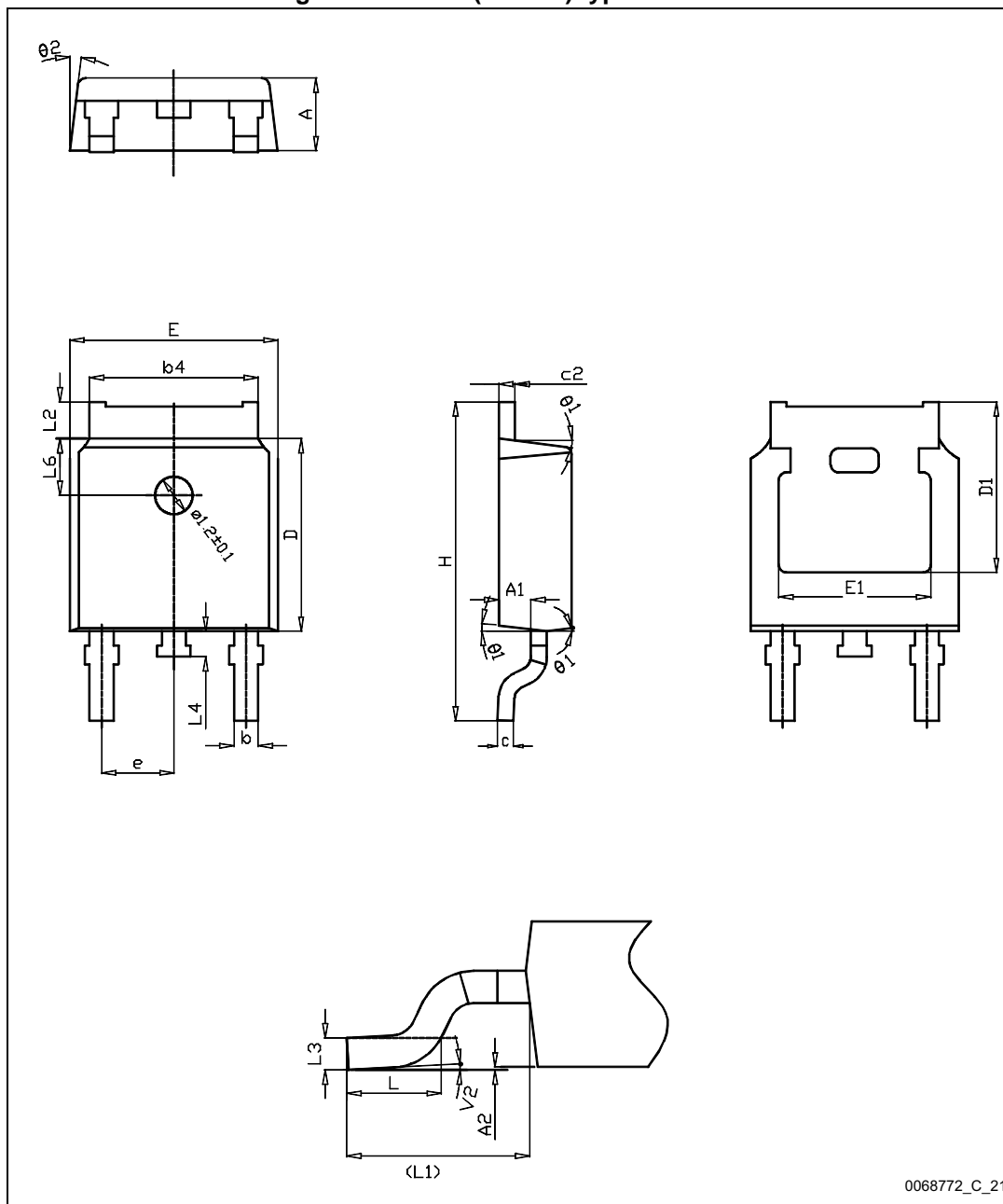
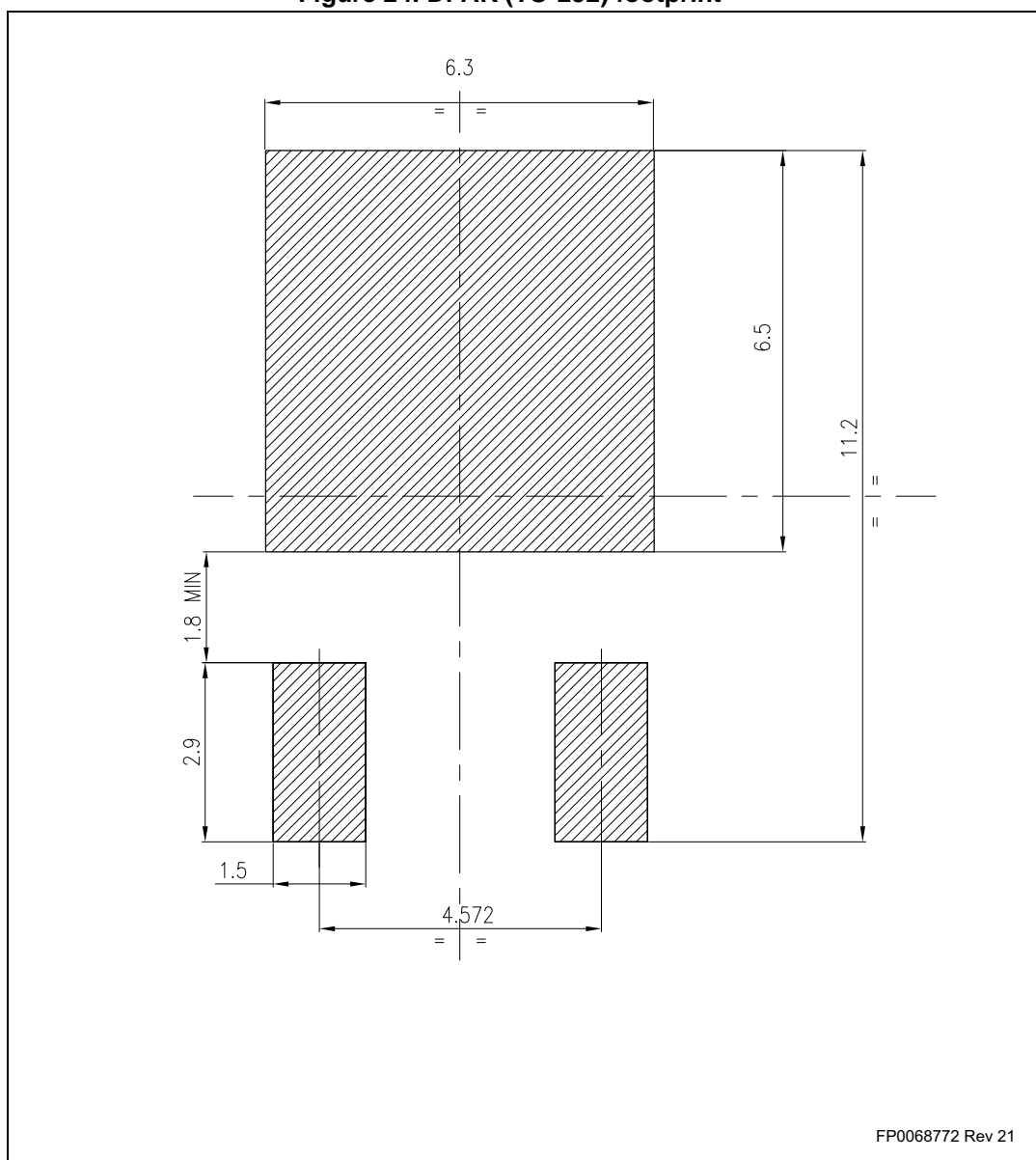


Table 10. DPAK (TO-252) type C package mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	2.20	2.30	2.38
A1	0.90	1.01	1.10
A2	0.00		0.10
b	0.72		0.85
b4	5.13	5.33	5.46
c	0.47		0.60
c2	0.47		0.60
D	6.00	6.10	6.20
D1	5.25		
E	6.50	6.60	6.70
e	2.186	2.286	2.386
E1	4.70		
H	9.80	10.10	10.40
L	1.40	1.50	1.70
L1	2.90 REF		
L2	0.90		1.25
L3	0.51 BSC		
L4	0.60	0.80	1.00
L6	1.80 BSC		
θ1	5°	7°	9°
θ2	5°	7°	9°
V2	0°		8°

Figure 24. DPAK (TO-252) footprint (b)



b. All dimensions are in millimeters

5 Packing information

Table 11. D²PAK (TO-263) tape and reel mechanical data

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	10.5	10.7	A		330
B0	15.7	15.9	B	1.5	
D	1.5	1.6	C	12.8	13.2
D1	1.59	1.61	D	20.2	
E	1.65	1.85	G	24.4	26.4
F	11.4	11.6	N	100	
K0	4.8	5.0	T		30.4
P0	3.9	4.1			
P1	11.9	12.1		Base qty	1000
P2	1.9	2.1		Bulk qty	1000
R	50				
T	0.25	0.35			
W	23.7	24.3			

Table 12. DPAK (TO-252) tape and reel mechanical data

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	6.8	7	A		330
B0	10.4	10.6	B	1.5	
B1		12.1	C	12.8	13.2
D	1.5	1.6	D	20.2	
D1	1.5		G	16.4	18.4
E	1.65	1.85	N	50	
F	7.4	7.6	T		22.4
K0	2.55	2.75			
P0	3.9	4.1	Base qty.		2500
P1	7.9	8.1	Bulk qty.		2500
P2	1.9	2.1			
R	40				
T	0.25	0.35			
W	15.7	16.3			

Figure 25. Tape

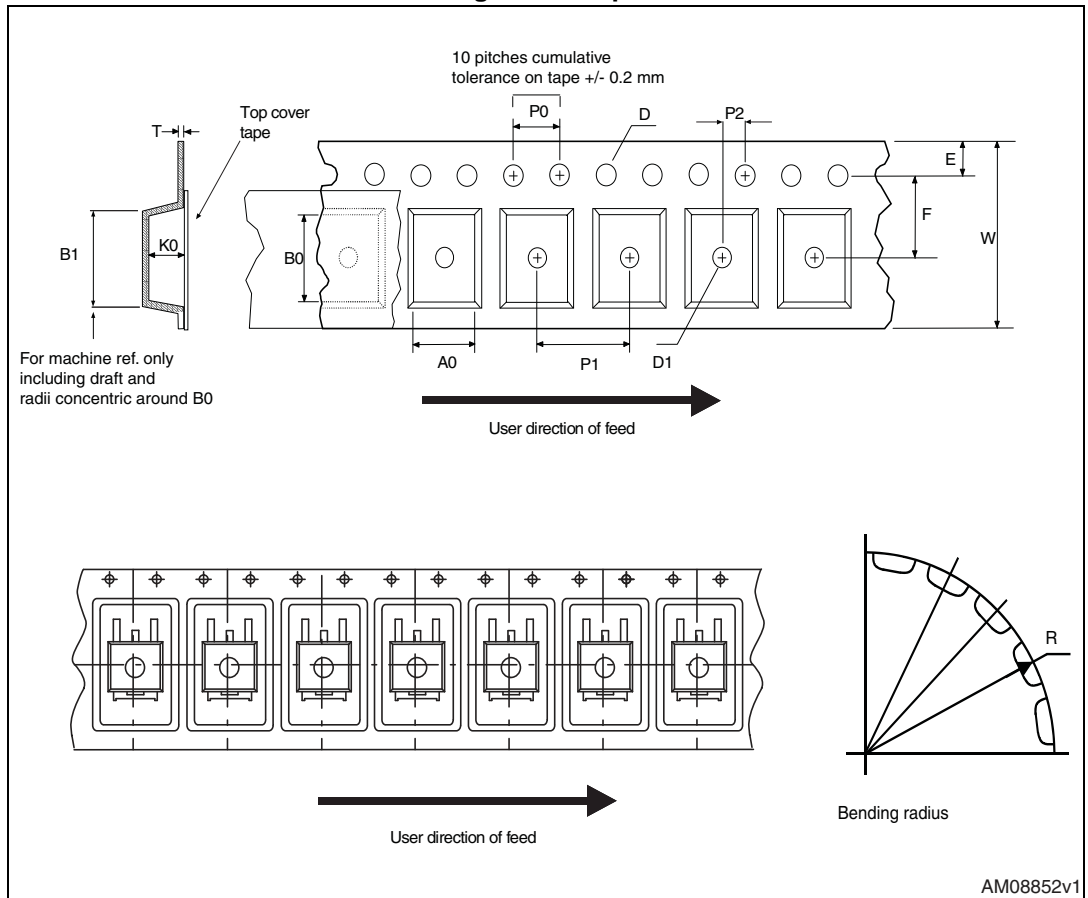
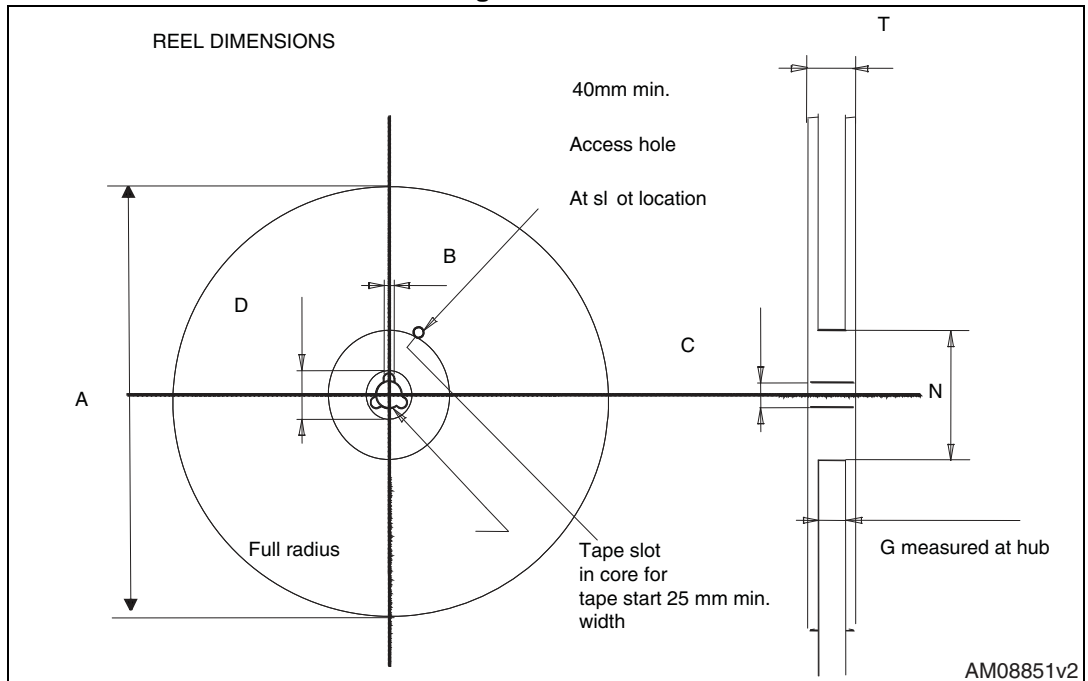


Figure 26. Reel



6 Revision history

Table 13. Document revision history

Date	Revision	Changes
11-Jun-2013	1	First release.
09-Jul-2013	2	– Minor text changes – Modified: $R_{thj-case}$ value for D ² PAK in table 3
30-May-2016	3	Updated title, features and description. Updated Table 6: Dynamic and Table 8: Source drain diode . Updated Section 4: Package information and Section 5: Packing information . Minor text changes.

IMPORTANT NOTICE – PLEASE READ CAREFULLY

STMicroelectronics NV and its subsidiaries ("ST") reserve the right to make changes, corrections, enhancements, modifications, and improvements to ST products and/or to this document at any time without notice. Purchasers should obtain the latest relevant information on ST products before placing orders. ST products are sold pursuant to ST's terms and conditions of sale in place at the time of order acknowledgement.

Purchasers are solely responsible for the choice, selection, and use of ST products and ST assumes no liability for application assistance or the design of Purchasers' products.

No license, express or implied, to any intellectual property right is granted by ST herein.

Resale of ST products with provisions different from the information set forth herein shall void any warranty granted by ST for such product.

ST and the ST logo are trademarks of ST. All other product or service names are the property of their respective owners.

Information in this document supersedes and replaces information previously supplied in any prior versions of this document.

© 2016 STMicroelectronics – All rights reserved