# TPS22950-Q1 Evaluation Module User's Guide



### **ABSTRACT**

This user's guide describes the characteristics, operation, and use of the TPS22950-Q1 adjustable current limited load switch Evaluation Module (EVM). This document contains the complete EVM schematic diagram, printed-circuit board layouts, bill of materials, and necessary instructions on how to operate the EVM.

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### 1 Introduction

The TPS22950-Q1 EVM is a two-layer PCB containing the TPS22950-Q1 load switch device. The VIN and VOUT connections to the device and the PCB layout routing are capable of handling high continuous currents and provide a low-resistance pathway into and out of the device under test. Test point connections allow the EVM user to control the device with user-defined test conditions and make accurate R<sub>ON</sub> measurements.

### 1.1 Description

Table 1-1 lists a short description of the TPS22950-Q1 load switch performance specification. For additional details on load switch performance, application notes, and data sheet, see *Load Switches*.

Table 1-1. TPS22950-Q1 Characteristics

EVM	Device	Rise Time Typical (µs)	V <sub>IN</sub> (V)	Output Current Limit (A)	Enable (ON Pin)	Fault Indication
PSIL224	TPS22950-Q1	Fixed	1.8 V to 5.5 V	Adjustable	Active High	Adjustable

### 1.2 Features

This EVM has the following features:

- V<sub>IN</sub> input voltage range: 1.8 V to 5.5 V
- · Access to the VIN, VOUT, ON, FLT, GND, and ILIM pins of the TPS22950-Q1 load switch
- Onboard CIN and COUT capacitors
- · Adjustable current limiting

www.ti.com Electrical Performance

# **2 Electrical Performance**

For detailed electrical characteristics of the TPS22950-Q1, see the TPS22950-Q1 5-V, 2-A, 40- $m\Omega$  Adjustable Current Limited Load Switch data sheet.

# 3 Schematic

Figure 3-1 illustrates the TPS22950Q1EVM schematic.

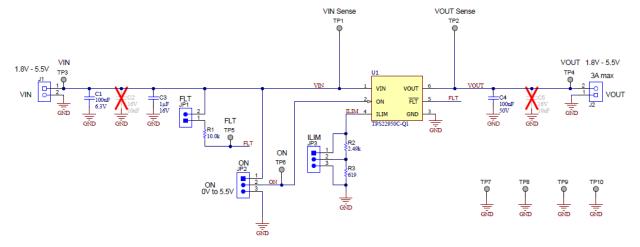


Figure 3-1. TPS22950Q1EVM Schematic



# **4 PCB Layout**

Figure 4-1 and Figure 4-2 show the PCB layout images.

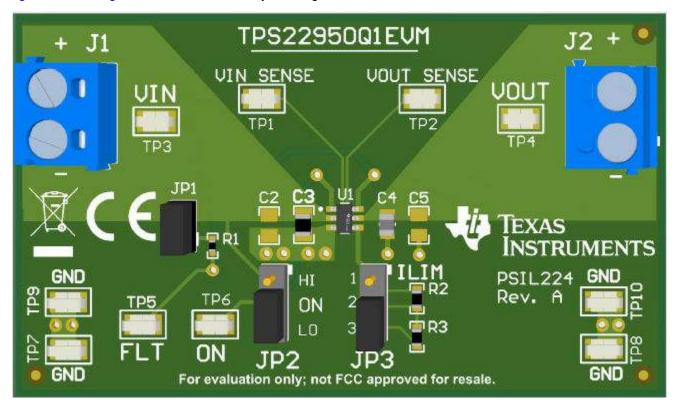


Figure 4-1. TPS22950Q1EVM Top Layout

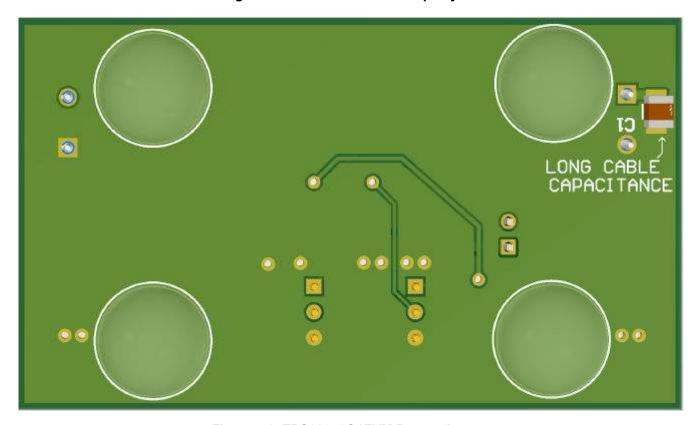


Figure 4-2. TPS22950Q1EVM Bottom Layout

www.ti.com PCB Layout

### 4.1 Setup

This section describes the jumpers and connectors on the EVM as well as how to properly connect, set up and use the EVM. Table 4-1 describes the input and output connectors and jumpers. Table 4-2 describes the different test points and functionality. Table 4-3 describes the jumper functionality and configurations.

Table 4-1. TPS22950Q1EVM Input and Output Connector Functionality

Input	Connector and Test Point	Label	Description		
	J1	+/-	Input block header for VIN		
VIN	TP1	VIN Sense	Sense test point for VIN		
	TP3	VIN	Input test point for VIN		
VOUT	J2	+/-	Output block header for VOUT		
	TP2	VOUT Sense	Sense test point for VOUT		
	TP4	VOUT	Output test point for VOUT		
GND	TP7, TP8, TP9, TP10	GND	Test point for GND		

Table 4-2. TPS22950Q1EVM Test Point Description

Input	Test Point	Label	Description
VIN	TP5	ON	Enable signal test point
	TP6	FLT	Fault test point

Table 4-3. TPS22950Q1EVM Jumper Configuration

Input	Jumper	Label	Description	
	JP1	JP1	FLT signal pullup resistor	
VIN	JP2	ON	ON-pin enable signal Position 1 and 2 sets ON-pin HI Position 2 and 3 sets ON-pin LO	
ILIM	JP3	ILIM	Current limit control     Position 1 and 2 sets 2-A limit     Position 2 and 3 sets 0.5-A limit	

# 5 Operation

Connect the VIN power supply to the J1 terminal (VIN). The input voltage range of the TPS22950Q1EVM is 1.8 V to 5.5 V.

External output loads can be applied to the switch by using the J2 terminal (VOUT). Adjust the current limit on the TPS22950Q1EVM accordingly. When the ON pin is asserted high, the output of the TPS22950-Q1 is enabled.

# **6 Test Configurations**

# 6.1 On-Resistance (Ron) Test Setup

Figure 6-1 shows the typical setup for measuring on-resistance. The voltage drop across the switch is measured using the sense connections, and this result can be divided by the load current to calculate the R<sub>on</sub> resistance.

Test Configurations | INSTRUMENTS | www.ti.com

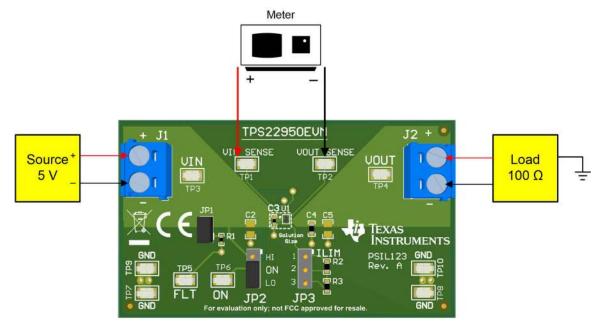


Figure 6-1. Ron Test Setup

# 6.2 Rise Time Test Setup

Figure 6-2 shows the test setup for measuring the rise time of the TPS22950-Q1. Apply a squarewave to the ON pin of the switch using a function generator and apply a voltage to the VIN terminal using a power supply. Observe the waveform at VOUT Sense(TP2) with an oscilloscope to measure the slew rate and rise time of the switch with a given input voltage.

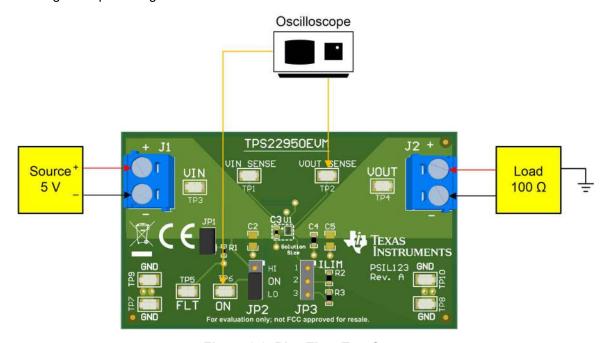


Figure 6-2. Rise Time Test Setup

www.ti.com Bill of Materials (BOM)

# 7 Bill of Materials (BOM)

Table 7-1 lists the TPS22950Q1EVM BOM.

# Table 7-1. Bill of Materials

Designator	Quantity	Value	Description	Package Reference	Part Number	Manufacturer
!PCB1	1		Printed Circuit Board		PSIL224	Any
C1	1	100 μF	Multi-Layer Ceramic Capacitor 100uF 6.3 V X7S ±20% 1210 Emboss T/R	1210	GRT32EC70J107 ME13L	Murata
C3	1	1 uF	CAP, CERM, 1 µF, 16 V,+/- 10%, X7R, AEC-Q200 Grade 1, 0805	805	C0805C105K4RA CAUTO	Kemet
C4	1	0.1 uF	CAP, CERM, 0.1 uF, 50 V, +/- 10%, X7R, AEC-Q200 Grade 1, 0805	805	CEU4J2X7R1H10 4K125AE	TDK
H1, H2, H3, H4	4		Bumpon, Hemisphere, 0.44 X 0.20, Clear	Transparent Bumpon	SJ-5303 (CLEAR)	3M
J1, J2	2		Terminal Block, 5 mm, 2x1, Tin, TH	Terminal Block, 5 mm, 2x1, TH	691 101 710 002	Wurth Elektronik
JP1	1		Header, 100 mil, 2x1, Tin, TH	Header, 2 PIN, 100mil, Tin	PEC02SAAN	Sullins Connector Solutions
JP2, JP3	2		Header, 100mil, 3x1, TH	Header, 3x1, 100mil, TH	800-10-003-10-00 1000	Mill-Max
R1	1	10.0 k	RES, 10.0 k, 0.1%, 0.063 W, 0402	402	PCF0402-12-10K0 BT1	TT Electronics/IRC
R2	1	2.49 k	RES, 2.49 k, 1%, 0.1 W, 0603	603	CRCW06032K49F KEA	Vishay-Dale
R3	1	619	RES, 619, 0.1%, 0.1 W, 0603	603	RT0603BRD0761 9RL	Yageo America
SH-J1, SH-J2, SH-J3	3	1x2	Shunt, 100 mil, Flash Gold, Black	Closed Top 100mil Shunt	SPC02SYAN	Sullins Connector Solutions
TP1, TP2, TP3, TP4, TP5, TP6, TP7, TP8, TP9, TP10	10		Test Point, Miniature, SMT	Test Point, Miniature, SMT	5019	Keystone
U1	1		5.5-V, 2.7-A, 34-mΩ Adjustable Current Limited Load Switch	SOT23-6	TPS22950C-Q1	Texas Instruments
C2, C5	0	10 uF	CAP, CERM, 10 uF, 16 V, +/- 10%, X7S, AEC-Q200 Grade 1, 0805	805	CGA4J1X7S1C10 6K125AC	TDK

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This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

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NOTE: This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

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- · Reorient or relocate the receiving antenna.
- Increase the separation between the equipment and receiver.
- Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.
- Consult the dealer or an experienced radio/TV technician for help.

### 3.2 Canada

3.2.1 For EVMs issued with an Industry Canada Certificate of Conformance to RSS-210 or RSS-247

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(1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

# Concernant les EVMs avec appareils radio:

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