19-3837; Rev 2; 10/10

EVALUATION KIT AVAILABLE

Precision Temperature Monitor for DDR Memory Modules

MAX6604

General Description

The MAX6604 high-precision temperature sensor is designed for thermal monitoring functions in DDR memory modules. The device is readable and programmable through the 2-wire SMBus™/I²C-compatible interface. Three address inputs set the bus address for the temperature sensor to provide up to eight devices on one bus.

The internal thermal sensor continuously monitors the temperature and updates the temperature data eight times per second. The master can read the temperature data at any time. Since the thermal sensor is located on the memory module, temperature data recorded accurately represents the temperature of the components on the module. Consequently, the MAX6604 provides a much more accurate measurement of module temperature than techniques involving temperature sensors on the motherboard. In addition, the device responds more quickly to temperature changes on the module than a motherboard sensor.

The MAX6604 also features an interrupt-output indicator for temperature-threshold monitoring. The threshold levels are programmable through the digital interface.

The MAX6604 operates from -20°C to +125°C, and is available in JEDEC-standard 8-pin TSSOP and 8-pin TDFN (2mm x 3mm) packages.

Applications

Memory Modules

Desktop Computers

Notebook Computers

Workstations

Networking Equipment

Features

- **JEDEC Compliant**
- **±1°C Temperature-Monitoring Accuracy**
- **Overtemperature Interrupt with Programmable Threshold**
- **+2.7V to +3.6V Operating Voltage Range**
- **SMBus/I²C-Compatible Interface**
- **300µA Typical Operating Current**
- **3µA Typical Shutdown Current**
- **-20°C to +125°C Operating Temperature Range**
- **8-Pin TSSOP and 8-Pin TDFN (2mm x 3mm) Packages**

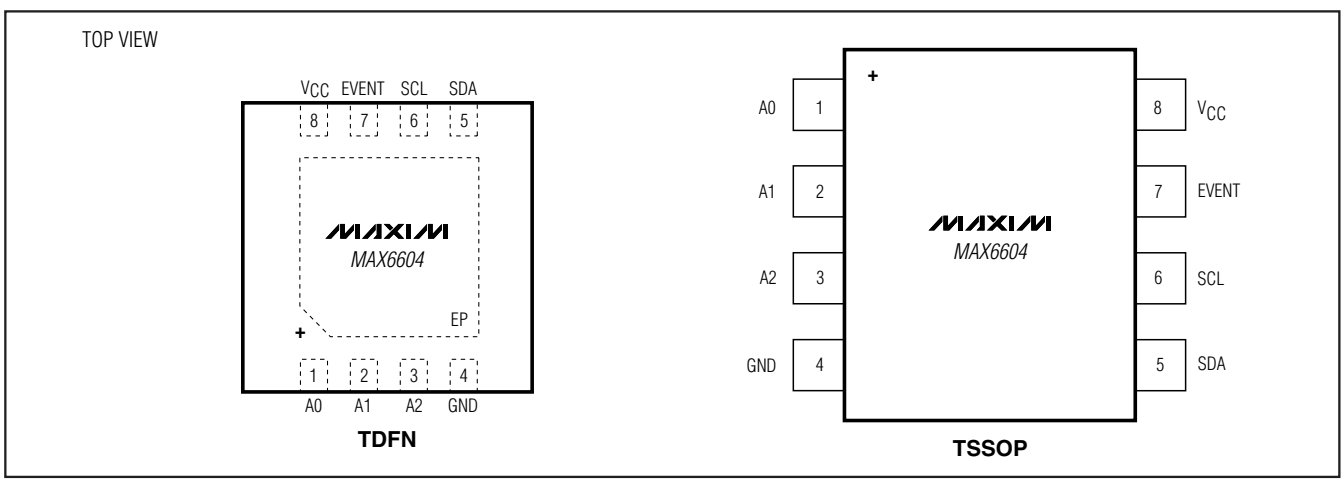
Ordering Information

PART	SERIAL-CLOCK FREQUENCY (kHz)	PIN-PACKAGE	SPECIAL TOP MARK
MAX6604ATA+	100	8 TDFN-EP*	AAA
MAX6604AATA+	400	8 TDFN-EP* (MO229-WCED-2)	AAR
MAX6604AAHA+	400	8 TSSOP	—

+Denotes a lead(Pb)-free/RoHS-compliant package.
**EP = Exposed pad.*
***Note:** These devices operate over the -20°C to +125°C operating temperature range.*

Typical Application Circuit appears at end of data sheet.

Pin Configurations



SMBus is a trademark of Intel Corporation.

Precision Temperature Monitor for DDR Memory Modules

ABSOLUTE MAXIMUM RATINGS

All Input and Output Voltages .....-0.3V to +6V
Continuous Power Dissipation (T_A = +70°C)
8-Pin TDFN (derate 16.7mW/°C above +70°C) 1333.3mW
8-Pin TSSOP (derate 8.1mW/°C above +70°C) 646.7mW
ESD Protection (all pins, Human Body Model) .....±2kV

Junction Temperature .....+150°C
Operating Temperature Range .....-20°C to +125°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C
Soldering Temperature (reflow) .....+260°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = +2.7V to +3.6V, T_A = -20°C to +125°C, unless otherwise noted. Typical values are at V_{CC} = +3.3V, T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Supply Voltage Range	V_{CC}		+2.7		+3.6	V
Temperature Resolution				0.125		°C
				11		bits
Temperature Accuracy		+3V ≤ V_{CC} ≤ +3.6V, +75°C ≤ T_A ≤ +95°C	-1		+1	°C
		+3V ≤ V_{CC} ≤ +3.6V, +40°C ≤ T_A ≤ +125°C	-2		+2	
		+3V ≤ V_{CC} ≤ +3.6V, -20°C ≤ T_A ≤ +125°C	-3		+3	
Power-On Reset (POR) Threshold		V_{CC} falling edge		2.0		V
POR Threshold Hysteresis				90		mV
Undervoltage-Lockout Threshold				2.4		V
Operating Current		During conversion		0.3	0.5	mA
Standby Current				3	6	µA
Conversion Time	t_{CONV}				125	ms
Conversion Rate	f_{CONV}		8			Hz
DIGITAL INTERFACE (Note 2)						
Logic-Input High Voltage (SCL, SDA)	V_{IH}		2.1			V
Logic-Input Low Voltage (SCL, SDA)	V_{IL}				0.8	V
Logic-Input Hysteresis (SCL, SDA)				500		mV
Leakage Current (EVENT, SCL, SDA, A2, A1, A0)	I_{LEAK}	V_{IN} = V_{GND} or V_{CC}	-1		+1	µA
Logic-Output Low Voltage (SDA, EVENT)	V_{OL}	I_{PULL_UP} = 350µA			50	mV
Logic-Output Low Sink Current (SDA, EVENT)	I_{OL}	V_{OL} = 0.6V	6			mA
Input Capacitance (SCL, SDA)	C_{IN}			5		pF

TIMING CHARACTERISTICS—MAX6604ATA+

(V_{CC} = +2.7V to +3.6V, T_A = -20°C to +125°C, unless otherwise noted. Typical values are at V_{CC} = +3.3V, T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Serial-Clock Frequency	f_{SCL}		10		100	kHz
Bus Free Time Between STOP and START Condition	t_{BUF}		4.7			µs
Repeat START Condition Setup Time	$t_{SU:STA}$	90% of SMBCLK to 90% of SMBDATA	4.7			µs
START Condition Hold Time	$t_{HD:STA}$	10% of SMBDATA to 90% of SMBCLK	4			µs
STOP Condition Setup Time	$t_{SU:STO}$	90% of SMBCLK to 10% of SMBDATA	4			µs
Clock Low Period	t_{LOW}	10% of SMBCLK to 10% of SMBCLK	4.7			µs
Clock High Period	t_{HIGH}	90% of SMBCLK to 90% of SMBCLK	4			µs
Data Hold Time	$t_{HD:DAT}$		300			ns
Data Setup Time	$t_{SU:DAT}$	90% of SMBDATA to 10% of SMBCLK	250			ns
Receive SCL/SDA Rise Time	t_R				1000	ns
Receive SCL/SDA Fall Time	t_F				300	ns
Pulse Width of Spike Suppressed	t_{SP}		0		50	ns

TIMING CHARACTERISTICS—MAX6604AATA+, MAX6604AAHA+

(V_{CC} = +2.7V to +3.6V, T_A = -20°C to +125°C, unless otherwise noted. Typical values are at V_{CC} = +3.3V, T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
TIMING CHARACTERISTICS FOR FAST MODE						
Serial-Clock Frequency	f_{SCL}				400	kHz
Bus Free Time Between a STOP and a START Condition	t_{BUF}		1.3			µs
Hold Time for START Condition	$t_{HD:STA}$		0.6			µs
Low Period of the SCL Clock	t_{LOW}		1.3			µs
High Period of the SCL Clock	t_{HIGH}		0.6			µs
Setup Time for a Repeated START Condition	$t_{SU:STA}$		0.6			µs
Data Hold Time	$t_{HD:DAT}$		0		900	ns
Data Setup Time	$t_{SU:DAT}$		100			ns
Rise Time of Both SDA and SCL Signals, Receiving	t_R	Measured from $0.3V_{DD}$ - $0.7V_{DD}$	$20 + 0.1C_B$		300	ns
Fall Time of SDA Transmitting	t_F	Measured from $0.3V_{DD}$ - $0.7V_{DD}$	$20 + 0.1C_B$		300	ns
Setup Time for STOP Condition	$t_{SU:STO}$		0.6			µs
Capacitive Load for Each Bus Line	C_B				400	pF
Pulse Width of Spike Suppressed	t_{SP}				50	ns

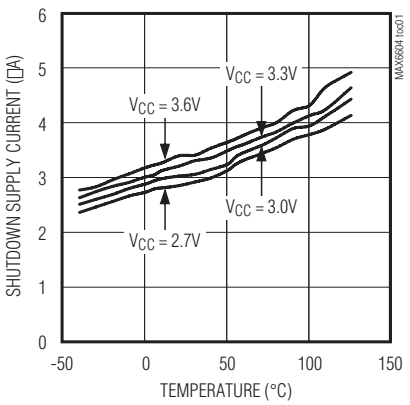
Note 1: All parameters are tested at T_A = +25°C. Specifications over temperature are guaranteed by design.
Note 2: Guaranteed by design.

Precision Temperature Monitor for DDR Memory Modules

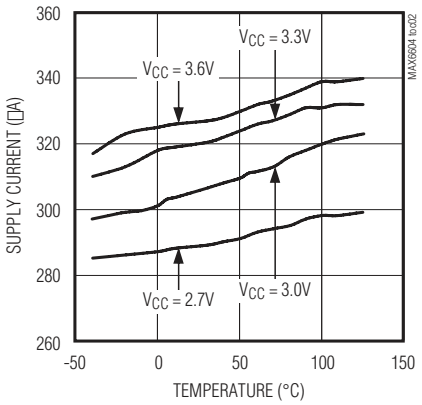
Typical Operating Characteristics

(Typical values are at V_{CC} = +3.3V, T_A = +25°C.)

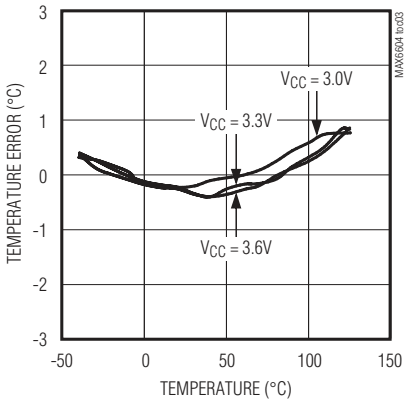
SHUTDOWN SUPPLY CURRENT vs. TEMPERATURE



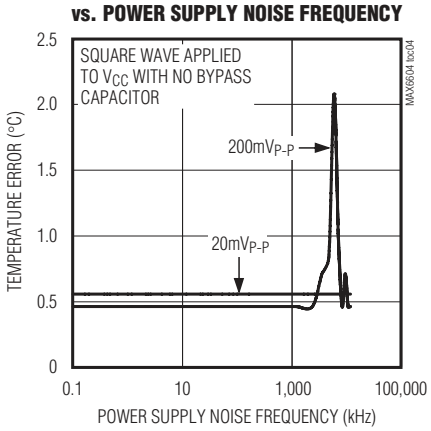
SUPPLY CURRENT vs. TEMPERATURE



TEMPERATURE ERROR vs. TEMPERATURE



TEMPERATURE ERROR vs. POWER SUPPLY NOISE FREQUENCY



Pin Description

PIN	NAME	FUNCTION
1	A0	Address Input. Must connect to GND or V_{CC} to set value.
2	A1	Address Input. Must connect to GND or V_{CC} to set value.
3	A2	Address Input. Must connect to GND or V_{CC} to set value.
4	GND	Ground
5	SDA	Serial-Data Input/Output. Open drain. Connect to a pullup resistor.
6	SCL	Serial-Clock Input. Connect to a pullup resistor.
7	EVENT	Event Output. Open drain. Connect to a pullup resistor.
8	V_{CC}	Supply Voltage. Connect a 0.1µF capacitor to GND as close as possible to the device.
—	EP	Exposed Pad (TDFN only). Internally connected to GND. Connect EP to a large PCB ground plane.

Detailed Description

The MAX6604 high-precision temperature sensor continuously monitors temperature and updates the temperature data eight times per second. The device functions as a slave on the SMBus/I²C-compatible interface. The master can read the temperature data at any time through the digital interface. The MAX6604 also features an open-drain, event-output indicator for temperature-threshold monitoring.

Serial Interface

SMBus/I²C

The MAX6604 is readable and programmable through the SMBus/I²C-compatible interface. The device functions as a slave on the interface. Figure 1 shows the general timing diagram of the clock (SCL) and the data (SDA) signals for the SMBus/I²C-compatible interface.

The SDA and SCL bus lines are at logic-high when the bus is not in use. Pullup resistors from the bus lines to the supply are required when push-pull circuitry is not driving the lines. The data on the SDA line can change only when the SCL line is low. Start and stop conditions occur when SDA changes state while the SCL line is high (Figure 1). Data on SDA must be stable for the duration of the setup time ($t_{SU:DAT}$) before SCL goes high. Data on SDA is sampled when SCL toggles high with data on SDA is stable for the duration of the hold time ($t_{HD:DAT}$). Note that a segment of data is transmitted in an 8-bit byte. A total of nine clock cycles are required to transfer a byte to the MAX6604. Since the MAX6604 employs 16-bit registers, data is transmitted or received in two 8-bit bytes (16 bits). The device acknowledges the successful receipt for each byte by pulling the SDA line low (issuing an ACK) during the ninth clock cycle of each byte transfer.

From a software perspective, the MAX6604 appears as a set of 16-bit registers that contain temperature data, alarm threshold values, and control bits. A standard SMBus/I²C-compatible, 2-wire serial interface reads temperature data and writes control bits and alarm threshold data. Each device responds to its own SMBus/I²C slave address, which is selected using A0, A1, and A2. See the *Device Addressing* section for details.

The MAX6604 employs standard I²C/SMBus protocols using 16-bit registers: write word and read word. Write a word of data (16 bits) by first sending MAX6604's I²C address (0011-A2-A1-A0-0), then sending the 8-bit command byte, followed by the first 8-bit data byte. Note that the slave issues an acknowledge after each byte is written. After the first 8-bit data byte is written, the MAX6604 also returns an acknowledge. However, the master does not generate a stop condition after the first byte has been written. The master continues to write the second byte of data with the slave acknowledging. After the second byte has been written, the master then generates a stop condition. See Figure 2. To read a word of data, the master generates a new start condition and sends MAX6604's I²C address with the R/W bit low (0011-A2-A1-A0-0), then sends the 8-bit command byte. Again, the MAX6604 issues an ACK for each byte received. The master again sends the device address with the R/W bit high (0011-A2-A1-A0-1), following an acknowledge. Next, the master reads the contents of the selected register, beginning with the most significant bit, and acknowledges if the most significant data byte is successfully received. Finally, the master reads the least significant data byte and issues a NACK, followed by a stop condition to terminate the read cycle.

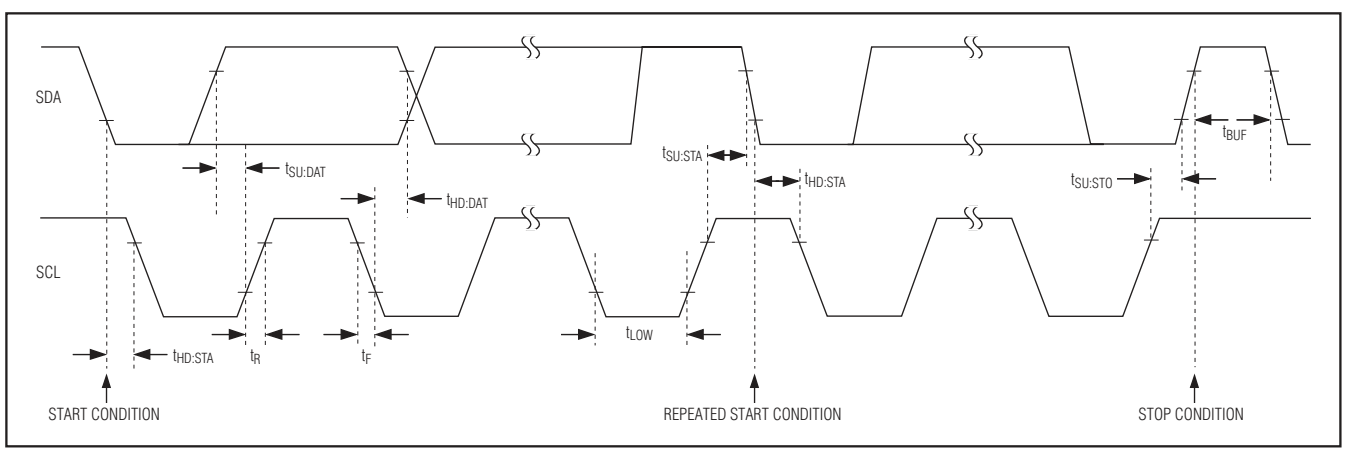


Figure 1. SDA and SCL Timing Diagram

Precision Temperature Monitor for DDR Memory Modules

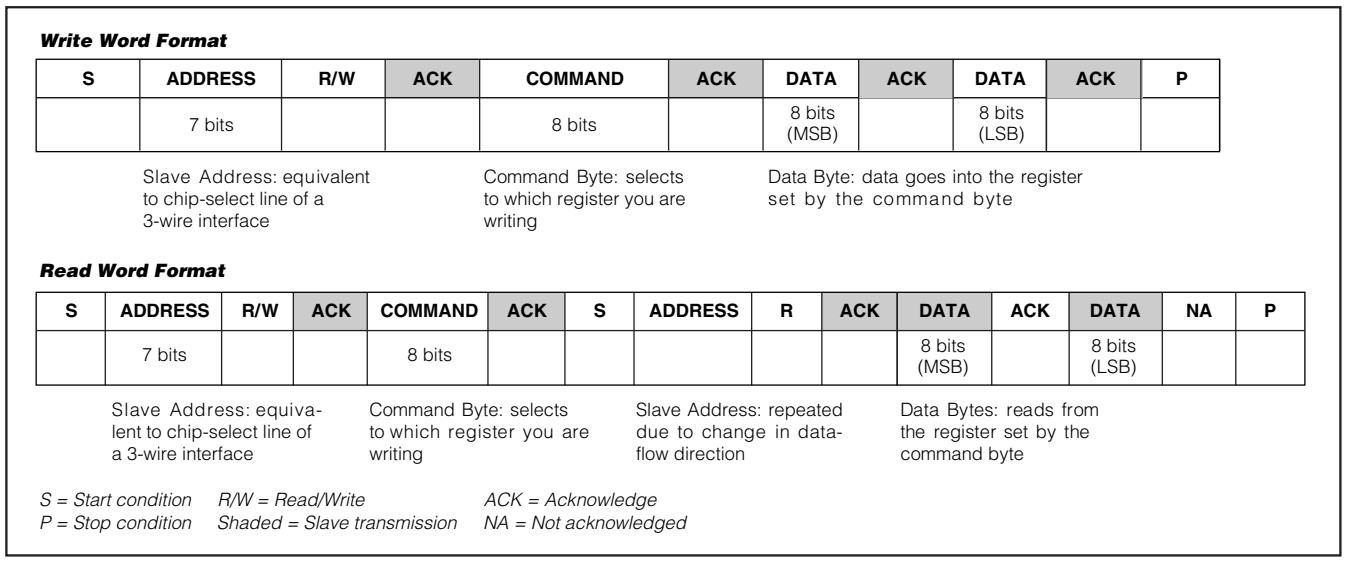


Figure 2. SMBus/I²C Protocols

Device Addressing

The temperature sensor is accessed through the SMBus/I²C bus using an 8-bit address. The temperature sensor address begins with 0011 and is followed by the logic states of the A2, A1, and A0 inputs. These inputs must be hardwired to either GND or V_{CC}. The three address inputs set the bus address for the temperature sensor to allow up to eight devices on one bus. The 8th bit (R/W) dictates a read or write operation. Set the R/W bit low for a write operation and set the R/W bit high for a read operation. See Table 1 for a summary of the device address.

Temperature Sensor

The thermal sensor continuously monitors the temperature and records the temperature data at least eight times per second. Temperature data is latched internally by the MAX6604 and can be read by software from the bus host at any time.

Access to the temperature sensor is through the slave ID of 0011-A2-A1-A0-0. The I²C address-selection inputs (A2, A1, A0) allow up to eight such devices to coexist on the same bus. Consequently, eight memory modules can be supported, given each module has one such slave device address slot.

Upon application of power, the MAX6604's configuration registers are set to their default values. Table 2 lists the various temperature registers and their default states. Note that all registers are 16 bits in length.

Table 1. MAX6604 Sensor Address

FUNCTION	ADDRESS							
Temperature sensor	0	0	1	1	A2	A1	A0	R/W

Table 2. MAX6604 Registers

ADDRESS	POR STATE	DESCRIPTION
00h	0017h	Capability register
01h	0000h	Configuration register
02h	0000h	Alarm-temperature upper-boundary trip register
03h	0000h	Alarm-temperature lower-boundary trip register
04h	0000h	Critical-temperature trip register
05h	0000h	Temperature register
06h	004Dh	Manufacturer's ID register
07h	5400h	Device ID/revision register
08h–0Eh	0000h	Vendor-defined registers (not used)

EVENT-Output Functionality

The EVENT output indicates conditions such as the temperature crossing a predefined boundary. It operates in one of the three modes: interrupt mode, comparator mode, and critical-temperature-only mode. Figure 3 shows an example of the measured temperature vs. time, with the corresponding behavior of the EVENT output in each of these modes. See the *EVENT Operation Modes* section for descriptions of the two modes. The EVENT modes are selected using the configuration register.

Event-output polarity can be set to active high or active low through the configuration register (bit 1). The EVENT output can also be disabled so that EVENT is always high impedance (bit 3). Upon device power-up, the default condition for the EVENT output is high impedance. Writing a 1 to bit 3 of the configuration register enables the EVENT output.

EVENT Thresholds

Alarm Window Trip

The MAX6604 provides a comparison window with an upper-temperature trip point and a lower-temperature trip point, programmed through the alarm-upper-boundary register and the alarm-lower-boundary register, respectively. When enabled, the EVENT output triggers whenever entering or exiting (crossing above or below) the alarm window (Figure 3).

Critical Trip

The critical temperature setting is programmed in the critical temperature register. When the temperature reaches the critical temperature value in this register (and EVENT is enabled), the EVENT output asserts and cannot be deasserted until the temperature drops below the critical temperature threshold.

EVENT Operation Modes

Comparator Mode

In comparator mode, the EVENT output behaves like a window-comparator output that asserts when the temperature is outside the window. Reads/writes on the MAX6604's registers do not affect the EVENT output in comparator mode. The EVENT signal remains asserted until the temperature goes inside the alarm window or the window thresholds are reprogrammed so that the current temperature is within the alarm window.

Interrupt Mode

In interrupt mode, EVENT asserts whenever the temperature crosses an alarm window threshold. After such an event occurs, writing a 1 to the clear event bit in the configuration register deasserts the EVENT output until the next trigger condition occurs. The trip threshold value in

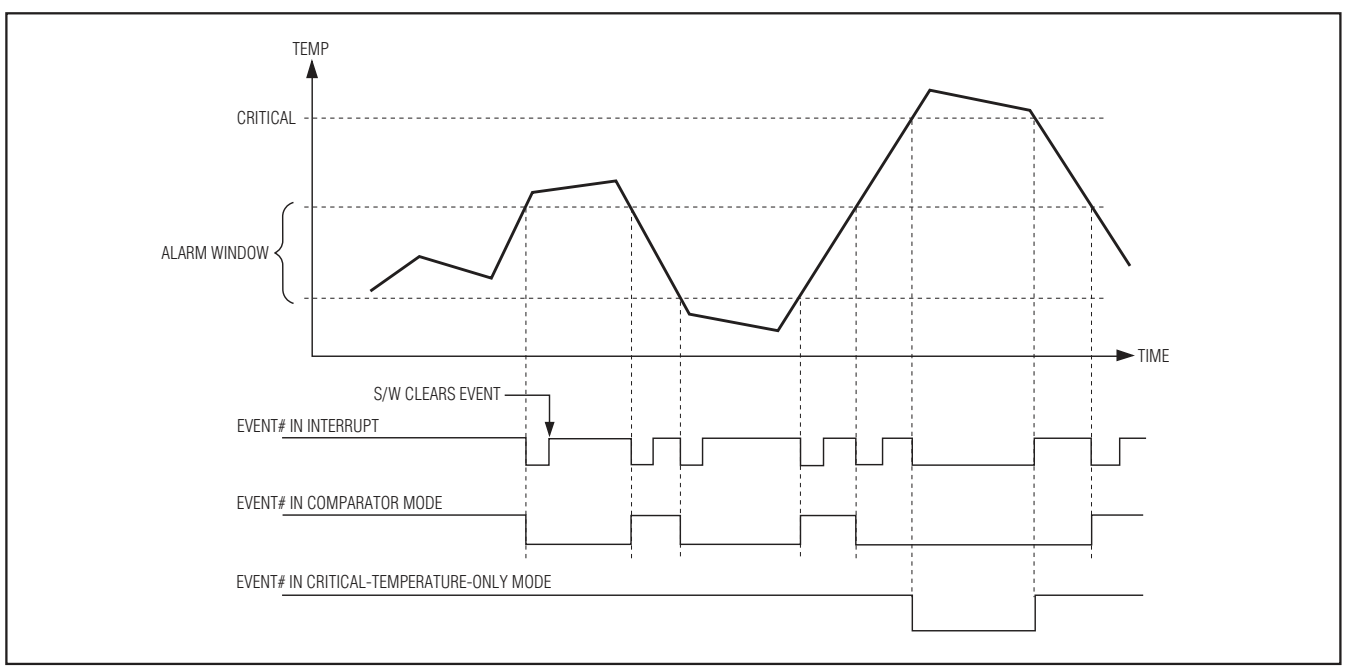


Figure 3. EVENT Behavior in Interrupt, Comparator, and Critical-Temperature-Only Modes

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the critical temperature register is likely to be higher than that of the alarm-upper-boundary register. As a result, when the temperature is above the critical temperature, it is likely that it is above the alarm-upper-boundary as well. In interrupt mode, EVENT asserts when the temperature crosses the alarm upper boundary.

If the EVENT output is cleared and the temperature continues to increase until it crosses the critical temperature threshold, EVENT asserts again. Because the temperature is greater than the critical temperature threshold, a clear event command does not clear the EVENT output. Once the temperature drops below the critical temperature, EVENT deasserts immediately.

If the EVENT output is not cleared before the temperature goes above the critical temperature threshold, EVENT remains asserted. Attempting a clear event command has no effect until the temperature drops below the critical temperature, at which point EVENT deasserts immediately because of the earlier clear event command. If no clear event command is attempted, EVENT remains asserted after the temperature drops below the critical temperature. At this point, a clear event command deasserts EVENT.

Detailed Register Descriptions

Capability Register (Read Only) [Address = 00h, POR = 0017h]

This register indicates the capabilities of the thermal sensor, including accuracy, temperature range, and resolution. See Table 3 for register details.

Configuration Register (Read/Write) [Address = 01h, POR = 0000h]

This register controls the various features of EVENT functionality, and controls the bit for thermal-sensor shutdown mode. See Table 4 for register details.

Hysteresis

When enabled, hysteresis is applied to temperature variations around trigger points. For example, consider the behavior of the alarm window bit (bit 14 of the temperature register) when the hysteresis is set to 3°C. As the temperature rises, bit 14 is set to 1 (temperature is above the alarm window) when the temperature register contains a value that is greater than the value in the alarm temperature upper boundary register. If the temperature decreases, bit 14 remains set until the measured temperature is less than or equal to the value in the alarm temperature upper boundary register minus 3°C.

Table 3. Capability Register (Read Only)

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RFU	RFU	RFU	RFU	RFU	RFU	RFU	RFU	RFU	RFU	RFU	TRES1	TRES0	Wider range	Higher precision	Has alarm and critical trips

BIT	DEFINITION (DESCRIPTIONS IN BOLD TYPE APPLY TO THE MAX6604)
0	**Basic capability** **1: Has alarm and critical trips capability**
1	**Accuracy** 0 = Default accuracy ±2°C over the active and ±3°C monitor ranges **1 = High accuracy ±1°C over the active and ±2°C monitor ranges**
2	**Wider range** 0 = Values lower than 0°C are clamped and represented as binary value 0 **1 = Can read temperature below 0°C and set sign bit accordingly**
4:3	**Temperature resolution** 00 = 0.5°C LSB 01 = 0.25°C LSB **10 = 0.125°C LSB** 11 = 0.0625°C LSB
15:5	0: Reserved for future use (RFU). Must be zero.

Table 4. Configuration Register (Read/Write)

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RFU	RFU	RFU	RFU	RFU	Hysteresis		Shutdown mode	Critical trip lock bit	Alarm window lock bit	Clear EVENT	EVENT output status	EVENT output control	Critical EVENT only	EVENT polarity	EVENT mode

BIT	DEFINITION (DESCRIPTIONS IN BOLD TYPE ARE THE DEFAULT VALUES)
0	**EVENT mode** **0 = Comparator output mode (default)** 1 = Interrupt mode When either of the lock bits is set, this bit cannot be altered until unlocked.
1	**EVENT polarity** **0 = Active low (default)** 1 = Active high When either of the lock bits is set, this bit cannot be altered until unlocked.
2	**Critical EVENT only** **0 = EVENT output on alarm or critical temperature mode (default)** 1 = EVENT only if temperature is above the value in the critical temp register When the alarm window lock bit is set, this bit cannot be altered until unlocked.
3	**EVENT output control** **0 = EVENT output disabled (default) [Disabled means EVENT remains in an inactive voltage level]** 1 = EVENT output enabled When either of the lock bits is set, this bit cannot be altered until unlocked.
4	**EVENT output status (read only)** **0 = EVENT output condition is not being asserted by this device** 1 = EVENT output is being asserted by this device due to alarm window or critical trip condition The actual conditions causing an EVENT output can be determined from the temperature register. Interrupt mode can be cleared by writing to the clear EVENT bit. Writing to this bit has no effect; this bit is not affected by the polarity setting.
5	**Clear EVENT (write only)** **0 = No effect** 1 = Clears active event in interrupt mode. Writing to this register has no effect in comparator mode When read, this bit always returns to zero.
6	**Alarm window lock bit** **0 = Alarm trips are not locked and can be altered (default)** 1 = Alarm trip register settings cannot be altered This bit is initially cleared. When set, this bit returns a 1 and remains locked until cleared by the internal power-on reset. Lock bits and other configuration register bits are updated during the same write; double writes are not necessary.
7	**Critical trip lock bit** **0 = Critical trip is not locked and can be altered (default)** 1 = Critical trip register settings cannot be altered This bit is initially cleared. When set, this bit returns a 1 and remains locked until cleared by the internal power-on reset. Lock bits and other configuration register bits are updated during the same write; double writes are not necessary.

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Table 4. Configuration Register (Read/Write) (continued)

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
RFU	RFU	RFU	RFU	RFU	Hysteresis		Shutdown mode	Critical trip lock bit	Alarm window lock bit	Clear EVENT	EVENT output status	EVENT output control	Critical EVENT only	EVENT polarity	EVENT mode

BIT	DEFINITION (DESCRIPTIONS IN BOLD TYPE ARE THE DEFAULT VALUES)
8	**Shutdown mode** **0 = Enable temperature monitoring (default)** 1 = Shutdown temperature monitoring When shutdown occurs, the thermal-sensing device and analog-to-digital converter are disabled to save power; no EVENT output signals are generated. When either of the lock bits is set, this bit cannot be set until unlocked. However, it can be cleared at any time.
10:9	**Hysteresis enable** **00 = Disable hysteresis** 01 = Enable hysteresis at 1.5°C 10 = Enable hysteresis at 3°C 11 = Enable hysteresis at 6°C
15:11	0: Reserved for future use (RFU). Must be zero.

Similarly, the below alarm window bit (bit 13 of the temperature register) is set to 0 (temperature is equal to or above the alarm window lower boundary trip temperature) when the value in the temperature register is equal to or greater than the value in the alarm-temperature lower-boundary register. As the temperature decreases, bit 13 is set to 1 when the value in the temperature register is equal to or less than the value in the alarm-temperature lower-boundary register minus 3°C.

Note that hysteresis is also applied to EVENT output functionality. When either of the lock bits is set, the hysteresis bits cannot be altered. Hysteresis is applied to both alarm window comparisons and critical temperature comparisons.

Alarm-Temperature Upper-Boundary Trip Register (Read/Write) [Address = 02h, POR = 0000h]

The data format for the upper-boundary trip threshold is in two's complement with one LSB = 0.25°C. The alarm-temperature upper-boundary trip register has a -256.00°C to +255.75°C range. All unused bits are set to zero.

Table 5. Alarm-Temperature Upper-Boundary Trip Register (Read/Write)

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	Sign MSB	128°C	64°C	32°C	16°C	8°C	4°C	2°C	1°C	0.5°C	0.25°C	0	0

FUNCTION	BELOW ALARM WINDOW BIT		ABOVE ALARM WINDOW BIT	
	Temperature slope	Threshold temperature	Temperature slope	Threshold temperature
Sets	Falling	T_L - Hyst	Rising	T_H
Clears	Rising	T_L	Falling	T_H - Hyst

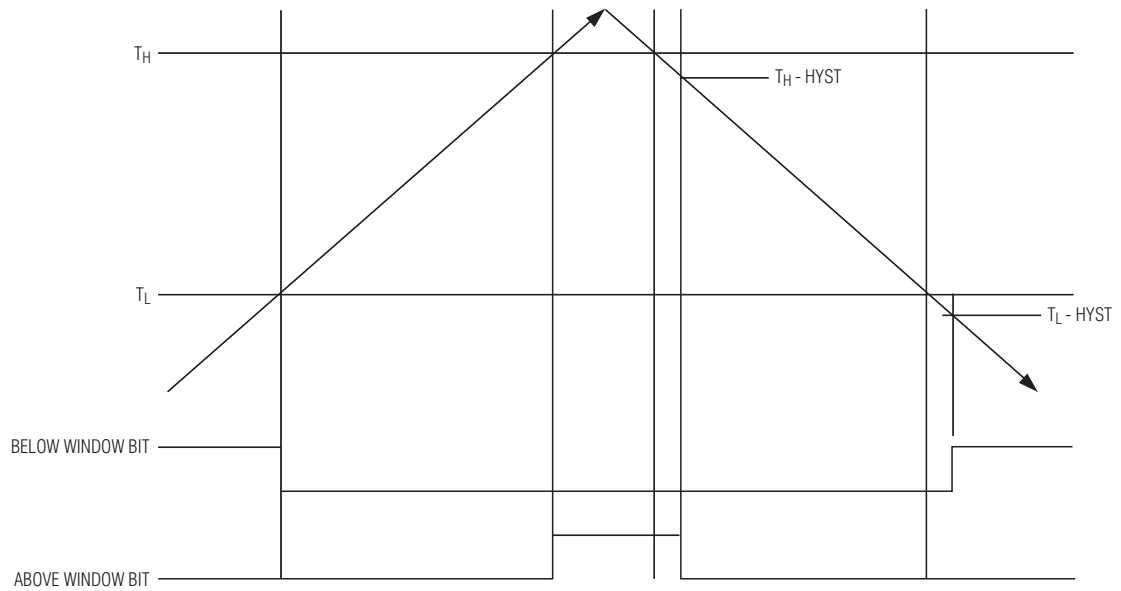


Figure 4. Hysteresis Applied to Temperature Comparisons

Alarm-Temperature Lower-Boundary Trip Register (Read/Write) [Address = 03h, POR = 0000h]

The data format for the lower-boundary trip threshold is in two's complement with one LSB = 0.25°C. The alarm-temperature lower-boundary trip register has a -256.00°C to +255.75°C range. All unused bits are set to zero.

Table 6. Alarm-Temperature Lower-Boundary Trip Register (Read/Write)

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	Sign MSB	128°C	64°C	32°C	16°C	8°C	4°C	2°C	1°C	0.5°C	0.25°C	0	0

Precision Temperature Monitor for DDR Memory Modules

Critical Temperature Register (Read/Write) [Address = 04h, POR = 0000h]

The data format for the critical temperature value is in two's complement with one LSB = 0.25°C. Critical temperature register has a -256.00°C to +255.75°C range. All unused bits are set to zero.

Table 7. Critical Temperature Register (Read/Write)

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	Sign MSB	128°C	64°C	32°C	16°C	8°C	4°C	2°C	1°C	0.5°C	0.25°C	0	0

Temperature Register (Read Only) [Address = 05h, POR = 0000h]

The data format is two's complement with one LSB = 0.125°C. All unused bits are set to zero. The most significant bit has a resolution of 128°C. The trip status bits represent the internal temperature trip detection, and are not affected by the status of the EVENT or configuration bits (e.g., event output control, clear event, etc.). If neither the above alarm window (bit 14) nor the below alarm window (bit 13) are set (i.e., both are 0), the current temperature is within the alarm window.

Table 8. Temperature Register (Read Only)

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Above critical trip	Above alarm window	Below alarm window	Sign MSB	128°C	64°C	32°C	16°C	8°C	4°C	2°C	1°C	0.5°C	0.25°C	0.125°C	0

BIT	DEFINITION
13	**Below alarm window** 0 = Temperature is equal to or above the alarm window lower boundary temperature 1 = Temperature is below the alarm window (temperature < alarm temperature lower boundary minus the hysteresis)
14	**Above alarm window** 0 = Temperature is equal to or below the alarm window upper boundary temperature minus the hysteresis 1 = Temperature is above the alarm window (temperature > alarm temperature upper boundary)
15	**Above critical trip** 0 = Temperature is below the critical temperature setting minus the hysteresis 1 = Temperature is equal to or above the critical temperature setting (temperature ≥ critical temperature)

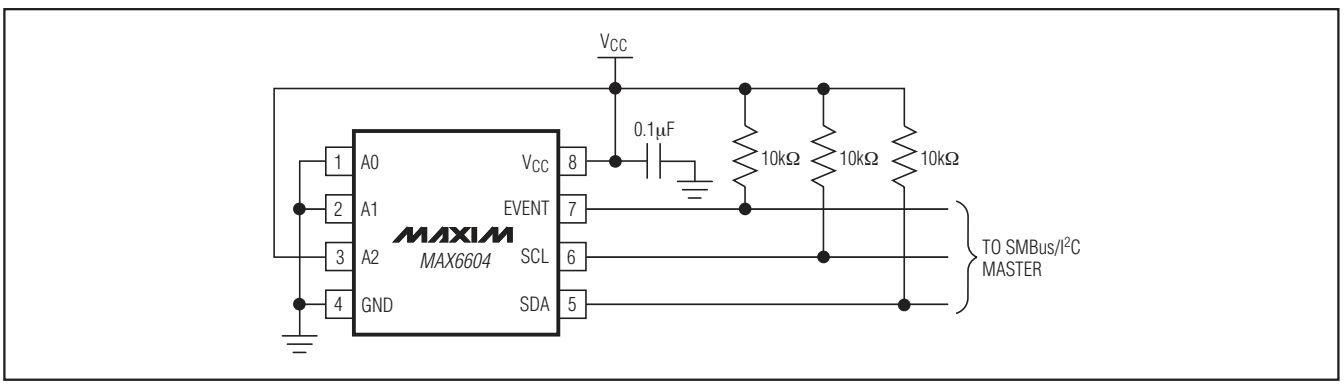
Table 9. Manufacturer's ID Register (Read Only) [Address = 06h, POR = 004Dh]

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	0	0	0	0	0	0	1	0	0	1	1	0	1

Table 10. Device ID and Revision Register (Read Only) [Address = 07h, POR = 5400h]

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Device ID (0101-0100)								Device revision (0000-0000)							

Typical Application Circuit



Precision Temperature Monitor for DDR Memory Modules

Chip Information

PROCESS: BiCMOS

Package Information

For the latest package outline information and land patterns, go to **www.maxim-ic.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
8 TDFN-EP	T823+1	21-0174	90-0091
8 TSSOP	H8+1	21-0175	90-0248

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	10/05	Initial release	—
1	8/09	Added 400kHz serial-clock-frequency capable parts	1-4, 14, 15
2	10/10	Added the soldering temperature to the *Absolute Maximum Ratings* section; corrected the POR state for Register 07h from 3E00h to 5400h in Table 2 and Table 10 and corrected the device ID in Table 10 from 0011-1110 to 0101-0100; added the land pattern drawing numbers to the *Package Information* table	2, 6, 13, 14