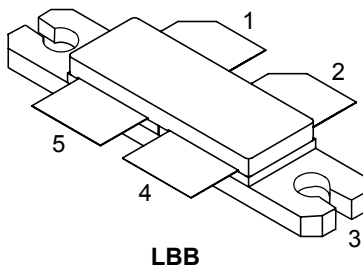


250 W, 28/32 V, HF to 1 GHz RF power LDMOS transistor



Pin connection	
Pin	Connection
1	Drain A
2	Drain B
3	Source (bottom side)
4	Gate B
5	Gate A



Product status link
RF3L05250CB4

Product summary	
Order code	RF3L05250CB4
Marking	3L05250
Package	LBB
Packing	Tape and reel 13"
Base/bulk quantity	100/100

Features

Order code	Frequency	V _{DD}	P _{OUT}	Gain	Efficiency
RF3L05250CB4	650 MHz	28 V	250 W	18 dB	62%

- High efficiency and linear gain operations
- Integrated ESD protection
- Large positive and negative gate-source voltage range for improved class C operation
- In compliance with the European directive 2002/95/EC

Applications

- 2-30 MHz HF or short wave communication
- 30-88 MHz ground communication
- 118-140 MHz Avionics
- 136-174 MHz commercial ground communication
- 30-512 MHz Jammer, ground/air communication
- HF to 1000 MHz ISM - instrumentation

Description

The **RF3L05250CB4** is a 250 W, 28/32 V, LDMOS FET designed for wideband communication and ISM applications in the frequency range from HF to 1 GHz. It can be used in class AB, B or C for all typical modulation formats.

1 Electrical ratings

Table 1. Absolute maximum ratings ($T_C = 25\text{ °C}$)

Symbol	Parameter	Value	Unit
V_{DS}	Drain-source voltage	90	V
V_{GS}	Gate-source voltage	-8 to 10	V
V_{DD}	Maximum operating voltage	36	V
T_{STG}	Storage temperature range	-65 to 150	°C
T_J	Maximum junction temperature	200	°C

Table 2. Thermal data

Symbol	Parameter	Value	Unit
$R_{thJC}^{(1)}$	Thermal resistance, junction-to-case	0.32	°C/W

1. $T_C = 85\text{ °C}$, $T_J = 200\text{ °C}$, DC test.

Table 3. ESD protection

Symbol	Test methodology	Class
HBM	Human body model (according to ANSI/ESDA/JEDEC JS001-2017)	2
CDM	Charge device model (according to ANSI/ESDA/JEDEC JS002-2014)	C3

2 Electrical characteristics

$T_C = 25\text{ }^\circ\text{C}$ unless otherwise specified.

Table 4. Static

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0\text{ V}$, $I_D = 100\text{ }\mu\text{A}$	90			V
I_{DSS}	Zero gate voltage drain leakage current	$V_{GS} = 0\text{ V}$, $V_{DS} = 28\text{ V}$			1	μA
		$V_{GS} = 0\text{ V}$, $V_{DS} = 75\text{ V}$			1	
I_{GSS}	Gate-source leakage current	$V_{GS} = -8/10\text{ V}$, $V_{DS} = 0\text{ V}$			± 100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = 42\text{ V}$, $I_D = 600\text{ }\mu\text{A}$	1.75		2.50	V
$V_{GS(Q)}$	Gate quiescent voltage	$V_{DS} = 28\text{ V}$, $I_D = 700\text{ mA}$		3.0		V
$V_{DS(on)}$	Static drain-source on-voltage	$V_{GS} = 10\text{ V}$, $I_D = 3\text{ A}$			550	mV
$I_{DS(on)}$	Static drain-source on-current	$V_{GS} = 10\text{ V}$, $V_{DS} = 100\text{ mV}$			2.5	A
$R_{DS(on)}$	Drain-source on-state resistance	$V_{GS} = 10\text{ V}$, $V_{DS} = 100\text{ mV}$			1	Ω
C_{ISS}	Common source input capacitance	$V_{GS} = 0\text{ V}$, $V_{DD} = 28\text{ V}$, $f = 1\text{ MHz}$		128		pF
C_{RSS}	Common source feedback capacitance			2.4		pF
C_{OSS}	Common source output capacitance			43		pF

Table 5. Dynamic

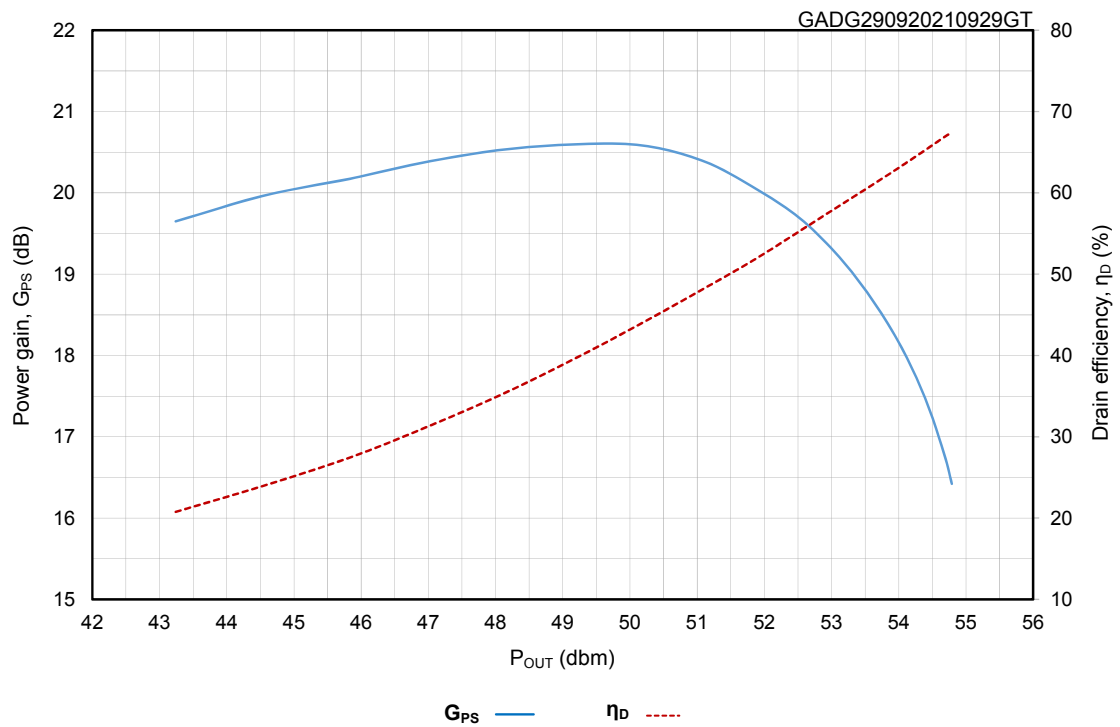
Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
f	Frequency				1000	MHz
P_{OUT}	Output power	$f = 650\text{ MHz}$, 2.5 dB compression		250		W
G_{PS}	Power gain			18		dB
η_D	Drain efficiency			62		%
VSWR	Load mismatch	$P_{OUT} = 250\text{ W}$, all phases			10:1	

Note: $V_{DD} = 28\text{ V}$, $I_{DQ} = 100\text{ mA}$, CW test signal.

3 Typical performances

Table 6. Output power, power gain and drain efficiency vs input power (f = 650 MHz)

P_{IN} (dBm)	P_{OUT} (dBm)	P_{OUT} (W)	I_{DS} (A)	G_{PS} (dB)	η_D (%)
23.65	43.18	21	3.65	19.53	20
24.67	44.45	28	4.25	19.78	23
25.68	45.65	37	4.91	19.97	27
26.69	46.84	48	5.66	20.15	30
27.7	47.97	63	6.49	20.27	34
28.72	49.05	80	7.41	20.33	39
29.71	50	100	8.38	20.29	43
30.73	50.94	124	9.38	20.21	47
31.73	51.69	148	10.35	19.96	51
32.74	52.34	171	11.31	19.6	54
33.74	52.94	197	12.25	19.2	57
34.76	53.43	220	13.15	18.67	60
35.76	53.88	244	14.02	18.12	62
36.74	54.23	265	14.71	17.49	64

Figure 1. Power gain and drain efficiency versus output power (f = 650 MHz)


Note: $V_{DD} = 28$ V, $I_{DQ} = 100$ mA, CW test signal.

4 Test circuits

Figure 2. Test circuit layout (f = 650 MHz)

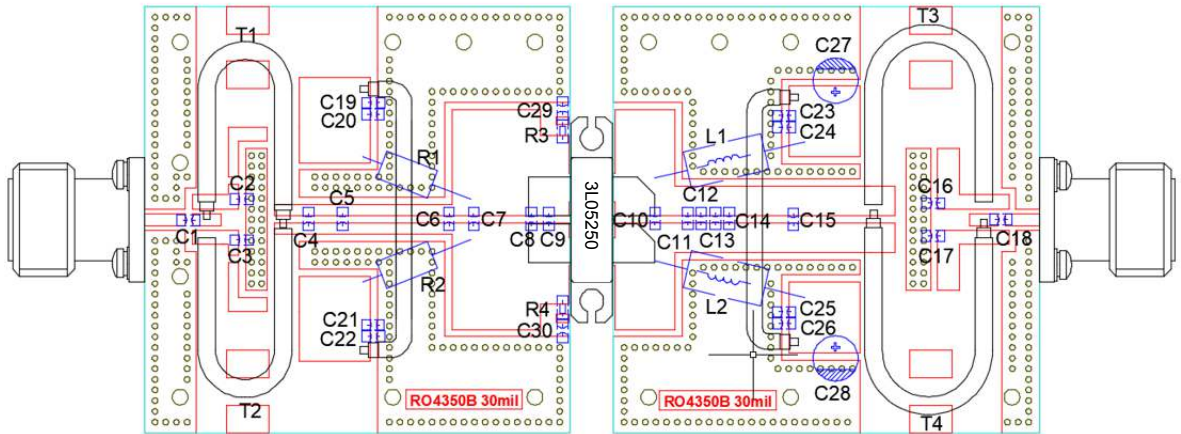


Figure 3. Test circuit photo

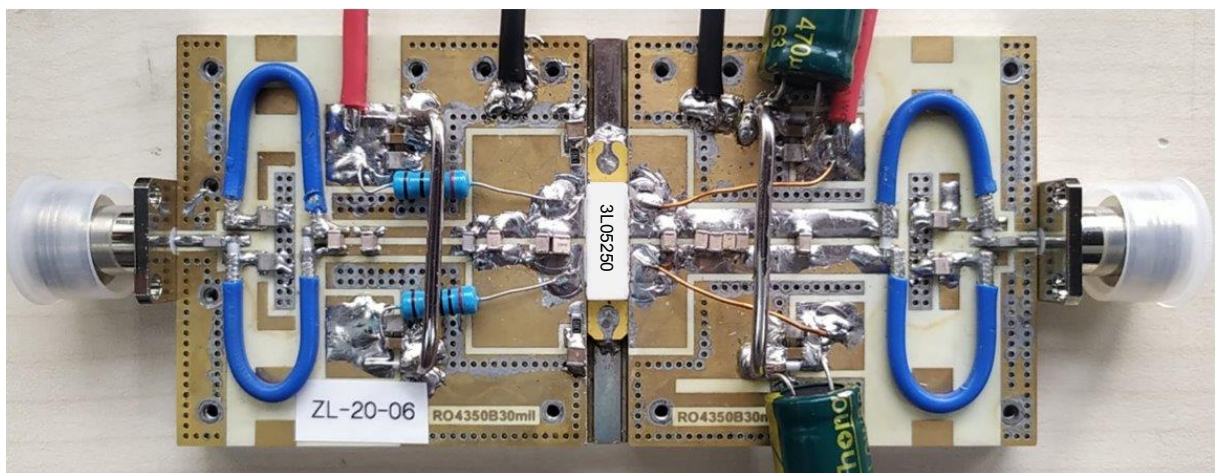


Table 7. Components list

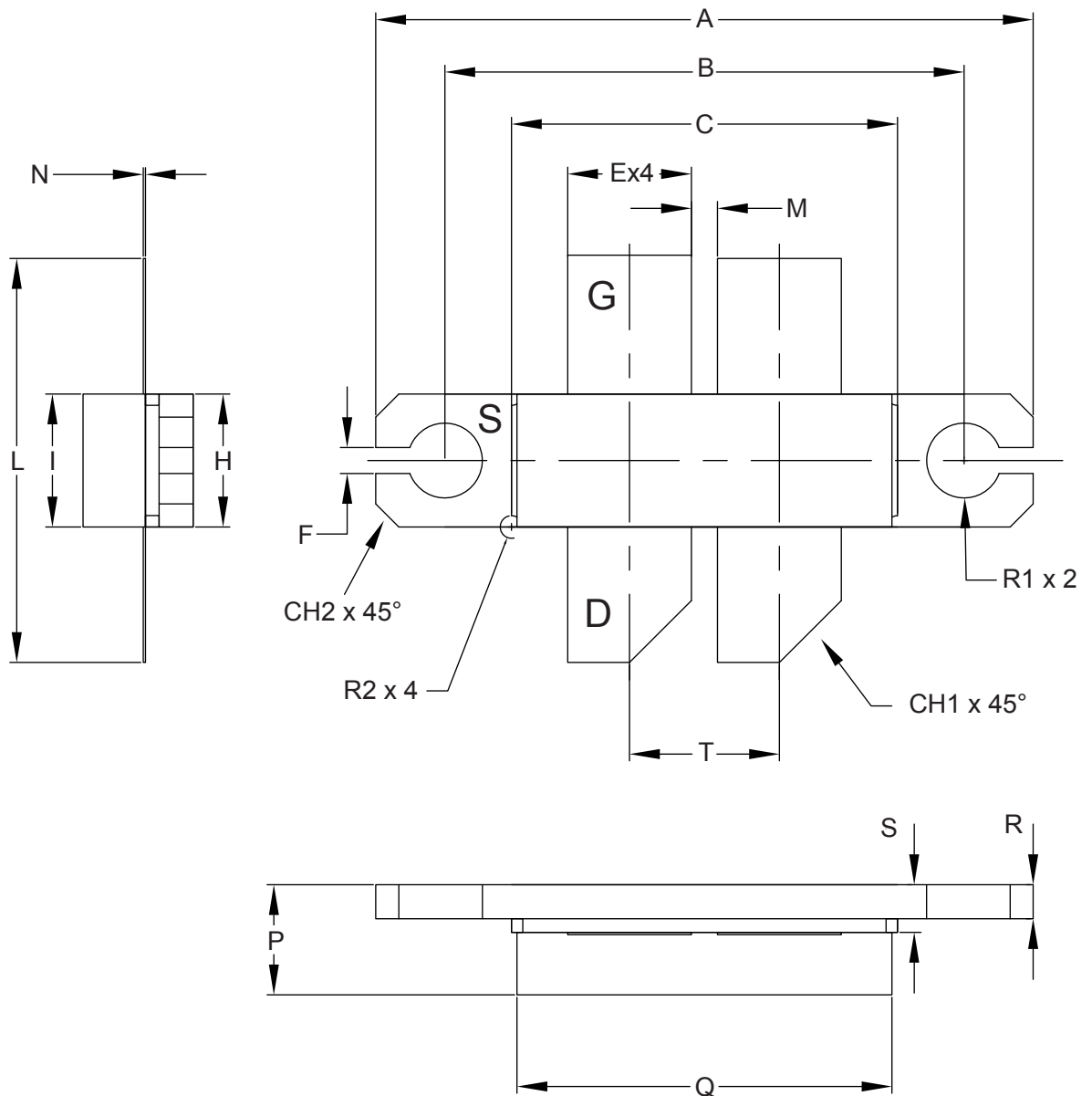
Component	Value	Reference
C1, C18, C20, C21, C24, C25	47 pF	ATC800B
C2, C3	120 pF	ATC800B
C4, C5	2 pF	DLC70B
C6, C12	10 pF	ATC800B
C7	20 pF	DLC70B
C8, C10	15 pF	DLC70B
C9, C13	6.8 pF	DLC70B
C11	4.7 pF	DLC70B
C14	1.8 pF	DLC70B
C15	3.9 pF	DLC70B
C16, C17	240 pF	DLC70B
C29, C30	1000 pF	ATC800B
C19, C22, C23, C26	10 uF	50 V ceramic multilayer capacitor
C27, C28	470 uF	63 V electrolytic capacitor
R1, R2	200 Ω	Metal film resistor
R3, R4	13 Ω	0805 chip resistor
L1, L2	Φ 0.8 mm	Copper wire
T1, T2, T3, T4	25 Ω , line length = 50 mm	SF-086-25
PCB	0.762 mm [0.030"] thick, $\epsilon_r = 3.48$, Rogers RO4350B, 1 oz. copper	

5 Package information

In order to meet environmental requirements, ST offers these devices in different grades of **ECOPACK** packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

5.1 LBB package information

Figure 4. LBB package outline



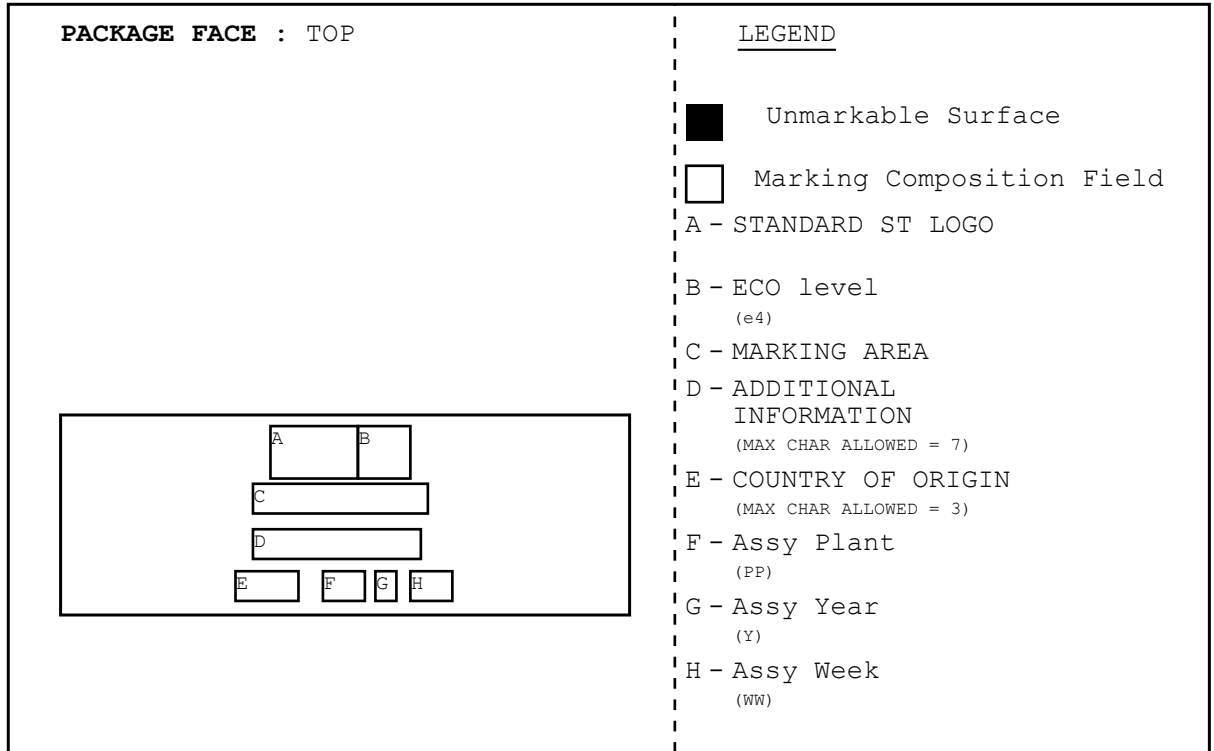
DM00666717_2

Table 8. LBB mechanical data

Symbol	Millimeters		
	Min.	Typ.	Max.
A	28.82	28.95	29.08
B	22.73	22.86	22.99
C	16.87	17.00	17.13
E	5.32	5.45	5.58
F	1.01	1.14	1.27
H	5.72	5.85	5.98
I	5.72	5.85	5.98
L	17.65	17.78	17.91
M	1.02	1.15	1.28
N		0.10	
P	4.72	4.85	4.98
Q	16.38	16.51	16.64
R	1.37	1.50	1.63
S	1.97	2.10	2.23
T		6.60	
CH1		2.72	
CH2		1.02	
R1		1.65	
R2		0.50	

5.2 Marking information

Figure 5. Marking composition



GADG040220211644GT

Revision history

Table 9. Document revision history

Date	Revision	Changes
16-Jun-2020	1	First release
29-Sep-2021	2	Updated title and Device summary in cover page. Updated Section 1 Electrical ratings. Updated Section 2 Electrical characteristics. Updated Figure 1. Power gain and drain efficiency versus output power (f = 650 MHz). Updated Section 4 Test circuits. Added Section 5.2 Marking information. Minor text changes.

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