100 Pin Super I/O with LPC Interface for Notebook Applications

FEATURES

- 3.3 Volt Operation (5V Tolerant)
- PC99 and ACPI 1.0b Compliant
- Programmable Wakeup Event Interface (nIO_PME Pin)
- SMI Support (nIO_SMI Pin)
- GPIOs (29)
- Two IRQ Input Pins
- XNOR Chain
- Intelligent Auto Power Management
- 2.88MB Super I/O Floppy Disk Controller
  - Licensed CMOS 765B Floppy Disk Controller
  - Software and Register Compatible with SMSC's Proprietary 82077AA Compatible Core
  - Supports One Floppy Drive Directly
  - Configurable Open Drain/Push-Pull Output Drivers
  - Supports Vertical Recording Format
  - 16-Byte Data FIFO
  - 100% IBM Compatibility
  - Detects All Overrun and Underrun Conditions
  - Sophisticated Power Control Circuitry (PCC) Including Multiple Powerdown Modes for Reduced Power Consumption
  - DMA Enable Logic
  - Data Rate and Drive Control Registers
  - Swap Drives A and B
  - Non-Burst Mode DMA Option
  - 48 Base I/O Address, 15 IRQ and 3 DMA Options
  - Forceable Write Protect and Disk Change Controls
- Floppy Disk Available on Parallel Port Pins (ACPI Compliant)
- Enhanced Digital Data Separator
  - 2 Mbps, 1 Mbps, 500 Kbps, 300 Kbps, 250 Kbps Data Rates
  - Programmable Precompensation Modes
- Serial Ports
  - Two Full Function Serial Ports
  - High Speed NS16C550 Compatible UARTs with Send/Receive 16-Byte FIFOs
  - Supports 230k and 460k Baud
  - Programmable Baud Rate Generator
  - Modem Control Circuitry
- Infrared Communications Controller
  - IrDA v1.2 (4Mbps), HPSIR, ASKIR, Consumer IR Support
  - 2 IR Ports
  - 96 Base I/O Address, 15 IRQ Options and 3 DMA Options
- Multi-Mode Parallel Port with ChiProtect
  - Standard Mode IBM PC/XT, PC/AT, and PS/2 Compatible Bidirectional Parallel Port
  - Enhanced Parallel Port (EPP) Compatible - EPP 1.7 and EPP 1.9 (IEEE 1284 Compliant)
  - IEEE 1284 Compliant Enhanced Capabilities Port (ECP)
  - ChiProtect Circuitry for Protection Against Damage Due to Printer Power-On
  - 192 Base I/O Address, 15 IRQ and 3 DMA Options

ORDERING INFORMATION

Order Numbers:
LPC47N227TQFP for 100 Pin TQFP Package
LPC47N227-MN for 100 Pin STQFP Package
LPC47N227-MT for 100 Pin TQN Package (Green, Lead-Free)
LPC47N227-MV for 100 Pin STQN Package (Green, Lead-Free)

- LPC Bus Host Interface
  - Multiplexed Command, Address and Data Bus
  - 8-Bit I/O Transfers
  - 8-Bit DMA Transfers
  - 16-Bit Address Qualification
  - Serial IRQ Interface Compatible with Serialized IRQ Support for PCI Systems
  - PCI nCLKRUN Support
  - Power Management Event (nIO_PME) Interface Pin
- 100 Pin TQFP package and STQFP package
- 100 Pin TQN package and STQN package (green, lead-free)

GENERAL DESCRIPTION

The SMSC LPC47N227 is a 3.3V PC 99 and ACPI 1.0b compliant Super I/O Controller. The LPC47N227 implements the LPC interface, a pin reduced ISA interface which provides the same or better performance as the ISA/X-bus with a substantial savings in pins used. The part also includes 29 GPIO pins.

The LPC47N227 incorporates SMSC's true CMOS 765B floppy disk controller, advanced digital data separator, 16-byte data FIFO, two 16C550 compatible UARTs, one Multi-Mode parallel port with ChiProtect circuitry plus EPP and ECP support and one floppy direct drive support. The LPC47N227 does not require any external filter components, is easy to use and offers lower system cost and reduced board area. The LPC47N227 is software and register compatible with SMSC's proprietary 82077AA core.

The true CMOS 765B core provides 100% compatibility with IBM PC/XT and PC/AT architectures and provides data overflow and underflow protection. The SMSC advanced digital data separator incorporates SMSC's patented data separator technology allowing for ease of testing and use. The LPC47N227 supports both 1Mbps and 2Mbps data rates and vertical recording operation at 1Mbps Data Rate.

The LPC47N227 also features a full 16-bit internally decoded address bus, a Serial IRQ interface with PCI nCLKRUN support, relocatable configuration ports and three DMA channel options.
Both on-chip UARTs are compatible with the NS16C550. One UART includes additional support for a Serial Infrared Interface that complies with IrDA v1.2 (Fast IR), HPSIR, and ASKIR formats (used by Sharp and other PDAs), as well as Consumer IR.

The parallel port is compatible with IBM PC/AT architectures, as well as IEEE 1284 EPP and ECP. The parallel port ChiProtect circuitry prevents damage caused by an attached powered printer when the LPC47N227 is not powered.

The LPC47N227 incorporates sophisticated power control circuitry (PCC). The PCC supports multiple low power down modes. The LPC47N227 also features Software Configurable Logic (SCL) for ease of use. SCL allows programmable system configuration of key functions such as the FDC, parallel port, and UARTs.

The LPC47N227 supports the ISA Plug-and-Play Standard (Version 1.0a) and provides the recommended functionaity to support Windows '95/'98 and PC99. The I/O Address, DMA Channel and Hardware IRQ of each device in the LPC47N227 may be reprogrammed through the internal configuration registers. There are 192 I/O address location options, a Serialized IRQ interface, and three DMA channels.

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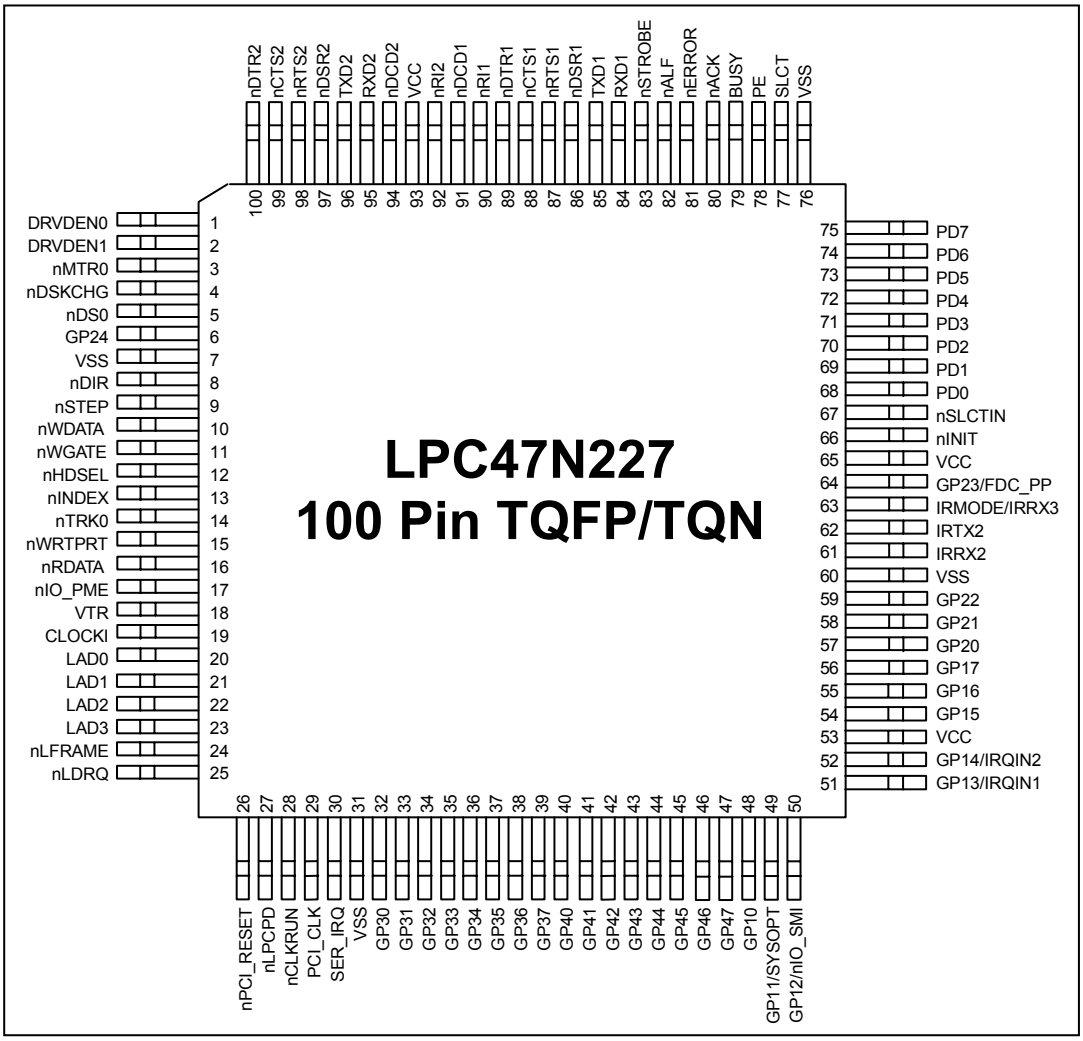
PIN CONFIGURATION

Note: *Pinouts are the same for the* ***TQFP, TQN, STQFP and STQN*** *packages.*



DESCRIPTION OF PIN FUNCTIONS

TQFP/STQFP TQN/STQN PIN #	NAME	SYMBOL	BUFFER TYPE PER FUNCTION[1]	DESCRIPTION
LPC INTERFACE				
23:20	LPC Address/ Data bus 3-0	LAD[3:0]	PCI_IO	Active high LPC signals used for multiplexed command, address and data bus.
24	LPC Frame	nLFRAME	PCI_I	Active low signal indicates start of new cycle and termination of broken cycle.
25	LPC DMA/Bus Master Request	nLDRQ	PCI_O	Active low signal used for encoded DMA/Bus Master request for the LPC interface.
26	PCI RESET	nPCI_RESET	PCI_I	Active low signal used as LPC Interface Reset.
27	LPC Power Down (Note 2)	nLPCPD	PCI_I	Active low Power Down signal indicates that the LPC47N227 should prepare for power to be shut on the LPC interface.
28	PCI Clock Controller	nCLKRUN	PCI_OD	This signal is used to indicate the PCI clock status and to request that a stopped clock be started.
29	PCI Clock	PCI_CLK	PCI_CLK	PCI clock input.
30	Serial IRQ	SER_IRQ	PCI_IO	Serial IRQ pin used with the PCI_CLK pin to transfer LPC47N227 interrupts to the host.
17	Power Mgt. Event *(Note 7)*	nIO_PME	(O12/OD12)	This active low Power Management Event signal allows the LPC47N227 to request wakeup.
FLOPPY DISK INTERFACE				
1	Drive Density 0	DRVDEN0	(O12/OD12)	Indicates the drive and media selected. Refer to configuration registers CR03, CR0B, CR1F.
2	Drive Density 1	DRVDEN1	(O12/OD12)	Indicates the drive and media selected. Refer to configuration registers CR03, CR0B, CR1F.
3	Motor On 0	nMTR0	(O12/OD12)	These active low output selects motor drive 0.

TQFP/STQFP TQN/STQN PIN #	NAME	SYMBOL	BUFFER TYPE PER FUNCTION[1]	DESCRIPTION
4	Disk Change	nDSKCHG	IS	This input senses that the drive door is open or that the diskette has possibly been changed since the last drive selection. This input is inverted and read via bit 7 of I/O address 3F7H. The nDSKCHG bit also depends upon the state of the Force Disk Change bits in the Force FDD Status Change configuration register (see subsection CR17 in the Configuration section).
5	Drive Select 0	nDS0	(O12/OD12)	Active low output selects drive 0.
8	Direction Control	nDIR	(O12/OD12)	This high current low active output determines the direction of the head movement. A logic “1” on this pin means outward motion, while a logic “0” means inward motion.
9	Step Pulse	nSTEP	(O12/OD12)	This active low high current driver issues a low pulse for each track-to-track movement of the head.
10	Write Data	nWDATA	(O12/OD12)	This active low high current driver provides the encoded data to the disk drive. Each falling edge causes a flux transition on the media.
11	Write Gate	nWGATE	(O12/OD12)	This active low high current driver allows current to flow through the write head. It becomes active just prior to writing to the diskette.
12	Head Select	nHDSEL	(O12/OD12)	This high current output selects the floppy disk side for reading or writing. A logic “1” on this pin means side 0 will be accessed, while a logic “0” means side 1 will be accessed.
13	Index	nINDEX	IS	This active low Schmitt Trigger input senses from the disk drive that the head is positioned over the beginning of a track, as marked by an index hole.
14	Track 0	nTRK0	IS	This active low Schmitt Trigger input senses from the disk drive that the head is positioned over the outermost track.

TQFP/STQFP TQN/STQN PIN #	NAME	SYMBOL	BUFFER TYPE PER FUNCTION[1]	DESCRIPTION
15	Write Protected	nWRTPRT	IS	This active low Schmitt Trigger input senses from the disk drive that a disk is write protected. Any write command is ignored. The nWRPRT bit also depends upon the state of the Force Write Protect bit in the Force FDD Status Change configuration register (see subsection CR17 in the Configuration section).
16	Read Disk Data	nRDATA	IS	Raw serial bit stream from the disk drive, low active. Each falling edge represents a flux transition of the encoded data.
SERIAL PORTS INTERFACE				
84	Receive Data 1	RXD1	IS	Receiver serial data input for port 1.
85	Transmit Data 1	TXD1	O12	Transmit serial data output for port 1.
86	Data Set Ready 1	nDSR1	I	Active low Data Set Ready inputs for the serial port. Handshake signal which notifies the UART that the modem is ready to establish the communication link. The CPU can monitor the status of nDSR signal by reading bit 5 of Modem Status Register (MSR). A nDSR signal state change from low to high after the last MSR read will set MSR bit 1 to a 1. If bit 3 of Interrupt Enable Register is set, the interrupt is generated when nDSR changes state. Note: Bit 5 of MSR is the complement of nDSR.
97	Data Set Ready 2	nDSR2	I	
87	Request to Send 1	nRTS1	O6	Active low Request to Send outputs for the Serial Port. Handshake output signal notifies modem that the UART is ready to transmit data. This signal can be programmed by writing to bit 1 of the Modem Control Register (MCR). The hardware reset will reset the nRTS signal to inactive mode (high). nRTS is forced inactive during loop mode operation.
98	Request to Send 2	nRTS2	O6	

TQFP/STQFP TQN/STQN PIN #	NAME	SYMBOL	BUFFER TYPE PER FUNCTION[1]	DESCRIPTION
88	Clear to Send 1	nCTS1	I	Active low Clear to Send inputs for the serial port. Handshake signal which notifies the UART that the modem is ready to receive data. The CPU can monitor the status of nCTS signal by reading bit 4 of Modem Status Register (MSR). A nCTS signal state change from low to high after the last MSR read will set MSR bit 0 to a 1. If bit 3 of the Interrupt Enable Register is set, the interrupt is generated when nCTS changes state. The nCTS signal has no effect on the transmitter. Note: Bit 4 of MSR is the complement of nCTS.
99	Clear to Send 2	nCTS2	I	

TQFP/STQFP TQN/STQN PIN #	NAME	SYMBOL	BUFFER TYPE PER FUNCTION[1]	DESCRIPTION
89	Data Terminal Ready 1	nDTR1	O6	Active low Data Terminal Ready outputs for the serial port. Handshake output signal notifies modem that the UART is ready to establish data communication link. This signal can be programmed by writing to bit 0 of Modem Control Register (MCR). The hardware reset will reset the nDTR signal to inactive mode (high). nDTR is forced inactive during loop mode operation.
100	Data Terminal Ready 2	nDTR2	O6	
90	Ring Indicator 1 *(Note 8)*	nRI1	I	Active low Ring Indicator inputs for the serial port. Handshake signal which notifies the UART that the telephone ring signal is detected by the modem. The CPU can monitor the status of nRI signal by reading bit 6 of Modem Status Register (MSR). A nRI signal state change from low to high after the last MSR read will set MSR bit 2 to a 1. If bit 3 of Interrupt Enable Register is set, the interrupt is generated when nRI changes state. Note: Bit 6 of MSR is the complement of nRI.
92	Ring Indicator 2 *(Note 8)*	nRI2	I	
91	Data Carrier Detect 1	nDCD1	I	Active low Data Carrier Detect inputs for the serial port. Handshake signal which notifies the UART that carrier signal is detected by the modem. The CPU can monitor the status of nDCD signal by reading bit 7 of Modem Status Register (MSR). A nDCD signal state change from low to high after the last MSR read will set MSR bit 3 to a 1. If bit 3 of Interrupt Enable Register is set, the interrupt is generated when nDCD changes state. Note: Bit 7 of MSR is the complement of nDCD.
94	Data Carrier Detect 2	nDCD2	I	
95	Receive Data 2	RXD2	IS	Receiver serial data input for port 2. IR Receive Data.
96	Transmit Data 2	TXD2	O12	Transmit serial data output for port 2. IR transmit data.
INFRARED INTERFACE				
61	IR Receive	IRRX2	IS	IR Receive.
62	IR Transmit	IRTX2	O12	IR Transmit.
63	IR Mode/ IR Receive 3	IRMODE/ IRRX3	O6/ IS	IR mode. IR Receive 3.
PARALLEL PORT INTERFACE (NOTE 3)				

TQFP/STQFP TQN/STQN PIN #	NAME	SYMBOL	BUFFER TYPE PER FUNCTION[1]	DESCRIPTION
66	Initiate Output/ FDC Direction Control (Note 4)	nINIT/ nDIR	(OD14/OP14)/ OD14	This output is bit 2 of the printer control register. This is used to initiate the printer when low. Refer to Parallel Port description for use of this pin in ECP and EPP mode. See FDC Pin definition.
67	Printer Select Input/ FDC Step Pulse (Note 4)	nSLCTIN/ nSTEP	(OD14/OP14)/ OD14	This active low output selects the printer. This is the complement of bit 3 of the Printer Control Register. Refer to Parallel Port description for use of this pin in ECP and EPP mode. See FDC Pin definition.
68	Port Data 0/ FDC Index	PD0/ nINDEX	IOP14/ IS	Port Data 0 See FDC Pin definition.
69	Port Data 1/ FDC Track 0	PD1/ nTRK0	IOP14/ IS	Port Data 1 See FDC Pin definition.
70	Port Data 2/ FDC Write Protected	PD2/ nWRTPRT	IOP14/ IS	Port Data 2 See FDC Pin definition.
71	Port Data 3/ FDC Read Disk Data	PD3/ nRDATA	IOP14/ IS	Port Data 3 See FDC Pin definition.
72	Port Data 4/ FDC Disk Change	PD4/ nDSKCHG	IOP14/ IS	Port Data 4 See FDC Pin definition.
73	Port Data 5	PD5	IOP14	Port Data 5
74	Port Data 6/ FDC Motor On 0	PD6/ nMTR0	IOP14/ OD14	Port Data 6 See FDC Pin definition.
75	Port Data 7	PD7	IOP14	Port Data 7
77	Printer Selected Status/ FDC Write Gate	SLCT/ nWGATE	I/ OD12	This high active output from the printer indicates that it has power on. Bit 4 of the Printer Status Register reads the SLCT input. Refer to Parallel Port description for use of this pin in ECP and EPP mode. See FDC Pin definition.

TQFP/STQFP TQN/STQN PIN #	NAME	SYMBOL	BUFFER TYPE PER FUNCTION[1]	DESCRIPTION
78	Paper End/ FDC Write Data	PE/ nWRDATA	I/ OD12	Another status output from the printer, a high indicating that the printer is out of paper. Bit 5 of the Printer Status Register reads the PE input. Refer to Parallel Port description for use of this pin in ECP and EPP mode. See FDC Pin definition.
79	Busy/ FDC Motor On 1	BUSY/ nMTR1	I/ OD12	This is a status output from the printer, a high indicating that the printer is not ready to receive new data. Bit 7 of the Printer Status Register is the complement of the BUSY input. Refer to Parallel Port description for use of this pin in ECP and EPP mode. See FDC Pin definition.
80	Acknowledge/ FDC Drive Select 1	nACK/ nDS1	I/ OD12	A low active output from the printer indicating that it has received the data and is ready to accept new data. Bit 6 of the Printer Status Register reads the nACK input. Refer to Parallel Port description for use of this pin in ECP and EPP mode. See FDC Pin definition.
81	Error/ FDC Head Select	nERROR nHDSEL	I/ OD12	A low on this input from the printer indicates that there is a error condition at the printer. Bit 3 of the Printer Status register reads the nERR input. Refer to Parallel Port description for use of this pin in ECP and EPP mode. See FDC Pin definition.
82	Autofeed Output/ FDC Density Select 0 (Note 4)	nALF/ nDRVDEN0	(OD14/OP14)/ OD14	This output goes low to cause the printer to automatically feed one line after each line is printed. The nALF output is the complement of bit 1 of the Printer Control Register. Refer to Parallel Port description for use of this pin in ECP and EPP mode. See FDC Pin definition.
83	Strobe Output/ FDC Drive Select 0 (Note 4)	nSTROBE/ nDS0	(OD14/OP14)/ OD14	An active low pulse on this output is used to strobe the printer data into the printer. The nSTROBE output is the complement of bit 0 of the Printer Control Register. Refer to Parallel Port description for use of this pin in ECP and EPP mode. See FDC Pin definition.

TQFP/STQFP TQN/STQN PIN #	NAME	SYMBOL	BUFFER TYPE PER FUNCTION[1]	DESCRIPTION
GENERAL PURPOSE I/O				
6, 32-39, 40-47 48, 54-56, 57-59	General Purpose I/O *(Note 9)*	GP24, GP30-GP37 GP40-GP47 GP10, GP15-GP17, GP20-GP22	(I/O8/OD8)	Dedicated General Purpose Input/Output.
49	General Purpose I/O (System Option) (Note 5) *(Note 9)*	GP11/ (SYSOPT)	(I/O8/OD8)	General Purpose Input/Output. At the trailing edge of hardware reset the GP11 pin is latched to determine the configuration base address: 0 = Index Base I/O Address 02E Hex; 1 = Index Base I/O Address 04E Hex.
50	General Purpose I/O/ System Mgt. Interrupt *(Note 9)*	GP12/ nIO_SMI	(I/O12/OD12)/ (O12/OD12)	General Purpose Input/Output. Active low System Management Interrupt Output.
51	General Purpose I/O/ IRQ Input 1 *(Note 9)*	GP13/ IRQIN1	(I/O8/OD8)/ I	General Purpose Input/Output. External Interrupt Input. Steerable onto one of the 15 Serial IRQs.
52	General Purpose I/O/ IRQ Input 2 *(Note 9)*	GP14/ IRQIN2	(I/O8/OD8)/ I	General Purpose Input/Output. External Interrupt Input. Steerable onto one of the 15 Serial IRQs.
64	General Purpose I/O/ Floppy on Parallel Port *(Note 9)*	GP23/ FDC_PP	(I/O8/OD8)/ I	General Purpose Input/Output. Floppy on the Parallel Port Indication.
CLOCK PINS				
19	14MHz Clock	CLOCKI	IS	14.318MHz Clock Input.
POWER PINS				
53,65,93	VCC (Note 6)	VCC		+3.3 Volt Supply Voltage.
18	VTR (Note 6)	VTR		+3.3 Volt Standby Voltage.
7,31, 60,76	VSS	VSS		Ground.

Note: The "n" as the first letter of a symbol indicates an "Active Low" signal.

Note 1: Buffer types per function on multiplexed pins are separated by a slash “/”. Buffer types in parenthesis represent multiple buffer types for a single pin function.

Note 2: The nLPCPD pin may be tied high.

Note 3: The FDD output pins multiplexed in the PARALLEL PORT INTERFACE are OD drivers only and are not affected by the FDD Output Driver Controls (see subsection CR05 in the Configuration section).

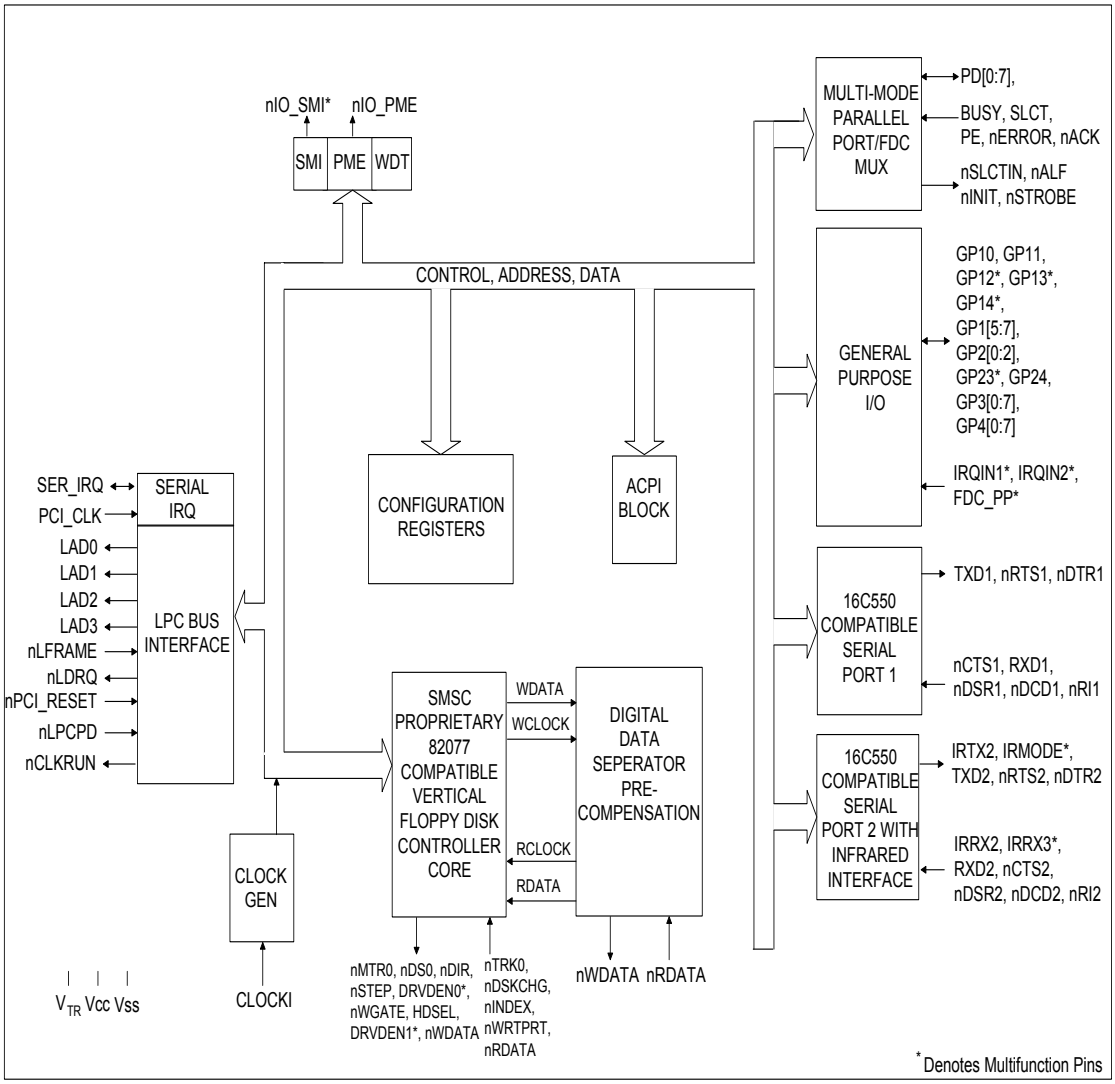
Note 4: Active (push-pull) output drivers are required on these pins in the enhanced parallel port modes.
Note 5: The GP11/SYSOPT pin requires an external pulldown resistor to put the base IO address for configuration at 0x02E. An external pullup resistor is required to move the base IO address for configuration to 0x04E.
Note 6: V_{CC} must not be greater than 0.5V above V_{TR}.
Note 7: This pin is output only and is powered by VTR.
Note 8: Ring indicator pins nRI1 and nRI2 have input buffers into the wakeup logic that are powered by VTR. These pins are also inputs to VCC powered logic.
Note 9: GP10-GP17, GP20-GP24 and GP30-GP37 pins have input buffers into the wakeup logic that are powered by VTR. GP40-47 pins are powered by VCC even as inputs.

Buffer Type Description

I	Input TTL Compatible.
IS	Input with Schmitt Trigger.
O6	Output, 6mA sink, 3mA source.
O8	Output, 8mA sink, 4mA source.
OD8	Open Drain Output, 8mA sink.
IO8	Input/Output, 8mA sink, 4mA source.
O12	Output, 12mA sink, 6mA source.
OD12	Open Drain Output, 12mA sink.
IO12	Input/Output, 12mA sink, 6mA source.
OD14	Open Drain Output, 14mA sink.
OP14	Output, 14mA sink, 14mA source.
IOP14	Input/Output, 14mA sink, 14mA source. Backdrive protected.
PCI_I	Input. These pins meet the PCI 3.3V AC and DC Characteristics. (Note 1)
PCI_O	Output. These pins meet the PCI 3.3V AC and DC Characteristics. (Note 1)
PCI_OD	Open Drain Output. These pins meet the PCI 3.3V AC and DC Characteristics. (Note 1)
PCI_IO	Input/Output. These pins meet the PCI 3.3V AC and DC Characteristics. (Note 1)
PCI_ICLK	Clock Input. These pins meet the PCI 3.3V AC and DC Characteristics and timing. (Note 2)

Note 1. See the PCI Local Bus Specification, Revision 2.1, Section 4.2.2.
Note 2. See the PCI Local Bus Specification, Revision 2.1, Section 4.2.2. and 4.2.3.

BLOCK DIAGRAM



3.3 Volt Operation / 5 Volt Tolerance

The LPC47N227 is a 3.3 Volt part. It is intended solely for 3.3V applications. Non-LPC bus pins are 5V tolerant; that is, the input voltage is 5.5V max, and the I/O buffer output pads are backdrive protected.

The LPC interface pins are 3.3 V only. These signals meet PCI DC specifications for 3.3V signaling. These pins are:

- LAD[3:0]
- nLFRAME
- nLDRQ
- nLPCPD

The input voltage for all other pins is 5.5V max. These pins include all non-LPC Bus pins and the following pins:

- nPCI_RESET
- PCI_CLK
- SER_IRQ
- nCLKRUN
- nIO_PME

Power Functionality

The LPC47N227 has two power planes: VCC and VTR.

VCC Power

The LPC47N227 is a 3.3 Volt part. The VCC supply is 3.3 Volts (nominal). See the Operational Description Section and the Maximum Current Values subsection.

VTR Support

The LPC47N227 requires a trickle supply (V_{TR}) to provide sleep current for the programmable wake-up events in the PME interface when V_{CC} is removed. The VTR supply is 3.3 Volts (nominal). See the Operational Description Section. The maximum VTR current that is required depends on the functions that are used in the part. See Trickle Power Functionality subsection and the Maximum Current Values subsection. If the LPC47N227 is not intended to provide wake-up capabilities on standby current, V_{TR} can be connected to V_{CC}. The V_{TR} pin generates a V_{TR} Power-on-Reset signal to initialize these components.

Note: If V_{TR} is to be used for programmable wake-up events when V_{CC} is removed, V_{TR} must be at its full minimum potential at least 10 μs before V_{CC} begins a power-on cycle. When V_{TR} and V_{CC} are fully powered, the potential difference between the two supplies must not exceed 500mV.

Internal PWRGOOD

An internal PWRGOOD logical control is included to minimize the effects of pin-state uncertainty in the host interface as V_{CC} cycles on and off. When the internal PWRGOOD signal is "1" (active), V_{CC} > 2.3V (nominal), and the LPC47N227 host interface is active. When the internal PWRGOOD signal is "0" (inactive), $V_{CC} \leq$ 2.3V (nominal), and the LPC47N227 host interface is inactive; that is, LPC bus reads and writes will not be decoded.

The LPC47N227 device pins nIO_PME, nRI1, nRI2, and most GPIOs (as input) are part of the PME interface and remain active when the internal PWRGOOD signal has gone inactive, provided V_{TR} is powered. See Trickle Power Functionality section.

Trickle Power Functionality

When the LPC47N227 is running under VTR only, the PME wakeup events are active and (if enabled) able to assert the nIO_PME pin active low. The following lists the wakeup events:

- UART 1 Ring Indicator
- UART 2 Ring Indicator
- GPIOs for wakeup. See below.

The following requirements apply to all I/O pins that are specified to be 5 volt tolerant.

- I/O buffers that are wake-up event compatible are powered by VCC. Under VTR power (VCC=0), these pins may only be configured as inputs. These pins have input buffers into the wakeup logic that are powered by VTR.

- I/O buffers that may be configured as either push-pull or open drain under VTR power (VCC=0), are powered by VTR. This means they will, at a minimum, source their specified current from VTR even when VCC is present. This applies to the nIO_PME pin only.

The GPIOs that are used for PME wakeup inputs are GP10-GP17, GP20-GP24, GP30-GP37. These GPIOs function as follows:

- Buffers are powered by VCC, but in the absence of VCC they are backdrive protected (they do not impose a load on any external VTR powered circuitry). They are wakeup compatible as inputs under VTR power. These pins have input buffers into the wakeup logic that are powered by VTR.

All GPIOs listed above are for PME wakeup as a GPIO function (or alternate function).

See the Table in the GPIO section for more information.

The following list summarizes the blocks, registers and pins that are powered by VTR.

- PME interface block
- Runtime register block (includes all PME, SMI, GP data registers)
- Pins for PME Wakeup:
  - GPIOs (GP10-GP17, GP20-GP24, GP30-GP37) as input
  - nIO_PME as input
  - nRI1, nRI2 as input

Maximum Current Values

See the “Operational Description” section for the maximum current values.

The maximum VTR current, I_{TR}, is given with all outputs open (not loaded), and all inputs in a fixed state (i.e., 0V or 3.3V). The total maximum current for the part is the unloaded value PLUS the maximum current sourced by the pin that is driven by VTR. The pin that is powered by VTR (as output) is nIO_PME. This pin, if configured as a push-pull output, will source a minimum of 6mA at 2.4V when driving.

The maximum VCC current, I_{CC}, is given with all outputs open (not loaded), and all inputs in a fixed state (i.e., 0V or 3.3V).

Power Management Events (PME/SCI)

The LPC47N227 offers support for Power Management Events (PMEs), also referred to as System Control Interrupt (SCI) events. The terms PME and SCI are used synonymously throughout this document to refer to the indication of an event to the chipset via the assertion of the nIO_PME output signal on pin 17. See the “PME Support” section. Do not connect the nIO_PME pin to PCI PME pins.

FUNCTIONAL DESCRIPTION

Super I/O Registers

The address map, shown below in Table 1, shows the addresses of the different blocks of the Super I/O immediately after power up. The base addresses of the FDC, serial and parallel ports, runtime register block and configuration register block can be moved via the configuration registers. Some addresses are used to access more than one register.

Host Processor Interface (LPC)

The host processor communicates with the LPC47N227 through a series of read/write registers via the LPC interface. The port addresses for these registers are shown in Table 1. Register access is accomplished through I/O cycles or DMA transfers. All registers are 8 bits wide.

Table 1 - Super I/O Block Addresses

ADDRESS	BLOCK NAME	NOTES
Base+(0-5) and +(7)	Floppy Disk	
Base+(0-7)	Serial Port Com 1	
Base1+(0-7) Base2+(0-7)	Serial Port Com 2	IR Support FIR and CIR
 Base+(0-3) Base+(0-7) Base+(0-3), +(400-402) Base+(0-7), +(400-402)	Parallel Port SPP EPP ECP ECP+EPP+SPP	
Base + (0-F)	Runtime Registers	
Base + (0-1)	Configuration	

Note 1: Refer to the configuration register descriptions for setting the base address.

LPC Interface

The following sub-sections specify the implementation of the LPC bus.

LPC Interface Signal Definition

The signals required for the LPC bus interface are described in the table below. LPC bus signals use PCI 33MHz electrical signal characteristics.

SIGNAL NAME	TYPE	DESCRIPTION
LAD[3:0]	I/O	LPC address/data bus. Multiplexed command, address and data bus.
nLFRAME	Input	Frame signal. Indicates start of new cycle and termination of broken cycle
nPCI_RESET	Input	PCI Reset. Used as LPC Interface Reset.
nLDRQ	Output	Encoded DMA/Bus Master request for the LPC interface.
nIO_PME	OD	Power Mgt Event signal. Allows the LPC47N227 to request wakeup.
nLPCPD	Input	Powerdown Signal. Indicates that the LPC47N227 should prepare for power to be shut on the LPC interface.
SER_IRQ	I/O	Serial IRQ.
PCI_CLK	Input	PCI Clock.
nCLKRUN	I/OD	Clock Run. Allows the LPC47N227 to request the stopped PCI_CLK be started.

LPC Cycles

The following cycle types are supported by the LPC protocol.

CYCLE TYPE	TRANSFER SIZE
I/O Write	1 Byte
I/O Read	1 Byte
DMA Write	1 Byte
DMA Read	1 Byte

The LPC47N227 ignores cycles that it does not support.

Field Definitions

The data transfers are based on specific fields that are used in various combinations, depending on the cycle type. These fields are driven onto the LAD[3:0] signal lines to communicate address, control and data information over the LPC bus between the host and the LPC47N227. See the *Low Pin Count (LPC) Interface Specification* Revision 1.0 from Intel, Section 4.2 for definition of these fields.

nLFRAME Usage

nLFRAME is used by the host to indicate the start of cycles and the termination of cycles due to an abort or time-out condition. This signal is to be used by the LPC47N227 to know when to monitor the bus for a cycle.

This signal is used as a general notification that the LAD[3:0] lines contain information relative to the start or stop of a cycle, and that the LPC47N227 monitors the bus to determine whether the cycle is intended for it. The use of nLFRAME allows the LPC47N227 to enter a lower power state internally. There is no need for the LPC47N227 to monitor the bus when it is inactive, so it can decouple its state machines from the bus, and internally gate its clocks.

When the LPC47N227 samples nLFRAME active, it immediately stops driving the LAD[3:0] signal lines on the next clock and monitor the bus for new cycle information.

The nLFRAME signal functions as described in the Low Pin Count (LPC) Interface Specification Revision 1.0.

I/O Read and Write Cycles

The LPC47N227 is the target for I/O cycles. I/O cycles are initiated by the host for register or FIFO accesses, and will generally have minimal Sync times. The minimum number of wait-states between bytes is 1. EPP cycles will depend on the speed of the external device, and may have much longer Sync times.

Data transfers are assumed to be exactly 1-byte. If the CPU requested a 16 or 32-bit transfer, the host will break it up into 8-bit transfers.

See the *Low Pin Count (LPC) Interface Specification* Reference, Section 5.2, for the sequence of cycles for the I/O Read and Write cycles.

DMA Read and Write Cycles

DMA read cycles involve the transfer of data from the host (main memory) to the LPC47N227. DMA write cycles involve the transfer of data from the LPC47N227 to the host (main memory). Data will be coming from or going to a FIFO and will have minimal Sync times. Data transfers to/from the LPC47N227 are 1 byte.

See the *Low Pin Count (LPC) Interface Specification* Reference, Section 6.4, for the field definitions and the sequence of the DMA Read and Write cycles.

DMA Protocol

DMA on the LPC bus is handled through the use of the nLDRQ line from the LPC47N227 and special encodings on LAD[3:0] from the host.

The DMA mechanism for the LPC bus is described in the Low Pin Count (LPC) Specification Revision 1.0.

Power Management

CLOCKRUN Protocol

See the *Low Pin Count (LPC) Interface Specification* Reference, Section 8.1.

LPCPD Protocol

The LPC47N227 will function properly if the nLPCPD signal goes active and then inactive again without nPCI_RESET becoming active. This is a requirement for notebook power management functions.

Although the LPC Bus spec 1.0 section 8.2 states, "After nLPCPD goes back inactive, the LPC I/F will always be reset using nLRST", this statement does not apply for mobile systems. nLRST (nPCI_RESET) will not occur if the LPC Bus power was not removed. For example, when exiting a "light" sleep state (ACPI S1, APM POS), nLRST (nPCI_RESET) will not occur. When exiting a "deeper" sleep state (ACPI S3-S5, APM STR, STD, soft-off), nLRST (nPCI_RESET) will occur.

The nLPCPD pin is implemented as a "local" powergood for the LPC interface in the LPC47N227. It is not used as a global powergood for the chip. It is used to reset the LPC block and hold it in reset.

An internal powergood is implemented in LPC47N227 to minimize power dissipation in the entire chip.

Prior to going to a low-power state, the system will assert the nLPCPD signal. It will go active at least 30 microseconds prior to the LCLK (PCI_CLK) signal stopping low and power being shut to the other LPC I/F signals.

Upon recognizing nLPCPD active, the LPC47N227 will tri-state the nLDRQ signal and do so until nLPCPD goes back active.

Upon recognizing nLPCPD inactive, the LPC47N227 will drive its nLDRQ signal high.

See the *Low Pin Count (LPC) Interface Specification* Reference, Section 8.2.

SYNC Protocol

See the *Low Pin Count (LPC) Interface Specification* Reference, Section 4.2.1.8 for a table of valid SYNC values.

Typical Usage

The SYNC pattern is used to add wait states. For read cycles, the LPC47N227 immediately drives the SYNC pattern upon recognizing the cycle. The host immediately drives the sync pattern for write cycles. If the LPC47N227 needs to assert wait states, it does so by driving 0101 or 0110 on LAD[3:0] until it is ready, at which point it will drive 0000 or 1001. The LPC47N227 will choose to assert 0101 or 0110, but not switch between the two patterns.

The data (or wait state SYNC) will immediately follow the 0000 or 1001 value.

The SYNC value of 0101 is intended to be used for normal wait states, wherein the cycle will complete within a few clocks. The LPC47N227 uses a SYNC of 0101 for all wait states in a DMA transfer.

The SYNC value of 0110 is intended to be used where the number of wait states is large. This is provided for EPP cycles, where the number of wait states could be quite large (>1 microsecond). However, the LPC47N227 uses a SYNC of 0110 for all wait states in an I/O transfer.

The SYNC value is driven within 3 clocks.

SYNC Timeout

The SYNC value is driven within 3 clocks. If the host observes 3 consecutive clocks without a valid SYNC pattern, it will abort the cycle.

The LPC47N227 does not assume any particular timeout. When the host is driving SYNC, it may have to insert a very large number of wait states, depending on PCI latencies and retries.

SYNC Patterns and Maximum Number of SYNCS

If the SYNC pattern is 0101, then the host assumes that the maximum number of SYNCs is 8.

If the SYNC pattern is 0110, then no maximum number of SYNCs is assumed. The LPC47N227 has protection mechanisms to complete the cycle. This is used for EPP data transfers and will utilize the same timeout protection that is in EPP.

SYNC Error Indication

The LPC47N227 reports errors via the LAD[3:0] = 1010 SYNC encoding.

If the host was reading data from the LPC47N227, data will still be transferred in the next two nibbles. This data may be invalid, but it will be transferred by the LPC47N227. If the host was writing data to the LPC47N227, the data had already been transferred.

In the case of multiple byte cycles, such as DMA cycles, an error SYNC terminates the cycle. Therefore, if the host is transferring 4 bytes from a device, if the device returns the error SYNC in the first byte, the other three bytes will not be transferred.

I/O and DMA START Fields

I/O and DMA cycles use a START field of 0000.

Reset Policy

The following rules govern the reset policy:

1) When nPCI_RESET goes inactive (high), the clock is assumed to have been running for 100usec prior to the removal of the reset signal, so that everything is stable. This is the same reset active time after clock is stable that is used for the PCI bus.
2) When nPCI_RESET goes active (low):
   a) The host drives the nLFRAME signal high, tristates the LAD[3:0] signals, and ignores the nLDRQ signal.
   b) The LPC47N227 ignores nLFRAME, tri-states the LAD[3:0] pins and drives the nLDRQ signal inactive (high).

LPC Transfers

Wait State Requirements

I/O Transfers

The LPC47N227 inserts three wait states for an I/O read and two wait states for an I/O write cycle. A SYNC of 0110 is used for all I/O transfers. The exception to this is for transfers where IOCHRDY would be deasserted in an ISA transfer (i.e., EPP or IrCC transfers) in which case the sync pattern of 0110 is used and a large number of syncs may be inserted (up to 330 which corresponds to a timeout of 10us).

DMA Transfers

The LPC47N227 inserts three wait states for a DMA read and four wait states for a DMA write cycle. A SYNC of 0101 is used for all DMA transfers.

See the example timing for the LPC cycles in the “Timing Diagrams” section.

FLOPPY DISK CONTROLLER

The Floppy Disk Controller (FDC) provides the interface between a host microprocessor and the floppy disk drives. The FDC integrates the functions of the Formatter/Controller, Digital Data Separator, Write Precompensation and Data Rate Selection logic for an IBM XT/AT compatible FDC. The true CMOS 765B core guarantees 100% IBM PC XT/AT compatibility in addition to providing data overflow and underflow protection.

The FDC is compatible to the 82077AA using SMSC's proprietary floppy disk controller core.

The LPC47N227 supports one floppy disk drive directly through the FDC interface pins and two floppy disk drives via the FDC interface on the parallel port pins. It can also be configured to support one drive on the FDC interface pins and one drive on the parallel port pins.

FDC Internal Registers

The Floppy Disk Controller contains eight internal registers that facilitate the interfacing between the host microprocessor and the disk drive. Table 2 shows the addresses required to access these registers. Registers other than the ones shown are not supported. The rest of the description assumes that the primary addresses have been selected.

Table 2 – Status, Data and Control Registers (Shown with base addresses of 3F0 and 370)

PRIMARY ADDRESS	SECONDARY ADDRESS	R/W	REGISTER
3F0	370	R	Status Register A (SRA)
3F1	371	R	Status Register B (SRB)
3F2	372	R/W	Digital Output Register (DOR)
3F3	373	R/W	Tape Drive Register (TDR)
3F4	374	R	Main Status Register (MSR)
3F4	374	W	Data Rate Select Register (DSR)
3F5	375	R/W	Data (FIFO)
3F6	376		Reserved
3F7	377	R	Digital Input Register (DIR)
3F7	377	W	Configuration Control Register (CCR)

Status Register A (SRA)

Address 3F0 READ ONLY

This register is read-only and monitors the state of the internal interrupt signal and several disk interface pins in PS/2 and Model 30 modes. The SRA can be accessed at any time when in PS/2 mode. In the PC/AT mode the data bus pins D0 - D7 are held in a high impedance state for a read of address 3F0.

PS/2 Mode

	7	6	5	4	3	2	1	0
	INT PENDING	nDRV2	STEP	nTRK0	HDSEL	nINDX	nWP	DIR
RESET COND.	0	1	0	N/A	0	N/A	N/A	0

BIT 0 DIRECTION
Active high status indicating the direction of head movement. A logic "1" indicates inward direction; a logic "0" indicates outward direction.

BIT 1 nWRITE PROTECT
Active low status of the WRITE PROTECT disk interface input. A logic "0" indicates that the disk is write protected.

BIT 2 nINDEX
Active low status of the INDEX disk interface input.

BIT 3 HEAD SELECT
Active high status of the HDSEL disk interface input. A logic "1" selects side 1 and a logic "0" selects side 0.

BIT 4 nTRACK 0
Active low status of the TRK0 disk interface input.

BIT 5 STEP
Active high status of the STEP output disk interface output pin.

BIT 6 nDRV2
This function is not supported. This bit is always read as “1”.

BIT 7 INTERRUPT PENDING
Active high bit indicating the state of the Floppy Disk Interrupt output.

PS/2 Model 30 Mode

	7	6	5	4	3	2	1	0
	INT PENDING	DRQ	STEP F/F	TRK0	nHDSEL	INDX	WP	nDIR
RESET COND.	0	0	0	N/A	1	N/A	N/A	1

BIT 0 nDIRECTION
Active low status indicating the direction of head movement. A logic "0" indicates inward direction; a logic "1" indicates outward direction.

BIT 1 WRITE PROTECT
Active high status of the WRITE PROTECT disk interface input. A logic "1" indicates that the disk is write protected.

BIT 2 INDEX
Active high status of the INDEX disk interface input.

BIT 3 nHEAD SELECT
Active low status of the HDSEL disk interface input. A logic "0" selects side 1 and a logic "1" selects side 0.

BIT 4 TRACK 0
Active high status of the TRK0 disk interface input.

BIT 5 STEP
Active high status of the latched STEP disk interface output pin. This bit is latched with the STEP output going active, and is cleared with a read from the DIR register, or with a hardware or software reset.

BIT 6 DMA REQUEST
Active high status of the DMA request pending.

BIT 7 INTERRUPT PENDING
Active high bit indicating the state of the Floppy Disk Interrupt.

Status Register B (SRB)

Address 3F1 READ ONLY
This register is read-only and monitors the state of several disk interface pins in PS/2 and model 30 modes. The SRB can be accessed at any time when in PS/2 mode. In the PC/AT mode the data bus pins D0 - D7 are held in a high impedance state for a read of address 3F1.

PS/2 Mode

	7	6	5	4	3	2	1	0
	1	1	DRIVE SEL0	WDATA TOGGLE	RDATA TOGGLE	WGATE	MOT EN1	MOT EN0
RESET COND.	1	1	0	0	0	0	0	0

BIT 0 MOTOR ENABLE 0
Active high status of the MTR0 disk interface output pin. This bit is low after a hardware reset and unaffected by a software reset.

BIT 1 MOTOR ENABLE 1
Active high status of the MTR1 disk interface output pin. This bit is low after a hardware reset and unaffected by a software reset.

BIT 2 WRITE GATE
Active high status of the WGATE disk interface output.

BIT 3 READ DATA TOGGLE

Every inactive edge of the RDATA input causes this bit to change state.

BIT 4 WRITE DATA TOGGLE
Every inactive edge of the WDATA input causes this bit to change state.

BIT 5 DRIVE SELECT 0
Reflects the status of the Drive Select 0 bit of the DOR (address 3F2 bit 0). This bit is cleared after a hardware reset and it is unaffected by a software reset.

BIT 6 RESERVED
Always read as a logic "1".

BIT 7 RESERVED
Always read as a logic "1".

PS/2 Model 30 Mode

	7	6	5	4	3	2	1	0
	nDRV2	nDS1	nDS0	WDATA F/F	RDATA F/F	WGATE F/F	nDS3	nDS2
RESET COND.	N/A	1	1	0	0	0	1	1

BIT 0 nDRIVE SELECT 2
The DS2 disk interface is not supported.

BIT 1 nDRIVE SELECT 3
The DS3 disk interface is not supported.

BIT 2 WRITE GATE
Active high status of the latched WGATE output signal. This bit is latched by the active going edge of WGATE and is cleared by the read of the DIR register.

BIT 3 READ DATA
Active high status of the latched RDATA output signal. This bit is latched by the inactive going edge of RDATA and is cleared by the read of the DIR register.

BIT 4 WRITE DATA
Active high status of the latched WDATA output signal. This bit is latched by the inactive going edge of WDATA and is cleared by the read of the DIR register. This bit is not gated with WGATE.

BIT 5 nDRIVE SELECT 0
Active low status of the DS0 disk interface output.

BIT 6 nDRIVE SELECT 1
Active low status of the DS1 disk interface output.

BIT 7 nDRV2
Active low status of the DRV2 disk interface input. Note: This function is not supported.

Digital Output Register (DOR)

Address 3F2 READ/WRITE
The DOR controls the drive select and motor enables of the disk interface outputs. It also contains the enable for the DMA logic and a software reset bit. The contents of the DOR are unaffected by a software reset. The DOR can be written to at any time.

	7	6	5	4	3	2	1	0
	MOT EN3	MOT EN2	MOT EN1	MOT EN0	DMAEN	nRESET	DRIVE SEL1	DRIVE SEL0
RESET COND.	0	0	0	0	0	0	0	0

BIT 0 and 1 DRIVE SELECT
These two bits are binary encoded for the drive selects, thereby allowing only one drive to be selected at one time.

BIT 2 nRESET
A logic "0" written to this bit resets the Floppy disk controller. This reset will remain active until a logic "1" is written to this bit. This software reset does not affect the DSR and CCR registers, nor does it affect the other bits of the DOR register. The minimum reset duration required is 100ns, therefore toggling this bit by consecutive writes to this register is a valid method of issuing a software reset.

BIT 3 DMAEN

PC/AT and Model 30 Mode:
Writing this bit to logic "1" will enable the DMA and interrupt functions. This bit being a logic "0" will disable the DMA and interrupt functions. This bit is a logic "0" after a reset and in these modes.

PS/2 Mode: In this mode the DMA and interrupt functions are always enabled. During a reset, this bit will be cleared to a logic "0".

BIT 4 MOTOR ENABLE 0
This bit controls the MTR0 disk interface output. A logic "1" in this bit will cause the output pin to go active.

BIT 5 MOTOR ENABLE 1
This bit controls the MTR1 disk interface output. A logic "1" in this bit will cause the output pin to go active.

BIT 6 MOTOR ENABLE 2
The MTR2 disk interface output is not supported.

BIT 7 MOTOR ENABLE 3
The MTR3 disk interface output is not supported.

DRIVE	DOR VALUE
0	1CH
1	2DH

Table 3 – Internal 2 Drive Decode (Normal)

DIGITAL OUTPUT REGISTER				DRIVE SELECT OUTPUTS (ACTIVE LOW)		MOTOR ON OUTPUTS (ACTIVE LOW)	
Bit 5	Bit 4	Bit1	Bit 0	nDS1	nDS0	nMTR1	nMTR0
X	1	0	0	1	0	nBIT 5	nBIT 4
1	X	0	1	0	1	nBIT 5	nBIT 4
0	0	X	X	1	1	nBIT 5	nBIT 4

Table 4 – Internal 2 Drive Decode (Drives 0 and 1 Swapped)

DIGITAL OUTPUT REGISTER				DRIVE SELECT OUTPUTS (ACTIVE LOW)		MOTOR ON OUTPUTS (ACTIVE LOW)	
Bit 5	Bit 4	Bit1	Bit 0	nDS1	nDS0	nMTR1	nMTR0
X	1	0	0	0	1	nBIT 4	nBIT 5
1	X	0	1	1	0	nBIT 4	nBIT 5
0	0	X	X	1	1	nBIT 4	nBIT 5

Tape Drive Register (TDR)

Address 3F3 READ/WRITE
The Tape Drive Register (TDR) is included for 82077 software compatibility and allows the user to assign tape support to a particular drive during initialization. Any future references to that drive automatically invokes tape support. The TDR Tape Select bits TDR.[1:0] determine the tape drive number. Table 5 illustrates the Tape Select Bit encoding. Note that drive 0 is the boot device and cannot be assigned tape support. The remaining Tape Drive Register bits TDR.[7:2] are tristated when read. The TDR is unaffected by a software reset.

Table 5 – Tape Select Bits

TAPE SEL1 (TDR.1)	TAPE SEL0 (TDR.0)	DRIVE SELECTED
0	0	None
0	1	1
1	0	2
1	1	3

Note: The LPC47N227 supports one floppy drive directly on the FDC interface pins and two floppy drives on the Parallel Port.

Normal Floppy Mode

Normal mode. Register 3F3 contains only bits 0 and 1. When this register is read, bits 2 - 7 are '0'.

	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
REG 3F3	0	0	0	0	0	0	tape sel1	tape sel0

Enhanced Floppy Mode 2 (OS2)

Register 3F3 for Enhanced Floppy Mode 2 operation.

	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
REG 3F3	Reserved	Reserved	Drive Type ID		Floppy Boot Drive		tape sel1	tape sel0

Table 6 – Drive Type ID

DIGITAL OUTPUT REGISTER		REGISTER 3F3 - DRIVE TYPE ID	
Bit 1	Bit 0	Bit 5	Bit 4
0	0	CR06 - B1	CR06 - B0
0	1	CR06 - B3	CR06 - B2
1	0	CR06 - B5	CR06 - B4
1	1	CR06 - B7	CR06 - B6

Note: CR06-Bx = Configuration Register 06, Bit x.

Data Rate Select Register (DSR)

Address 3F4 WRITE ONLY

This register is write only. It is used to program the data rate, amount of write precompensation, power down status, and software reset. The data rate is programmed using the Configuration Control Register (CCR) not the DSR, for PC/AT and PS/2 Model 30 applications. Other applications can set the data rate in the DSR. The data rate of the floppy controller is the most recent write of either the DSR or CCR. The DSR is unaffected by a software reset. A hardware reset will set the DSR to 02H, which corresponds to the default precompensation setting and 250 Kbps.

	7	6	5	4	3	2	1	0
	S/W RESET	POWER DOWN	0	PRE-COMP2	PRE-COMP1	PRE-COMP0	DRATE SEL1	DRATE SEL0
RESET COND.	0	0	0	0	0	0	1	0

BIT 0 and 1 DATA RATE SELECT
These bits control the data rate of the floppy controller. See Table 8 for the settings corresponding to the individual data rates. The data rate select bits are unaffected by a software reset, and are set to 250 Kbps after a hardware reset.

BIT 2 through 4 PRECOMPENSATION SELECT
These three bits select the value of write precompensation that will be applied to the WDATA output signal. Table 7 shows the precompensation values for the combination of these bits settings. Track 0 is the default starting track number to start precompensation. This starting track number can be changed by the configure command.

BIT 5 UNDEFINED
Should be written as a logic "0".

BIT 6 LOW POWER
A logic "1" written to this bit will put the floppy controller into manual low power mode. The floppy controller clock and data separator circuits will be turned off. The controller will come out of manual low power mode after a software reset or access to the Data Register or Main Status Register.

BIT 7 SOFTWARE RESET
This active high bit has the same function as the DOR RESET (DOR bit 2) except that this bit is self clearing.
Note: The DSR is Shadowed in the Floppy Data Rate Select Shadow Register, located in the Configuration section (CR14).

Table 7 – Precompensation Delays

PRECOMP 432	PRECOMPENSATION DELAY (nsec)	
	<2Mbps	2Mbps
111	0.00	0
001	41.67	20.8
010	83.34	41.7
011	125.00	62.5
100	166.67	83.3
101	208.33	104.2
110	250.00	125
000	Default	Default

Default: See Table 10

Table 8 – Data Rates

DRIVE RATE		DATA RATE		DATA RATE		DENSEL	DRATE(1)	
DRT1	DRT0	SEL1	SEL0	MFM	FM		1	0
0	0	1	1	1Meg	---	1	1	1
0	0	0	0	500	250	1	0	0
0	0	0	1	300	150	0	0	1
0	0	1	0	250	125	0	1	0
0	1	1	1	1Meg	---	1	1	1
0	1	0	0	500	250	1	0	0
0	1	0	1	500	250	0	0	1
0	1	1	0	250	125	0	1	0
1	0	1	1	1Meg	---	1	1	1
1	0	0	0	500	250	1	0	0
1	0	0	1	2Meg	---	0	0	1
1	0	1	0	250	125	0	1	0

Drive Rate Table (Recommended) 00 = 360K, 1.2M, 720K, 1.44M and 2.88M Vertical Format
01 = 3-Mode Drive
10 = 2 Meg Tape

Note 1: The DRATE and DENSEL values are mapped onto the DRVDEN pins.

Table 9 – DRVDEN Mapping0

DT1	DT0	DRVDEN1 (1)	DRVDEN0 (1)	DRIVE TYPE
0	0	DRATE0	DENSEL	4/2/1 MB 3.5" 2/1 MB 5.25" FDDS 2/1.6/1 MB 3.5" (3-MODE)
1	0	DRATE0	DRATE1	
0	1	DRATE0	nDENSEL	PS/2
1	1	DRATE1	DRATE0	

Table 10 – Default Precompensation Delays

DATA RATE	PRECOMPENSATION DELAYS
2 Mbps	20.8 ns
1 Mbps	41.67 ns
500 Kbps	125 ns
300 Kbps	125 ns
250 Kbps	125 ns

Main Status Register (MSR)

Address 3F4 READ ONLY

The Main Status Register is a read-only register and indicates the status of the disk controller. The Main Status Register can be read at any time. The MSR indicates when the disk controller is ready to receive data via the Data Register. It should be read before each byte transferring to or from the data register except in DMA mode. No delay is required when reading the MSR after a data transfer.

7	6	5	4	3	2	1	0
RQM	DIO	NON DMA	CMD BUSY	Reserved	Reserved	DRV1 BUSY	DRV0 BUSY

BIT 0 - 1 DRV x BUSY

These bits are set to 1s when a drive is in the seek portion of a command, including implied and overlapped seeks and recalibrates.

BIT 4 COMMAND BUSY

This bit is set to a 1 when a command is in progress. This bit will go active after the command byte has been accepted and goes inactive at the end of the results phase. If there is no result phase (Seek, Recalibrate commands), this bit is returned to a 0 after the last command byte.

BIT 5 NON-DMA

This mode is selected in the SPECIFY command and will be set to a 1 during the execution phase of a command. This is for polled data transfers and helps differentiate between the data transfer phase and the reading of result bytes.

BIT 6 DIO

Indicates the direction of a data transfer once a RQM is set. A 1 indicates a read and a 0 indicates a write is required.

BIT 7 RQM
Indicates that the host can transfer data if set to a 1. No access is permitted if set to a 0.

Data Register (FIFO)

Address 3F5 READ/WRITE
All command parameter information, disk data and result status are transferred between the host processor and the floppy disk controller through the Data Register.

Data transfers are governed by the RQM and DIO bits in the Main Status Register.

The Data Register defaults to FIFO disabled mode after any form of reset. This maintains PC/AT hardware compatibility. The default values can be changed through the Configure command (enable full FIFO operation with threshold control). The advantage of the FIFO is that it allows the system a larger DMA latency without causing a disk error. Table 11 gives several examples of the delays with a FIFO.

The data is based upon the following formula:

$$\text{Threshold \#} \times \frac{1}{\text{DATA RATE}} \times 8 - 1.5\ \mu s = \text{DELAY}$$

At the start of a command, the FIFO action is always disabled and command parameters are sent based upon the RQM and DIO bit settings. As the command execution phase is entered, the FIFO is cleared of any data to ensure that invalid data is not transferred.

An overrun or underrun will terminate the current command and the transfer of data. Disk writes will complete the current sector by generating a 00 pattern and valid CRC. Reads require the host to remove the remaining data so that the result phase may be entered.

Table 11 – FIFO Service Delay

FIFO THRESHOLD EXAMPLES	MAXIMUM DELAY TO SERVICING AT 2 Mbps DATA RATE
1 byte	1 x 4 μs - 1.5 μs = 2.5 μs
2 bytes	2 x 4 μs - 1.5 μs = 6.5 μs
8 bytes	8 x 4 μs - 1.5 μs = 30.5 μs
15 bytes	15 x 4 μs - 1.5 μs = 58.5 μs

FIFO THRESHOLD EXAMPLES	MAXIMUM DELAY TO SERVICING AT 1 Mbps DATA RATE
1 byte	1 x 8 μs - 1.5 μs = 6.5 μs
2 bytes	2 x 8 μs - 1.5 μs = 14.5 μs
8 bytes	8 x 8 μs - 1.5 μs = 62.5 μs
15 bytes	15 x 8 μs - 1.5 μs = 118.5 μs

FIFO THRESHOLD EXAMPLES	MAXIMUM DELAY TO SERVICING AT 500 Kbps DATA RATE
1 byte	1 x 16 μs - 1.5 μs = 14.5 μs
2 bytes	2 x 16 μs - 1.5 μs = 30.5 μs
8 bytes	8 x 16 μs - 1.5 μs = 126.5 μs
15 bytes	15 x 16 μs - 1.5 μs = 238.5 μs

Digital Input Register (DIR)

Address 3F7 READ ONLY
This register is read-only in all modes.

PC-AT Mode

	7	6	5	4	3	2	1	0
	DSK CHG	0	0	0	0	0	0	0
RESET COND.	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A

BIT 0 - 6 UNDEFINED
The data bus outputs D0 - 6 are read as '0'.

BIT 7 DSKCHG
This bit monitors the pin of the same name and reflects the opposite value seen on the disk cable or the value programmed in the Force FDD Status Change Register (CR17). See the Configuration section for register description.

PS/2 Mode

	7	6	5	4	3	2	1	0
	DSK CHG	1	1	1	1	DRATE SEL1	DRATE SEL0	nHIGH nDENS
RESET COND.	N/A	N/A	N/A	N/A	N/A	N/A	N/A	1

BIT 0 nHIGH DENS
This bit is low whenever the 500 Kbps or 1 Mbps data rates are selected, and high when 250 Kbps and 300 Kbps are selected.

BITS 1 - 2 DATA RATE SELECT
These bits control the data rate of the floppy controller. See Table 8 for the settings corresponding to the individual data rates. The data rate select bits are unaffected by a software reset, and are set to 250 Kbps after a hardware reset.

BITS 3 - 6 UNDEFINED
Always read as a logic "1"

BIT 7 DSKCHG
This bit monitors the pin of the same name and reflects the opposite value seen on the disk cable or the value programmed in the Force Disk Change Register (CR17). See the Configuration section for register description.

Model 30 Mode

	7	6	5	4	3	2	1	0
	DSK CHG	0	0	0	DMAEN	NOPREC	DRATE SEL1	DRATE SEL0
RESET COND.	N/A	0	0	0	0	0	1	0

BITS 0 - 1 DATA RATE SELECT
These bits control the data rate of the floppy controller. See Table 8 for the settings corresponding to the individual data rates. The data rate select bits are unaffected by a software reset, and are set to 250 Kbps after a hardware reset.

BIT 2 NOPREC
This bit reflects the value of NOPREC bit set in the CCR register.

BIT 3 DMAEN
This bit reflects the value of DMAEN bit set in the DOR register bit 3.

BITS 4 - 6 UNDEFINED
Always read as a logic "0"

BIT 7 DSKCHG
This bit monitors the pin of the same name and reflects the opposite value seen on the disk cable or the value programmed in the Force Disk Change Register (CR17). See the Configuration section for register description.

Configuration Control Register (CCR)

Address 3F7 WRITE ONLY
PC/AT and PS/2 Modes

	7	6	5	4	3	2	1	0
	0	0	0	0	0	0	DRATE SEL1	DRATE SEL0
RESET COND.	N/A	N/A	N/A	N/A	N/A	N/A	1	0

BIT 0 and 1 DATA RATE SELECT 0 and 1
These bits determine the data rate of the floppy controller. See Table 8 for the appropriate values.

BIT 2 - 7 RESERVED
Should be set to a logical "0".

PS/2 Model 30 Mode

	7	6	5	4	3	2	1	0
	0	0	0	0	0	NOPREC	DRATE SEL1	DRATE SEL0
RESET COND.	N/A	N/A	N/A	N/A	N/A	N/A	1	0

BIT 0 and 1 DATA RATE SELECT 0 and 1
These bits determine the data rate of the floppy controller. See Table 8 for the appropriate values.

BIT 2 NO PRECOMPENSATION
This bit can be set by software, but it has no functionality. It can be read by bit 2 of the DSR when in Model 30 register mode. Unaffected by software reset.

BIT 3 - 7 RESERVED
Should be set to a logical "0"

Table 9 shows the state of the DENSEL pin. The DENSEL pin is set high after a hardware reset and is unaffected by the DOR and the DSR resets.

Status Register Encoding

During the Result Phase of certain commands, the Data Register contains data bytes that give the status of the command just executed.

Table 12 – Status Register 0

BIT NO.	SYMBOL	NAME	DESCRIPTION
7,6	IC	Interrupt Code	00 - Normal termination of command. The specified command was properly executed and completed without error. 01 - Abnormal termination of command. Command execution was started, but was not successfully completed. 10 - Invalid command. The requested command could not be executed. 11 - Abnormal termination caused by Polling.
5	SE	Seek End	The FDC completed a Seek, Relative Seek or Recalibrate command (used during a Sense Interrupt Command).
4	EC	Equipment Check	The TRK0 pin failed to become a "1" after: 1. 80 step pulses in the Recalibrate command. 2. The Relative Seek command caused the FDC to step outward beyond Track 0.
3			Unused. This bit is always "0".
2	H	Head Address	The current head address.
1,0	DS1,0	Drive Select	The current selected drive.

Table 13 – Status Register 1

BIT NO.	SYMBOL	NAME	DESCRIPTION
7	EN	End of Cylinder	The FDC tried to access a sector beyond the final sector of the track (255D). Will be set if TC is not issued after Read or Write Data command.
6			Unused. This bit is always "0".
5	DE	Data Error	The FDC detected a CRC error in either the ID field or the data field of a sector.
4	OR	Overrun/ Underrun	Becomes set if the FDC does not receive CPU or DMA service within the required time interval, resulting in data overrun or underrun.
3			Unused. This bit is always "0".
2	ND	No Data	Any one of the following: 1. Read Data, Read Deleted Data command - the FDC did not find the specified sector. 2. Read ID command - the FDC cannot read the ID field without an error. 3. Read A Track command - the FDC cannot find the proper sector sequence.
1	NW	Not Writeable	WP pin became a "1" while the FDC is executing a Write Data, Write Deleted Data, or Format A Track command.
0	MA	Missing Address Mark	Any one of the following: 1. The FDC did not detect an ID address mark at the specified track after encountering the index pulse from the nINDEX pin twice. 2. The FDC cannot detect a data address mark or a deleted data address mark on the specified track.

Table 14 – Status Register 2

BIT NO.	SYMBOL	NAME	DESCRIPTION
7			Unused. This bit is always "0".
6	CM	Control Mark	Any one of the following: Read Data command - the FDC encountered a deleted data address mark. Read Deleted Data command - the FDC encountered a data address mark.
5	DD	Data Error in Data Field	The FDC detected a CRC error in the data field.
4	WC	Wrong Cylinder	The track address from the sector ID field is different from the track address maintained inside the FDC.
3			Unused. This bit is always "0".
2			Unused. This bit is always "0".
1	BC	Bad Cylinder	The track address from the sector ID field is different from the track address maintained inside the FDC and is equal to FF hex, which indicates a bad track with a hard error according to the IBM soft-sectored format.
0	MD	Missing Data Address Mark	The FDC cannot detect a data address mark or a deleted data address mark.

Table 15 – Status Register 3

BIT NO.	SYMBOL	NAME	DESCRIPTION
7			Unused. This bit is always "0".
6	WP	Write Protected	Indicates the status of the WRTPRT pin.
5			Unused. This bit is always "1".
4	T0	Track 0	Indicates the status of the TRK0 pin.
3			Unused. This bit is always "1".
2	HD	Head Address	Indicates the status of the HDSEL pin.
1,0	DS1,0	Drive Select	Indicates the status of the DS1, DS0 pins.

RESET

There are three sources of system reset on the FDC: the nPCI_RESET pin, a reset generated via a bit in the DOR, and a reset generated via a bit in the DSR. At power on, a Power On Reset initializes the FDC. All resets take the FDC out of the power down state.

All operations are terminated upon a nPCI_RESET, and the FDC enters an idle state. A reset while a disk write is in progress will corrupt the data and CRC.

On exiting the reset state, various internal registers are cleared, including the Configure command information, and the FDC waits for a new command. Drive polling will start unless disabled by a new Configure command.

nPCI_RESET Pin (Hardware Reset)
The nPCI_RESET pin is a global reset and clears all registers except those programmed by the Specify command. The DOR reset bit is enabled and must be cleared by the host to exit the reset state.

DOR Reset vs. DSR Reset (Software Reset)
These two resets are functionally the same. Both will reset the FDC core, which affects drive status information and the FIFO circuits. The DSR reset clears itself automatically while the DOR reset requires the host to manually clear it. DOR reset has precedence over the DSR reset. The DOR reset is set automatically upon a pin reset. The user must manually clear this reset bit in the DOR to exit the reset state.

MODES OF OPERATION
The FDC has three modes of operation, PC/AT mode, PS/2 mode and Model 30 mode. These are determined by the state of the Interface Mode bits (MFM and IDENT) in CR03[5,6].

PC/AT mode
The PC/AT register set is enabled, the DMA enable bit of the DOR becomes valid (controls the interrupt and DMA functions), and DENSEL is an active high signal.

PS/2 mode
This mode supports the PS/2 models 50/60/80 configuration and register set. The DMA bit of the DOR becomes a "don't care". The DMA and interrupt functions are always enabled, and DENSEL is active low.

Model 30 mode
This mode supports PS/2 Model 30 configuration and register set. The DMA enable bit of the DOR becomes valid (controls the interrupt and DMA functions), and DENSEL is active low.

DMA Transfers
DMA transfers are enabled with the Specify command and are initiated by the FDC by activating a DMA request cycle. DMA read, write and verify cycles are supported. The FDC supports two DMA transfer modes: single Transfer and Burst Transfer. Burst mode is enabled via CR05-Bit[2]. See the Configuration section.

Controller Phases
For simplicity, command handling in the FDC can be divided into three phases: Command, Execution, and Result. Each phase is described in the following sections.

Command Phase
After a reset, the FDC enters the command phase and is ready to accept a command from the host. For each of the commands, a defined set of command code bytes and parameter bytes has to be written to the FDC before the command phase is complete. (Please refer to Table 16 for the command set descriptions). These bytes of data must be transferred in the order prescribed.

Before writing to the FDC, the host must examine the RQM and DIO bits of the Main Status Register. RQM and DIO must be equal to "1" and "0" respectively before command bytes may be written. RQM is set false by the FDC after each write cycle until the received byte is processed. The FDC asserts RQM again to request each parameter byte of the command unless an illegal command condition is detected. After the last parameter byte is received, RQM remains "0" and the FDC automatically enters the next phase as defined by the command definition.

The FIFO is disabled during the command phase to provide for the proper handling of the "Invalid Command" condition.

Execution Phase
All data transfers to or from the FDC occur during the execution phase, which can proceed in DMA or non-DMA mode as indicated in the Specify command.

After a reset, the FIFO is disabled. Each data byte is transferred by a read/write or DMA cycle depending on the DMA mode. The Configure command can enable the FIFO and set the FIFO threshold value.

The following paragraphs detail the operation of the FIFO flow control. In these descriptions, <threshold> is defined as the number of bytes available to the FDC when service is requested from the host and ranges from 1 to 16. The parameter FIFOTHR, which the user programs, is one less and ranges from 0 to 15.

A low threshold value (i.e. 2) results in longer periods of time between service requests, but requires faster servicing of the request for both read and write cases. The host reads (writes) from (to) the FIFO until empty (full), then the transfer request goes inactive. The host must be very responsive to the service request. This is the desired case for use with a "fast" system.

A high value of threshold (i.e. 12) is used with a "sluggish" system by affording a long latency period after a service request, but results in more frequent service requests.

Non-DMA Mode - Transfers from the FIFO to the Host

The interrupt and RQM bit in the Main Status Register are activated when the FIFO contains (16-<threshold>) bytes or the last bytes of a full sector have been placed in the FIFO. The interrupt can be used for interrupt-driven systems, and RQM can be used for polled systems. The host must respond to the request by reading data from the FIFO. This process is repeated until the last byte is transferred out of the FIFO. The FDC will deactivate the interrupt and RQM bit when the FIFO becomes empty.

Non-DMA Mode - Transfers from the Host to the FIFO

The interrupt and RQM bit in the Main Status Register are activated upon entering the execution phase of data transfer commands. The host must respond to the request by writing data into the FIFO. The interrupt and RQM bit remain true until the FIFO becomes full. They are set true again when the FIFO has <threshold> bytes remaining in the FIFO. The FDC enters the result phase after the last byte is taken by the FDC from the FIFO (i.e. FIFO empty condition).

DMA Mode - Transfers from the FIFO to the Host

The FDC generates a DMA request cycle when the FIFO contains (16 - <threshold>) bytes, or the last byte of a full sector transfer has been placed in the FIFO. The DMA controller responds to the request by reading data from the FIFO. The FDC will deactivate the DMA request when the FIFO becomes empty by generating the proper sync for the data transfer.

DMA Mode - Transfers from the Host to the FIFO.

The FDC generates a DMA request cycle when entering the execution phase of the data transfer commands. The DMA controller responds by placing data in the FIFO. The DMA request remains active until the FIFO becomes full. The DMA request cycle is reasserted when the FIFO has <threshold> bytes

remaining in the FIFO. The FDC will terminate the DMA cycle after a TC, indicating that no more data is required.

Data Transfer Termination

The FDC supports terminal count explicitly through the TC cycle and implicitly through the underrun/overrun and end-of-track (EOT) functions. For full sector transfers, the EOT parameter can define the last sector to be transferred in a single or multi-sector transfer.

If the last sector to be transferred is a partial sector, the host can stop transferring the data in mid-sector, and the FDC will continue to complete the sector as if a TC cycle was received. The only difference between these implicit functions and TC cycle is that they return "abnormal termination" result status. Such status indications can be ignored if they were expected.

Note that when the host is sending data to the FIFO of the FDC, the internal sector count will be complete when the FDC reads the last byte from its side of the FIFO. There may be a delay in the removal of the transfer request signal of up to the time taken for the FDC to read the last 16 bytes from the FIFO. The host must tolerate this delay.

Result Phase

The generation of the interrupt determines the beginning of the result phase. For each of the commands, a defined set of result bytes has to be read from the FDC before the result phase is complete. These bytes of data must be read out for another command to start.

RQM and DIO must both equal "1" before the result bytes may be read. After all the result bytes have been read, the RQM and DIO bits switch to "1" and "0" respectively, and the CB bit is cleared, indicating that the FDC is ready to accept the next command.

Command Set/Descriptions

Commands can be written whenever the FDC is in the command phase. Each command has a unique set of needed parameters and status results. The FDC checks to see that the first byte is a valid command and, if valid, proceeds with the command. If it is invalid, an interrupt is issued. The user sends a Sense Interrupt Status command which returns an invalid command error. Refer to Table 16 for explanations of the various symbols used. Table 17 lists the required parameters and the results associated with each command that the FDC is capable of performing.

Table 16 – Description of Command Symbols

SYMBOL	NAME	DESCRIPTION
C	Cylinder Address	The currently selected address; 0 to 255.
D	Data Pattern	The pattern to be written in each sector data field during formatting.
D0, D1	Drive Select 0-1	Designates which drives are perpendicular drives on the Perpendicular Mode Command. A "1" indicates a perpendicular drive.
DIR	Direction Control	If this bit is 0, then the head will step out from the spindle during a relative seek. If set to a 1, the head will step in toward the spindle.
DS0, DS1	Disk Drive Select	DS1 DS0 DRIVE 0 0 Drive 0 0 1 Drive 1

SYMBOL	NAME	DESCRIPTION
DTL	Special Sector Size	By setting N to zero (00), DTL may be used to control the number of bytes transferred in disk read/write commands. The sector size (N = 0) is set to 128. If the actual sector (on the diskette) is larger than DTL, the remainder of the actual sector is read but is not passed to the host during read commands; during write commands, the remainder of the actual sector is written with all zero bytes. The CRC check code is calculated with the actual sector. When N is not zero, DTL has no meaning and should be set to FF HEX.
EC	Enable Count	When this bit is "1" the "DTL" parameter of the Verify command becomes SC (number of sectors per track).
EFIFO	Enable FIFO	This active low bit when a 0, enables the FIFO. A "1" disables the FIFO (default).
EIS	Enable Implied Seek	When set, a seek operation will be performed before executing any read or write command that requires the C parameter in the command phase. A "0" disables the implied seek.
EOT	End of Track	The final sector number of the current track.
GAP		Alters Gap 2 length when using Perpendicular Mode.
GPL	Gap Length	The Gap 3 size. (Gap 3 is the space between sectors excluding the VCO synchronization field).
H/HDS	Head Address	Selected head: 0 or 1 (disk side 0 or 1) as encoded in the sector ID field.
HLT	Head Load Time	The time interval that FDC waits after loading the head and before initializing a read or write operation. Refer to the Specify command for actual delays.
HUT	Head Unload Time	The time interval from the end of the execution phase (of a read or write command) until the head is unloaded. Refer to the Specify command for actual delays.
LOCK		Lock defines whether EFIFO, FIFOTHR, and PRETRK parameters of the CONFIGURE COMMAND can be reset to their default values by a "software Reset". (A reset caused by writing to the appropriate bits of either the DSR or DOR)
MFM	MFM/FM Mode Selector	A one selects the double density (MFM) mode. A zero selects single density (FM) mode.
MT	Multi-Track Selector	When set, this flag selects the multi-track operating mode. In this mode, the FDC treats a complete cylinder under head 0 and 1 as a single track. The FDC operates as this expanded track started at the first sector under head 0 and ended at the last sector under head 1. With this flag set, a multitrack read or write operation will automatically continue to the first sector under head 1 when the FDC finishes operating on the last sector under head 0.

SYMBOL	NAME	DESCRIPTION
N	Sector Size Code	This specifies the number of bytes in a sector. If this parameter is "00", then the sector size is 128 bytes. The number of bytes transferred is determined by the DTL parameter. Otherwise the sector size is (2 raised to the "N'th" power) times 128. All values up to "07" hex are allowable. "07"h would equal a sector size of 16k. It is the user's responsibility to not select combinations that are not possible with the drive. N SECTOR SIZE 00 128 Bytes 01 256 Bytes 02 512 Bytes 03 1024 Bytes … … 07 16K Bytes
NCN	New Cylinder Number	The desired cylinder number.
ND	Non-DMA Mode Flag	When set to 1, indicates that the FDC is to operate in the non-DMA mode. In this mode, the host is interrupted for each data transfer. When set to 0, the FDC operates in DMA mode.
OW	Overwrite	The bits D0-D3 of the Perpendicular Mode Command can only be modified if OW is set to 1. OW id defined in the Lock command.
PCN	Present Cylinder Number	The current position of the head at the completion of Sense Interrupt Status command.
POLL	Polling Disable	When set, the internal polling routine is disabled. When clear, polling is enabled.
PRETRK	Precompensation Start Track Number	Programmable from track 00 to FFH.
R	Sector Address	The sector number to be read or written. In multi-sector transfers, this parameter specifies the sector number of the first sector to be read or written.
RCN	Relative Cylinder Number	Relative cylinder offset from present cylinder as used by the Relative Seek command.
SC	Number of Sectors Per Track	The number of sectors per track to be initialized by the Format command. The number of sectors per track to be verified during a Verify command when EC is set.
SK	Skip Flag	When set to 1, sectors containing a deleted data address mark will automatically be skipped during the execution of Read Data. If Read Deleted is executed, only sectors with a deleted address mark will be accessed. When set to "0", the sector is read or written the same as the read and write commands.
SRT	Step Rate Interval	The time interval between step pulses issued by the FDC. Programmable from 0.5 to 8 milliseconds in increments of 0.5 ms at the 1 Mbit data rate. Refer to the SPECIFY command for actual delays.

SYMBOL	NAME	DESCRIPTION
ST0 ST1 ST2 ST3	Status 0 Status 1 Status 2 Status 3	Registers within the FDC which store status information after a command has been executed. This status information is available to the host during the result phase after command execution.
WGATE	Write Gate	Alters timing of WE to allow for pre-erase loads in perpendicular drives.

Instruction Set

Table 17 – Instruction Set

READ DATA										
		DATA BUS								
PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	MT	MFM	SK	0	0	1	1	0	Command Codes
	W	0	0	0	0	0	HDS	DS1	DS0	
	W	——— C ———								Sector ID information prior to Command execution.
	W	——— H ———								
	W	——— R ———								
	W	——— N ———								
	W	——— EOT ———								
	W	——— GPL ———								
	W	——— DTL ———								
Execution										Data transfer between the FDD and system.
Result	R	——— ST0 ———								Status information after Command execution.
	R	——— ST1 ———								
	R	——— ST2 ———								
	R	——— C ———								Sector ID information after Command execution.
	R	——— H ———								
	R	——— R ———								
	R	——— N ———								

READ DELETED DATA									
		DATA BUS							
PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	MT	MFM	SK	0	1	1	0	0	Command Codes
	W	0	0	0	0	0	HDS	DS1	DS0	
	W	——— C ———								Sector ID information prior to Command execution.
	W	——— H ———								
	W	——— R ———								
	W	——— N ———								
	W	——— EOT ———								
	W	——— GPL ———								
	W	——— DTL ———								
Execution										Data transfer between the FDD and system.
Result	R	——— ST0 ———								Status information after Command execution.
	R	——— ST1 ———								
	R	——— ST2 ———								
	R	——— C ———								Sector ID information after Command execution.
	R	——— H ———								
	R	——— R ———								
	R	——— N ———								

WRITE DATA									
		DATA BUS							
PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	MT	MFM	0	0	0	1	0	1	Command Codes
	W	0	0	0	0	0	HDS	DS1	DS0	
	W	——— C ———								Sector ID information prior to Command execution.
	W	——— H ———								
	W	——— R ———								
	W	——— N ———								
	W	——— EOT ———								
	W	——— GPL ———								
	W	——— DTL ———								
Execution										Data transfer between the FDD and system.
Result	R	——— ST0 ———								Status information after Command execution.
	R	——— ST1 ———								
	R	——— ST2 ———								
	R	——— C ———								Sector ID information after Command execution.
	R	——— H ———								
	R	——— R ———								
	R	——— N ———								

WRITE DELETED DATA									
		DATA BUS							
PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	MT	MFM	0	0	1	0	0	1	Command Codes
	W	0	0	0	0	0	HDS	DS1	DS0	
	W	——— C ———								Sector ID information prior to Command execution.
	W	——— H ———								
	W	——— R ———								
	W	——— N ———								
	W	——— EOT ———								
	W	——— GPL ———								
	W	——— DTL ———								
Execution										Data transfer between the FDD and system.
Result	R	——— ST0 ———								Status information after Command execution.
	R	——— ST1 ———								
	R	——— ST2 ———								
	R	——— C ———								Sector ID information after Command execution.
	R	——— H ———								
	R	——— R ———								
	R	——— N ———								

READ A TRACK									
		DATA BUS							
PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	0	MFM	0	0	0	0	1	0	Command Codes
	W	0	0	0	0	0	HDS	DS1	DS0	
	W	——— C ———								Sector ID information prior to Command execution.
	W	——— H ———								
	W	——— R ———								
	W	——— N ———								
	W	——— EOT ———								
	W	——— GPL ———								
	W	——— DTL ———								
Execution										Data transfer between the FDD and system. FDC reads all of cylinders' contents from index hole to EOT.
Result	R	——— ST0 ———								Status information after Command execution.
	R	——— ST1 ———								
	R	——— ST2 ———								
	R	——— C ———								Sector ID information after Command execution.
	R	——— H ———								
	R	——— R ———								
	R	——— N ———								

VERIFY									
		DATA BUS							
PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	MT	MFM	SK	1	0	1	1	0	Command Codes
	W	EC	0	0	0	0	HDS	DS1	DS0	
	W	——— C ———								Sector ID information prior to Command execution.
	W	——— H ———								
	W	——— R ———								
	W	——— N ———								
	W	——— EOT ———								
	W	——— GPL ———								
	W	——— DTL/SC ———								
Execution										No data transfer takes place.
Result	R	——— ST0 ———								Status information after Command execution.
	R	——— ST1 ———								
	R	——— ST2 ———								
	R	——— C ———								Sector ID information after Command execution.
	R	——— H ———								
	R	——— R ———								
	R	——— N ———								

VERSION									
		DATA BUS							
PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	0	0	0	1	0	0	0	0	Command Code
Result	R	1	0	0	1	0	0	0	0	Enhanced Controller

FORMAT A TRACK									
		DATA BUS							
PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	0	MFM	0	0	1	1	0	1	Command Codes
	W	0	0	0	0	0	HDS	DS1	DS0	
	W	——— N ———								Bytes/Sector
	W	——— SC ———								Sectors/Cylinder
	W	——— GPL ———								Gap 3
	W	——— D ———								Filler Byte
Execution for Each Sector Repeat:	W	——— C ———								Input Sector Parameters
	W	——— H ———								
	W	——— R ———								
	W	——— N ———								
										FDC formats an entire cylinder
Result	R	——— ST0 ———								Status information after Command execution
	R	——— ST1 ———								
	R	——— ST2 ———								
	R	——— Undefined ———								
	R	——— Undefined ———								
	R	——— Undefined ———								
	R	——— Undefined ———								

RECALIBRATE									
		DATA BUS							
PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	0	0	0	0	0	1	1	1	Command Codes
	W	0	0	0	0	0	0	DS1	DS0	
Execution										Head retracted to Track 0 Interrupt.

SENSE INTERRUPT STATUS										
		DATA BUS								
PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	0	0	0	0	1	0	0	0	Command Codes
Result	R	———— ST0 ————								Status information at the end of each seek operation.
	R	———— PCN ————								

SPECIFY										
		DATA BUS								
PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	0	0	0	0	0	0	1	1	Command Codes
	W	—— SRT ——				—— HUT ——				
	W	———— HLT ————							ND	

SENSE DRIVE STATUS										
		DATA BUS								
PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	0	0	0	0	0	1	0	0	Command Codes
	W	0	0	0	0	0	HDS	DS1	DS0	
Result	R	——— ST3 ———								Status information about FDD

SEEK										
		DATA BUS								
PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	0	0	0	0	1	1	1	1	Command Codes
	W	0	0	0	0	0	HDS	DS1	DS0	
	W	——— NCN ———								
Execution										Head positioned over proper cylinder on diskette.

CONFIGURE										
		DATA BUS								
PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	0	0	0	1	0	0	1	1	Configure Information
	W	0	0	0	0	0	0	0	0	
	W	0	EIS	EFIFO	POLL	—— FIFOTHR ——				
Execution	W	——— PRETRK ———								

RELATIVE SEEK									
		DATA BUS							
PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	1	DIR	0	0	1	1	1	1	
	W	0	0	0	0	0	HDS	DS1	DS0	
	W	———— RCN ————								

DUMPREG										
		DATA BUS								
PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	0	0	0	0	1	1	1	0	*Note: Registers placed in FIFO
Execution										
Result	R	———— PCN-Drive 0 ————								
	R	———— PCN-Drive 1 ————								
	R	———— PCN-Drive 2 ————								
	R	———— PCN-Drive 3 ————								
	R	——— SRT ———				|	—— HUT ——			
	R	———— HLT ————						|	ND	
	R	———— SC/EOT ————								
	R	LOCK	0	D3	D2	D1	D0	GAP	WGATE	
	R	0	EIS	EFIFO	POLL	|	—— FIFOTHR ——			
	R	———— PRETRK ————								

READ ID									
		DATA BUS							
PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	0	MFM	0	0	1	0	1	0	Commands
	W	0	0	0	0	0	HDS	DS1	DS0	
Execution										The first correct ID information on the Cylinder is stored in Data Register
Result	R	——— ST0 ———								Status information after Command execution.
	R	——— ST1 ———								
	R	——— ST2 ———								
	R	——— C ———								
	R	——— H ———								
	R	——— R ———								
	R	——— N ———								

PERPENDICULAR MODE										
		DATA BUS								
PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	0	0	0	1	0	0	1	0	Command Codes
		OW	0	D3	D2	D1	D0	GAP	WGATE	

INVALID CODES										
		DATA BUS								
PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	——— Invalid Codes ———								Invalid Command Codes (NoOp - FDC goes into Stand-by State)
Result	R	————— ST0 —————								ST0 = 80H

LOCK										
		DATA BUS								
PHASE	R/W	D7	D6	D5	D4	D3	D2	D1	D0	REMARKS
Command	W	LOCK	0	0	1	0	1	0	0	Command Codes
Result	R	0	0	0	LOCK	0	0	0	0	

SC is returned if the last command that was issued was the Format command. EOT is returned if the last command was a Read or Write.

Note: These bits are used internally only. They are not reflected in the Drive Select pins. It is the user's responsibility to maintain correspondence between these bits and the Drive Select pins (DOR).

Data Transfer Commands

All of the Read Data, Write Data and Verify type commands use the same parameter bytes and return the same results information, the only difference being the coding of bits 0-4 in the first byte.

An implied seek will be executed if the feature was enabled by the Configure command. This seek is completely transparent to the user. The Drive Busy bit for the drive will go active in the Main Status Register during the seek portion of the command. If the seek portion fails, it is reflected in the results status normally returned for a Read/Write Data command. Status Register 0 (ST0) would contain the error code and C would contain the cylinder on which the seek failed.

Read Data
A set of nine (9) bytes is required to place the FDC in the Read Data Mode. After the Read Data command has been issued, the FDC loads the head (if it is in the unloaded state), waits the specified head settling time (defined in the Specify command), and begins reading ID Address Marks and ID fields. When the sector address read off the diskette matches with the sector address specified in the command, the FDC reads the sector's data field and transfers the data to the FIFO.

After completion of the read operation from the current sector, the sector address is incremented by one and the data from the next logical sector is read and output via the FIFO. This continuous read function is called "Multi-Sector Read Operation". Upon receipt of the TC cycle, or an implied TC (FIFO overrun/underrun), the FDC stops sending data but will continue to read data from the current sector, check the CRC bytes, and at the end of the sector, terminate the Read Data Command.

N determines the number of bytes per sector (see Table 18 below). If N is set to zero, the sector size is set to 128. The DTL value determines the number of bytes to be transferred. If DTL is less than 128, the FDC transfers the specified number of bytes to the host. For reads, it continues to read the entire 128-byte sector and checks for CRC errors. For writes, it completes the 128-byte sector by filling in zeros. If N is not set to 00 Hex, DTL should be set to FF Hex and has no impact on the number of bytes transferred.

Table 18 – Sector Sizes

N	SECTOR SIZE
00	128 bytes
01	256 bytes
02	512 bytes
03	1024 bytes
..	...
07	16 Kbytes

The amount of data which can be handled with a single command to the FDC depends upon MT (multi-track) and N (number of bytes/sector).

The Multi-Track function (MT) allows the FDC to read data from both sides of the diskette. For a particular cylinder, data will be transferred starting at Sector 1, Side 0 and completing the last sector of the same track at Side 1.

If the host terminates a read or write operation in the FDC, the ID information in the result phase is dependent upon the state of the MT bit and EOT byte. Refer to Table 19.

At the completion of the Read Data command, the head is not unloaded until after the Head Unload Time Interval (specified in the Specify command) has elapsed. If the host issues another command before the head unloads, then the head settling time may be saved between subsequent reads.

If the FDC detects a pulse on the nINDEX pin twice without finding the specified sector (meaning that the diskette's index hole passes through index detect logic in the drive twice), the FDC sets the IC code in Status Register 0 to "01" indicating abnormal termination, sets the ND bit in Status Register 1 to "1" indicating a sector not found, and terminates the Read Data Command.

After reading the ID and Data Fields in each sector, the FDC checks the CRC bytes. If a CRC error occurs in the ID or data field, the FDC sets the IC code in Status Register 0 to "01" indicating abnormal termination, sets the DE bit flag in Status Register 1 to "1", sets the DD bit in Status Register 2 to "1" if CRC is incorrect in the ID field, and terminates the Read Data Command. Table 20 describes the effect of the SK bit on the Read Data command execution and results. Except where noted in Table 20, the C or R value of the sector address is automatically incremented (see Table 22)

Table 19 - Effects of MT and N Bits

MT	N	MAXIMUM TRANSFER CAPACITY	FINAL SECTOR READ FROM DISK
0	1	256 x 26 = 6,656	26 at side 0 or 1
1	1	256 x 52 = 13,312	26 at side 1
0	2	512 x 15 = 7,680	15 at side 0 or 1
1	2	512 x 30 = 15,360	15 at side 1
0	3	1024 x 8 = 8,192	8 at side 0 or 1
1	3	1024 x 16 = 16,384	16 at side 1

Table 20 – Skip Bit vs Read Data command

SK BIT VALUE	DATA ADDRESS MARK TYPE ENCOUNTERED	RESULTS		
		SECTOR READ?	CM BIT OF ST2 SET?	DESCRIPTION OF RESULTS
0	Normal Data	Yes	No	Normal termination.
0	Deleted Data	Yes	Yes	Address not incremented. Next sector not searched for.
1	Normal Data	Yes	No	Normal termination.
1	Deleted Data	No	Yes	Normal termination. Sector not read ("skipped").

Read Deleted Data

This command is the same as the Read Data command, only it operates on sectors that contain a Deleted Data Address Mark at the beginning of a Data Field.

Table 21 describes the effect of the SK bit on the Read Deleted Data command execution and results.

Except where noted in Table 21, the C or R value of the sector address is automatically incremented (see Table 22).

Table 21 - Skip Bit vs. Read Deleted Data Command

SK BIT VALUE	DATA ADDRESS MARK TYPE ENCOUNTERED	RESULTS		
		SECTOR READ?	CM BIT OF ST2 SET?	DESCRIPTION OF RESULTS
0	Normal Data	Yes	Yes	Address not incremented. Next sector not searched for.
0	Deleted Data	Yes	No	Normal termination.
1	Normal Data	No	Yes	Normal termination. Sector not read ("skipped").
1	Deleted Data	Yes	No	Normal termination.

Read A Track

This command is similar to the Read Data command except that the entire data field is read continuously from each of the sectors of a track. Immediately after encountering a pulse on the nINDEX pin, the FDC starts to read all data fields on the track as continuous blocks of data without regard to logical sector numbers. If the FDC finds an error in the ID or DATA CRC check bytes, it continues to read data from the track and sets the appropriate error bits at the end of the command. The FDC compares the ID information read from each sector with the specified value in the command and sets the ND flag of Status Register 1 to a “1” if there no comparison. Multi-track or skip operations are not allowed with this command. The MT and SK bits (bits D7 and D5 of the first command byte respectively) should always be set to "0".

This command terminates when the EOT specified number of sectors has not been read. If the FDC does not find an ID Address Mark on the diskette after the second occurrence of a pulse on the nINDEX pin, then it sets the IC code in Status Register 0 to "01" (abnormal termination), sets the MA bit in Status Register 1 to "1", and terminates the command.

Table 22 - Result Phase Table

MT	HEAD	FINAL SECTOR TRANSFERRED TO HOST	ID INFORMATION AT RESULT PHASE			
			C	H	R	N
0	0	Less than EOT	NC	NC	R + 1	NC
		Equal to EOT	C + 1	NC	01	NC
	1	Less than EOT	NC	NC	R + 1	NC
		Equal to EOT	C + 1	NC	01	NC
1	0	Less than EOT	NC	NC	R + 1	NC
		Equal to EOT	NC	LSB	01	NC
	1	Less than EOT	NC	NC	R + 1	NC
		Equal to EOT	C + 1	LSB	01	NC

NC: No Change, the same value as the one at the beginning of command execution.
LSB: Least Significant Bit, the LSB of H is complemented.

Write Data
After the Write Data command has been issued, the FDC loads the head (if it is in the unloaded state), waits the specified head load time if unloaded (defined in the Specify command), and begins reading ID fields. When the sector address read from the diskette matches the sector address specified in the command, the FDC reads the data from the host via the FIFO and writes it to the sector's data field.

After writing data into the current sector, the FDC computes the CRC value and writes it into the CRC field at the end of the sector transfer. The Sector Number stored in "R" is incremented by one, and the FDC continues writing to the next data field. The FDC continues this "Multi-Sector Write Operation". Upon receipt of a terminal count signal or if a FIFO over/under run occurs while a data field is being written, then the remainder of the data field is filled with zeros. The FDC reads the ID field of each sector and checks the CRC bytes. If it detects a CRC error in one of the ID fields, it sets the IC code in Status Register 0 to "01" (abnormal termination), sets the DE bit of Status Register 1 to "1", and terminates the Write Data command.
The Write Data command operates in much the same manner as the Read Data command. The following items are the same. Please refer to the Read Data Command for details:

Transfer Capacity
EN (End of Cylinder) bit
ND (No Data) bit
Head Load, Unload Time Interval
ID information when the host terminates the command

Definition of DTL when N = 0 and when N does not = 0

Write Deleted Data
This command is almost the same as the Write Data command except that a Deleted Data Address Mark is written at the beginning of the Data Field instead of the normal Data Address Mark. This command is typically used to mark a bad sector containing an error on the floppy disk.

Verify

The Verify command is used to verify the data stored on a disk. This command acts exactly like a Read Data command except that no data is transferred to the host. Data is read from the disk and CRC is computed and checked against the previously-stored value.

Because data is not transferred to the host, the TC cycle cannot be used to terminate this command. By setting the EC bit to "1", an implicit TC will be issued to the FDC. This implicit TC will occur when the SC value has decremented to 0 (an SC value of 0 will verify 256 sectors). This command can also be terminated by setting the EC bit to "0" and the EOT value equal to the final sector to be checked. If EC is set to "0", DTL/SC should be programmed to 0FFH. Refer to Table 22 and Table 23 for information concerning the values of MT and EC versus SC and EOT value.

Definitions:

Sectors Per Side = Number of formatted sectors per each side of the disk.

Sectors Remaining = Number of formatted sectors left which can be read, including side 1 of the disk if MT is set to "1".

Table 23 – Verify Command Result Phase Table

MT	EC	SC/EOT VALUE	TERMINATION RESULT
0	0	SC = DTL EOT <= # Sectors Per Side	Success Termination Result Phase Valid
0	0	SC = DTL EOT > # Sectors Per Side	Unsuccessful Termination Result Phase Invalid
0	1	SC <= # Sectors Remaining AND EOT <= # Sectors Per Side	Successful Termination Result Phase Valid
0	1	SC > # Sectors Remaining OR EOT > # Sectors Per Side	Unsuccessful Termination Result Phase Invalid
1	0	SC = DTL EOT <= # Sectors Per Side	Successful Termination Result Phase Valid
1	0	SC = DTL EOT > # Sectors Per Side	Unsuccessful Termination Result Phase Invalid
1	1	SC <= # Sectors Remaining AND EOT <= # Sectors Per Side	Successful Termination Result Phase Valid
1	1	SC > # Sectors Remaining OR EOT > # Sectors Per Side	Unsuccessful Termination Result Phase Invalid

Note: If MT is set to "1" and the SC value is greater than the number of remaining formatted sectors on Side 0, verifying will continue on Side 1 of the disk.

Format A Track

The Format command allows an entire track to be formatted. After a pulse from the nINDEX pin is detected, the FDC starts writing data on the disk including gaps, address marks, ID fields, and data fields per the IBM System 34 or 3740 format (MFM or FM respectively). The particular values that will be written to the gap and data field are controlled by the values programmed into N, SC, GPL, and D which are specified by the host during the command phase. The data field of the sector is filled with the data byte specified by D. The ID field for each sector is supplied by the host; that is, four data bytes per sector are needed by the FDC for C, H, R, and N (cylinder, head, sector number and sector size respectively).

After formatting each sector, the host must send new values for C, H, R and N to the FDC for the next sector on the track. The R value (sector number) is the only value that must be changed by the host after each sector is formatted. This allows the disk to be formatted with nonsequential sector addresses (interleaving). This incrementing and formatting continues for the whole track until the FDC encounters a pulse on the nINDEX pin again and it terminates the command.

Table 24 contains typical values for gap fields which are dependent upon the size of the sector and the number of sectors on each track. Actual values can vary due to drive electronics.

FORMAT FIELDS

SYSTEM 34 (DOUBLE DENSITY) FORMAT

GAP4a 80x 4E	SYNC 12x 00	IAM		GAP1 50x 4E	SYNC 12x 00	IDAM		C Y L	H D	S E C	N O	C R C	GAP2 22x 4E	SYNC 12x 00	DATA AM		DATA	C R C	GAP3	GAP 4b
		3x C2	FC			3x A1	FE								3x A1	FB F8				

SYSTEM 3740 (SINGLE DENSITY) FORMAT

GAP4a 40x FF	SYNC 6x 00	IAM	GAP1 26x FF	SYNC 6x 00	IDAM	C Y L	H D	S E C	N O	C R C	GAP2 11x FF	SYNC 6x 00	DATA AM	DATA	C R C	GAP3	GAP 4b
		FC			FE								FB or F8				

PERPENDICULAR FORMAT

GAP4a 80x 4E	SYNC 12x 00	IAM		GAP1 50x 4E	SYNC 12x 00	IDAM		C Y L	H D	S E C	N O	C R C	GAP2 41x 4E	SYNC 12x 00	DATA AM		DATA	C R C	GAP3	GAP 4b
		3x C2	FC			3x A1	FE								3x A1	FB F8				

Table 24 – Typical Values for Formatting

	FORMAT	SECTOR SIZE	N	SC	GPL1	GPL2
5.25" Drives	FM	128	00	12	07	09
		128	00	10	10	19
		512	02	08	18	30
		1024	03	04	46	87
		2048	04	02	C8	FF
		4096	05	01	C8	FF
		...	...			
	MFM	256	01	12	0A	0C
		256	01	10	20	32
		512*	02	09	2A	50
		1024	03	04	80	F0
		2048	04	02	C8	FF
		4096	05	01	C8	FF
		...	...			
3.5" Drives	FM	128	0	0F	07	1B
		256	1	09	0F	2A
		512	2	05	1B	3A
	MFM	256	1	0F	0E	36
		512**	2	09	1B	54
		1024	3	05	35	74

GPL1 = suggested GPL values in Read and Write commands to avoid splice point between data field and ID field of contiguous sections.
GPL2 = suggested GPL value in Format A Track command.
*PC/AT values (typical)
**PS/2 values (typical). Applies with 1.0 MB and 2.0 MB drives.
NOTE: All values except sector size are in hex.

Control Commands
Control commands differ from the other commands in that no data transfer takes place. Three commands generate an interrupt when complete: Read ID, Recalibrate, and Seek. The other control commands do not generate an interrupt.

Read ID
The Read ID command is used to find the present position of the recording heads. The FDC stores the values from the first ID field it is able to read into its registers. If the FDC does not find an ID address mark on the diskette after the second occurrence of a pulse on the nINDEX pin, it then sets the IC code in Status Register 0 to "01" (abnormal termination), sets the MA bit in Status Register 1 to "1", and terminates the command.

The following commands will generate an interrupt upon completion. They do not return any result bytes. It is highly recommended that control commands be followed by the Sense Interrupt Status command. Otherwise, valuable interrupt status information will be lost.

Recalibrate
This command causes the read/write head within the FDC to retract to the track 0 position. The FDC clears the contents of the PCN counter and checks the status of the nTRK0 pin from the FDD. As long as the nTRK0 pin is low, the DIR pin remains 0 and step pulses are issued. When the nTRK0 pin goes high, the SE bit in Status Register 0 is set to "1" and the command is terminated. If the nTR0 pin is still low after 79 step pulses have been issued, the FDC sets the SE and the EC bits of Status Register 0 to "1" and terminates the command. Disks capable of handling more than 80 tracks per side may require more than one Recalibrate command to return the head back to physical Track 0.

The Recalibrate command does not have a result phase. The Sense Interrupt Status command must be issued after the Recalibrate command to effectively terminate it and to provide verification of the head position (PCN). During the command phase of the recalibrate operation, the FDC is in the BUSY state, but during the execution phase it is in a NON-BUSY state. At this time, another Recalibrate command may be issued, and in this manner parallel Recalibrate operations may be done on up to four drives at once. Upon power up, the software must issue a Recalibrate command to properly initialize all drives and the controller.

Seek
The read/write head within the drive is moved from track to track under the control of the Seek command. The FDC compares the PCN, which is the current head position, with the NCN and performs the following operation if there is a difference:

PCN < NCN: Direction signal to drive set to "1" (step in) and issues step pulses.
PCN > NCN: Direction signal to drive set to "0" (step out) and issues step pulses.

The rate at which step pulses are issued is controlled by SRT (Stepping Rate Time) in the Specify command. After each step pulse is issued, NCN is compared against PCN, and when NCN = PCN the SE bit in Status Register 0 is set to "1" and the command is terminated. During the command phase of the seek or recalibrate operation, the FDC is in the BUSY state, but during the execution phase it is in the NON-BUSY state. At this time, another Seek or Recalibrate command may be issued, and in this manner, parallel seek operations may be done on up to four drives at once.
Note that if implied seek is not enabled, the read and write commands should be preceded by:

1) Seek command - Step to the proper track
2) Sense Interrupt Status command - Terminate the Seek command

3) Read ID - Verify head is on proper track
4) Issue Read/Write command.

The Seek command does not have a result phase. Therefore, it is highly recommended that the Sense Interrupt Status command is issued after the Seek command to terminate it and to provide verification of the head position (PCN). The H bit (Head Address) in ST0 will always return to a "0". When exiting POWERDOWN mode, the FDC clears the PCN value and the status information to zero. Prior to issuing the POWERDOWN command, it is highly recommended that the user service all pending interrupts through the Sense Interrupt Status command.

Sense Interrupt Status
An interrupt signal is generated by the FDC for one of the following reasons:

1. Upon entering the Result Phase of:
   a. Read Data command
   b. Read A Track command
   c. Read ID command
   d. Read Deleted Data command
   e. Write Data command
   f. Format A Track command
   g. Write Deleted Data command
   h. Verify command

2. End of Seek, Relative Seek, or Recalibrate command

3. FDC requires a data transfer during the execution phase in the non-DMA mode

The Sense Interrupt Status command resets the interrupt signal and, via the IC code and SE bit of Status Register 0, identifies the cause of the interrupt.

Table 25 - Interrupt Identification

SE	IC	INTERRUPT DUE TO
0	11	Polling
1	00	Normal termination of Seek or Recalibrate command
1	01	Abnormal termination of Seek or Recalibrate command

The Seek, Relative Seek, and Recalibrate commands have no result phase. The Sense Interrupt Status command must be issued immediately after these commands to terminate them and to provide verification of the head position (PCN). The H (Head Address) bit in ST0 will always return a "0". If a Sense Interrupt Status is not issued, the drive will continue to be BUSY and may affect the operation of the next command.

Sense Drive Status
Sense Drive Status obtains drive status information. It has not execution phase and goes directly to the result phase from the command phase. Status Register 3 contains the drive status information.

Specify
The Specify command sets the initial values for each of the three internal times. The HUT (Head Unload Time) defines the time from the end of the execution phase of one of the read/write commands

to the head unload state. The SRT (Step Rate Time) defines the time interval between adjacent step pulses. Note that the spacing between the first and second step pulses may be shorter than the remaining step pulses. The HLT (Head Load Time) defines the time between when the Head Load signal goes high and the read/write operation starts. The values change with the data rate speed selection and are documented in Table 26. The values are the same for MFM and FM.

The choice of DMA or non-DMA operations is made by the ND bit. When this bit is "1", the non-DMA mode is selected, and when ND is "0", the DMA mode is selected. In DMA mode, data transfers are signaled by the DMA request cycles. Non-DMA mode uses the RQM bit and the interrupt to signal data transfers.

Configure
The Configure command is issued to select the special features of the FDC. A Configure command need not be issued if the default values of the FDC meet the system requirements.

Table 26 – Drive Control Delays (ms)

	HUT					SRT				
	2M	**1M**	**500K**	**300K**	**250K**	**2M**	**1M**	**500K**	**300K**	**250K**
0	64	128	256	426	512	4	8	16	26.7	32
1	4	8	16	26.7	32	3.75	7.5	15	25	30
..	..	..	..	..	..	..	..	..	..	..
E	56	112	224	373	448	0.5	1	2	3.33	4
F	60	120	240	400	480	0.25	0.5	1	1.67	2

	HLT				
	2M	**1M**	**500K**	**300K**	**250K**
00	64	128	256	426	512
01	0.5	1	2	3.3	4
02	1	2	4	6.7	8
..	..	..	..	..	.
7F	63	126	252	420	504
7F	63.5	127	254	423	508

Configure Default Values:

EIS - No Implied Seeks
EFIFO - FIFO Disabled
POLL - Polling Enabled
FIFOTHR - FIFO Threshold Set to 1 Byte
PRETRK - Pre-Compensation Set to Track 0

EIS - Enable Implied Seek. When set to "1", the FDC will perform a Seek operation before executing a read or write command. Defaults to no implied seek.

EFIFO - A "1" disables the FIFO (default). This means data transfers are asked for on a byte-by-byte basis. Defaults to "1", FIFO disabled. The threshold defaults to "1".

POLL - Disable polling of the drives. Defaults to "0", polling enabled. When enabled, a single interrupt is generated after a reset. No polling is performed while the drive head is loaded and the head unload delay has not expired.

FIFOTHR - The FIFO threshold in the execution phase of read or write commands. This is programmable from 1 to 16 bytes. Defaults to one byte. A "00" selects one byte; "0F" selects 16 bytes.

PRETRK - Pre-Compensation Start Track Number. Programmable from track 0 to 255. Defaults to track 0. A "00" selects track 0; "FF" selects track 255.

Version
The Version command checks to see if the controller is an enhanced type or the older type (765A). A value of 90 H is returned as the result byte.

Relative Seek
The command is coded the same as for Seek, except for the MSB of the first byte and the DIR bit.

DIR Head Step Direction Control

RCN Relative Cylinder Number that determines how many tracks to step the head in or out from the current track number.

DIR	ACTION
0	Step Head Out
1	Step Head In

The Relative Seek command differs from the Seek command in that it steps the head the absolute number of tracks specified in the command instead of making a comparison against an internal register. The Seek command is good for drives that support a maximum of 256 tracks. Relative Seeks cannot be overlapped with other Relative Seeks. Only one Relative Seek can be active at a time. Relative Seeks may be overlapped with Seeks and Recalibrates. Bit 4 of Status Register 0 (EC) will be set if Relative Seek attempts to step outward beyond Track 0.

As an example, assume that a floppy drive has 300 useable tracks. The host needs to read track 300 and the head is on any track (0-255). If a Seek command is issued, the head will stop at track 255. If a Relative Seek command is issued, the FDC will move the head the specified number of tracks, regardless of the internal cylinder position register (but will increment the register). If the head was on track 40 (d), the maximum track that the FDC could position the head on using Relative Seek will be 295 (D), the initial track + 255 (D). The maximum count that the head can be moved with a single Relative Seek command is 255 (D).

The internal register, PCN, will overflow as the cylinder number crosses track 255 and will contain 39 (D). The resulting PCN value is thus (RCN + PCN) mod 256. Functionally, the FDC starts counting from 0 again as the track number goes above 255 (D). It is the user's responsibility to compensate FDC functions (precompensation track number) when accessing tracks greater than 255. The FDC does not keep track that it is working in an "extended track area" (greater than 255). Any command issued will use the current PCN value except for the Recalibrate command, which only looks for the TRACK0 signal. Recalibrate will return an error if the head is farther than 79 due to its limitation of issuing a maximum of 80 step pulses. The user simply needs to issue a second Recalibrate command. The Seek command and implied seeks will function correctly within the 44 (D) track (299-255) area of the "extended track area". It is the user's responsibility not to issue a new track position that will exceed the maximum track that is present in the extended area.

To return to the standard floppy range (0-255) of tracks, a Relative Seek should be issued to cross the track 255 boundary.

A Relative Seek can be used instead of the normal Seek, but the host is required to calculate the difference between the current head location and the new (target) head location. This may require the host to issue a Read ID command to ensure that the head is physically on the track that software assumes it to be. Different FDC commands will return different cylinder results which may be difficult to keep track of with software without the Read ID command.

Perpendicular Mode

The Perpendicular Mode command should be issued prior to executing Read/Write/Format commands that access a disk drive with perpendicular recording capability. With this command, the length of the Gap2 field and VCO enable timing can be altered to accommodate the unique requirements of these drives. Table 27 describes the effects of the WGATE and GAP bits for the Perpendicular Mode command. Upon a reset, the FDC will default to the conventional mode (WGATE = 0, GAP = 0).

Selection of the 500 Kbps and 1 Mbps perpendicular modes is independent of the actual data rate selected in the Data Rate Select Register. The user must ensure that these two data rates remain consistent.

The Gap2 and VCO timing requirements for perpendicular recording type drives are dictated by the design of the read/write head. In the design of this head, a pre-erase head precedes the normal read/write head by a distance of 200 micrometers. This works out to about 38 bytes at a 1 Mbps recording density. Whenever the write head is enabled by the Write Gate signal, the pre-erase head is also activated at the same time. Thus, when the write head is initially turned on, flux transitions recorded on the media for the first 38 bytes will not be preconditioned with the pre-erase head since it has not yet been activated. To accommodate this head activation and deactivation time, the Gap2 field is expanded to a length of 41 bytes. The Format Fields table illustrates the change in the Gap2 field size for the perpendicular format.

On the read back by the FDC, the controller must begin synchronization at the beginning of the sync field. For the conventional mode, the internal PLL VCO is enabled (VCOEN) approximately 24 bytes from the start of the Gap2 field. But, when the controller operates in the 1 Mbps perpendicular mode (WGATE = 1, GAP = 1), VCOEN goes active after 43 bytes to accommodate the increased Gap2 field size. For both cases, and approximate two-byte cushion is maintained from the beginning of the sync field for the purposes of avoiding write splices in the presence of motor speed variation.

For the Write Data case, the FDC activates Write Gate at the beginning of the sync field under the conventional mode. The controller then writes a new sync field, data address mark, data field, and CRC. With the pre-erase head of the perpendicular drive, the write head must be activated in the Gap2 field to insure a proper write of the new sync field. For the 1 Mbps perpendicular mode (WGATE = 1, GAP = 1), 38 bytes will be written in the Gap2 space. Since the bit density is proportional to the data rate, 19 bytes will be written in the Gap2 field for the 500 Kbps perpendicular mode (WGATE = 1, GAP =0).

It should be noted that none of the alterations in Gap2 size, VCO timing, or Write Gate timing affect normal program flow. The information provided here is just for background purposes and is not needed for normal operation. Once the Perpendicular Mode command is invoked, FDC software behavior from the user standpoint is unchanged.

The perpendicular mode command is enhanced to allow specific drives to be designated Perpendicular recording drives. This enhancement allows data transfers between Conventional and Perpendicular drives without having to issue Perpendicular mode commands between the accesses of the different drive types, nor having to change write pre-compensation values.

When both GAP and WGATE bits of the PERPENDICULAR MODE COMMAND are both programmed to "0" (Conventional mode), then D0, D1, D2, D3, and D4 can be programmed independently to "1" for that drive to be set automatically to Perpendicular mode. In this mode the following set of conditions also apply:

1. The GAP2 written to a perpendicular drive during a write operation will depend upon the programmed data rate.
2. The write pre-compensation given to a perpendicular mode drive will be 0ns.
3. For D0-D3 programmed to "0" for conventional mode drives any data written will be at the currently programmed write pre-compensation.

Note: Bits D0-D3 can only be overwritten when OW is programmed as a "1".If either GAP or WGATE is a "1" then D0-D3 are ignored.

Software and hardware resets have the following effect on the PERPENDICULAR MODE COMMAND:

1. "Software" resets (via the DOR or DSR registers) will only clear GAP and WGATE bits to "0". D0-D3 are unaffected and retain their previous value.
2. "Hardware" resets will clear all bits

(GAP, WGATE and D0-D3) to "0", i.e all conventional mode.

Table 27 – Effects of WGATE and GAP Bits

WGATE	GAP	MODE	LENGTH OF GAP2 FORMAT FIELD	PORTION OF GAP 2 WRITTEN BY WRITE DATA OPERATION
0	0	Conventional	22 Bytes	0 Bytes
0	1	Perpendicular (500 Kbps)	22 Bytes	19 Bytes
1	0	Reserved (Conventional)	22 Bytes	0 Bytes
1	1	Perpendicular (1 Mbps)	41 Bytes	38 Bytes

LOCK

In order to protect systems with long DMA latencies against older application software that can disable the FIFO the LOCK Command has been added. This command should only be used by the FDC routines, and application software should refrain from using it. If an application calls for the FIFO to be disabled then the CONFIGURE command should be used.

The LOCK command defines whether the EFIFO, FIFOTHR, and PRETRK parameters of the CONFIGURE command can be RESET by the DOR and DSR registers. When the LOCK bit is set to logic "1" all subsequent "software RESETS by the DOR and DSR registers will not change the previously set parameters to their default values. All "hardware" RESET from the nPCI_RESET pin will set the LOCK bit to logic "0" and return the EFIFO, FIFOTHR, and PRETRK to their default values. A status byte is returned immediately after issuing a LOCK command. This byte reflects the value of the LOCK bit set by the command byte.

Enhanced DUMPREG

The DUMPREG command is designed to support system run-time diagnostics and application software development and debug. To accommodate the LOCK command and the enhanced PERPENDICULAR MODE command the eighth byte of the DUMPREG command has been modified to contain the additional data from these two commands.

Compatibility

The LPC47N227 was designed with software compatibility in mind. It is a fully backwards- compatible solution with the older generation 765A/B disk controllers. The FDC also implements on-board registers for compatibility with the PS/2, as well as PC/AT and PC/XT, floppy disk controller subsystems. After a hardware reset of the FDC, all registers, functions and enhancements default to a PC/AT, PS/2 or PS/2 Model 30 compatible operating mode, depending on how the IDENT and MFM bits are configured by the system BIOS.

SERIAL PORT (UART)

The LPC47N227 incorporates two full function UARTs. They are compatible with the NS16450, the 16450 ACE registers and the NS16C550A. The UARTS perform serial-to-parallel conversion on received characters and parallel-to-serial conversion on transmit characters. The data rates are independently programmable from 460.8K baud down to 50 baud. The character options are programmable for 1 start; 1, 1.5 or 2 stop bits; even, odd, sticky or no parity; and prioritized interrupts. The UARTs each contain a programmable baud rate generator that is capable of dividing the input clock or crystal by a number from 1

to 65535. The UARTs are also capable of supporting the MIDI data rate. Refer to the Configuration Registers for information on disabling, power down and changing the base address of the UARTs. The interrupt from a UART is enabled by programming OUT2 of that UART to a logic "1". OUT2 being a logic "0" disables that UART's interrupt. The second UART also supports IrDA 1.2 (4Mbps), HP-SIR, ASK-IR and Consumer IR infrared modes of operation.

Register Description

Addressing of the accessible registers of the Serial Port is shown below. The base addresses of the serial ports are defined by the configuration registers (see Configuration section). The Serial Port registers are located at sequentially increasing addresses above these base addresses. The LPC47N227 contains two serial ports, each of which contain a register set as described below.

Table 28 - Addressing the Serial Port

DLAB*	A2	A1	A0	REGISTER NAME
0	0	0	0	Receive Buffer (read)
0	0	0	0	Transmit Buffer (write)
0	0	0	1	Interrupt Enable (read/write)
X	0	1	0	Interrupt Identification (read)
X	0	1	0	FIFO Control (write)
X	0	1	1	Line Control (read/write)
X	1	0	0	Modem Control (read/write)
X	1	0	1	Line Status (read/write)
X	1	1	0	Modem Status (read/write)
X	1	1	1	Scratchpad (read/write)
1	0	0	0	Divisor LSB (read/write)
1	0	0	1	Divisor MSB (read/write

*Note: DLAB is Bit 7 of the Line Control Register

The following section describes the operation of the registers.

Receive Buffer Register (RB)

Address Offset = 0H, DLAB = 0, READ ONLY

This register holds the received incoming data byte. Bit 0 is the least significant bit, which is transmitted and received first. Received data is double buffered; this uses an additional shift register to receive the serial data stream and convert it to a parallel 8 bit word which is transferred to the Receive Buffer register. The shift register is not accessible.

Transmit Buffer Register (TB)

Address Offset = 0H, DLAB = 0, WRITE ONLY

This register contains the data byte to be transmitted. The transmit buffer is double buffered, utilizing an additional shift register (not accessible) to convert the 8 bit data word to a serial format. This shift register is loaded from the Transmit Buffer when the transmission of the previous byte is complete.

Interrupt Enable Register (IER)

Address Offset = 1H, DLAB = 0, READ/WRITE

The lower four bits of this register control the enables of the five interrupt sources of the Serial Port interrupt. It is possible to totally disable the interrupt system by resetting bits 0 through 3 of this register. Similarly, setting the appropriate bits of this register to a high, selected interrupts can be enabled. Disabling

the interrupt system inhibits the Interrupt Identification Register and disables any Serial Port interrupt out of the LPC47N227. All other system functions operate in their normal manner, including the Line Status and MODEM Status Registers. The contents of the Interrupt Enable Register are described below.

Bit 0
This bit enables the Received Data Available Interrupt (and timeout interrupts in the FIFO mode) when set to logic "1".

Bit 1
This bit enables the Transmitter Holding Register Empty Interrupt when set to logic "1".

Bit 2
This bit enables the Received Line Status Interrupt when set to logic "1". The error sources causing the interrupt are Overrun, Parity, Framing and Break. The Line Status Register must be read to determine the source.

Bit 3
This bit enables the MODEM Status Interrupt when set to logic "1". This is caused when one of the Modem Status Register bits changes state.

Bits 4 through 7
These bits are always logic "0".

FIFO Control Register (FCR)
Address Offset = 2H, DLAB = X, WRITE

This is a write only register at the same location as the IIR. This register is used to enable and clear the FIFOs, set the RCVR FIFO trigger level. Note: DMA is not supported. The UART1 and UART2 FCR's are shadowed in the UART1 FIFO Control Shadow Register (CR15) and UART2 FIFO Control Shadow Register (CR16). See the Configuration section for description on these registers.

Bit 0
Setting this bit to a logic "1" enables both the XMIT and RCVR FIFOs. Clearing this bit to a logic "0" disables both the XMIT and RCVR FIFOs and clears all bytes from both FIFOs. When changing from FIFO Mode to non-FIFO (16450) mode, data is automatically cleared from the FIFOs. This bit must be a 1 when other bits in this register are written to or they will not be properly programmed.

Bit 1
Setting this bit to a logic "1" clears all bytes in the RCVR FIFO and resets its counter logic to 0. The shift register is not cleared. This bit is self-clearing.

Bit 2
Setting this bit to a logic "1" clears all bytes in the XMIT FIFO and resets its counter logic to 0. The shift register is not cleared. This bit is self-clearing.

Bit 3
Writing to this bit has no effect on the operation of the UART. DMA modes are not supported in this chip.

Bit 4,5
Reserved

Bit 6,7
These bits are used to set the trigger level for the RCVR FIFO interrupt.

Bit 7	Bit 6	RCVR FIFO Trigger Level (BYTES)
0	0	1
0	1	4
1	0	8
1	1	14

Interrupt Identification Register (IIR)
Address Offset = 2H, DLAB = X, READ

By accessing this register, the host CPU can determine the highest priority interrupt and its source. Four levels of priority interrupt exist. They are in descending order of priority:

1. Receiver Line Status (highest priority)
2. Received Data Ready
3. Transmitter Holding Register Empty
4. MODEM Status (lowest priority)

Information indicating that a prioritized interrupt is pending and the source of that interrupt is stored in the Interrupt Identification Register (refer to Interrupt Control Table). When the CPU accesses the IIR, the Serial Port freezes all interrupts and indicates the highest priority pending interrupt to the CPU. During this CPU access, even if the Serial Port records new interrupts, the current indication does not change until access is completed. The contents of the IIR are described below.

Bit 0
This bit can be used in either a hardwired prioritized or polled environment to indicate whether an interrupt is pending. When bit 0 is a logic "0", an interrupt is pending and the contents of the IIR may be used as a pointer to the appropriate internal service routine. When bit 0 is a logic "1", no interrupt is pending.

Bits 1 and 2
These two bits of the IIR are used to identify the highest priority interrupt pending as indicated by the Interrupt Control Table.

Bit 3
In non-FIFO mode, this bit is a logic "0". In FIFO mode this bit is set along with bit 2 when a timeout interrupt is pending.

Bits 4 and 5
These bits of the IIR are always logic "0".

Bits 6 and 7
These two bits are set when the FIFO CONTROL Register bit 0 equals 1.

Table 29 - Interrupt Control Table

FIFO MODE ONLY	INTERRUPT IDENTIFICATION REGISTER			INTERRUPT SET AND RESET FUNCTIONS			
BIT 3	BIT 2	BIT 1	BIT 0	PRIORITY LEVEL	INTERRUPT TYPE	INTERRUPT SOURCE	INTERRUPT RESET CONTROL
0	0	0	1	-	None	None	-
0	1	1	0	Highest	Receiver Line Status	Overrun Error, Parity Error, Framing Error or Break Interrupt	Reading the Line Status Register
0	1	0	0	Second	Received Data Available	Receiver Data Available	Read Receiver Buffer or the FIFO drops below the trigger level.
1	1	0	0	Second	Character Timeout Indication	No Characters Have Been Removed From or Input to the RCVR FIFO during the last 4 Char times and there is at least 1 char in it during this time	Reading the Receiver Buffer Register
0	0	1	0	Third	Transmitter Holding Register Empty	Transmitter Holding Register Empty	Reading the IIR Register (if Source of Interrupt) or Writing the Transmitter Holding Register
0	0	0	0	Fourth	MODEM Status	Clear to Send or Data Set Ready or Ring Indicator or Data Carrier Detect	Reading the MODEM Status Register

Line Control Register (LCR)
Address Offset = 3H, DLAB = 0, READ/WRITE

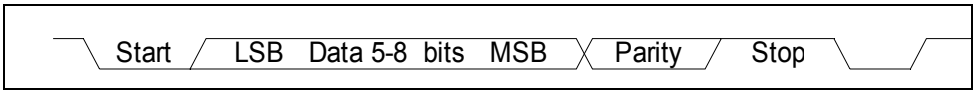


Figure 1 - Serial Data

This register contains the format information of the serial line. The bit definitions are:

Bits 0 and 1
These two bits specify the number of bits in each transmitted or received serial character. The encoding of bits 0 and 1 is as follows:
The Start, Stop and Parity bits are not included in the word length.

BIT 1	BIT 0	WORD LENGTH
0	0	5 Bits
0	1	6 Bits
1	0	7 Bits
1	1	8 Bits

Bit 2
This bit specifies the number of stop bits in each transmitted or received serial character. The following table summarizes the information.

BIT 2	WORD LENGTH	NUMBER OF STOP BITS
0	--	1
1	5 bits	1.5
1	6 bits	2
1	7 bits	2
1	8 bits	2

Note: The receiver will ignore all stop bits beyond the first, regardless of the number used in transmitting.

Bit 3
Parity Enable bit. When bit 3 is a logic "1", a parity bit is generated (transmit data) or checked (receive data) between the last data word bit and the first stop bit of the serial data. (The parity bit is used to generate an even or odd number of 1s when the data word bits and the parity bit are summed).

Bit 4
Even Parity Select bit. When bit 3 is a logic "1" and bit 4 is a logic "0", an odd number of logic "1"'s is transmitted or checked in the data word bits and the parity bit. When bit 3 is a logic "1" and bit 4 is a logic "1" an even number of bits is transmitted and checked.

Bit 5
Stick Parity bit. When parity is enabled it is used in conjunction with bit 4 to select Mark or Space Parity. When LCR bits 3, 4 and 5 are 1 the Parity bit is transmitted and checked as 0 (Space Parity). If bits 3 and 5 are 1 and bit 4 is a 0, then the Parity bit is transmitted and checked as 1 (Mark Parity). If bit 5 is 0 Stick Parity is disabled.

Bit 6
Set Break Control bit. When bit 6 is a logic "1", the transmit data output (TXD) is forced to the Spacing or logic "0" state and remains there (until reset by a low level bit 6) regardless of other transmitter activity. This feature enables the Serial Port to alert a terminal in a communications system.

Bit 7
Divisor Latch Access bit (DLAB). It must be set high (logic "1") to access the Divisor Latches of the Baud Rate Generator during read or write operations. It must be set low (logic "0") to access the Receiver Buffer Register, the Transmitter Holding Register, or the Interrupt Enable Register.

Modem Control Register (MCR)
Address Offset = 4H, DLAB = X, READ/WRITE

This 8 bit register controls the interface with the MODEM or data set (or device emulating a MODEM). The contents of the MODEM control register are described below.

Bit 0
This bit controls the Data Terminal Ready (nDTR) output. When bit 0 is set to a logic "1", the nDTR output is forced to a logic "0". When bit 0 is a logic "0", the nDTR output is forced to a logic "1".

Bit 1
This bit controls the Request To Send (nRTS) output. Bit 1 affects the nRTS output in a manner identical to that described above for bit 0.

Bit 2
This bit controls the Output 1 (OUT1) bit. This bit does not have an output pin and can only be read or written by the CPU.

Bit 3
Output 2 (OUT2). This bit is used to enable an UART interrupt. When OUT2 is a logic "0", the serial port interrupt output is forced to a high impedance state - disabled. When OUT2 is a logic "1", the serial port interrupt outputs are enabled.

Bit 4
This bit provides the loopback feature for diagnostic testing of the Serial Port. When bit 4 is set to logic "1", the following occur:

1. The TXD is set to the Marking State(logic "1").
2. The receiver Serial Input (RXD) is disconnected.
3. The output of the Transmitter Shift Register is "looped back" into the Receiver Shift Register input.
4. All MODEM Control inputs (nCTS, nDSR, nRI and nDCD) are disconnected.

5. The four MODEM Control outputs (nDTR, nRTS, OUT1 and OUT2) are internally connected to the four MODEM Control inputs (nDSR, nCTS, RI, DCD).

6. The Modem Control output pins are forced inactive high.
7. Data that is transmitted is immediately received.

This feature allows the processor to verify the transmit and receive data paths of the Serial Port. In the diagnostic mode, the receiver and the transmitter interrupts are fully operational. The MODEM Control Interrupts are also operational but the interrupts' sources are now the lower four bits of the MODEM Control Register instead of the MODEM Control inputs. The interrupts are still controlled by the Interrupt Enable Register.

Bits 5 through 7
These bits are permanently set to logic zero.

Line Status Register (LSR)
Address Offset = 5H, DLAB = X, READ/WRITE

Bit 0
Data Ready (DR). It is set to a logic "1" whenever a complete incoming character has been received and transferred into the Receiver Buffer Register or the FIFO. Bit 0 is reset to a logic "0" by reading all of the data in the Receive Buffer Register or the FIFO.

Bit 1
Overrun Error (OE). Bit 1 indicates that data in the Receiver Buffer Register was not read before the next character was transferred into the register, thereby destroying the previous character. In FIFO mode, an overrunn error will occur only when the FIFO is full and the next character has been completely received in the shift register, the character in the shift register is overwritten but not transferred to the FIFO. The OE indicator is set to a logic "1" immediately upon detection of an overrun condition, and reset whenever the Line Status Register is read.

Bit 2
Parity Error (PE). Bit 2 indicates that the received data character does not have the correct even or odd parity, as selected by the even parity select bit. The PE is set to a logic "1" upon detection of a parity error and is reset to a logic "0" whenever the Line Status Register is read. In the FIFO mode this error is associated with the particular character in the FIFO it applies to. This error is indicated when the associated character is at the top of the FIFO.

Bit 3
Framing Error (FE). Bit 3 indicates that the received character did not have a valid stop bit. Bit 3 is set to a logic "1" whenever the stop bit following the last data bit or parity bit is detected as a zero bit (Spacing level). The FE is reset to a logic "0" whenever the Line Status Register is read. In the FIFO mode this error is associated with the particular character in the FIFO it applies to. This error is indicated when the associated character is at the top of the FIFO. The Serial Port will try to resynchronize after a framing error. To do this, it assumes that the framing error was due to the next start bit, so it samples this 'start' bit twice and then takes in the 'data'.

Bit 4
Break Interrupt (BI). Bit 4 is set to a logic "1" whenever the received data input is held in the Spacing state (logic "0") for longer than a full word transmission time (that is, the total time of the start bit + data bits + parity bits + stop bits). The BI is reset after the CPU reads the contents of the Line Status Register. In the FIFO mode this error is associated with the particular character in the FIFO it applies to. This error is indicated when the associated character is at the top of the FIFO. When break occurs only one zero character is loaded into the FIFO. Restarting after a break is received, requires the serial data (RXD) to be logic "1" for at least 1/2 bit time.

Note: Bits 1 through 4 are the error conditions that produce a Receiver Line Status Interrupt whenever any of the corresponding conditions are detected and the interrupt is enabled.

Bit 5
Transmitter Holding Register Empty (THRE). Bit 5 indicates that the Serial Port is ready to accept a new character for transmission. In addition, this bit causes the Serial Port to issue an interrupt when the Transmitter Holding Register interrupt enable is set high. The THRE bit is set to a logic "1" when a character is transferred from the Transmitter Holding Register into the Transmitter Shift Register. The bit is reset to logic "0" whenever the CPU loads the Transmitter Holding Register. In the FIFO mode this bit is set when the XMIT FIFO is empty, it is cleared when at least 1 byte is written to the XMIT FIFO. Bit 5 is a read only bit.

Bit 6
Transmitter Empty (TEMT). Bit 6 is set to a logic "1" whenever the Transmitter Holding Register (THR) and Transmitter Shift Register (TSR) are both empty. It is reset to logic "0" whenever either the THR or TSR contains a data character. Bit 6 is a read only bit. In the FIFO mode this bit is set whenever the THR and TSR are both empty.

Bit 7
This bit is permanently set to logic "0" in the 450 mode. In the FIFO mode, this bit is set to a logic "1" when there is at least one parity error, framing error or break indication in the FIFO. This bit is cleared when the LSR is read if there are no subsequent errors in the FIFO.

Modem Status Register (MSR)
Address Offset = 6H, DLAB = X, READ/WRITE

This 8 bit register provides the current state of the control lines from the MODEM (or peripheral device). In addition to this current state information, four bits of the MODEM Status Register (MSR) provide change information. These bits are set to logic "1" whenever a control input from the MODEM changes state. They are reset to logic "0" whenever the MODEM Status Register is read.

Bit 0
Delta Clear To Send (DCTS). Bit 0 indicates that the nCTS input to the chip has changed state since the last time the MSR was read.

Bit 1
Delta Data Set Ready (DDSR). Bit 1 indicates that the nDSR input has changed state since the last time the MSR was read.

Bit 2

Trailing Edge of Ring Indicator (TERI). Bit 2 indicates that the nRI input has changed from logic "0" to logic "1".

Bit 3
Delta Data Carrier Detect (DDCD). Bit 3 indicates that the nDCD input to the chip has changed state.

Note: Whenever bit 0, 1, 2, or 3 is set to a logic "1", a MODEM Status Interrupt is generated.

Bit 4
This bit is the complement of the Clear To Send (nCTS) input. If bit 4 of the MCR is set to logic "1", this bit is equivalent to nRTS in the MCR.

Bit 5
This bit is the complement of the Data Set Ready (nDSR) input. If bit 4 of the MCR is set to logic "1", this bit is equivalent to DTR in the MCR.

Bit 6
This bit is the complement of the Ring Indicator (nRI) input. If bit 4 of the MCR is set to logic "1", this bit is equivalent to OUT1 in the MCR.

Bit 7
This bit is the complement of the Data Carrier
Detect (nDCD) input. If bit 4 of the MCR is set to logic "1", this bit is equivalent to OUT2 in the MCR.

Scratchpad Register (SCR)
Address Offset =7H, DLAB =X, READ/WRITE

This 8 bit read/write register has no effect on the operation of the Serial Port. It is intended as a scratchpad register to be used by the programmer to hold data temporarily.

Programmable Baud Rate Generator (AND Divisor Latches DLH, DLL)
The Serial Port contains a programmable Baud Rate Generator that is capable of dividing the internal PLL clock by any divisor from 1 to 65535. The internal PLL clock is divided down to generate a 1.8462MHz frequency for Baud Rates less than 38.4k, a 1.8432MHz frequency for 115.2k, a 3.6864MHz frequency for 230.4k and a 7.3728MHz frequency for 460.8k. This output frequency of the Baud Rate Generator is 16x the Baud rate. Two 8 bit latches store the divisor in 16 bit binary format. These Divisor Latches must be loaded during initialization in order to insure desired operation of the Baud Rate Generator. Upon loading either of the Divisor Latches, a 16 bit Baud counter is immediately loaded. This prevents long counts on initial load. If a 0 is loaded into the BRG registers the output divides the clock by the number 3. If a 1 is loaded the output is the inverse of the input oscillator. If a two is loaded the output is a divide by 2 signal with a 50% duty cycle. If a 3 or greater is loaded the output is low for 2 bits and high for the remainder of the count. The input clock to the BRG is a 1.8462 MHz clock.

Table 30 shows the baud rates possible.
Effect Of The Reset on Register File
The Reset Function Table (Table 31) details the effect of the Reset input on each of the registers of the Serial Port.

FIFO Interrupt Mode Operation

When the RCVR FIFO and receiver interrupts are enabled (FCR bit 0 = "1", IER bit 0 = "1"), RCVR interrupts occur as follows:

A. The receive data available interrupt will be issued when the FIFO has reached its programmed trigger level; it is cleared as soon as the FIFO drops below its programmed trigger level.
B. The IIR receive data available indication also occurs when the FIFO trigger level is reached. It is cleared when the FIFO drops below the trigger level.
C. The receiver line status interrupt (IIR=06H), has higher priority than the received data available (IIR=04H) interrupt.
D. The data ready bit (LSR bit 0) is set as soon as a character is transferred from the shift register to the RCVR FIFO. It is reset when the FIFO is empty.

When RCVR FIFO and receiver interrupts are enabled, RCVR FIFO timeout interrupts occur as follows:

A. A FIFO timeout interrupt occurs if all the following conditions exist:
At least one character is in the FIFO.
The most recent serial character received was longer than 4 continuous character times ago. (If 2 stop bits are programmed, the second one is included in this time delay).
The most recent CPU read of the FIFO was longer than 4 continuous character times ago.
This will cause a maximum character received to interrupt issued delay of 160 msec at 300 BAUD with a 12 bit character.
B. Character times are calculated by using the RCLK input for a clock signal (this makes the delay proportional to the baudrate).
C. When a timeout interrupt has occurred it is cleared and the timer reset when the CPU reads one character from the RCVR FIFO.
D. When a timeout interrupt has not occurred the timeout timer is reset after a new character is received or after the CPU reads the RCVR FIFO.

When the XMIT FIFO and transmitter interrupts are enabled (FCR bit 0 = "1", IER bit 1 = "1"), XMIT interrupts occur as follows:

A. The transmitter holding register interrupt (02H) occurs when the XMIT FIFO is empty; it is cleared as soon as the transmitter holding register is written to (1 of 16 characters may be written to the XMIT FIFO while servicing this interrupt) or the IIR is read.
B. The transmitter FIFO empty indications will be delayed 1 character time minus the last stop bit time whenever the following occurs: THRE=1 and there have not been at least two bytes at the same time in the transmitter FIFO since the last THRE=1. The transmitter interrupt after changing FCR0 will be immediate, if it is enabled.

Character timeout and RCVR FIFO trigger level interrupts have the same priority as the current received data available interrupt; XMIT FIFO empty has the same priority as the current transmitter holding register empty interrupt.

FIFO Polled Mode Opertion
With FCR bit 0 = "1" resetting IER bits 0, 1, 2 or 3 or all to zero puts the UART in the FIFO Polled Mode of operation. Since the RCVR and XMITTER are controlled separately, either one or both can be in the polled mode of operation. In this mode, the user's program will check RCVR and XMITTER status via the LSR. LSR definitions for the FIFO Polled Mode are as follows:

Bit 0=1 as long as there is one byte in the RCVR FIFO.

Bits 1 to 4 specify which error(s) have occurred. Character error status is handled the same way as when in the interrupt mode, the IIR is not affected since EIR bit 2=0.
Bit 5 indicates when the XMIT FIFO is empty.
Bit 6 indicates that both the XMIT FIFO and shift register are empty.
Bit 7 indicates whether there are any errors in the RCVR FIFO.

There is no trigger level reached or timeout condition indicated in the FIFO Polled Mode, however, the RCVR and XMIT FIFOs are still fully capable of holding characters.

Table 30 – Baud Rates

DESIRED BAUD RATE	DIVISOR USED TO GENERATE 16X CLOCK	PERCENT ERROR DIFFERENCE BETWEEN DESIRED AND ACTUAL[1]	HIGH SPEED BIT[2]
50	2304	0.001	X
75	1536	-	X
110	1047	-	X
134.5	857	0.004	X
150	768	-	X
300	384	-	X
600	192	-	X
1200	96	-	X
1800	64	-	X
2000	58	0.005	X
2400	48	-	X
3600	32	-	X
4800	24	-	X
7200	16	-	X
9600	12	-	X
19200	6	-	X
38400	3	0.030	X
57600	2	0.16	X
115200	1	0.16	X
230400	32770	0.16	1
460800	32769	0.16	1

Note[1]: The percentage error for all baud rates, except where indicated otherwise, is 0.2%.
Note [2]: The High Speed bit is located in the Device Configuration Space.

Table 31 - Reset Function Table

REGISTER/SIGNAL	RESET CONTROL	RESET STATE
Interrupt Enable Register	RESET	All bits low
Interrupt Identification Reg.	RESET	Bit 0 is high; Bits 1 - 7 low
FIFO Control	RESET	All bits low
Line Control Reg.	RESET	All bits low
MODEM Control Reg.	RESET	All bits low
Line Status Reg.	RESET	All bits low except 5, 6 high
MODEM Status Reg.	RESET	Bits 0 - 3 low; Bits 4 - 7 input
TXD1, TXD2	RESET	High
INTRPT (RCVR errs)	RESET/Read LSR	Low
INTRPT (RCVR Data Ready)	RESET/Read RBR	Low
INTRPT (THRE)	RESET/ReadIIR/Write THR	Low
OUT2B	RESET	High
RTSB	RESET	High
DTRB	RESET	High
OUT1B	RESET	High
RCVR FIFO	RESET/ FCR1*FCR0/_FCR0	All Bits Low
XMIT FIFO	RESET/ FCR1*FCR0/_FCR0	All Bits Low

Table 32 – Register Summary for an Individual UART Channel

REGISTER ADDRESS*	REGISTER NAME	REGISTER SYMBOL	BIT 0	BIT 1
ADDR = 0 DLAB = 0	Receive Buffer Register (Read Only)	RBR	Data Bit 0 (Note 1)	Data Bit 1
ADDR = 0 DLAB = 0	Transmitter Holding Register (Write Only)	THR	Data Bit 0	Data Bit 1
ADDR = 1 DLAB = 0	Interrupt Enable Register	IER	Enable Received Data Available Interrupt (ERDAI)	Enable Transmitter Holding Register Empty Interrupt (ETHREI)
ADDR = 2	Interrupt Ident. Register (Read Only)	IIR	"0" if Interrupt Pending	Interrupt ID Bit
ADDR = 2	FIFO Control Register (Write Only)	FCR (Note 7)	FIFO Enable	RCVR FIFO Reset
ADDR = 3	Line Control Register	LCR	Word Length Select Bit 0 (WLS0)	Word Length Select Bit 1 (WLS1)
ADDR = 4	MODEM Control Register	MCR	Data Terminal Ready (DTR)	Request to Send (RTS)
ADDR = 5	Line Status Register	LSR	Data Ready (DR)	Overrun Error (OE)
ADDR = 6	MODEM Status Register	MSR	Delta Clear to Send (DCTS)	Delta Data Set Ready (DDSR)
ADDR = 7	Scratch Register (Note 4)	SCR	Bit 0	Bit 1
ADDR = 0 DLAB = 1	Divisor Latch (LS)	DDL	Bit 0	Bit 1
ADDR = 1 DLAB = 1	Divisor Latch (MS)	DLM	Bit 8	Bit 9

*DLAB is Bit 7 of the Line Control Register (ADDR = 3).
Note 1: Bit 0 is the least significant bit. It is the first bit serially transmitted or received.
Note 2: When operating in the XT mode, this bit will be set any time that the transmitter shift register is empty.

Table 32 - Register Summary for an Individual UART Channel (continued)

BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7
Data Bit 2	Data Bit 3	Data Bit 4	Data Bit 5	Data Bit 6	Data Bit 7
Data Bit 2	Data Bit 3	Data Bit 4	Data Bit 5	Data Bit 6	Data Bit 7
Enable Receiver Line Status Interrupt (ELSI)	Enable MODEM Status Interrupt (EMSI)	0	0	0	0
Interrupt ID Bit	Interrupt ID Bit (Note 5)	0	0	FIFOs Enabled (Note 5)	FIFOs Enabled (Note 5)
XMIT FIFO Reset	DMA Mode Select (Note 6)	Reserved	Reserved	RCVR Trigger LSB	RCVR Trigger MSB
Number of Stop Bits (STB)	Parity Enable (PEN)	Even Parity Select (EPS)	Stick Parity	Set Break	Divisor Latch Access Bit (DLAB)
OUT1 (Note 3)	OUT2 (Note 3)	Loop	0	0	0
Parity Error (PE)	Framing Error (FE)	Break Interrupt (BI)	Transmitter Holding Register (THRE)	Transmitter Empty (TEMT) (Note 2)	Error in RCVR FIFO (Note 5)
Trailing Edge Ring Indicator (TERI)	Delta Data Carrier Detect (DDCD)	Clear to Send (CTS)	Data Set Ready (DSR)	Ring Indicator (RI)	Data Carrier Detect (DCD)
Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7
Bit 10	Bit 11	Bit 12	Bit 13	Bit 14	Bit 15

Note 3: This bit no longer has a pin associated with it.
Note 4: When operating in the XT mode, this register is not available.
Note 5: These bits are always zero in the non-FIFO mode.
Note 6: Writing a one to this bit has no effect. DMA modes are not supported in this chip.
Note 7: The UART1 and UART2 FCR's are shadowed in the UART1 FIFO Control Shadow Register (CR15) and UART2 FIFO Control Shadow Register (CR16).

Notes On Serial Port Operation

FIFO Mode Operation

GENERAL
The RCVR FIFO will hold up to 16 bytes regardless of which trigger level is selected.

TX AND RX FIFO Operation
The Tx portion of the UART transmits data through TXD as soon as the CPU loads a byte into the Tx FIFO. **The UART will prevent loads to the Tx FIFO if it currently holds 16 characters.** Loading to the Tx FIFO will again be enabled as soon as the next character is transferred to the Tx shift register. These capabilities account for the largely autonomous operation of the Tx.

The UART starts the above operations typically with a Tx interrupt. The chip issues a Tx interrupt whenever the Tx FIFO is empty and the Tx interrupt is enabled, except in the following instance. Assume that the Tx FIFO is empty and the CPU starts to load it. When the first byte enters the FIFO the Tx FIFO empty interrupt will transition from active to inactive. Depending on the execution speed of the service routine software, the UART may be able to transfer this byte from the FIFO to the shift register before the CPU loads another byte. If this happens, the Tx FIFO will be empty again and typically the UART's interrupt line would transition to the active state. This could cause a system with an interrupt control unit to record a Tx FIFO empty condition, even though the CPU is currently servicing that interrupt. **Therefore, after the first byte has been loaded into the FIFO the UART will wait one serial character transmission time before issuing a new Tx FIFO empty interrupt. This one character Tx interrupt delay will remain active until at least two bytes have the Tx FIFO empties after this condition, the Tx been loaded into the FIFO, concurrently. When interrupt will be activated without a one character delay.**

Rx support functions and operation are quite different from those described for the transmitter. The Rx FIFO receives data until the number of bytes in the FIFO equals the selected interrupt trigger level. At that time if Rx interrupts are enabled, the UART will issue an interrupt to the CPU. The Rx FIFO will continue to store bytes until it holds 16 of them. It will not accept any more data when it is full. Any more data entering the Rx shift register will set the Overrun Error flag. Normally, the FIFO depth and the programmable trigger levels will give the CPU ample time to empty the Rx FIFO before an overrun occurs.

One side-effect of having a Rx FIFO is that the selected interrupt trigger level may be above the data level in the FIFO. This could occur when data at the end of the block contains fewer bytes than the trigger level. No interrupt would be issued to the CPU and the data would remain in the UART. **To prevent the software from having to check for this situation the chip incorporates a timeout interrupt.**

The timeout interrupt is activated when there is a least one byte in the Rx FIFO, and neither the CPU nor the Rx shift register has accessed the Rx FIFO within 4 character times of the last byte. The timeout interrupt is cleared or reset when the CPU reads the Rx FIFO or another character enters it.

These FIFO related features allow optimization of CPU/UART transactions and are especially useful given the higher baud rate capability (256 kbaud).

INFRARED INTERFACE

The LPC47N227 infrared interface provides a two-way wireless communications port using infrared as the transmission medium. Several infrared protocols have been provided in this implementation including IrDA v1.2 (SIR/FIR), ASKIR, and Consumer IR (FIGURE 2). For more information consult the SMSC Infrared Communication Controller (IRCC) specification.

The IrDA v1.0 (SIR) and ASKIR formats are driven by the ACE registers found in UART2. The UART2 registers are described in "Serial Port (UART)" section. The base address for UART2 is programmed in CR25, the UART2 Base Address Register (see section CR25 subsection in the Configuration seciton).

The IrDA V1.2 (FIR) and Consumer IR formats are driven by the SCE registers. Descriptions of these registers can be found in the SMSC Infrared Communications Controller Specification. The Base Address for the SCE registers is programmed in CR2B, the SCE Base Address Register (see CR28 subsection in the Configuration section).

IrDA SIR/FIR and ASKIR

IrDA SIR (v1.0) specifies asynchronous serial communication at baud rates up to 115.2Kbps. Each byte is sent serially LSB first beginning with a zero value start bit. A zero is signaled by sending a single infrared pulse at the beginning of the serial bit time. A one is signaled by the absence of an infrared pulse during the bit time. Please refer to "Timing Diagrams" section for the parameters of these pulses and the IrDA waveforms.

IrDA FIR (v1.2) includes IrDA v1.0 SIR and additionally specifies synchronous serial communications at data rates up to 4Mbps.

Data is transferred LSB first in packets that can be up to 2048 bits in length. IrDA v1.2 includes .576Mbps and 1.152Mbps data rates using an encoding scheme that is similar to SIR. The 4Mbps data rate uses a pulse position modulation (PPM) technique.

The ASKIR infrared allows asynchronous serial communication at baud rates up to 19.2Kbps. Each byte is sent serially LSB first beginning with a zero value start bit. A zero is signaled by sending a 500KHz carrier waveform for the duration of the serial bit time. A one is signaled by the absence of carrier during the bit time. Refer to "Timing Diagrams" section for the parameters of the ASKIR waveforms.

Consumer IR

The LPC47N227 Consumer IR interface is a general-purpose Amplitude Shift Keyed encoder/decoder with programmable carrier and bit-cell rates that can emulate many popular TV Remote encoding formats; including, 38KHz PPM, PWM and RC-5. The carrier frequency is programmable from 1.6MHz to 6.25KHz. The bit-cell rate range is 100KHz to 390Hz.

Hardware Interface

The LPC47N227 IR hardware interface is shown in

FIGURE 2. This interface supports two types of external FIR transceiver modules. One uses a mode pin (IR Mode) to program the data rate, while the other has a second Rx data pin (IRRX3). The LPC47N227 uses Pin 63 for these functions. Pin 63 has IR Mode and IRRX3 as its first and second alternate function, respectively. These functions are selected through CR29 as shown in Table 33.

Table 33 - FIR Transceiver Module-Type Select

HP MODE[1]	FUNCTION
0	IR Mode
1	IRRX3

Note[1] HPMODE is CR29, BIT 4 (see CR29 subsection in the Configuration section). Refer to the Infrared Interface Block Diagram on the following page for HPMODE implementation.

The FAST bit is used to select between the SIR mode and FIR mode receiver, regardless of the transceiver type. If FAST = 1, the FIR mode receiver is selected; if FAST = 0, the SIR mode receiver is selected (Table 34).

Table 34 – IR Rx Data Pin Selection

CONTROL SIGNALS		INPUTS	
FAST	HPMODE	RX1	RX2
0	X	RX1=RXD2	RX2=IRRX2
X	0	RX1=RXD2	RX2=IRRX2
1	1	RX1=IR Mode/IRRX3	RX2=IR Mode/IRRX3

IR Half Duplex Turnaround Delay Time

If the Half Duplex option is chosen there is an IR Half Duplex Time-out that constrains IRCC direction mode changes. This time-out starts as each bit is transferred and prevents direction mode changes until the time-out expires. The timer is restarted whenever new data arrives in the current direction mode. For example, if data is loaded into the transmit buffer while a character is being received, the transmission will not start until the last bit has been received and the time-out expires. If the start bit of another character is received during this time-out, the timer is restarted after the new character is received. The Half Duplex Time-out is programmable from 0 to 25.5ms in 100μs increments (see section (See subsection CR2D in the Configuration section).

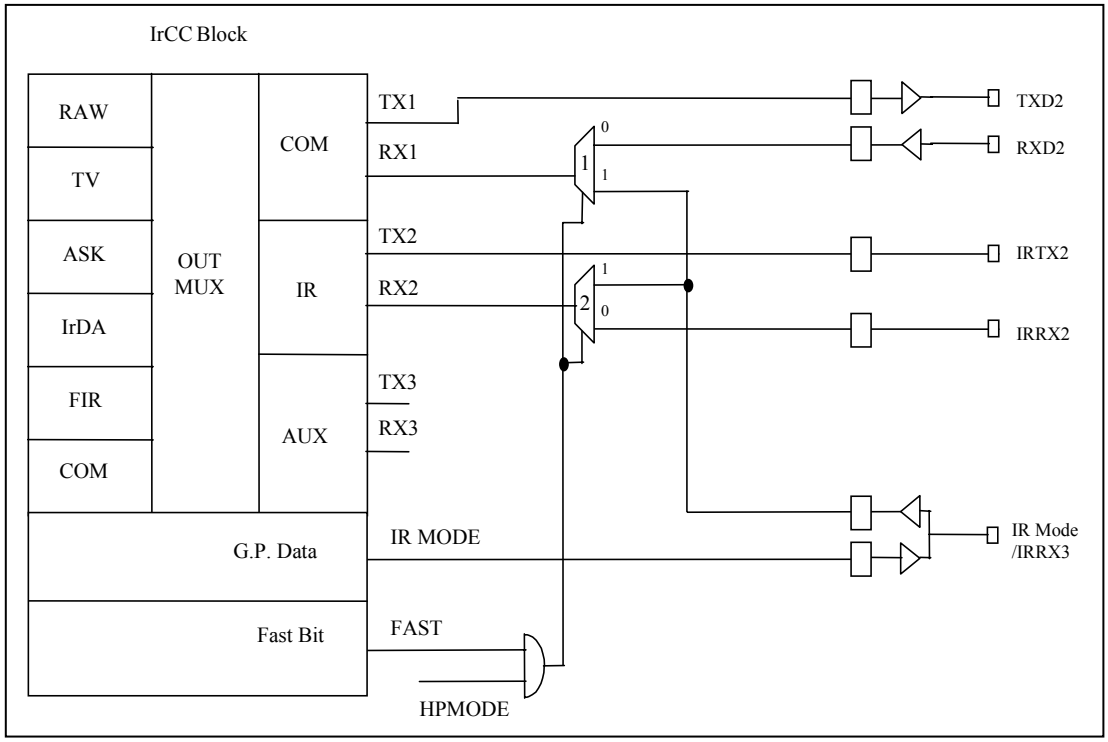


FIGURE 2 – INFRARED INTERFACE BLOCK DIAGRAM

IR Transmit Pins

The TXD2 and IRTX2 pins default to output, low on VCC POR and hard reset. These pins are not powered by VTR. These pins function as described below.

Following a VCC POR, the TXD2 and IRTX2 pins will be output and low. They will remain low until one of the following conditions are met.

IRTX2 Pin (CR0A bits [7:6]=01):

- This pin will remain low following a VCC POR until serial port 2 is enabled by setting the UART2 power down bit (CR02, bit 7), at which time the pin will reflect the state of the IR transmit output of the IRCC block (if IR is enabled through the IR Option Register for Serial Port 2).

TXD2 Pin (CR0A bits [7:6]=00):

1. This pin will remain low following a VCC POR until serial port 2 is enabled by setting the UART2 power down bit (CR02, bit 7), at which time the pin will reflect the state of the transmit output of serial port 2 (if COM is enabled through CR0C Register for Serial Port 2).
2. This pin will remain low following a VCC POR until serial port 2 is enabled by setting the UART2 power down bit (CR02, bit 7), at which time the pin will reflect the state of the IR transmit output of the IRCC block (if IR is enabled through the CR0C Register for Serial Port 2).

The IRTX2 and TXD2 pins will be driven low whenever serial port 2 is disabled (UART2 power down bit is cleared).

Note that bits[7,6] of CR0A can be used to override this functionality of driving the IRTX2 and TXD2 pins low when UART2 is powered down. If these bits are set to '11', then the IRTX (TXD2) and IRTX2 pins are high-z.

PARALLEL PORT

The LPC47N227 incorporates an IBM XT/AT compatible parallel port. This supports the optional PS/2 type bi-directional parallel port (SPP), the Enhanced Parallel Port (EPP) and the Extended Capabilities Port (ECP) parallel port modes. Refer to the Configuration Registers for information on disabling, power down, changing the base address of the parallel port, and selecting the mode of operation.

The LPC47N227 also provides a mode for support of the floppy disk controller on the parallel port.

The parallel port also incorporates SMSC's ChiProtect circuitry, which prevents possible damage to the parallel port due to printer power-up.

The functionality of the Parallel Port is achieved through the use of eight addressable ports, with their associated registers and control gating. The control and data port are read/write by the CPU, the status port is read/write in the EPP mode. The address map of the Parallel Port is shown below

DATA PORT	BASE ADDRESS + 00H
STATUS PORT	BASE ADDRESS + 01H
CONTROL PORT	BASE ADDRESS + 02H
EPP ADDR PORT	BASE ADDRESS + 03H
EPP DATA PORT 0	BASE ADDRESS + 04H
EPP DATA PORT 1	BASE ADDRESS + 05H
EPP DATA PORT 2	BASE ADDRESS + 06H
EPP DATA PORT 3	BASE ADDRESS + 07H

The bit map of these registers is:

	D0	D1	D2	D3	D4	D5	D6	D7	Note
DATA PORT	PD0	PD1	PD2	PD3	PD4	PD5	PD6	PD7	1
STATUS PORT	TMOUT	0	0	nERR	SLCT	PE	nACK	nBUSY	1
CONTROL PORT	STROBE	AUTOFD	nINIT	SLC	IRQE	PCD	0	0	1
EPP ADDR PORT	PD0	PD1	PD2	PD3	PD4	PD5	PD6	PD7	2
EPP DATA PORT 0	PD0	PD1	PD2	PD3	PD4	PD5	PD6	PD7	2
EPP DATA PORT 1	PD0	PD1	PD2	PD3	PD4	PD5	PD6	PD7	2
EPP DATA PORT 2	PD0	PD1	PD2	PD3	PD4	PD5	PD6	PD7	2
EPP DATA PORT 3	PD0	PD1	PD2	PD3	PD4	PD5	PD6	PD7	2

Note 1: These registers are available in all modes.
Note 2: These registers are only available in EPP mode.

Table 35 - Parallel Port Connector

HOST CONNECTOR	PIN NUMBER	STANDARD	EPP	ECP
1	83	nSTROBE	nWrite	nStrobe
2-9	68-75	PD<0:7>	PData<0:7>	PData<0:7>
10	80	nACK	Intr	nAck
11	79	BUSY	nWait	Busy, PeriphAck(3)
12	78	PE	(User Defined)	PError, nAckReverse(3)
13	77	SLCT	(User Defined)	Select
14	82	nALF	nDatastb	nAutoFd, HostAck(3)
15	81	nERROR	(User Defined)	nFault(1) nPeriphRequest(3)
16	66	nINIT	nRESET	nInit(1) nReverseRqst(3)
17	67	nSLCTIN	nAddrstrb	nSelectIn(1,3)

(1) = Compatible Mode
(3) = High Speed Mode

Note: For the cable interconnection required for ECP support and the Slave Connector pin numbers, refer to the IEEE 1284 Extended Capabilities Port Protocol and ISA Standard, Rev. 1.14, July 14, 1993. This document is available from Microsoft.

IBM XT/AT Compatible, Bi-Directional And EPP Modes

Data Port
ADDRESS OFFSET = 00H

The Data Port is located at an offset of '00H' from the base address. The data register is cleared at initialization by RESET. During a WRITE operation, the Data Register latches the contents of the internal data bus. The contents of this register are buffered (non inverting) and output onto the PD0 - PD7 ports. During a READ operation in SPP mode, PD0 - PD7 ports are buffered (not latched) and output to the host CPU.

Status Port
ADDRESS OFFSET = 01H

The Status Port is located at an offset of '01H' from the base address. The contents of this register are latched for the duration of a read cycle. The bits of the Status Port are defined as follows:

BIT 0 TMOUT - TIME OUT
This bit is valid in EPP mode only and indicates that a 10 usec time out has occurred on the EPP bus. A logic zero means that no time out error has occurred; a logic 1 means that a time out error has been detected.

The means of clearing the TIMEOUT bit is controlled by the TIMEOUT_SELECT bit as follows. The TIMEOUT_SELECT bit is located at bit 2 of CR21.

- If the TIMEOUT_SELECT bit is cleared (‘0’), the TIMEOUT bit is cleared on the trailing edge of the read of the EPP Status Register (default)
- If the TIMEOUT_SELECT bit is set (‘1’), the TIMEOUT bit is cleared on a write of ‘1’ to the TIMEOUT bit.

The TIMEOUT bit is cleared on PCI_RESET regardless of the state of the TIMEOUT_SELECT bit.

BITS 1, 2 - are not implemented as register bits, during a read of the Printer Status Register these bits are a low level.

BIT 3 nERR - nERROR
The level on the nERROR input is read by the CPU as bit 3 of the Printer Status Register. A logic 0 means an error has been detected; a logic 1 means no error has been detected.

BIT 4 SLCT - PRINTER SELECTED STATUS
The level on the SLCT input is read by the CPU as bit 4 of the Printer Status Register. A logic 1 means the printer is on line; a logic 0 means it is not selected.

BIT 5 PE - PAPER END
The level on the PE input is read by the CPU as bit 5 of the Printer Status Register. A logic 1 indicates a paper end; a logic 0 indicates the presence of paper.

BIT 6 nACK - nACKNOWLEDGE
The level on the nACK input is read by the CPU as bit 6 of the Printer Status Register. A logic 0 means that the printer has received a character and can now accept another. A logic 1 means that it is still processing the last character or has not received the data.

BIT 7 nBUSY - nBUSY
The complement of the level on the BUSY input is read by the CPU as bit 7 of the Printer Status Register. A logic 0 in this bit means that the printer is busy and cannot accept a new character. A logic 1 means that it is ready to accept the next character.

Control Port
ADDRESS OFFSET = 02H

The Control Port is located at an offset of '02H' from the base address. The Control Register is initialized by the RESET input, bits 0 to 5 only being affected; bits 6 and 7 are hard wired low.

BIT 0 STROBE - STROBE
This bit is inverted and output onto the nSTROBE output.

BIT 1 AUTOFD - AUTOFEED
This bit is inverted and output onto the nAUTOFD output. A logic 1 causes the printer to generate a line feed after each line is printed. A logic 0 means no autofeed.

BIT 2 nINIT - nINITIATE OUTPUT
This bit is output onto the nINIT output without inversion.

BIT 3 SLCTIN - PRINTER SELECT INPUT
This bit is inverted and output onto the nSLCTIN output. A logic 1 on this bit selects the printer; a logic 0 means the printer is not selected.

BIT 4 IRQE - INTERRUPT REQUEST ENABLE
The interrupt request enable bit when set to a high level may be used to enable interrupt requests from the Parallel Port to the CPU. An interrupt request is generated on the IRQ port by a positive going nACK input. When the IRQE bit is programmed low the IRQ is disabled.

BIT 5 PCD - PARALLEL CONTROL DIRECTION
Parallel Control Direction is not valid in printer mode. In printer mode, the direction is always out regardless of the state of this bit. In bi-directional, EPP or ECP mode, a logic 0 means that the printer port is in output mode (write); a logic 1 means that the printer port is in input mode (read).

Bits 6 and 7 during a read are a low level, and cannot be written.

EPP Address Port
ADDRESS OFFSET = 03H

The EPP Address Port is located at an offset of '03H' from the base address. The address register is cleared at initialization by RESET. During a WRITE operation, the contents of the internal data bus DB0-DB7 are buffered (non inverting) and output onto the PD0 - PD7 ports. An LPC I/O write cycle causes an EPP ADDRESS WRITE cycle to be performed, during which the data is latched for the duration of the EPP write cycle. During a READ operation, PD0 - PD7 ports are read. An LPC I/O read cycle causes an EPP ADDRESS READ cycle to be performed and the data output to the host CPU, the deassertion of ADDRSTB latches the PData for the duration of the read cycle. This register is only available in EPP mode.

EPP Data Port 0
ADDRESS OFFSET = 04H

The EPP Data Port 0 is located at an offset of '04H' from the base address. The data register is cleared at initialization by RESET. During a WRITE operation, the contents of the internal data bus DB0-DB7 are buffered (non inverting) and output onto the PD0 - PD7 ports. An LPC I/O write cycle causes an EPP DATA WRITE cycle to be performed, during which the data is latched for the duration of the EPP write cycle. During a READ operation, PD0 - PD7 ports are read. An LPC I/O read cycle causes an EPP READ cycle to be performed and the data output to the host CPU, the deassertion of DATASTB latches the PData for the duration of the read cycle. This register is only available in EPP mode.

EPP Data Port 1
ADDRESS OFFSET = 05H

The EPP Data Port 1 is located at an offset of '05H' from the base address. Refer to EPP DATA PORT 0 for a description of operation. This register is only available in EPP mode.
EPP Data Port 2

ADDRESS OFFSET = 06H

The EPP Data Port 2 is located at an offset of '06H' from the base address. Refer to EPP DATA PORT 0 for a description of operation. This register is only available in EPP mode.

EPP Data Port 3
ADDRESS OFFSET = 07H

The EPP Data Port 3 is located at an offset of '07H' from the base address. Refer to EPP DATA PORT 0 for a description of operation. This register is only available in EPP mode.

EPP 1.9 Operation
When the EPP mode is selected in the configuration register, the standard and bi-directional modes are also available. If no EPP Read, Write or Address cycle is currently executing, then the PDx bus is in the standard or bi-directional mode, and all output signals (STROBE, AUTOFD, INIT) are as set by the SPP Control Port and direction is controlled by PCD of the Control port.

In EPP mode, the system timing is closely coupled to the EPP timing. For this reason, a watchdog timer is required to prevent system lockup. The timer indicates if more than 10usec have elapsed from the start of the EPP cycle to nWAIT being deasserted (after command). If a time-out occurs, the current EPP cycle is aborted and the time-out condition is indicated in Status bit 0.

During an EPP cycle, if STROBE is active, it overrides the EPP write signal forcing the PDx bus to always be in a write mode and the nWRITE signal to always be asserted.

Software Constraints
Before an EPP cycle is executed, the software must ensure that the control register bit PCD is a logic "0" (i.e., a 04H or 05H should be written to the Control port). If the user leaves PCD as a logic "1", and attempts to perform an EPP write, the chip is unable to perform the write (because PCD is a logic "1") and will appear to perform an EPP read on the parallel bus, no error is indicated.

EPP 1.9 Write
The timing for a write operation (address or data) is shown in timing diagram EPP Write Data or Address cycle. The chip inserts wait states into the LPC I/O write cycle until it has been determined that the write cycle can complete. The write cycle can complete under the following circumstances:

1. If the EPP bus is not ready (nWAIT is active low) when nDATASTB or nADDRSTB goes active then the write can complete when nWAIT goes inactive high.
2. If the EPP bus is ready (nWAIT is inactive high) then the chip must wait for it to go active low before changing the state of nDATASTB, nWRITE or nADDRSTB. The write can complete once nWAIT is determined inactive.

Write Sequence of operation
1. The host initiates an I/O write cycle to the selected EPP register.
2. If WAIT is not asserted, the chip must wait until WAIT is asserted.
3. The chip places address or data on PData bus, clears PDIR, and asserts nWRITE.
4. Chip asserts nDATASTB or nADDRSTRB indicating that PData bus contains valid information, and the WRITE signal is valid.
5. Peripheral deasserts nWAIT, indicating that any setup requirements have been satisfied and the chip may begin the termination phase of the cycle.

6. a) The chip deasserts nDATASTB or nADDRSTRB, this marks the beginning of the termination phase. If it has not already done so, the peripheral should latch the information byte now.
   b) The chip latches the data from the internal data bus for the PData bus and drives the sync that indicates that no more wait states are required followed by the TAR to complete the write cycle.
7. Peripheral asserts nWAIT, indicating to the host that any hold time requirements have been satisfied and acknowledging the termination of the cycle.
8. Chip may modify nWRITE and nPDATA in preparation for the next cycle.

EPP 1.9 Read

The timing for a read operation (data) is shown in timing diagram EPP Read Data cycle. The chip inserts wait states into the LPC I/O read cycle until it has been determined that the read cycle can complete. The read cycle can complete under the following circumstances:

1 If the EPP bus is not ready (nWAIT is active low) when nDATASTB goes active then the read can complete when nWAIT goes inactive high.

2. If the EPP bus is ready (nWAIT is inactive high) then the chip must wait for it to go active low before changing the state of WRITE or before nDATASTB goes active. The read can complete once nWAIT is determined inactive.

Read Sequence of Operation

1. The host initiates an I/O read cycle to the selected EPP register.
2. If WAIT is not asserted, the chip must wait until WAIT is asserted.
3. The chip tri-states the PData bus and deasserts nWRITE.
4. Chip asserts nDATASTB or nADDRSTRB indicating that PData bus is tri-stated, PDIR is set and the nWRITE signal is valid.
5. Peripheral drives PData bus valid.
6. Peripheral deasserts nWAIT, indicating that PData is valid and the chip may begin the termination phase of the cycle.
7. a) The chip latches the data from the PData bus for the internal data bus and deasserts nDATASTB or nADDRSTRB. This marks the beginning of the termination phase.
   b) The chip drives the sync that indicates that no more wait states are required and drives valid data onto the LAD[3:0] signals, followed by the TAR to complete the read cycle.
8. Peripheral tri-states the PData bus and asserts nWAIT, indicating to the host that the PData bus is tri-stated.
9. Chip may modify nWRITE, PDIR and nPDATA in preparation for the next cycle.

EPP 1.7 Operation

When the EPP 1.7 mode is selected in the configuration register, the standard and bi-directional modes are also available. If no EPP Read, Write or Address cycle is currently executing, then the PDx bus is in the standard or bi-directional mode, and all output signals (STROBE, AUTOFD, INIT) are as set by the SPP Control Port and direction is controlled by PCD of the Control port.

In EPP mode, the system timing is closely coupled to the EPP timing. For this reason, a watchdog timer is required to prevent system lockup. The timer indicates if more than 10usec have elapsed from the start of the EPP cycle to the end of the cycle. If a time-out occurs, the current EPP cycle is aborted and the time-out condition is indicated in Status bit 0.

Software Constraints

Before an EPP cycle is executed, the software must ensure that the control register bits D0, D1 and D3 are set to zero. Also, bit D5 (PCD) is a logic "0" for an EPP write or a logic "1" for and EPP read.

EPP 1.7 Write

The timing for a write operation (address or data) is shown in timing diagram EPP 1.7 Write Data or Address cycle. The chip inserts wait states into the I/O write cycle when nWAIT is active low during the EPP cycle. This can be used to extend the cycle time. The write cycle can complete when nWAIT is inactive high.

Write Sequence of Operation

1. The host sets PDIR bit in the control register to a logic "0". This asserts nWRITE.
2. The host initiates an I/O write cycle to the selected EPP register.
3. The chip places address or data on PData bus.
4. Chip asserts nDATASTB or nADDRSTRB indicating that PData bus contains valid information, and the WRITE signal is valid.
5. If nWAIT is asserted, the chip inserts wait states into I/O write cycle until the peripheral deasserts nWAIT or a time-out occurs.
6. The chip drives the final sync, deasserts nDATASTB or nADDRSTRB and latches the data from the internal data bus for the PData bus.
7. Chip may modify nWRITE, PDIR and nPDATA in preparation of the next cycle.

EPP 1.7 Read

The timing for a read operation (data) is shown in timing diagram EPP 1.7 Read Data cycle. The chip inserts wait states into the I/O read cycle when nWAIT is active low during the EPP cycle. This can be used to extend the cycle time. The read cycle can complete when nWAIT is inactive high.

Read Sequence of Operation

1. The host sets PDIR bit in the control register to a logic "1". This deasserts nWRITE and tri-states the PData bus.
2. The host initiates an I/O read cycle to the selected EPP register.
3. Chip asserts nDATASTB or nADDRSTRB indicating that PData bus is tri-stated, PDIR is set and the nWRITE signal is valid.
4. If nWAIT is asserted, the chip inserts wait states into the I/O read cycle until the peripheral deasserts nWAIT or a time-out occurs.
5. The Peripheral drives PData bus valid.
6. The Peripheral deasserts nWAIT, indicating that PData is valid and the chip may begin the termination phase of the cycle.
7. The chip drives the final sync and deasserts nDATASTB or nADDRSTRB.
8. Peripheral tri-states the PData bus.
9. Chip may modify nWRITE, PDIR and nPDATA in preparation of the next cycle.

Table 36 - EPP Pin Descriptions

EPP SIGNAL	EPP NAME	TYPE	EPP DESCRIPTION
nWRITE	nWrite	O	This signal is active low. It denotes a write operation.
PD<0:7>	Address/Data	I/O	Bi-directional EPP byte wide address and data bus.
INTR	Interrupt	I	This signal is active high and positive edge triggered. (Pass through with no inversion, Same as SPP).
WAIT	nWait	I	This signal is active low. It is driven inactive as a positive acknowledgement from the device that the transfer of data is completed. It is driven active as an indication that the device is ready for the next transfer.
DATASTB	nData Strobe	O	This signal is active low. It is used to denote data read or write operation.
RESET	nReset	O	This signal is active low. When driven active, the EPP device is reset to its initial operational mode.
ADDRSTB	nAddress Strobe	O	This signal is active low. It is used to denote address read or write operation.
PE	Paper End	I	Same as SPP mode.
SLCT	Printer Selected Status	I	Same as SPP mode.
nERR	Error	I	Same as SPP mode.

Note 1: SPP and EPP can use 1 common register.
Note 2: nWrite is the only EPP output that can be over-ridden by SPP control port during an EPP cycle. For correct EPP read cycles, PCD is required to be a low.

Extended Capabilities Parallel Port
ECP provides a number of advantages, some of which are listed below. The individual features are explained in greater detail in the remainder of this section.

High performance half-duplex forward and reverse channel Interlocked handshake, for fast reliable transfer Optional single byte RLE compression for improved throughput (64:1) Channel addressing for low-cost peripherals Maintains link and data layer separation Permits the use of active output drivers permits the use of adaptive signal timing Peer-to-peer capability.

Vocabulary
The following terms are used in this document:

assert: When a signal asserts it transitions to a "true" state, when a signal deasserts it transitions to a "false" state.
forward: Host to Peripheral communication.
reverse: Peripheral to Host communication
Pword: A port word; equal in size to the width of the LPC interface. For this implementation, PWord is always 8 bits.
1 A high level.
0 A low level.

These terms may be considered synonymous: PeriphClk, nAck
HostAck, nAutoFd

PeriphAck, Busy
nPeriphRequest, nFault
nReverseRequest, nInit
nAckReverse, PError

Xflag, Select
ECPMode, nSelectIn
HostClk, nStrobe

Reference Document: IEEE 1284 Extended Capabilities Port Protocol and ISA Interface Standard, Rev 1.14, July 14, 1993. This document is available from Microsoft.

The bit map of the Extended Parallel Port registers is:

	D7	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**	**Note**
data	PD7	PD6	PD5	PD4	PD3	PD2	PD1	PD0	
ecpAFifo	Addr/RLE	Address or RLE field							2
dsr	nBusy	nAck	PError	Select	nFault	0	0	0	1
dcr	0	0	Direction	ackIntEn	SelectIn	nInit	autofd	strobe	1
cFifo	Parallel Port Data FIFO								2
ecpDFifo	ECP Data FIFO								2
tFifo	Test FIFO								2
cnfgA	0	0	0	1	0	0	0	0	
cnfgB	compress	intrValue	Parallel Port IRQ			Parallel Port DMA			
ecr	MODE			nErrIntrEn	dmaEn	serviceIntr	full	empty	

Note 1: These registers are available in all modes.
Note 2: All FIFOs use one common 16 byte FIFO.
Note 3: The ECP Parallel Port Config Reg B reflects the IRQ and DMA channel selected by the Configuration Registers.

ECP Implementation Standard
This specification describes the standard interface to the Extended Capabilities Port (ECP). All LPC devices supporting ECP must meet the requirements contained in this section or the port will not be supported by Microsoft. For a description of the ECP Protocol, please refer to the IEEE 1284 Extended Capabilities Port Protocol and ISA Interface Standard, Rev. 1.14, July 14, 1993. This document is available from Microsoft.

Description
The port is software and hardware compatible with existing parallel ports so that it may be used as a standard LPT port if ECP is not required. The port is designed to be simple and requires a small number of gates to implement. It does not do any "protocol" negotiation, rather it provides an automatic high burst-bandwidth channel that supports DMA for ECP in both the forward and reverse directions.

Small FIFOs are employed in both forward and reverse directions to smooth data flow and improve the maximum bandwidth requirement. The size of the FIFO is 16 bytes deep. The port supports an automatic handshake for the standard parallel port to improve compatibility mode transfer speed.

The port also supports run length encoded (RLE) decompression (required) in hardware. Compression is accomplished by counting identical bytes and transmitting an RLE byte that indicates how many times the next byte is to be repeated. Decompression simply intercepts the RLE byte and repeats the following byte the specified number of times. Hardware support for compression is optional.

Table 37 - ECP Pin Descriptions

NAME	TYPE	DESCRIPTION
nStrobe	O	During write operations nStrobe registers data or address into the slave on the asserting edge (handshakes with Busy).
PData 7:0	I/O	Contains address or data or RLE data.
nAck	I	Indicates valid data driven by the peripheral when asserted. This signal handshakes with nAutoFd in reverse.
PeriphAck (Busy)	I	This signal deasserts to indicate that the peripheral can accept data. This signal handshakes with nStrobe in the forward direction. In the reverse direction this signal indicates whether the data lines contain ECP command information or data. The peripheral uses this signal to flow control in the forward direction. It is an "interlocked" handshake with nStrobe. PeriphAck also provides command information in the reverse direction.
PError (nAckReverse)	I	Used to acknowledge a change in the direction the transfer (asserted = forward). The peripheral drives this signal low to acknowledge nReverseRequest. It is an "interlocked" handshake with nReverseRequest. The host relies upon nAckReverse to determine when it is permitted to drive the data bus.
Select	I	Indicates printer on line.
nAutoFd (HostAck)	O	Requests a byte of data from the peripheral when asserted, handshaking with nAck in the reverse direction. In the forward direction this signal indicates whether the data lines contain ECP address or data. The host drives this signal to flow control in the reverse direction. It is an "interlocked" handshake with nAck. HostAck also provides command information in the forward phase.
nFault (nPeriphRequest)	I	Generates an error interrupt when asserted. This signal provides a mechanism for peer-to-peer communication. This signal is valid only in the forward direction. During ECP Mode the peripheral is permitted (but not required) to drive this pin low to request a reverse transfer. The request is merely a "hint" to the host; the host has ultimate control over the transfer direction. This signal would be typically used to generate an interrupt to the host CPU.
nInit	O	Sets the transfer direction (asserted = reverse, deasserted = forward). This pin is driven low to place the channel in the reverse direction. The peripheral is only allowed to drive the bi-directional data bus while in ECP Mode and HostAck is low and nSelectIn is high.
nSelectIn	O	Always deasserted in ECP mode.

Register Definitions

The register definitions are based on the standard IBM addresses for LPT. All of the standard printer ports are supported. The additional registers attach to an upper bit decode of the standard LPT port definition to avoid conflict with standard ISA devices. The port is equivalent to a generic parallel port interface and may be operated in that mode. The port registers vary depending on the mode field in the ecr. The table below lists these dependencies. Operation of the devices in modes other that those specified is undefined.

Table 38 - ECP Register Definitions

NAME	ADDRESS (Note 1)	ECP MODES	FUNCTION
data	+000h R/W	000-001	Data Register
ecpAFifo	+000h R/W	011	ECP FIFO (Address)
dsr	+001h R/W	All	Status Register
dcr	+002h R/W	All	Control Register
cFifo	+400h R/W	010	Parallel Port Data FIFO
ecpDFifo	+400h R/W	011	ECP FIFO (DATA)
tFifo	+400h R/W	110	Test FIFO
cnfgA	+400h R	111	Configuration Register A
cnfgB	+401h R/W	111	Configuration Register B
ecr	+402h R/W	All	Extended Control Register

Note 1: These addresses are added to the parallel port base address as selected by configuration register or jumpers.
Note 2: All addresses are qualified with AEN. Refer to the AEN pin definition.

Table 39 - Mode Descriptions

MODE	DESCRIPTION*
000	SPP mode
001	PS/2 Parallel Port mode
010	Parallel Port Data FIFO mode
011	ECP Parallel Port mode
100	EPP mode (If this option is enabled in the configuration registers)
101	Reserved
110	Test mode
111	Configuration mode

*Refer to ECR Register Description

Data And ecpAFifo Port
ADDRESS OFFSET = 00H

Modes 000 and 001 (Data Port)

The Data Port is located at an offset of '00H' from the base address. The data register is cleared at initialization by RESET. During a WRITE operation, the Data Register latches the contents of the data bus. The contents of this register are buffered (non inverting) and output onto the PD0 - PD7 ports. During a READ operation, PD0 - PD7 ports are read and output to the host CPU.
Mode 011 (ECP FIFO - Address/RLE)

A data byte written to this address is placed in the FIFO and tagged as an ECP Address/RLE. The hardware at the ECP port transmits this byte to the peripheral automatically. The operation of this register is ony defined for the forward direction (direction is 0). Refer to the ECP Parallel Port Forward Timing Diagram, located in the Timing Diagrams section of this data sheet .

Device Status Register (DSR)
ADDRESS OFFSET = 01H
The Status Port is located at an offset of '01H' from the base address. Bits 0 - 2 are not implemented as register bits, during a read of the Printer Status Register these bits are a low level. The bits of the Status Port are defined as follows:

BIT 3 nFault
The level on the nFault input is read by the CPU as bit 3 of the Device Status Register.

BIT 4 Select
The level on the Select input is read by the CPU as bit 4 of the Device Status Register.

BIT 5 PError
The level on the PError input is read by the CPU as bit 5 of the Device Status Register. Printer Status Register.

BIT 6 nAck
The level on the nAck input is read by the CPU as bit 6 of the Device Status Register.

BIT 7 nBusy
The complement of the level on the BUSY input is read by the CPU as bit 7 of the Device Status Register.

Device Control Register (DCR)
ADDRESS OFFSET = 02H

The Control Register is located at an offset of '02H' from the base address. The Control Register is initialized to zero by the RESET input, bits 0 to 5 only being affected; bits 6 and 7 are hard wired low.

BIT 0 STROBE - STROBE
This bit is inverted and output onto the nSTROBE output.

BIT 1 AUTOFD - AUTOFEED
This bit is inverted and output onto the nAUTOFD output. A logic 1 causes the printer to generate a line feed after each line is printed. A logic 0 means no autofeed.

BIT 2 nINIT - nINITIATE OUTPUT
This bit is output onto the nINIT output without inversion.

BIT 3 SELECTIN
This bit is inverted and output onto the nSLCTIN output. A logic 1 on this bit selects the printer; a logic 0 means the printer is not selected.

BIT 4 ackIntEn - INTERRUPT REQUEST ENABLE
The interrupt request enable bit when set to a high level may be used to enable interrupt requests from the Parallel Port to the CPU due to a low to high transition on the nACK input. Refer to the description of the interrupt under Operation, Interrupts.
BIT 5 DIRECTION
If mode=000 or mode=010, this bit has no effect and the direction is always out regardless of the state of this bit. In all other modes, Direction is valid and a logic 0 means that the printer port is in output mode (write); a logic 1 means that the printer port is in input mode (read).

BITS 6 and 7 during a read are a low level, and cannot be written.

cFifo (Parallel Port Data FIFO)
ADDRESS OFFSET = 400h
Mode = 010

Bytes written or DMAed from the system to this FIFO are transmitted by a hardware handshake to the peripheral using the standard parallel port protocol. Transfers to the FIFO are byte aligned. This mode is only defined for the forward direction.

ecpDFifo (ECP Data FIFO)
ADDRESS OFFSET = 400H
Mode = 011

Bytes written or DMAed from the system to this FIFO, when the direction bit is 0, are transmitted by a hardware handshake to the peripheral using the ECP parallel port protocol. Transfers to the FIFO are byte aligned.

Data bytes from the peripheral are read under automatic hardware handshake from ECP into this FIFO when the direction bit is 1. Reads or DMAs from the FIFO will return bytes of ECP data to the system.

tFifo (Test FIFO Mode)
ADDRESS OFFSET = 400H
Mode = 110

Data bytes may be read, written or DMAed to or from the system to this FIFO in any direction. Data in the tFIFO will not be transmitted to the to the parallel port lines using a hardware protocol handshake. However, data in the tFIFO may be displayed on the parallel port data lines.

The tFIFO will not stall when overwritten or underrun. If an attempt is made to write data to a full tFIFO, the new data is not accepted into the tFIFO. If an attempt is made to read data from an empty tFIFO, the last data byte is re-read again. The full and empty bits must always keep track of the correct FIFO state. The tFIFO will transfer data at the maximum ISA rate so that software may generate performance metrics.

The FIFO size and interrupt threshold can be determined by writing bytes to the FIFO and checking the full and serviceIntr bits.

The writeIntrThreshold can be determined by starting with a full tFIFO, setting the direction bit to 0 and emptying it a byte at a time until serviceIntr is set. This may generate a spurious interrupt, but will indicate that the threshold has been reached.

The readIntrThreshold can be determined by setting the direction bit to 1 and filling the empty tFIFO a byte at a time until serviceIntr is set. This may generate a spurious interrupt, but will indicate that the threshold has been reached.

Data bytes are always read from the head of tFIFO regardless of the value of the direction bit. For example if 44h, 33h, 22h is written to the FIFO, then reading the tFIFO will return 44h, 33h, 22h in the same order as was written.

cnfgA (Configuration Register A)
ADDRESS OFFSET = 400H
Mode = 111
This register is a read only register. When read, 10H is returned. This indicates to the system that this is an 8-bit implementation. (PWord = 1 byte)

cnfgB (Configuration Register B)
ADDRESS OFFSET = 401H
Mode = 111

BIT 7 compress
This bit is read only. During a read it is a low level. This means that this chip does not support hardware RLE compression. It does support hardware de-compression!

BIT 6 intrValue
Returns the value of the interrupt to determine possible conflicts.

BITS [5:3] Parallel Port IRQ (read-only)
Refer to Table 40B.

BITS [2:0] Parallel Port DMA (read-only)
Refer to Table 40C.

ecr (Extended Control Register)
ADDRESS OFFSET = 402H
Mode = all
This register controls the extended ECP parallel port functions.

BITS 7,6,5
These bits are Read/Write and select the Mode.

BIT 4 nErrIntrEn
Read/Write (Valid only in ECP Mode)
1: Disables the interrupt generated on the asserting edge of nFault.
0: Enables an interrupt pulse on the high to low edge of nFault. Note that an interrupt will be generated if nFault is asserted (interrupting) and this bit is written from a 1 to a 0. This prevents interrupts from being lost in the time between the read of the ecr and the write of the ecr.

BIT 3 dmaEn
Read/Write
1: Enables DMA (DMA starts when serviceIntr is 0).
0: Disables DMA unconditionally.

BIT 2 serviceIntr
Read/Write
1: Disables DMA and all of the service interrupts.
0: Enables one of the following 3 cases of interrupts. Once one of the 3 service interrupts has occurred serviceIntr bit shall be set to a 1 by hardware. It must be reset to 0 to re-enable the interrupts. Writing this bit to a 1 will not cause an interrupt.
case dmaEn=1:

During DMA (this bit is set to a 1 when terminal count is reached).

case dmaEn=0 direction=0:

This bit shall be set to 1 whenever there are writeIntrThreshold or more bytes free in the FIFO.

case dmaEn=0 direction=1:

This bit shall be set to 1 whenever there are readIntrThreshold or more valid bytes to be read from the FIFO.

BIT 1 full

Read only

1: The FIFO cannot accept another byte or the FIFO is completely full.

0: The FIFO has at least 1 free byte.

BIT 0 empty

Read only

1: The FIFO is completely empty.

0: The FIFO contains at least 1 byte of data.

Table 40A - Extended Control Register

R/W	MODE
000:	Standard Parallel Port Mode . In this mode the FIFO is reset and common collector drivers are used on the control lines (nStrobe, nAutoFd, nInit and nSelectIn). Setting the direction bit will not tri-state the output drivers in this mode.
001:	PS/2 Parallel Port Mode. Same as above except that direction may be used to tri-state the data lines and reading the data register returns the value on the data lines and not the value in the data register. All drivers have active pull-ups (push-pull).
010:	Parallel Port FIFO Mode. This is the same as 000 except that bytes are written or DMAed to the FIFO. FIFO data is automatically transmitted using the standard parallel port protocol. Note that this mode is only useful when direction is 0. All drivers have active pull-ups (push-pull).
011:	ECP Parallel Port Mode. In the forward direction (direction is 0) bytes placed into the ecpDFifo and bytes written to the ecpAFifo are placed in a single FIFO and transmitted automatically to the peripheral using ECP Protocol. In the reverse direction (direction is 1) bytes are moved from the ECP parallel port and packed into bytes in the ecpDFifo. All drivers have active pull-ups (push-pull).
100:	Selects EPP Mode: In this mode, EPP is selected if the EPP supported option is selected in configuration register CR04 (Bits[1,0] and Bit[6]). All drivers have active pull-ups (push-pull).
101:	Reserved
110:	Test Mode. In this mode the FIFO may be written and read, but the data will not be transmitted on the parallel port. All drivers have active pull-ups (push-pull).
111:	Configuration Mode. In this mode the confgA, confgB registers are accessible at 0x400 and 0x401. All drivers have active pull-ups (push-pull).

Table 40B

IRQ SELECTED	cnfgB BITS [5:3]
15	110
14	101
11	100
10	011
9	010
7	001
5	111
All Others	000

Table 40C

DMA SELECTED	cnfgB BITS [2:0]
3	011
2	010
1	001
All Others	000

Operation

Mode Switching/Software Control

Software will execute P1284 negotiation and all operation prior to a data transfer phase under programmed I/O control (mode 000 or 001). Hardware provides an automatic control line handshake, moving data between the FIFO and the ECP port only in the data transfer phase (modes 011 or 010).

Setting the mode to 011 or 010 will cause the hardware to initiate data transfer. If the port is in mode 000 or 001 it may switch to any other mode. If the port is not in mode 000 or 001 it can only be switched into mode 000 or 001. The direction can only be changed in mode 001.

ECP Operation
Prior to ECP operation the Host must negotiate on the parallel port to determine if the peripheral supports the ECP protocol. This is a somewhat complex negotiation carried out under program control in mode 000.

After negotiation, it is necessary to initialize some of the port bits. The following are required:

Set Direction = 0, enabling the drivers.
Set strobe = 0, causing the nStrobe signal to default to the deasserted state.
Set autoFd = 0, causing the nAutoFd signal to default to the deasserted state.
Set mode = 011 (ECP Mode)

ECP address/RLE bytes or data bytes may be sent automatically by writing the ecpAFifo or ecpDFifo respectively.

Note that all FIFO data transfers are byte wide and byte aligned. Address/RLE transfers are byte-wide and only allowed in the forward direction.

The host may switch directions by first switching to mode = 001, negotiating for the forward or reverse channel, setting direction to 1 or 0, then setting mode = 011. When direction is 1 the hardware shall handshake for each ECP read data byte and attempt to fill the FIFO. Bytes may then be read from the ecpDFifo as long as it is not empty.

ECP transfers may also be accomplished (albeit slowly) by handshaking individual bytes under program control in mode = 001, or 000.

Termination from ECP Mode
Termination from ECP Mode is similar to the termination from Nibble/Byte Modes. The host is permitted to terminate from ECP Mode only in specific well-defined states. The termination can only be executed while the bus is in the forward direction. To terminate while the channel is in the reverse direction, it must first be transitioned into the forward direction.

Command/Data
ECP Mode supports two advanced features to improve the effectiveness of the protocol for some applications. The features are implemented by allowing the transfer of normal 8 bit data or 8 bit commands.

When in the forward direction, normal data is transferred when HostAck is high and an 8 bit command is transferred when HostAck is low.

The most significant bit of the command indicates whether it is a run-length count (for compression) or a channel address.

When in the reverse direction, normal data is transferred when PeriphAck is high and an 8 bit command is transferred when PeriphAck is low. The most significant bit of the command is always zero. Reverse channel addresses are seldom used and may not be supported in hardware.

Table 41 -
Forward Channel Commands (HostAck Low)
Reverse Channel Commands (PeripAck Low)

D7	D[6:0]
0	Run-Length Count (0-127) (mode 0011 0X00 only)
1	Channel Address (0-127)

Data Compression
The ECP port supports run length encoded (RLE) decompression in hardware and can transfer compressed data to a peripheral. Run length encoded (RLE) compression in hardware is not supported. To transfer compressed data in ECP mode, the compression count is written to the ecpAFifo and the data byte is written to the ecpDFifo.

Compression is accomplished by counting identical bytes and transmitting an RLE byte that indicates how many times the next byte is to be repeated. Decompression simply intercepts the RLE byte and repeats the following byte the specified number of times. When a run-length count is received from a peripheral, the subsequent data byte is replicated the specified number of times. A run-length count of zero specifies that only one byte of data is represented by the next data byte, whereas a run-length count of 127 indicates that the next byte should be expanded to 128 bytes. To prevent data expansion, however, run-length counts of zero should be avoided.

Pin Definition
The drivers for nStrobe, nAutoFd, nInit and nSelectIn are open-collector in mode 000 and are push-pull in all other modes.

LPC Connections
The interface can never stall causing the host to hang. The width of data transfers is strictly controlled on an I/O address basis per this specification. All FIFO-DMA transfers are byte wide, byte aligned and end on a byte boundary. (The PWord value can be obtained by reading Configuration Register A, cnfgA, described in the next section). Single byte wide transfers are always possible with standard or PS/2 mode using program control of the control signals.

Interrupts
The interrupts are enabled by serviceIntr in the ecr register.

serviceIntr = 1 Disables the DMA and all of the service interrupts.

serviceIntr = 0 Enables the selected interrupt condition. If the interrupting condition is valid, then the interrupt is generated immediately when this bit is changed from a 1 to a 0. This can occur during Programmed I/O if the number of bytes removed or added from/to the FIFO does not cross the threshold.

An interrupt is generated when:
1. For DMA transfers: When serviceIntr is 0, dmaEn is 1 and the DMA TC cycle is received.
2. For Programmed I/O:
   a. When serviceIntr is 0, dmaEn is 0, direction is 0 and there are writeIntrThreshold or more free bytes in the FIFO. Also, an interrupt is generated when serviceIntr is cleared to 0 whenever there are writeIntrThreshold or more free bytes in the FIFO.

b. When serviceIntr is 0, dmaEn is 0, direction is 1 and there are readIntrThreshold or more bytes in the FIFO. Also, an interrupt is generated when serviceIntr is cleared to 0 whenever there are readIntrThreshold or more bytes in the FIFO.

3. When nErrIntrEn is 0 and nFault transitions from high to low or when nErrIntrEn is set from 1 to 0 and nFault is asserted.
4. When ackIntEn is 1 and the nAck signal transitions from a low to a high.

FIFO Operation

The FIFO threshold is set in the chip configuration registers. All data transfers to or from the parallel port can proceed in DMA or Programmed I/O (non-DMA) mode as indicated by the selected mode. The FIFO is used by selecting the Parallel Port FIFO mode or ECP Parallel Port Mode. (FIFO test mode will be addressed separately.) After a reset, the FIFO is disabled. Each data byte is transferred by a Programmed I/O cycle or DMA cycle depending on the selection of DMA or Programmed I/O mode.

The following paragraphs detail the operation of the FIFO flow control. In these descriptions, <threshold> ranges from 1 to 16. The parameter FIFOTHR, which the user programs, is one less and ranges from 0 to 15.

A low threshold value (i.e. 2) results in longer periods of time between service requests, but requires faster servicing of the request for both read and write cases. The host must be very responsive to the service request. This is the desired case for use with a "fast" system. A high value of threshold (i.e. 12) is used with a "sluggish" system by affording a long latency period after a service request, but results in more frequent service requests.

DMA Transfers

DMA transfers are always to or from the ecpDFifo, tFifo or CFifo. DMA utilizes the standard PC DMA services. To use the DMA transfers, the host first sets up the direction and state as in the programmed I/O case. Then it programs the DMA controller in the host with the desired count and memory address. Lastly it sets dmaEn to 1 and serviceIntr to 0. The ECP requests DMA transfers from the host by encoding the nLDRQ pin. The DMA will empty or fill the FIFO using the appropriate direction and mode. When the terminal count in the DMA controller is reached, an interrupt is generated and serviceIntr is asserted, disabling DMA. In order to prevent possible blocking of refresh requests a DMA cycle shall not be requested for more than 32 DMA cycles in a row. The FIFO is enabled directly by the host initiating a DMA cycle for the requested channel, and addresses need not be valid. An interrupt is generated when a TC cycle is received. (Note: The only way to properly terminate DMA transfers is with a TC cycle.)

DMA may be disabled in the middle of a transfer by first disabling the host DMA controller. Then setting serviceIntr to 1, followed by setting dmaEn to 0, and waiting for the FIFO to become empty or full. Restarting the DMA is accomplished by enabling DMA in the host, setting dmaEn to 1, followed by setting serviceIntr to 0.

DMA Mode - Transfers from the FIFO to the Host

(Note: In the reverse mode, the peripheral may not continue to fill the FIFO if it runs out of data to transfer, even if the chip continues to request more data from the peripheral.)

The ECP requests a DMA cycle whenever there is data in the FIFO. The DMA controller responds to the request by reading data from the FIFO. The ECP stop requesting DMA cycles when the FIFO becomes empty or when a TC cycle is received, indicating that no more data is required. If the ECP stops requesting DMA cycles due to the FIFO going empty, then a DMA cycle is requested again as soon as there is one byte in the FIFO. If the ECP stops requesting DMA cycles due to the TC cycle, then a DMA cycle is requested again when there is one byte in the FIFO, and serviceIntr has been re-enabled.

Programmed I/O Mode or Non-DMA Mode
The ECP or parallel port FIFOs may also be operated using interrupt driven programmed I/O. Software can determine the writeIntrThreshold, readIntrThreshold, and FIFO depth by accessing the FIFO in Test Mode.

Programmed I/O transfers are to the ecpDFifo at 400H and ecpAFifo at 000H or from the ecpDFifo located at 400H, or to/from the tFifo at 400H. To use the programmed I/O transfers, the host first sets up the direction and state, sets dmaEn to 0 and serviceIntr to 0.

The ECP requests programmed I/O transfers from the host by activating the interrupt. The programmed I/O will empty or fill the FIFO using the appropriate direction and mode.

Note: A threshold of 16 is equivalent to a threshold of 15. These two cases are treated the same.

Programmed I/O - Transfers from the FIFO to the Host
In the reverse direction an interrupt occurs when serviceIntr is 0 and readIntrThreshold bytes are available in the FIFO. If at this time the FIFO is full it can be emptied completely in a single burst, otherwise readIntrThreshold bytes may be read from the FIFO in a single burst.

readIntrThreshold =(16-<threshold>) data bytes in FIFO
An interrupt is generated when serviceIntr is 0 and the number of bytes in the FIFO is greater than or equal to (16-<threshold>). (If the threshold = 12, then the interrupt is set whenever there are 4-16 bytes in the FIFO). The host must respond to the request by reading data from the FIFO. This process is repeated until the last byte is transferred out of the FIFO. If at this time the FIFO is full, it can be completely emptied in a single burst, otherwise a minimum of (16-<threshold>) bytes may be read from the FIFO in a single burst.

Programmed I/O - Transfers from the Host to the FIFO
In the forward direction an interrupt occurs when serviceIntr is 0 and there are writeIntrThreshold or more bytes free in the FIFO. At this time if the FIFO is empty it can be filled with a single burst before the empty bit needs to be re-read. Otherwise it may be filled with writeIntrThreshold bytes.

writeIntrThreshold = (16-<threshold>) free bytes in FIFO

An interrupt is generated when serviceIntr is 0 and the number of bytes in the FIFO is less than or equal to <threshold>. (If the threshold = 12, then the interrupt is set whenever there are 12 or less bytes of data in the FIFO.) The host must respond to the request by writing data to the FIFO. If at this time the FIFO is empty, it can be completely filled in a single burst, otherwise a minimum of (16-<threshold>) bytes may be written to the FIFO in a single burst. This process is repeated until the last byte is transferred into the FIFO.
Parallel Port Floppy Disk Controller
The Floppy Disk Control signals are available optionally on the parallel port pins. When this mode is selected, the parallel port is not available. There are two modes of operation, PPFD1 and PPFD2. These modes can be selected in the Parallel and Serial Extended Setup Register (CR04). PPFD1 has only drive 1 on the parallel port pins; PPFD2 has drive 0 and 1 on the parallel port pins. See the Configuration section for description of the register. The FDC_PP pin can be used to switch the parallel port pins between the FDC and the parallel port functions. See the following sub-section.

The following parallel port pins are read as follows by a read of the parallel port register:

1. Data Register (read) = last Data Register (write)

2. Control Register read as "cable not connected" STROBE, AUTOFD and SLC = 0 and nINIT =1
3. Status Register reads: nBUSY = 0, PE = 0, SLCT = 0, nACK = 1, nERR = 1

The following FDC pins are all in the high impedence state when the PPFDC is actually selected by the drive select register:
1. nWDATA, DENSEL, nHDSEL, nWGATE, nDIR, nSTEP, nDS1, nDS0, nMTR0, nMTR1.
2. If PPFDx is selected, then the parallel port can not be used as a parallel port until "Normal" mode is selected.

The FDC signals are muxed onto the Parallel Port pins as shown in Table 43.

For ACPI compliance the FDD pins that are multiplexed onto the Parallel Port function independently of the state of the Parallel Port controller. For example, if the FDC is enabled onto the Parallel Port the multiplexed FDD interface functions normally regardless of the Parallel Port Power control, CR01.2.

Table 42 illustrates this functionality.

Table 42 - Modified Parallel Port FDD Control

PARALLEL PORT POWER	PARALLEL PORT FDC CONTROL		PARALLEL PORT FDC STATE	PARALLEL PORT STATE
CR01.2	**CR04.3**	**CR04.2**		
1	0	0	OFF	ON
0	0	0	OFF	OFF
X	1	X	ON	OFF
	X	1		(NOTE[1])

NOTE[1]: The Parallel Port Control register reads as “Cable Not Connected” when the Parallel Port FDC is enabled; i.e., STROBE = AUTOFD = SLC = 0 and nINIT = 1.

Table 43 – FDC Parallel Port Pins

CONNECTOR PIN #	CHIP PIN #	SPP MODE	PIN DIRECTION	FDC MODE	PIN DIRECTION
1	83	nSTROBE	I/O	(nDS0)	I/(O) Note1
2	68	PD0	I/O	nINDEX	I
3	69	PD1	I/O	nTRK0	I
4	70	PD2	I/O	nWP	I
5	71	PD3	I/O	nRDATA	I
6	72	PD4	I/O	nDSKCHG	I
7	73	PD5	I/O	-	-
8	74	PD6	I/O	(nMTR0)	I/(O) Note1
9	75	PD7	I/O	-	-
10	80	nACK	I	nDS1	O
11	79	BUSY	I	nMTR1	O
12	78	PE	I	nWDATA	O
13	77	SLCT	I	nWGATE	O
14	82	nALF	I/O	DRVDEN0	O
15	81	nERROR	I	nHDSEL	O
16	66	nINIT	I/O	nDIR	O
17	67	nSLCTIN	I/O	nSTEP	O

Note 1: These pins are outputs in mode PPFD2, inputs in mode PPFD1.

FDC on Parallel Port Pin

The “floppy on the parallel port” pin function, FDC_PP, is muxed onto GP23. This pin function can be used to switch the parallel port pins between the FDC and the parallel port. The FDC_PP pin can generate a PME and an SMI by enabling GP23 in the appropriate PME and SMI enable registers (bit 5 of PME_EN2 and bit 4 of SMI_EN2 – see the Runtime Registers section). This pin generates an SMI and PME on both a low-to-high and a high-to-low edge.

The pin function for GP23 and the polarity of GP23 is selected through GPIO Polarity Register 2. When the FDC_PP function is selected, the pin must also be selected as an input via bit 3 of the GPIO Direction Register 2.

If the Floppy_PP bits, CR21 bits[1:0] = 01 or 10, and the FDC_PP function is selected on GP23, then the default functionality (non-inverted polarity) for this pin is as follows: when the pin is low, the parallel port pins are used for a floppy disk controller; when the pin is high, the parallel port pins are used for a parallel port. The polarity bit controls the state of the pin.

If the Floppy_PP bits, CR21 bits[1:0]=00 then the pin is not used to switch the parallel port pins between the FDC and the parallel port, even if the FDC_PP function is selected on GP23. See the Configuration section for register description.

Note: When the floppy is selected on the parallel port, the parallel port IRQ, SMI and the parallel port DRQ will not come out of the part.

POWER MANAGEMENT

Power management capabilities are provided for the following logical devices: floppy disk, UART 1, UART 2 and the parallel port. For each logical device, two types of power management are provided: direct powerdown and auto powerdown.

FDC Power Management
Direct power management is controlled by Bit[3] in CR00. Refer to the Configuration section for more information.

Auto Power Management is enabled by Bit[7] in CR07. When set, this bit allows FDC to enter powerdown when all of the following conditions have been met:

1. The motor enable pins of register 3F2H are inactive (zero).
2. The part must be idle; MSR=80H and INT = 0 (INT may be high even if MSR = 80H due to polling interrupts).
3. The head unload timer must have expired.
4. The Auto powerdown timer (10msec) must have timed out.

An internal timer is initiated as soon as the auto powerdown command is enabled. The part is then powered down when all the conditions are met.

Disabling the auto powerdown mode cancels the timer and holds the FDC block out of auto powerdown.

DSR From Powerdown
If DSR powerdown is used when the part is in auto powerdown, the DSR powerdown will override the auto powerdown. However, when the part is awakened from DSR powerdown, the auto powerdown will once again become effective.

Wake Up From Auto Powerdown
If the part enters the powerdown state through the auto powerdown mode, then the part can be awakened by reset or by appropriate access to certain registers.

If a hardware or software reset is used then the part will go through the normal reset sequence. If the access is through the selected registers, then the FDC resumes operation as though it was never in powerdown. Besides activating the nPCI_RESET pin or one of the software reset bits in the DOR or DSR, the following register accesses will wake up the part:

1. Enabling any one of the motor enable bits in the DOR register (reading the DOR does not awaken the part).
2. A read from the MSR register.
3. A read or write to the Data register.

Once awake, the FDC will reinitiate the auto powerdown timer for 10 ms. The part will powerdown again when all the powerdown conditions are satisfied.

Register Behavior
Table 44 illustrates the AT and PS/2 (including Model 30) configuration registers available and the type of access permitted. In order to maintain software transparency, access to all the registers must be

maintained. As Table 44 shows, two sets of registers are distinguished based on whether their access results in the part remaining in powerdown state or exiting it.

Access to all other registers is possible without awakening the part. These registers can be accessed during powerdown without changing the status of the part. A read from these registers will reflect the true status as shown in the register description in the FDC description. A write to the part will result in the part retaining the data and subsequently reflecting it when the part awakens. Accessing the part during powerdown may cause an increase in the power consumption by the part. The part will revert back to its low power mode when the access has been completed.

Pin Behavior

The LPC47N227 is specifically designed for systems in which power conservation is a primary concern. This makes the behavior of the pins during powerdown very important.

The pins of the LPC47N227 can be divided into two major categories: system interface and floppy disk drive interface. The floppy disk drive pins are disabled so that no power will be drawn through the part as a result of any voltage applied to the pin within the part's power supply range. Most of the system interface pins are left active to monitor system accesses that may wake up the part.

Table 44 - PC/AT and PS/2 Available Registers

	AVAILABLE REGISTERS		
BASE + ADDRESS	**PC-AT**	**PS/2 (MODEL 30)**	**ACCESS PERMITTED**
Access to these registers DOES NOT wake up the part			
00H	----	SRA	R
01H	----	SRB	R
02H	DOR (1)	DOR (1)	R/W
03H	---	---	---
04H	DSR (1)	DSR (1)	W
06H	---	---	---
07H	DIR	DIR	R
07H	CCR	CCR	W
Access to these registers wakes up the part			
04H	MSR	MSR	R
05H	Data	Data	R/W

Note 1: Writing to the DOR or DSR does not wake up the part, however, writing any of the motor enable bits or doing a software reset (via DOR or DSR reset bits) will wake up the part.

System Interface Pins

Table 45 gives the state of the interface pins in the powerdown state. Pins unaffected by the powerdown are labeled "Unchanged".

Table 45 – State of System Pins in Auto Powerdown

SYSTEM PINS	STATE IN AUTO POWERDOWN
LAD[3:0]	Unchanged
nLDRQ	Unchanged
nLPCPD	Unchanged
nLFRAME	Unchanged

nPCI_RESET	Unchanged
PCI_CLK	Unchanged
SER_IRQ	Unchanged

FDD Interface Pins
All pins in the FDD interface which can be connected directly to the floppy disk drive itself are either DISABLED or TRISTATED.

Pins used for local logic control or part programming are unaffected. Table 46 depicts the state of the floppy disk drive interface pins in the powerdown state.

Table 46 - State of Floppy Disk Drive Interface Pins in Powerdown

FDD PINS	STATE IN AUTO POWERDOWN
INPUT PINS	
nRDATA	Input
nWRTPRT	Input
nTRK0	Input
nINDEX	Input
nDSKCHG	Input
OUTPUT PINS	
nMTR0	Tristated
nDS0	Tristated
nDIR	Active
nSTEP	Active
nWDATA	Tristated
nWGATE	Tristated
nHDSEL	Active
DRVDEN[0:1]	Active

UART Power Management
Direct power management is controlled by CR02. Refer to the Configuration section for more information.

Auto Power Management is enabled by the UART1 and UART2 enable bits in CR07. When set, these bits allow the following auto power management operations:

1. The transmitter enters auto powerdown when the transmit buffer and shift register are empty.
2. The receiver enters powerdown when the following conditions are all met:

    A. Receive FIFO is empty
    B. The receiver is waiting for a start bit.

Note: While in powerdown the Ring Indicator interrupt is still valid and transitions when the RI input changes.

Exit Auto Powerdown
The transmitter exits powerdown on a write to the XMIT buffer. The receiver exits auto powerdown when RXDx changes state.

Parallel Port

Direct power management is controlled by Bit[2] in CR01. Refer to the Configuration section for more information.

Auto Power Management is enabled by Bit[4] in CR07 . When set, this bit allows the ECP or EPP logical parallel port blocks to be placed into powerdown when not being used.

The EPP logic is in powerdown under any of the following conditions:

1. EPP is not enabled in the configuration registers.
2. EPP is not selected through ecr while in ECP mode.

The ECP logic is in powerdown under any of the following conditions:

1. ECP is not enabled in the configuration registers.
2 SPP, PS/2 Parallel port or EPP mode is selected through ecr while in ECP mode.

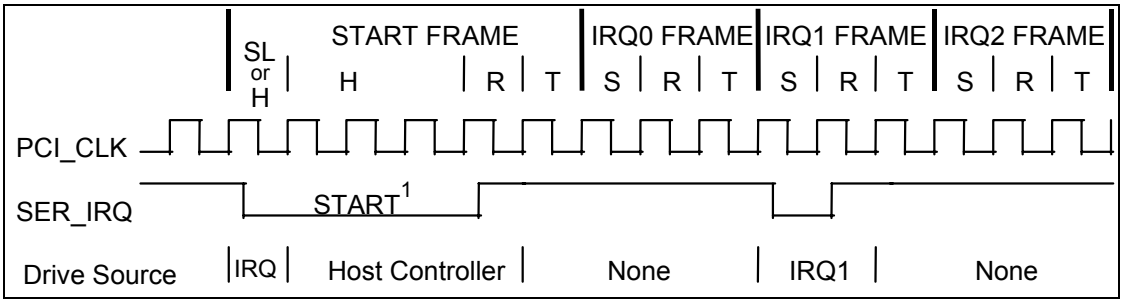
Exit Auto Powerdown
The parallel port logic can change powerdown modes when the ECP mode is changed through the ecr register or when the parallel port mode is changed through the configuration registers.

SERIAL IRQ

The LPC47N227 supports the serial interrupt to transmit interrupt information to the host system. The serial interrupt scheme adheres to the Serial IRQ Specification for PCI Systems, Version 6.0. The PCI_CLK, SER_IRQ and nCLKRUN pins are used for this interface. The Serial IRQ/CLKRUN Enable bit D7 in CR29 activates the serial interrupt interface.

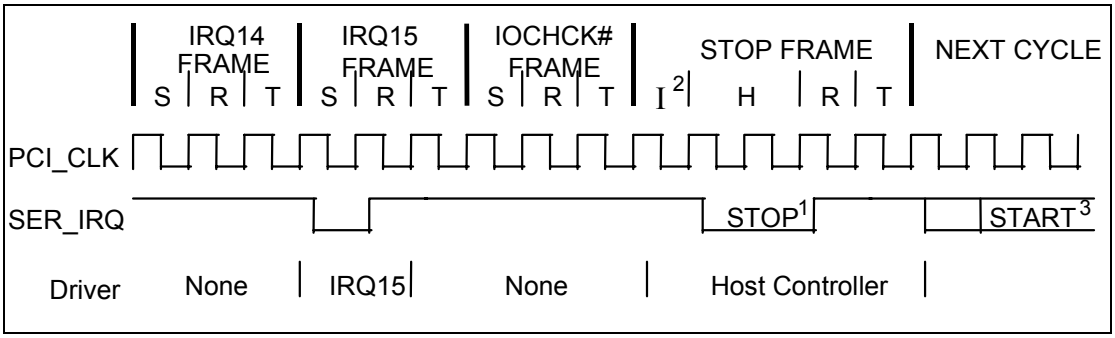
Timing Diagrams For SER_IRQ Cycle

A) Start Frame timing with source sampled a low pulse on IRQ1



Note: H=Host Control; R=Recovery; T=Turn-Around; SL=Slave Control; S=Sample
Note 1: Start Frame pulse can be 4-8 clocks wide depending on the location of the device in the PCI bridge hierarchy in a synchronous bridge design.

B) Stop Frame Timing with Host using 17 SER_IRQ sampling period



Note: H=Host Control; R=Recovery; T=Turn-Around; S=Sample; I=Idle
Note 1: Stop pulse is 2 clocks wide for Quiet mode, 3 clocks wide for Continuous mode.
Note 2: There may be none, one or more Idle states during the Stop Frame.
Note 3: The next SER_IRQ cycle's Start Frame pulse may or may not start immediately after the turn-around clock of the Stop Frame.

SER_IRQ Cycle Control
There are two modes of operation for the SER_IRQ Start Frame.

1) **Quiet (Active) Mode**: Any device may initiate a Start Frame by driving the SER_IRQ low for one clock, while the SER_IRQ is Idle. After driving low for one clock the SER_IRQ is immediately tri-stated without at any time driving high. A Start Frame may not be initiated while the SER_IRQ is Active. The SER_IRQ is Idle between Stop and Start Frames. The SER_IRQ is Active between Start and Stop Frames. This mode of operation allows the SER_IRQ to be Idle when there are no IRQ/Data transitions which should be most of the time.

Once a Start Frame has been initiated the Host Controller will take over driving the SER_IRQ low in the next clock and will continue driving the SER_IRQ low for a programmable period of three to seven clocks. This makes a total low pulse width of four to eight clocks. Finally, the Host Controller will drive the SER_IRQ back high for one clock, then tri-state.

Any SER_IRQ Device (i.e., The LPC47N227) which detects any transition on an IRQ/Data line for which it is responsible must initiate a Start Frame in order to update the Host Controller unless the SER_IRQ is already in an SER_IRQ Cycle and the IRQ/Data transition can be delivered in that SER_IRQ Cycle.

2) **Continuous (Idle) Mode**: Only the Host controller can initiate a Start Frame to update IRQ/Data line information. All other SER_IRQ agents become passive and may not initiate a Start Frame. SER_IRQ will be driven low for four to eight clocks by Host Controller. This mode has two functions. It can be used to stop or idle the SER_IRQ or the Host Controller can operate SER_IRQ in a continuous mode by initiating a Start Frame at the end of every Stop Frame.

An SER_IRQ mode transition can only occur during the Stop Frame. Upon reset, SER_IRQ bus is defaulted to Continuous mode, therefore only the Host controller can initiate the first Start Frame. Slaves must continuously sample the Stop Frames pulse width to determine the next SER_IRQ Cycle's mode.

SER_IRQ Data Frame
Once a Start Frame has been initiated, the LPC47N227 will watch for the rising edge of the Start Pulse and start counting IRQ/Data Frames from there. Each IRQ/Data Frame is three clocks: Sample phase, Recovery phase, and Turn-around phase. During the Sample phase the LPC47N227 drives the SER_IRQ low, if and only if, its last detected IRQ/Data value was low. If its detected IRQ/Data value is high, SER_IRQ is left tri-stated. During the Recovery phase the LPC47N227 drives the SER_IRQ high, if and only if, it had driven the SER_IRQ low during the previous Sample Phase. During the Turn-around Phase the LPC47N227 tri-states the SER_IRQ. The LPC47N227 will drive the SER_IRQ line low at the appropriate sample point if its associated IRQ/Data line is low, regardless of which device initiated the Start Frame.

The Sample Phase for each IRQ/Data follows the low to high transition of the Start Frame pulse by a number of clocks equal to the IRQ/Data Frame times three, minus one. (e.g. The IRQ5 Sample clock is the sixth IRQ/Data Frame, (6 x 3) - 1 = 17th clock after the rising edge of the Start Pulse).

SER_IRQ Sampling Periods

SER_IRQ PERIOD	SIGNAL SAMPLED	# OF CLOCKS PAST START
1	Not Used	2
2	IRQ1	5
3	nIO_SMI/IRQ2	8
4	IRQ3	11
5	IRQ4	14
6	IRQ5	17
7	IRQ6	20
8	IRQ7	23
9	IRQ8	26
10	IRQ9	29
11	IRQ10	32
12	IRQ11	35
13	IRQ12	38
14	IRQ13	41
15	IRQ14	44
16	IRQ15	47

The SER_IRQ data frame supports IRQ2 from a logical device on Period 3, which can be used for the System Management Interrupt (nSMI). When using Period 3 for IRQ2 the user should mask off the SMI via the SMI Enable Register. Likewise, when using Period 3 for nSMI the user should not configure any logical devices as using IRQ2.

SER_IRQ Period 14 is used to transfer IRQ13. Logical devices FDC, Parallel Port, Serial Port 1, Serial Port 2 have IRQ13 as a choice for their primary interrupt.

The SMI is enabled onto the SMI frame of the Serial IRQ via bit 6 of SMI Enable Register 2 and onto the nIO_SMI pin via bit 7 of the SMI Enable Register 2.

Stop Cycle Control

Once all IRQ/Data Frames have completed the Host Controller will terminate SER_IRQ activity by initiating a Stop Frame. Only the Host Controller can initiate the Stop Frame. A Stop Frame is indicated when the SER_IRQ is low for two or three clocks. If the Stop Frame's low time is two clocks then the next SER_IRQ Cycle's sampled mode is the Quiet mode; and any SER_IRQ device may initiate a Start Frame in the second clock or more after the rising edge of the Stop Frame's pulse. If the Stop Frame's low time is three clocks then the next SER_IRQ Cycle's sampled mode is the Continuos mode; and only the Host Controller may initiate a Start Frame in the second clock or more after the rising edge of the Stop Frame's pulse.

Latency

Latency for IRQ/Data updates over the SER_IRQ bus in bridge-less systems with the minimum Host supported IRQ/Data Frames of seventeen, will range up to 96 clocks (3.84μS with a 25MHz PCI Bus or 2.88uS with a 33MHz PCI Bus). If one or more PCI to PCI Bridge is added to a system, the latency for IRQ/Data updates from the secondary or tertiary buses will be a few clocks longer for synchronous buses, and approximately double for asynchronous buses.

EOI/ISR Read Latency
Any serialized IRQ scheme has a potential implementation issue related to IRQ latency. IRQ latency could cause an EOI or ISR Read to precede an IRQ transition that it should have followed. This could cause a system fault. The host interrupt controller is responsible for ensuring that these latency issues are mitigated. The recommended solution is to delay EOIs and ISR Reads to the interrupt controller by the same amount as the SER_IRQ Cycle latency in order to ensure that these events do not occur out of order.

AC/DC Specification Issue
All SER_IRQ agents must drive / sample SER_IRQ synchronously related to the rising edge of PCI bus clock. The SER_IRQ pin uses the electrical specification of PCI bus. Electrical parameters will follow PCI spec. section 4, sustained tri-state.

Reset and Initialization
The SER_IRQ bus uses nPCI_RESET as its reset signal. The SER_IRQ pin is tri-stated by all agents while nPCI_RESET is active. With reset, SER_IRQ Slaves are put into the (continuous) IDLE mode. The Host Controller is responsible for starting the initial SER_IRQ Cycle to collect system's IRQ/Data default values. The system then follows with the Continuous/Quiet mode protocol (Stop Frame pulse width) for subsequent SER_IRQ Cycles. It is Host Controller's responsibility to provide the default values to 8259's and other system logic before the first SER_IRQ Cycle is performed. For SER_IRQ system suspend, insertion, or removal application, the Host controller should be programmed into Continuous (IDLE) mode first. This is to guarantee SER_IRQ bus is in IDLE state before the system configuration changes.

Routable IRQ Inputs
The routable IRQ input (IRQINx) functions are on pins 51 (IRQIN1) and 52 (IRQIN2), muxed onto GP13 and GP14 respectively as inputs. The IRQINx pin's IRQ time slot in the Serial IRQ stream is selected via a 4-bit control register for each IRQIN function (CR29 for IRQIN1, CR2A for IRQIN2). A value of 0000 disables the IRQ function.

The part is able to generate a PME and an SMI from both of the IRQ inputs through the GPIO bits in the PME and SMI status and enable registers. The edge is programmable through the polarity bit of the GPIO control register.

User Note: In order to use an IRQ for one of the IRQINx inputs that are muxed on the GPIO pins, the corresponding IRQ must not be used for any of the devices in the LPC47N227. Otherwise contention may occur.

PCI CLKRUN SUPPORT

Overview
The LPC47N227 supports the PCI nCLKRUN signal. nCLKRUN is used to indicate the PCI clock status as well as to request that a stopped clock be started. The LPC47N227 nCLKRUN signal is on pin number 28. See FIGURE 3 for an example of a typical system implementation using nCLKRUN.

If the LPC47N227 SIRQ_CLKRUN_EN signal is disabled, it will disable the nCLKRUN support related to nLDRQ in addition to disabling the SER_IRQ and the nCLKRUN associated with SER_IRQ.

nCLKRUN is an open drain output and an input. Refer to the *PCI Mobile Design Guide Rev 1.0* for a description of the nCLKRUN function.

nCLKRUN for Serial IRQ
The LPC47N227 supports the PCI nCLKRUN signal for the Serial IRQs. If an SIO interrupt occurs while the PCI clock is stopped, nCLKRUN is asserted before the serial interrupt signal is driven active.

See “Using nCLKRUN” section below for more details.

nCLKRUN for nLDRQ

nCLKRUN support is also provided in the LPC47N227 for the nLDRQ signal. If a device requests DMA service while the PCI clock is stopped, nCLKRUN is asserted to restart the PCI clock. This is required to drive the nLDRQ signal active.

See “Using nCLKRUN” section for more details.

Using nCLKRUN
If nCLKRUN is sampled “high”, the PCI clock is stopped or stopping. If nCLKRUN is sampled “low”, the PCI clock is starting or started (running). If a device in the LPC47N227 asserts or de-asserts an interrupt or asserts a DMA request, and nCLKRUN is sampled “high”, the LPC47N227 requests the restoration of the clock by asserting the nCLKRUN signal asynchronously (Table 47). The LPC47N227 holds nCLKRUN low until it detects two rising edges of the clock. After the second clock edge, the LPC47N227 disables the open drain driver (FIGURE 4).

The LPC47N227 will not assert nCLKRUN under any conditions if SIRQ_CLKRUN_EN is inactive (“0”). The SIRQ_CLKRUN_EN bit is D7 in CR29.

The LPC47N227 will not assert nCLKRUN if it is already driven low by the central resource; i.e., the PCI CLOCK GENERATOR in FIGURE 3. The LPC47N227 will not assert nCLKRUN unless the line has been deasserted for two successive clocks; i.e., before the clock was stopped (FIGURE 4).

Table 47 – LPC47N227 nCLKRUN Function

SIRQ_CLKRUN_EN	INTERNAL INTERRUPTS/ DMA REQUESTS	nCLKRUN	ACTION
0	X	X	None
1	NO CHANGE	X	None
	CHANGE/ASSERTION[1]	0	None
		1	Assert nCLKRUN[2]

Note[1]: "Change/Assertion" means either-edge change on any internal IRQs routed to the SIRQ block or assertion of an internal DMA request by a device in LPC47N227. The "assertion" detection logic runs asynchronously to the PCI Clock and regardless of the Serial IRQ mode; i.e., "continuous" or "quiet".
Note[2]: The nCLKRUN signal is '1' for at least two consecutive clocks before LPC47N227 asserts ('0') it.

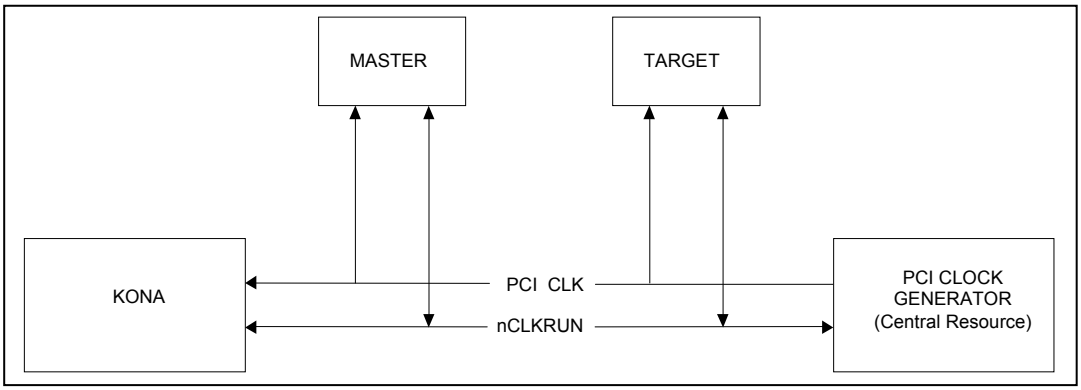


FIGURE 3 – nCLKRUN SYSTEM IMPLEMENTATION EXAMPLE

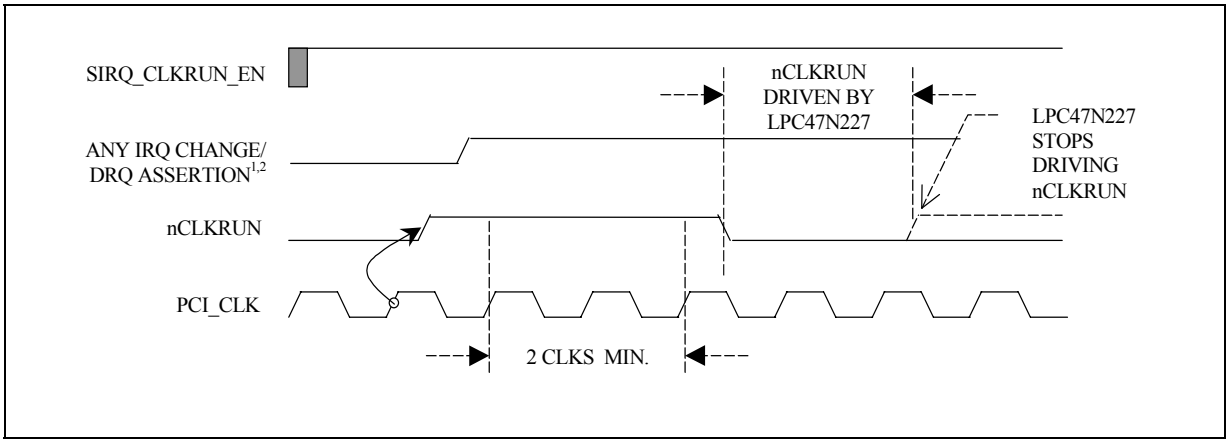


FIGURE 4 – CLOCK START ILLUSTRATION

Note 1: The signal “ANY IRQ CHANGE/DRQ ASSERTION” is the same as “CHANGE/ASSERTION” in Table 47.

Note 2: The LPC47N227 continually monitors the state of nCLKRUN to maintain the PCI Clock until an active “ANY IRQ CHANGE/DRQ ASSERTION” condition has been transferred to the host in a SER_IRQ/DMA cycle. For example, if “ANY IRQ CHANGE/DRQ ASSERTION” is asserted before nCLKRUN is de-asserted (not shown in FIGURE 4), the LPC47N227 must assert nCLKRUN as needed until the SER_IRQ/DMA cycle has completed.

GENERAL PURPOSE I/O

The LPC47N227 provides a set of flexible Input/Output control functions to the system designer through the 29 independently programmable General Purpose I/O pins (GPIO). The GPIO pins can perform basic I/O and many of them can be individually enabled to generate an SMI and a PME.

GPIO Pins
The following pins include GPIO functionality as defined in the table below.

Table 48 – GPIO Pin Functionality

Pin	Name	Power Well	Default on VTR POR	Default on VCC POR	PME/SMI Function
6	GP24	VCC Note 1	Input	Programmable	PME/SMI
32	GP30	VCC Note 1	Input	Programmable	PME
33	GP31	VCC Note 1	Input	Programmable	PME
34	GP32	VCC Note 1	Input	Programmable	PME
35	GP33	VCC Note 1	Input	Programmable	PME
36	GP34	VCC Note 1	Input	Programmable	PME
37	GP35	VCC Note 1	Input	Programmable	PME
38	GP36	VCC Note 1	Input	Programmable	PME
39	GP37	VCC Note 1	Input	Programmable	PME
40	GP40	VCC	Input	Programmable	-
41	GP41	VCC	Input	Programmable	-
42	GP42	VCC	Input	Programmable	-
43	GP43	VCC	Input	Programmable	-
44	GP44	VCC	Input	Programmable	-
45	GP45	VCC	Input	Programmable	-
46	GP46	VCC	Input	Programmable	-
47	GP47	VCC	Input	Programmable	-
48	GP10	VCC Note 1	Input	Programmable	PME/SMI
49	GP11/SYSOPT	VCC Note 1	Input	Programmable	PME/SMI
50	GP12/nIO_SMI	VCC Note 1	Input	Programmable	nIO_SMI/ PME/SMI
51	GP13/IRQIN1	VCC Note 1	Input	Programmable	PME/SMI
52	GP14/IRQIN2	VCC Note 1	Input	Programmable	PME/SMI
54	GP15	VCC Note 1	Input	Programmable	PME/SMI
55	GP16	VCC Note 1	Input	Programmable	PME/SMI
56	GP17	VCC Note 1	Input	Programmable	PME/SMI
57	GP20	VCC Note 1	Input	Programmable	PME
58	GP21	VCC Note 1	Input	Programmable	PME
59	GP22	VCC Note 1	Input	Programmable	PME
64	GP23/FDC_PP	VCC Note 1	Input	Programmable	PME/SMI

Note 1: These pins have input buffers into the wakeup logic that are powered by VTR.

Description

Each GPIO port has a 1-bit data register. GPIOs are controlled by GPIO control registers located in the Configuration section. The data register for each GPIO port is represented as a bit in one of the 8-bit GPIO DATA Registers, GP1 to GP4. The bits in these registers reflect the value of the associated GPIO pin as follows. Pin is an input: The bit is the value of the GPIO pin. Pin is an output: The value written to the bit goes to the GPIO pin. Latched on read and write. The GPIO data registers are located in the Runtime Register block; see the Runtime Registers section. The GPIO ports with their alternate functions and configuration state register addresses are listed in Table 49.

Table 49 – General Purpose I/O Port Assignments

PIN NO. /QFP	DEFAULT FUNCTION	ALTERNATE FUNCTION	DATA REGISTER[1]	DATA REGISTER BIT NO.	REGISTER OFFSET (HEX)
48	GPIO		GP1	0	0C
49	GPIO			1	
50	GPIO	nIO_SMI		2	
51	GPIO	IRQIN1		3	
52	GPIO	IRQIN2		4	
54	GPIO			5	
55	GPIO			6	
56	GPIO			7	
57	GPIO		GP2	0	0D
58	GPIO			1	
59	GPIO			2	
64	GPIO	FDC_PP		3	
6	GPIO			4	
N/A	Reserved			5	
N/A	Reserved			6	
N/A	Reserved			7	
32	GPIO		GP3	0	0E
33	GPIO			1	
34	GPIO			2	
35	GPIO			3	
36	GPIO			4	
37	GPIO			5	
38	GPIO			6	
39	GPIO			7	
40	GPIO		GP4	0	0F
41	GPIO			1	
42	GPIO			2	
43	GPIO			3	
44	GPIO			4	
45	GPIO			5	
46	GPIO			6	
47	GPIO			7	

Note 1: The GPIO Data Registers are located at the offset shown from the RUNTIME REGISTERS BLOCK address.

GPIO Control
Each GPIO port has an 8-bit control register that controls the behavior of the pin. These registers are defined in the Configuration section of this specification.

Each GPIO port may be configured as either an input or an output. If the pin is configured as an output, it can be programmed as open-drain or push-pull. Inputs and outputs can be configured as non-inverting or inverting. GPIO Direction Registers determine the port direction, GPIO Polarity Registers determine the signal polarity, and GPIO Output Type Register determines the output driver type select. The GPIO Output Type Register applies to certain GPIOs (GP12-GP17 and GP20). The GPIO Direction, Polarity and Output Type Registers control the GPIO pin when the pin is configured for the GPIO function and when the pin is configured for the alternate function for all pins.

The basic GPIO configuration options are summarized in Table 50.

Table 50 - GPIO Configuration Summary

SELECTED FUNCTION	DIRECTION BIT	POLARITY BIT	DESCRIPTION
	B0	B1	
GPIO	0	0	Pin is a non-inverted output.
	0	1	Pin is an inverted output.
	1	0	Pin is a non-inverted input.
	1	1	Pin is an inverted input.

GPIO Operation
The operation of the GPIO ports is illustrated in FIGURE 5.

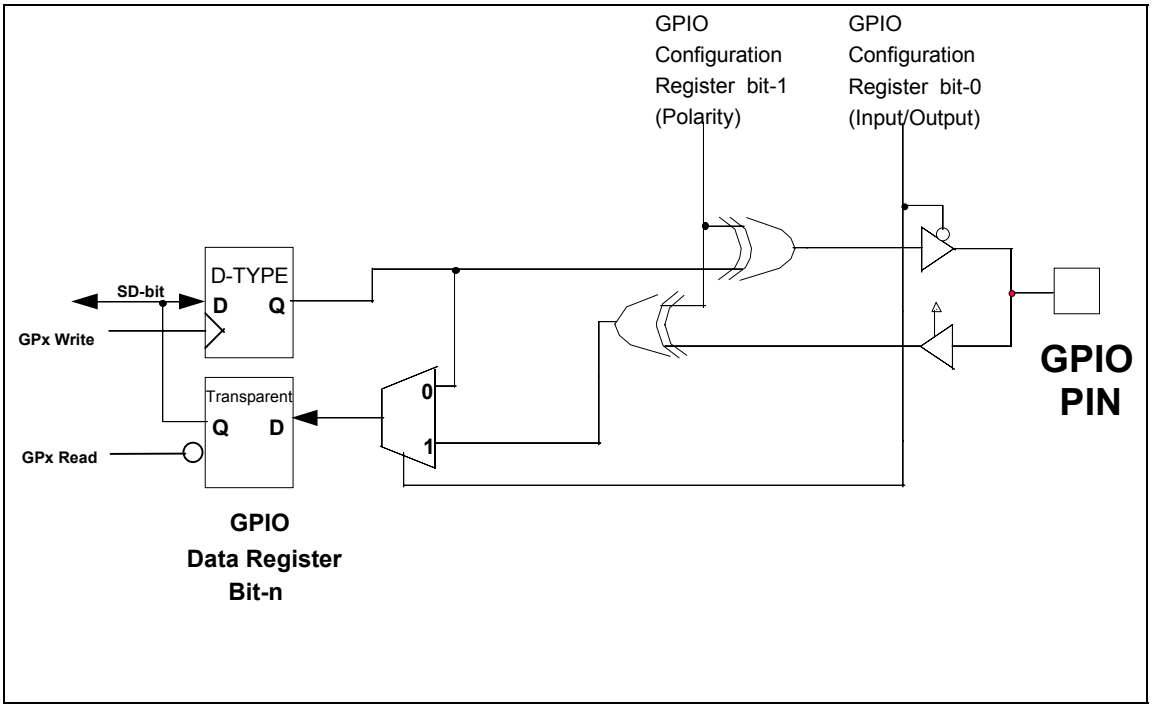


FIGURE 5 - GPIO FUNCTION ILLUSTRATION

Note: FIGURE 5 is for illustration purposes only and in not intended to suggest specific implementation details.

When a GPIO port is programmed as an input, reading it through the GPIO data register latches either the inverted or non-inverted logic value present at the GPIO pin. Writing to a GPIO port that is programmed as an input has no effect (Table 51).

When a GPIO port is programmed as an output, the logic value or the inverted logic value that has been written into the GPIO data register is output to the GPIO pin. Reading from a GPIO port that is programmed as an output returns the last value written to the data register (Table 51).

Table 51 – GPIO Read/Write Behavior

HOST OPERATION	GPIO INPUT PORT	GPIO OUTPUT PORT
READ	LATCHED VALUE OF GPIO PIN	LAST WRITE TO GPIO DATA REGISTER
WRITE	NO EFFECT	BIT PLACED IN GPIO DATA REGISTER

The LPC47N227 provides 21 GPIOs that can directly generate a PME. See the table in the next section. The GPIO Polarity Registers in the Configuration section select the edge on these GPIO pins that will set the associated status bit in the PME_STS1 – PME_STS3 registers. The default is the low-to-high edge. If the corresponding enable bit in the PME_EN1 – PME_EN3 registers and the PME_EN bit in the PME_EN register is set, a PME will be generated. These registers are located in the Runtime Registers Block, which is located at the address contained in the configuration registers CR30. The

PME status bits for the GPIOs are cleared on a write of '1'. In addition, the LPC47N227 provides 10 GPIOs that can directly generate an SMI. See the table in the next section.

GPIO PME and SMI Functionality
The following GPIOs are dedicated wakeup GPIOs with a status and enable bit in the PME status and enable registers:

GP10-GP17
GP20-GP24
GP30-GP37

This following is the list of PME status and enable registers for their corresponding GPIOs:
PME_STS1 and PME_EN1 for GP10-GP17
PME_STS2 and PME_EN2 for GP20-GP24
PME_STS3 and PME_EN3 for GP30-GP37

The following GPIOs can directly generate an SMI and have a status and enable bit in the SMI status and enable registers.

GP10-GP17
GP23, GP24

The following SMI status and enable registers for these GPIOs:
SMI_STS1 and SMI_EN1 for GP10-17
SMI_STS2 and SMI_EN2 for GP23-GP24

The following table summarizes the PME and SMI functionality for each GPIO.

GPIO	PME	SMI	OUTPUT BUFFER POWER	NOTES
GP10-GP11	Yes	Yes	VCC	
GP12	Yes	Yes/nIO_SMI	VCC	1
GP13-GP17	Yes	Yes	VCC	
GP20-GP22	Yes	No	VCC	
GP23-GP24	Yes	Yes	VCC	
GP30-GP37	Yes	No	VCC	
GP40-GP47	No	No	VCC	2

Note 1: Since GP12 can be used to generate an SMI and as the nIO_SMI output, do not enable GP12 to generate an SMI (by setting bit 2 of the SMI Enable Register 1) if the nIO_SMI function is selected on the GP12 pin. Use GP12 to generate an SMI event only if the SMI output is enabled on the Serial IRQ stream.

Note 2: GP40-GP47 should not be connected to any VTR powered external circuitry. These pins are not used for wakeup.

SYSTEM MANAGEMENT INTERRUPT (SMI)

The LPC47N227 implements a “group” nIO_SMI output pin. The System Management Interrupt is a non-maskable interrupt with the highest priority level used for OS transparent power management. The nSMI group interrupt output consists of the enabled interrupts from Super I/O Device Interrupts (Parallel Port, Serial Port 1 and 2 and FDC) and many of the GPIOs pins. The GP12/nIO_SMI pin, when selected for the nIO_SMI function, can be programmed to be active high or active low via bit 2 in the GPIO Polarity Register 1 (CR32). The nIO_SMI pin function defaults to active low. The output buffer type of the pin can be programmed to be open-drain or push-pull via GPIO Output Type Register (CR39).

The interrupts are enabled onto the group nSMI output via the SMI Enable Registers 1 and 2. The nSMI output is then enabled onto the nIO_SMI output pin via bit[7] in the SMI Enable Register 2. The SMI output can also be enabled onto the serial IRQ stream (IRQ2) via Bit[6] in the SMI Enable Register 2.

SMI Registers
The SMI event bits for the GPIOs events are located in the SMI status and Enable registers 1 and 2. The polarity of the edge used to set the status bit and generate an SMI is controlled by the GPIO Polarity Registers located in the Configuration section. For non-inverted polarity (default) the status bit is set on the low-to-high edge. Status bits for the GPIOs are cleared on a write of ‘1’.

The SMI logic for the GPIO events is implemented such that the output of the status bit for each event is combined with the corresponding enable bit in order to generate an SMI.

The SMI event bits for the super I/O devices are located in the SMI status and enable register 1 and 2. All of these status bits are cleared at the source; these status bits are not cleared by a write of ‘1’. The SMI logic for these events is implemented such that each event is directly combined with the corresponding enable bit in order to generate an SMI.

See the “Runtime Registers” section for the definition of the SMI status and enable registers.

PME SUPPORT

The LPC47N227 offers support for Power Management Events (PMEs), also referred to as System Control Interrupt (SCI) events in an ACPI system. A power management event is indicated to the chipset via the assertion of the nIO_PME signal. In the LPC47N227, the nIO_PME is asserted by active transitions on the ring indicator inputs nRI1 and nRI2, and programmable edges on GPIO pins. The nIO_PME pin can be programmed to be active high or active low via bit 5 in the GPIO Polarity Register 2 (CR34). The nIO_PME pin function defaults to active low, open-drain output. The output buffer type of the pin can be programmed to be open-drain or push-pull via bit 7 in the GPIO Output Type Register (CR39). This pin is powered by VTR. See the Configuration section for description on these registers.

PME functionality is controlled by the PME status and enable registers in the runtime registers block, which is located at the address programmed in register 0x30 in the Configuration section. The PME Enable bit, PME_EN, globally controls PME Wake-up events. When PME_EN is inactive, the nIO_PME signal can not be asserted. When PME_EN is asserted, any wake source whose individual PME Wake Enable register bit is asserted can cause nIO_PME to become asserted.

The PME Status register indicates that an enabled wake source has occurred and if the PME_EN bit is set, asserted the nIO_PME signal. The PME Status bit is asserted by active transitions of PME wake sources. PME_STS will become asserted independent of the state of the global PME enable, PME_EN.

The following pertains to the PME status bits for each event:

- The output of the status bit for each event is combined with the corresponding enable bit to set the PME status bit.
- The status bit for any pending events must be cleared in order to clear the PME_STS bit. Status bits are cleared on a write of '1'.

For the GPIO events, the polarity of the edge used to set the status bit and generate a PME is controlled by the GPIO Polarity Registers in the Configuration section. For non-inverted polarity (default) the status bit is set on the low-to-high edge. Status bits are cleared on a write of '1'.

In the LPC47N227 the nIO_PME pin can be programmed to be an open drain, active low, driver. The LPC47N227 nIO_PME pin is fully isolated from other external devices that might pull the nIO_PME signal low; i.e., the nIO_PME signal is capable of being driven high externally by another active device or pullup even when the LPC47N227 VCC is grounded, providing VTR power is active.

PME Registers

The PME registers are run-time registers as follows. These registers are located in system I/O space at an offset from Runtime Registers Block, the address programmed at register 0x30 in the Configuration section.

The following registers are for GPIO PME events:

- PME Wake Status 1 (PME_STS1), PME Wake Enable 1 (PME_EN1)
- PME Wake Status 2 (PME_STS2), PME Wake Enable 2 (PME_EN2)
- PME Wake Status 3 (PME_STS3), PME Wake Enable 3 (PME_EN3)

See PME register description in the Runtime Registers Section.

RUNTIME REGISTERS

Runtime Registers Block Summary

The runtime registers are located at the address programmed in the Runtime Register Block Base Address configuration register located in CR30. The part performs 16-bit address qualification on the Runtime Register Base Address (bits[11:0] are decoded and bits[15:12] must be zero). The runtime register block may be located within the range 0x0100-0x0FFF on 16-byte boundaries. Decodes are disabled if the Runtime Register Base Address is located below 0x100. These registers are powered by VTR.

Table 52 - Runtime Register Block Summary

REGISTER OFFSET (hex)	TYPE	HARD RESET	VCC POR	VTR POR	REGISTER
00	R/W	-	-	0x00	PME_STS
01	R/W	-	-	0x00	PME_EN
02	R/W	-	-	0x00	PME_STS1
03	R/W	-	-	0x00	PME_STS2
04	R/W	-	-	0x00	PME_STS3
05	R/W	-	-	0x00	PME_EN1
06	R/W	-	-	0x00	PME_EN2
07	R/W	-	-	0x00	PME_EN3
08	R/W	-	-	0x00	SMI_STS1
09	R/W	Note 1	Note 1	0x01 Note 1	SMI_STS2
0A	R/W	-	-	0x00	SMI_EN1
0B	R/W	-	-	0x00	SMI_EN2
0C	R/W	-	-	0x00	GP1
0D	R/W	-	-	0x00	GP2
0E	R/W	-	-	0x00	GP3
0F	R/W	-	-	0x00	GP4

Note: Hard Reset: nPCI_RESET pin asserted.
Note: Reserved bits return 0 on read.
Note 1: The parallel port interrupt defaults to 1 when the parallel port power bit is cleared. When the parallel port is activated, PINT follows the nACK input.

Table 53 – Runtime Registers Block Description

NAME/DEFAULT	REGISTER OFFSET	DESCRIPTION
PME_STS Default = 0x00 on VTR POR	00 (R/W)	Bit[0] PME_Status = 0 (default) = 1 Set when LPC47N227 would normally assert the nIO_PME signal, independent of the state of the PME_En bit. Set when a bit in a PME Wake Status register and its associated enable bit set. Bit[7:1] Reserved PME_Status is not affected by Vcc POR, SOFT RESET or HARD RESET. Writing a "1" to PME_Status will clear it and cause the LPC47N227 to stop asserting nIO_PME, if enabled. Writing a "0" to PME_Status has no effect.
PME_EN Default = 0x00 on VTR POR	01 (R/W)	Bit[0] PME_En = 0 nIO_PME signal assertion is disabled (default) = 1 Enables LPC47N227 to assert nIO_PMEsignal Bit[7:1] Reserved PME_En is not affected by Vcc POR, SOFT RESET or HARD RESET
PME_STS1 Default = 0x00 on VTR POR	02 (R/W)	PME Wake Status Register 1 This register indicates the state of the individual PME wake sources, independent of the individual source enables or the PME_En bit. If the wake source has asserted a wake event, the associated PME Wake Status bit will be a "1". Bit[0] GP10 Bit[1] GP11 Bit[2] GP12 Bit[3] GP13 Bit[4] GP14 Bit[5] GP15 Bit[6] GP16 Bit[7] GP17 The PME Wake Status register is not affected by Vcc POR, SOFT RESET or HARD RESET. Writing a "1" to Bit[7:0] will clear it. Writing a "0" to any bit in PME Wake Status Register has no effect.

NAME/DEFAULT	REGISTER OFFSET	DESCRIPTION
PME_STS2 Default = 0x00 on VTR POR	03 (R/W)	PME Wake Status Register 2 This register indicates the state of the individual PME wake sources, independent of the individual source enables or the PME_En bit. If the wake source has asserted a wake event, the associated PME Wake Status bit will be a “1”. Bit[0] RI1 Bit[1] RI2 Bit[2] GP20 Bit[3] GP21 Bit[4] GP22 Bit[5] GP23 Bit[6] GP24 Bit[7] Reserved The PME Wake Status register is not affected by Vcc POR, SOFT RESET or HARD RESET. Writing a “1” to Bit[7:0] will clear it. Writing a “0” to any bit in PME Wake Status Register has no effect.
PME_STS3 Default = 0x00 on VTR POR	04 (R/W)	PME Wake Status Register 3 This register indicates the state of the individual PME wake sources, independent of the individual source enables or the PME_En bit. If the wake source has asserted a wake event, the associated PME Wake Status bit will be a “1”. Bit[0] GP30 Bit[1] GP31 Bit[2] GP32 Bit[3] GP33 Bit[4] GP34 Bit[5] GP35 Bit[6] GP36 Bit[7] GP37 The PME Wake Status register is not affected by Vcc POR, SOFT RESET or HARD RESET. Writing a “1” to Bit[7:0] will clear it. Writing a “0” to any bit in PME Wake Status Register has no effect.

NAME/DEFAULT	REGISTER OFFSET	DESCRIPTION
PME_EN1 Default = 0x00 on VTR POR	05 (R/W)	PME Wake Enable Register 1 This register is used to enable individual LPC47N227 PME wake sources onto the nIO_PME wake bus. When the PME Wake Enable register bit for a wake source is active (“1”), if the source asserts a wake event so that the associated status bit is “1” and the PME_En bit is “1”, the source will assert the nIO_PME signal. When the PME Wake Enable register bit for a wake source is inactive (“0”), the PME Wake Status register will indicate the state of the wake source but will not assert the nIO_PME signal. Bit[0] GP10 Bit[1] GP11 Bit[2] GP12 Bit[3] GP13 Bit[4] GP14 Bit[5] GP15 Bit[6] GP16 Bit[7] GP17 The PME Wake Enable register is not affected by Vcc POR, SOFT RESET or HARD RESET.
PME_EN2 Default = 0x00 on VTR POR	06 (R/W)	PME Wake Enable Register 2 This register is used to enable individual LPC47N227 PME wake sources onto the nIO_PME wake bus. When the PME Wake Enable register bit for a wake source is active (“1”), if the source asserts a wake event so that the associated status bit is “1” and the PME_En bit is “1”, the source will assert the nIO_PME signal. When the PME Wake Enable register bit for a wake source is inactive (“0”), the PME Wake Status register will indicate the state of the wake source but will not assert the nIO_PME signal. Bit[0] RI1 Bit[1] RI2 Bit[2] GP20 Bit[3] GP21 Bit[4] GP22 Bit[5] GP23 Bit[6] GP24 Bit[7] Reserved The PME Wake Enable register is not affected by Vcc POR, SOFT RESET or HARD RESET.

NAME/DEFAULT	REGISTER OFFSET	DESCRIPTION
PME_EN3 Default = 0x00 on VTR POR	07 (R/W)	PME Wake Enable Register 3 This register is used to enable individual LPC47N227 PME wake sources onto the nIO_PME wake bus. When the PME Wake Enable register bit for a wake source is active (“1”), if the source asserts a wake event so that the associated status bit is “1” and the PME_En bit is “1”, the source will assert the nIO_PME signal. When the PME Wake Enable register bit for a wake source is inactive (“0”), the PME Wake Status register will indicate the state of the wake source but will not assert the nIO_PME signal. Bit[0] GP30 Bit[1] GP31 Bit[2] GP32 Bit[3] GP33 Bit[4] GP34 Bit[5] GP35 Bit[6] GP36 Bit[7] GP37 The PME Wake Enable register is not affected by Vcc POR, SOFT RESET or HARD RESET.
SMI_STS1 Default = 0x00 on VTR POR	08 (R/W)	SMI Status Register 1 This register is used to read the status of the SMI inputs. The following bits are cleared on a write of ‘1’. Bit[0] GP10 Bit[1] GP11 Bit[2] GP12 Bit[3] GP13 Bit[4] GP14 Bit[5] GP15 Bit[6] GP16 Bit[7] GP17
SMI_STS2 Default = 0x01 on VTR POR Bit 0 is set to ‘1’ on VCC POR, VTR POR and HARD RESET	09 (R/W)	SMI Status Register 2 This register is used to read the status of the SMI inputs. The bits[3:0] must be cleared at their source. Bits[5:4] are cleared on a write of ‘1’. Bit[0] PINT. The parallel port interrupt defaults to ‘1’ when the parallel port activate bit is cleared. When the parallel port is activated, PINT follows the nACK input. Bit[1] U2INT Bit[2] U1INT Bit[3] FINT Bit[4] GP23 Bit[5] GP24 Bit[7:6] Reserved

NAME/DEFAULT	REGISTER OFFSET	DESCRIPTION
SMI_EN1 Default = 0x00 on VTR POR	0A (R/W)	SMI Enable Register 1 This register is used to enable the different interrupt sources onto the internal group nSMI signal. 1=Enable 0=Disable Bit[0] GP10 Bit[1] GP11 Bit[2] GP12 Bit[3] GP13 Bit[4] GP14 Bit[5] GP15 Bit[6] GP16 Bit[7] GP17
SMI_EN2 Default = 0x00 on VTR POR	0B (R/W)	SMI Enable Register 2 This register is used to enable the different interrupt sources onto the internal group nSMI signal, and the internal group nSMI signal onto the nIO_SMI GPI/O pin or the serial IRQ stream on IRQ2. 1=Enable 0=Disable Bit[0] EN_PINT Bit[1] EN_U2INT Bit[2] EN_U1INT Bit[3] EN_FINT Bit[4] GP23 Bit[5] GP24 Bit[6] EN_SMI_S (Enable group nSMI signal onto serial IRQ2) Bit[7] EN_SMI (Enable group nSMI signal onto nIO_SMI pin)
GP1 Default = 0x00 on VTR POR	0C R/W	General Purpose I/O Data Register 1 Bit[0]GP10 Bit[1]GP11 Bit[2]GP12 Bit[3]GP13 Bit[4]GP14 Bit[5]GP15 Bit[6]GP16 Bit[7]GP17
GP2 Default = 0x00 on VTR POR	0D R/W	General Purpose I/O Data Register 2 Bit[0]GP20 Bit[1]GP21 Bit[2]GP22 Bit[3]GP23 Bit[4]GP24 Bit[7:5]Reserved

NAME/DEFAULT	REGISTER OFFSET	DESCRIPTION
GP3 Default = 0x00 on VTR POR	0E R/W	General Purpose I/O Data Register 3 Bit[0]GP30 Bit[1]GP31 Bit[2]GP32 Bit[3]GP33 Bit[4]GP34 Bit[5]GP35 Bit[6]GP36 Bit[7]GP37
GP4 Default = 0x00 on VTR POR	0F R/W	General Purpose I/O Data Register 4 Bit[0]GP40 Bit[1]GP41 Bit[2]GP42 Bit[3]GP43 Bit[4]GP44 Bit[5]GP45 Bit[6]GP46 Bit[7]GP47

Note: Reserved bits return 0 on read.

CONFIGURATION

The configuration of the LPC47N227 is programmed through hardware selectable Configuration Access Ports that appear when the chip is placed into the configuration state. The LPC47N227 logical device blocks, if enabled, will operate normally in the configuration state.

Configuration Access Ports

The Configuration Access Ports are the CONFIG PORT, the INDEX PORT, and the DATA PORT (Table 54). The base address of these registers is controlled by the GP11/SYSOPT pin and by the Configuration Port Base Address registers CR12 and CR13. To determine the configuration base address at power-up, the state of the GP11/SYSOPT pin is latched by the falling edge of a hardware reset. If the latched state is a 0, the base address of the Configuration Access Ports is located at address 0x02E; if the latched state is a 1, the base address is located at address 0x04E. The base address is relocatable via CR12 and CR13.

Table 54 – Configuration Access Ports

PORT NAME	SYSOPT = 0	SYSOPT = 1	TYPE
CONFIG PORT	0x02E	0x04E	WRITE
INDEX PORT	0x02E	0x04E	READ/WRITE[1,2]
DATA PORT	INDEX PORT + 1		READ/WRITE[1]

Note[1]: The INDEX and DATA ports are active only when the LPC47N227 is in the configuration state.
Note[2]: The INDEX PORT is only readable in the configuration state.

Configuration State

The configuration registers are used to select programmable chip options. The LPC47N227 operates in two possible states: the run state and the configuration state. After power up by default the chip is in the run state. To program the configuration registers, the configuration state must be explicitly enabled. Programming the configuration registers typically follows this sequence:

1. Enter the Configuration State,
2. Program the Configuration Register(s),
3. Exit the Configuration State.

Entering the Configuration State

To enter the configuration state write the Configuration Access Key to the CONFIG PORT. The Configuration Access Key is one byte of 55H data. The LPC47N227 will automatically activate the Configuration Access Ports following this procedure.

Configuration Register Programming

The LPC47N227 contains configuration registers CR00-CR39. After the LPC47N227 enters the configuration state, configuration registers can be programmed by first writing the register index number (00 - 39H) to the Configuration Select Register (CSR) through the INDEX PORT and then writing or reading the configuration register contents through the DATA PORT. Configuration register access remains enabled until the configuration state is explicitly exited.

Exiting the Configuration State

To exit the configuration state, write one byte of AAH data to the CONFIG PORT. The LPC47N227 will automatically deactivate the Configuration Access Ports following this procedure, at which point configuration register access cannot occur until the configuration state is explicitly re-enabled.

Programming Example

The following is a configuration register programming example written in Intel 8086 assembly language.

```
;-----------------------------.
; ENTER CONFIGURATION STATE   |
;-----------------------------'
MOV    DX,02EH       ;SYSOPT = 0
MOV    AX,055H
OUT    DX,AL
;-----------------------------.
; CONFIGURE REGISTER CR0-CRx  |
;-----------------------------'
MOV    DX,02EH
MOV    AL,00H
OUT    DX,AL         ;Point to CR0
MOV    DX,02FH
MOV    AL,3FH
OUT    DX,AL         ;Update CR0
;
MOV    DX,02EH
MOV    AL,01H
OUT    DX,AL         ;Point to CR1
MOV    DX,02FH
MOV    AL,9FH
OUT    DX,AL         ;Update CR1
;
; Repeat for all CRx registers
;
;-----------------------------.
; EXIT CONFIGURATION STATE    |
;-----------------------------'
MOV    DX,02EH
MOV    AX,AAH
OUT    DX,AL
```

Configuration Select Register (CSR)

The Configuration Select Register can only be accessed when the LPC47N227 is in the configuration state. The CSR is located at the INDEX PORT address and must be initialized with configuration register index before the register can be accessed using the DATA PORT.

Configuration Registers Summary

The configuration registers are set to their default values at power up (Table 55) and are RESET as indicated in Table 55 and the register descriptions that follow.

Table 55 – Configuration Registers Summary

REGISTER INDEX	TYPE	HARD RESET[1]	VCC POR	VTR POR	REGISTER
CR00	R/W	-	0x28	-	FDC Power/Valid Config Cycle
CR01	R/W	bit[7]=1	0x9C	-	PP Power/Mode/CR Lock
CR02	R/W	bit[7]=0	0x08	-	UART 1,2 Power
CR03	R/W	-	0x70	-	FDC Miscellaneous
CR04	R/W	-	0x00	-	PP and UART Miscellaneous
CR05	R/W	-	0x00	-	FDC Setup
CR06	R/W	-	0xFF	-	Drive Type ID
CR07	R/W	bit[7:4]=0	0x00	-	Auto Power Mgt/Boot Drive Select
CR08	R/W	-	0x00	-	Reserved
CR09	R/W	-	0x00	-	Test 4
CR0A	R/W	bit[7:6]=0	0x00	-	ECP FIFO Threshold/IR MUX
CR0B	R/W	-	0x00	-	Drive Rate
CR0C	R/W	0x02	0x02	-	UART Mode
CR0D	R	-	0x5A	-	Device ID
CR0E	R	-	Revision	-	Revision ID
CR0F	R/W	-	0x00	-	Test 1
CR10	R/W	-	0x00	-	Test 2
CR11	R/W	-	0x80	-	Test 3
CR12	R/W	SYSOPT=0:0x2E SYSOPT=1:0x4E		-	Configuration Base Address 0
CR13	R/W	SYSOPT=0:0x00 SYSOPT=1:0x00		-	Configuration Base Address 1
CR14	R	-	-	-	DSR Shadow
CR15	R	-	-	-	UART1 FCR Shadow
CR16	R	-	-	-	UART2 FCR Shadow
CR17	R/W	-	0x03	-	Force FDD Status Change
CR18	R	-	0x00	-	Reserved
CR19	R	-	0x00	-	Reserved
CR1A	R	-	0x00	-	Reserved
CR1B	R	-	0x00	-	Reserved
CR1C	R	-	0x00	-	Reserved
CR1D	R	-	0x00	-	Reserved
CR1E	R	-	0x00	-	Reserved
CR1F	R/W	-	0x00	-	Drive Type
CR20	R/W	-	0x3C	-	FDC Base Address
CR21	R/W	-	0x00	-	FDC on PP/EPP Timeout Select
CR22	R/W	-	0x00	-	ECP Software Select
CR23	R/W	-	0x00	-	Parallel Port Base Address
CR24	R/W	-	0x00	-	UART1 Base Address
CR25	R/W	-	0x00	-	UART2 Base Address

REGISTER INDEX	TYPE	HARD RESET[1]	VCC POR	VTR POR	REGISTER
CR26	R/W	-	0x00	-	FDC and PP DMA Select
CR27	R/W	-	0x00	-	FDC and PP IRQ Select
CR28	R/W	-	0x00	-	UART IRQ Select
CR29	R/W	-	0x80	-	IRQIN1/HPMODE/SIRQ_CLKRUN_ En
CR2A	R/W	-	0x00	-	IRQIN2
CR2B	R/W	-	0x00	-	SCE (FIR) Base Address
CR2C	R/W	-	0x00	-	SCE (FIR) DMA Select
CR2D	R/W	-	0x03	-	IR Half Duplex Timeout
CR2E	R/W	-	0x00	-	Software Select A
CR2F	R/W	-	0x00	-	Software Select B
CR30	R/W	-	0x00	-	Runtime Register Block Address
CR31	R/W	-	-	0x00	GPIO Direction Register 1
CR32	R/W	-	-	0x00	GPIO Polarity Register 1
CR33	R/W	-	-	0x00	GPIO Direction Register 2
CR34	R/W	-	-	0x00	GPIO Polarity Register 2
CR35	R/W	-	-	0x00	GPIO Direction Register 3
CR36	R/W	-	-	0x00	GPIO Polarity Register 3
CR37	R/W	-	-	0x00	GPIO Direction Register 4
CR38	R/W	-	-	0x00	GPIO Polarity Register 4
CR39	R/W	-	-	0x80	GPIO Output Type Register

Note: The bits that control the direction, polarity and output buffer type of each GPIO also affect the alternate function on the GPIO.

Note 1: Hard Reset: nPCI_RESET pin asserted.

Configuration Registers Description

CR00
CR00 can only be accessed in the configuration state and after the CSR has been initialized to 00H.

Table 56 – CR00

FDC Power/Valid Configuration Cycle		
Type: R/W		Default: 0x28 on VCC POR
BIT NO.	**BIT NAME**	**DESCRIPTION**
0-2	Reserved	Read Only. A read returns 0
3	FDC Power [1]	A high level on this bit, supplies power to the FDC (default). A low level on this bit puts the FDC in low power mode.
4,5,6	Reserved	Read only. A read returns bit 5 as a 1 and bits 4 and 6 as a 0.
7	Valid	A high level on this software controlled bit can be used to indicate that a valid configuration cycle has occurred. The control software must take care to set this bit at the appropriate times. Set to zero after power up. This bit has no effect on any other hardware in the chip.

NOTE[1]: Power Down bits disable the respective logical device and associated pins, however the power down bit does not disable the selected address range for the logical device. To disable the host address registers the logical device's base address must be set below 100h. Devices that are powered down but still reside at a valid I/O base address will participate in Plug-and-Play range checking.

CR01
CR01 can only be accessed in the configuration state and after the CSR has been initialized to 01H.

Table 57 – CR01

PP Power/Mode/CR Lock		
Type: R/W		**Default: 0x9C on VCC POR; Bit[7] = 1 on HARD RESET**
BIT NO.	**BIT NAME**	**DESCRIPTION**
0,1	Reserved	Read Only. A read returns "0".
2	Parallel Port Power[1]	A high level on this bit, supplies power to the Parallel Port (Default). A low level on this bit puts the Parallel Port in low power mode.
3	Parallel Port Mode	Parallel Port Mode. A high level on this bit, sets the Parallel Port for Printer Mode (Default). A low level on this bit enables the Extended Parallel port modes. Refer to Bits 0 and 1 of CR4
4	Reserved	Read Only. A read returns "1".
5,6	Reserved	Read Only. A read returns "0".
7	Lock CRx	A high level on this bit enables the reading and writing of CR00 – CR39 (Default). A low level on this bit disables the reading and writing of CR00 – CR39. Note: once the Lock CRx bit is set to "0", this bit can only be set to "1" by a hard reset or power-up reset.

NOTE[1] Power Down bits disable the respective logical device and associated pins, however the power down bit does not disable the selected address range for the logical device. To disable the host address registers the logical device's base address must be set below 100h. Devices that are powered down but still reside at a valid I/O base address will participate in Plug-and-Play range checking.

CR02

CR02 can only be accessed in the configuration state and after the CSR has been initialized to 02H.

Table 58 – CR02

UART 1 and 2 Power		
Type: R/W		**Default: 0x08 on VCC POR; Bit[7] = 0 on HARD RESET**
BIT NO.	**BIT NAME**	**DESCRIPTION**
0-2	Reserved	Read Only. A read returns "0".
3	UART1 Power Down[1]	A high level on this bit, allows normal operation of the Primary Serial Port (Default). A low level on this bit places the Primary Serial Port into Power Down Mode.
4-6	Reserved	Read Only. A read returns "0".
7	UART2 Power Down[1]	A high level on this bit, allows normal operation of the Secondary Serial Port, including the SCE/FIR block (Default). A low level on this bit places the Secondary Serial Port including the SCE/FIR block into Power Down Mode.

NOTE[1]: Power Down bits disable the respective logical device and associated pins, however the power down bit does not disable the selected address range for the logical device. To disable the host address registers the logical device's base address must be set below 100h. Devices that are powered down but still reside at a valid I/O base address will participate in Plug-and-Play range checking.

CR03
CR03 can only be accessed in the configuration state and after the CSR has been initialized to 03H.

Table 59 - CR03

FDC Miscellaneous				
Type: R/W			Default: 0x70 on VCC POR	
BIT NO.	**BIT NAME**	**DESCRIPTION**		
0	Reserved	Read Only. A read returns 0.		
1	Enhanced Floppy Mode 2	Bit 1	Floppy Mode – Refer to the description of the TAPE DRIVE REGISTER (TDR) for more information on these modes.	
		0	NORMAL Floppy Mode (Default)	
		1	Enhanced Floppy Mode 2 (OS2)	
2,3	Reserved	Read Only. A read returns 0.		
4	DRVDEN1	Bit 4	Pin DRVDEN1 Output[1]	
		0	Output Programmed DRVDEN1 Value	
		1	Force DRVDEN1 Output High (default)	
5	MFM	IDENT is used in conjunction with MFM to define the FDC interface mode.		
6	IDENT	**IDENT**	**MFM**	**MODE**
		1	1	AT Mode (Default)
		1	0	Reserved
		0	1	PS/2
		0	0	Model 30
7	Reserved	Read Only. A read returns 0.		

NOTE[1]: See NOTE[2] in section CR05.

CR04

CR04 can only be accessed in the configuration state and after the CSR has been initialized to 04H.

Table 60 – CR04

PP and UART Miscellaneous				
Type: R/W				Default: 0x00 on VCC POR
BIT NO.	**BIT NAME**	**DESCRIPTION**		
1,0	Parallel Port Extended Modes	Bit 1	Bit 0	If CR1 bit 3 is a low level then:
		0	0	Standard and Bi-directional Modes (SPP) (default)
		0	1	EPP Mode and SPP
		1	0	ECP Mode[2]
		1	1	ECP Mode & EPP Mode[1,2]
2,3	Parallel Port FDC	Refer to Parallel Port Floppy Disk Controller description.		
		Bit 3	Bit 2	
		0	0	Normal
		0	1	PPFD1
		1	0	PPFD2
		1	1	Reserved
4	MIDI 1[3]	Serial Clock Select Port 1: A low level on this bit disables MIDI support (default). A high level on this bit enables MIDI support.		
5	MIDI 2[3]	Serial Clock Select Port 2: A low level on this bit disables MIDI support (default). A high level on this bit enables MIDI support.		
6	EPP Type	0 = EPP 1.9 (default) 1 = EPP 1.7		
7	Reserved	Reserved - Read as 0.		

Note[1]: In this mode, EPP can be selected through the ecr register of ECP as mode 100.

Note[2]: In these modes, 2 drives can be supported directly, 3 or 4 drives must use external 4 drive support. SPP can be selected through the ecr register of ECP as mode 000.

Note[3]: MIDI Support: The Musical Instrumental Digital Interface (MIDI) operates at 31.25Kbaud (+/-1%).

CR05

CR05 can only be accessed in the configuration state and after the CSR has been initialized to 05H.

Table 61 – CR05

Floppy Disk Setup Register				
Type: R/W			Default: 0x00 on VCC POR	
BIT NO.	**BIT NAME**	**DESCRIPTION**		
0[1]	FDC Output Type Control (R/W)	0 = FDC Outputs are open drain (default). 1 = FDC Outputs are push-pull.		
1[1,2]	FDC Output Control (R/W)	0 = FDC Outputs Active (default). 1 = FDC Outputs Tri-State.		
2	FDC DMA Mode	0 = Burst mode is enabled for the FDC FIFO execution phase data transfers (default). 1 = Non-Burst mode enabled.		
4,3	DenSel	**BIT 4**	**BIT 3**	**DENSEL OUTPUT**
		0	0	Normal (default)
		0	1	Reserved
		1	0	1
		1	1	0
5	Swap Drives 0,1	0= do not swap (default). 1= swap drives and motor select 0 and 1 of the FDC on the parallel port.		
6,7	Reserved	Read Only. A read returns 0.		

Note[1]: Bits CR05[1:0] do not affect the Parallel Port FDC.

Note[2]: In the LPC47N227, the behavior of the DRVDEN1 Control CR03.4 depends upon the FDC Output Control CR05.1 (Table 62). If the FDC Output Control is active DRVDEN1 will behave as follows if CR03.4 is 0 the DRVDEN1 output pin assumes the value of the DRVDEN1 function, if CR03.4 is 1 the DRVDEN1 output pin stays high. If the FDC Output Control is inactive the DRVDEN1 Control will have no affect on the DRVDEN1 output pin.

Table 62 – DRVDEN1 Control

FDC OUTPUT CONTROL (CR05.1)	DRVDEN1 CONTROL (CR03.4)	DRVDEN1 (PIN 2)	DESCRIPTION
0	0	1/0	NORMAL DRVDEN1 FUNCTION
0	1	1	DRVDEN1 FORCED HIGH
1	X	TRISTATE	ALL FDD OUTPUT PINS ARE TRISTATED

CR06
CR06 can only be accessed in the configuration state and after the CSR has been initialized to 06H. CR06 holds the floppy disk drive type IDs for up to four floppy disk drives (see Table 6 – Drive Type ID in the Floppy Disk Controller).

Table 63 – CR06

Drive Type ID Register		
Type: R/W		Default: 0xFF on VCC POR
BIT NO.	**BIT NAME**	**DESCRIPTION**
0	ID00	Floppy Disk Drive 0 type ID 0
1	ID01	Floppy Disk Drive 0 type ID 1
2	ID10	Floppy Disk Drive 1 type ID 0
3	ID11	Floppy Disk Drive 1 type ID 1
4	ID20	Floppy Disk Drive 2 type ID 0
5	ID21	Floppy Disk Drive 2 type ID 1
6	ID30	Floppy Disk Drive 3 type ID 0
7	ID31	Floppy Disk Drive 3 type ID 1

CR07
CR07 can only be accessed in the configuration state and after the CSR has been initialized to 07H. CR07 controls auto power management and the floppy boot drive.

Table 64 – CR07

Auto Power Management and Boot Drive Select		
Type: R/W		Default: 0x00 on VCC POR; Bits[7:4] = 0000 on HARD RESET
BIT NO.	**BIT NAME**	**DESCRIPTION**
0,1	Floppy Boot	This bit is used to define the boot floppy. 0 = Drive A (default) 1 = Drive B
2,3	Reserved	Read Only. A read returns 0.
4	Parallel Port Enable	This bit controls the AUTOPOWER DOWN feature of the Parallel Port. The function is: 0 = Auto powerdown disabled (default) 1 = Auto powerdown enabled This bit is reset to the default state by POR or a hardware reset.
5	UART 2 Enable	This bit controls the AUTOPOWER DOWN feature of the UART2. The function is: 0 = Auto powerdown disabled (default) 1 = Auto powerdown enabled This bit is reset to the default state by POR or a hardware reset.
6	UART 1 Enable	This bit controls the AUTOPOWER DOWN feature of the UART1. The function is: 0 = Auto powerdown disabled (default) 1 = Auto powerdown enabled This bit is reset to the default state by POR or a hardware reset.

Auto Power Management and Boot Drive Select		
Type: R/W		Default: 0x00 on VCC POR; Bits[7:4] = 0000 on HARD RESET
BIT NO.	**BIT NAME**	**DESCRIPTION**
7	Floppy Disk Enable	This bit controls the AUTOPOWER DOWN feature of the Floppy Disk. The function is: 0 = Auto powerdown disabled (default) 1 = Auto powerdown enabled This bit is reset to the default state by POR or a hardware reset.

CR08
Register CR08 is reserved. The default value of this register after power up is 00H.

CR09
CR09 can only be accessed in the configuration state and after the CSR has been initialized to 09H. CR09 is a test control register and all bits must be treated as Reserved. Note: all test modes are reserved for SMSC use. Activating test mode registers may produce undesired results.

Table 65 – CR09

Test 4		
Type: R/W		Default: 0x00 on VCC POR
BIT NO.	**BIT NAME**	**DESCRIPTION**
0	Test 24	RESERVED FOR SMSC USE
1	Test 25	
2	Test 26	
3	Test 27	
4	Test 28	
5	Test 29	
6	Test 30	
7	Test 31	

CR0A
CR0A can only be accessed in the configuration state and after the CSR has been initialized to 0AH. CR0A defines the FIFO threshold for the ECP mode parallel port. Bits [5:4] are Reserved. Reserved Bits cannot be written and return 0 when read. Bits [7:6] are the IR OUTPUT MUX bits and are reset to the default state by a POR and a hardware reset.

Table 66 – CR0A

<table>
<tr><th colspan="5">ECP FIFO Threshold/IR MUX</th></tr>
<tr><th colspan="2">Type: R/W</th><th colspan="3">Default: 0x00 on VCC POR;
Bits[7:6] = 00 on HARD RESET</th></tr>
<tr><th>BIT NO.</th><th>BIT NAME</th><th colspan="3">DESCRIPTION</th></tr>
<tr><td>0</td><td>THR0</td><td colspan="3">ECP FIFO Threshold 0.</td></tr>
<tr><td>1</td><td>THR1</td><td colspan="3">ECP FIFO Threshold 1.</td></tr>
<tr><td>2</td><td>THR2</td><td colspan="3">ECP FIFO Threshold 2.</td></tr>
<tr><td>3</td><td>THR3</td><td colspan="3">ECP FIFO Threshold 3.</td></tr>
<tr><td>4,5</td><td>Reserved</td><td colspan="3">Read Only. A read returns 0.</td></tr>
<tr><td rowspan="5">6,7</td><td rowspan="5">IR Output Mux</td><td colspan="3">These bits are used to select IR Output Mux Mode.</td></tr>
<tr><td>BIT7</td><td>BIT6</td><td>MUX MODE</td></tr>
<tr><td>0</td><td>0</td><td>Active device to COM port (Default). That is, depending on the mode of Serial Port 2, use Pins 92, 94-100 for COM signals or use RXD2 and TXD2 (pins 95 and 96) for IR. When Serial Port 2 is inactive (Power Down bit = 0), then TXD2 pin is low. The IRTX2 pin is low.</td></tr>
<tr><td>0</td><td>1</td><td>Active device to IR port. That is, use IRRX2, IRTX2 (pins 61, 62). When Serial Port 2 is inactive (Power Down bit = 0), then IRTX2 pin is low. The TXD2 pin is low.</td></tr>
<tr><td>1</td><td>0</td><td>Reserved.</td></tr>
<tr><td>1</td><td>1</td><td>Outputs Inactive: TXD2 and IRTX2 are High-Z, regardless of mode of UART2 and state of UART2 powerdown bit.</td></tr>
</table>

CR0B

CR0B can only be accessed in the configuration state and after the CSR has been initialized to 0BH. CR0B indicates the Drive Rate table (Table 68) used for each drive. Refer to section CR1F for the Drive Type register.

Table 67 – CR0B

Drive Rate		
Type: R/W		Default: 0x00 on VCC POR
BIT NO.	**BIT NAME**	**DESCRIPTION**
0	FDD0 DTR0	Floppy Disk Drive 0 Drive Rate Table Bit 0.
1	FDD0 DTR1	Floppy Disk Drive 0 Drive Rate Table Bit 1.
2	FDD1 DTR0	Floppy Disk Drive 1 Drive Rate Table Bit 0.
3	FDD1 DTR1	Floppy Disk Drive 1 Drive Rate Table Bit 1.
4	FDD2 DTR0	Floppy Disk Drive 2 Drive Rate Table Bit 0.
5	FDD2 DTR1	Floppy Disk Drive 2 Drive Rate Table Bit 1.
6	FDD3 DTR0	Floppy Disk Drive 3 Drive Rate Table Bit 0.
7	FDD3 DTR1	Floppy Disk Drive 3 Drive Rate Table Bit 1.

Table 68 – Drive Rate Table (Recommended)

DRT1	DRT0	FORMAT
0	0	360K, 1.2M, 720K, 1.44M and 2.88M Vertical Format
0	1	3-Mode Drive
1	0	2 Meg Tape
1	1	Reserved

CR0C

CR0C can only be accessed in the configuration state and after the CSR has been initialized to 0CH. CR0C controls the operating mode of the UART. This register is reset to the default state by a POR or a hardware reset.

Table 69 – CR0C

UART Mode		
Type: R/W		Default: 0x02 on VCC POR and HARD RESET
BIT NO.	**BIT NAME**	**DESCRIPTION**
0	UART 2 RCV Polarity	0 = RX input active high (default). 1 = RX input active low.
1	UART 2 XMIT Polarity	0 = TX output active high. 1 = TX output active low (default).
2	UART 2 Duplex	This bit is used to define the FULL/HALF DUPLEX operation of UART 2. 1 = Half duplex 0 = Full duplex (default)
3, 4, 5	UART 2 MODE	UART 2 Mode 5 4 3 0 0 0 Standard COM Functionality (default) 0 0 1 IrDA (HPSIR) 0 1 0 Amplitude Shift Keyed IR 0 1 1 Reserved 1 x x Reserved
6	UART 1 Speed	This bit enables the high speed mode of UART 1. 1 = High speed enabled 0 = Standard (default)

UART Mode		
Type: R/W		Default: 0x02 on VCC POR and HARD RESET
BIT NO.	BIT NAME	DESCRIPTION
7	UART 2 Speed	This bit enables the high speed mode of UART 2. 1 = High speed enabled 0 = Standard (default)

CR0D

CR0D can only be accessed in the configuration state and after the CSR has been initialized to 0DH. This register is read only. CR0D contains the LPC47N227 Device ID. The default value of this register after power up is 5AH on VCC POR.

CR0E

CR0E can only be accessed in the configuration state and after the CSR has been initialized to 0EH. This register is read only. CR0E contains the current LPC47N227 Chip Revision Level starting at 00H.

CR0F

CR0F can only be accessed in the configuration state and after the CSR has been initialized to 0FH. CR0F is a test control register and all bits must be treated as Reserved. Note: all test modes are reserved for SMSC use. Activating test mode registers may produce undesired results.

Table 70 – CR0F

Test 1		
Type: R/W		Default: 0x00 on VCC POR
BIT NO.	BIT NAME	DESCRIPTION
0	Test 0	RESERVED FOR SMSC USE
1	Test 1	
2	Test 2	
3	Test 3	
4	Test 4	
5	Test 5	
6	Test 6	
7	Test 7	

CR10
CR10 can only be accessed in the configuration state and after the CSR has been initialized to 10H. CR10 is a test control register and all bits must be treated as Reserved. NOTE: All test modes are reserved for SMSC use. Activating test mode registers may produce undesired results.

Table 71 – CR10

Test 2		
Type: R/W		**Default: 0x00 on VCC POR**
BIT NO.	**BIT NAME**	**DESCRIPTION**
0	Test 8	RESERVED FOR SMSC USE
1	Test 9	
2	Test 10	
3	Test 11	
4	Test 12	
5	Test 13	
6	Test 14	
7	Test 15	

CR11
CR11 can only be accessed in the configuration state and after the CSR has been initialized to 11H. CR11 is a test control register and all bits must be treated as Reserved. NOTE: all test modes are reserved for SMSC use. Activating test mode registers may produce undesired results.

Table 72 – CR11

Test 3		
Type: R/W		**Default: 0x80 on VCC POR**
BIT NO.	**BIT NAME**	**DESCRIPTION**
0	Test 16	RESERVED FOR SMSC USE
1	Test 17	
2	Test 18	
3	Test 19	
4	Test 20	
5	Test 21	
6	Test 22	
7	Test 23	

CR12 - CR13
CR12 and CR13 are the LPC47N227 Configuration Ports base address registers (Table 73 and Table 74). These registers are used to relocate the Configuration Ports base address beyond the power-up defaults determined by the SYSOPT pin programming.

CR12 contains the Configuration Ports base address bits A[7:0]. CR13 contains the Configuration Ports base address bits A[10:8]. The address bits A[15:11] must be '00000' to access the configuration port.

The Configuration Ports base address is relocatable on even-byte boundaries; i.e., A0 = '0'.

At power-up the Configuration Ports base address is determined by the SYSOPT pin programming. To relocate the Configuration Ports base address after power-up, first write the lower address bits of the

new base address to CR12 and then write the upper address bits to CR13. Note: Writing CR13 changes the Configuration Ports base address.

Table 73 – CR12

Configuration Ports Base Address Byte 0 (Note)		
Type: R/W		**Default: 0x2E (SYSOPT=0) 0x4E (SYSOPT=1) on VCC POR and HARD RESET**
BIT NO.	**BIT NAME**	**DESCRIPTION**
0	Reserved	Read Only. A read returns 0.
1	A1	Configuration Ports Base Address Byte 0 for decoder.
2	A2	
3	A3	
4	A4	
5	A5	
6	A6	
7	A7	

Note: The Configuration Ports Base Address is relocatable on even-byte boundaries; i.e., A0 = “0”.

Table 74 – CR13

Configuration Ports Base Address Byte 1 (Note)		
Type: R/W		**Default: 0x00 (SYSOPT=0) 0x00 (SYSOPT=1) on VCC POR and HARD RESET**
BIT NO.	**BIT NAME**	**DESCRIPTION**
0	A8	Configuration Ports Base Address Byte 1 for decoder.
1	A9	
2	A10	
3-7	Reserved	Read Only. A read returns 0.

Note: Writing CR13 changes the Configuration Ports base address.

CR14
CR14 can only be accessed in the configuration state and after the CSR has been initialized to 14H. CR14 shadows the bits in the write-only FDC run-time DSR register.

Table 75 – CR14

DSR Shadow Register		
Type: R		**Default: N/A**
BIT NO.	**BIT NAME**	**DESCRIPTION**
0,1	Data Rate Select 0-1	These bits select the data rate of the floppy controller.
2-4	PRECOMP 0-2	These three bits select the value of write precompensation that will be applied to the WDATA output signal.
5	Reserved	Read Only. A read returns 0.
6	PWRDOWN	A logic "1" written to this bit will put the floppy controller into manual low power mode.
7	SOFTRESET	A logic "0" written to this bit resets the floppy disk controller. This bit is self clearing.

CR15
CR15 can only be accessed in the configuration state and after the CSR has been initialized to 15H. CR15 shadows the bits in the write-only UART1 run-time FCR register.

Table 76 - CR15

UART1 FCR Shadow Register				
Type: R/W				**Default: N/A**
BIT NO.	**BIT NAME**	**DESCRIPTION**		
0	FIFO Enable	Setting this bit to a logic "1" enables both the XMIT and RCVR FIFOs		
1	RCVR FIFO Reset	Setting this bit to a logic "1" clears all bytes in the RCVR FIFO and resets its counter logic to 0. This bit is self clearing.		
2	XMIT FIFO Reset	Setting this bit to a logic "1" clears all bytes in the XMIT FIFO and resets its counter logic to 0. This bit is self-clearing.		
3	DMA Mode Select	Writing to this bit has no effect on the operation of the UART.		
4,5	Reserved	Read Only. A read returns 0.		
6,7	RCVR Trigger	These bits are used to set the trigger level for the RCVR FIFO interrupt.		
		BIT7	**BIT6**	**RCVR FIFO Trigger Level (BYTES)**
		0	0	1
		0	1	4
		1	0	8
		1	1	14

CR16
CR16 can only be accessed in the configuration state and after the CSR has been initialized to 16H. CR16 shadows the bits in the write-only UART2 run-time FCR register. See CR15 for register description.

CR17
CR17 can only be accessed in the configuration state and after the CSR has been initialized to 17H. CR17 is the Force FDD Status Change register.

Table 77 - CR17

Force FDD Status Change Register		
Type: R/W		**Default: 0x03 on VCC POR**
BIT NO.	**BIT NAME**	**DESCRIPTION**
0,1	Force DSKCHG 0-1	Setting either of the Force Disk Change bits active (1) forces the FDD nDSKCHG input active when the appropriate drive has been selected. FORCE DSKCHG1 and FORCE DSKCHG0 can be written to a 1 but are not clearable by software. FORCE DSKCHG1 is cleared on (nSTEP AND nDS1), FORCE DSKCHG0 is cleared on (nSTEP AND nDS0). Note: The DSK CHG bit in the Floppy DIR register, Bit 7 = (nDS0 AND FORCE DSKCHG0) OR (nDS1 AND FORCE DSKCHG1) OR nDSKCHG. Setting either of the Force Disk Change bits active (1) forces the FDD nDSKCHG input active when the appropriate drive has been selected. Bit[0] Force Change for FDC0 0=Inactive 1=Active Bit[1] Force Change for FDC1 0=Inactive 1=Active
2	Force WRTPRT	FORCE WRTPRT asserts the internal nWRTPRT input to the controller when the FORCE WRTPRT bit is active (“1”) and a drive has been selected. The FORCE WRTPRT function applies to the nWRTPRT pin in the FDD Interface as well as the nWRTPRT pin in the Parallel Port FDC.
3-7	Reserved	Read Only. A read returns 0.

Note: The controls in the Force FDD Status Change register (CR17) apply to the FDD Interface pins as well as to the Parallel Port FDC.

CR18 - CR1E

CR18 - CR1E registers are reserved. Reserved registers cannot be written and return 0 when read. The default value of these registers after power up is 00H on VCC POR.

CR1F

CR1F can only be accessed in the configuration state and after the CSR has been initialized to 1FH. CR1F indicates the floppy disk Drive Type for each of four floppy disk drives. The floppy disk Drive Type is used to map the three FDC DENSEL, DRATE1 and DRATE0 outputs onto two Super I/O output pins DRVDEN1 and DRVDEN0 (Table 79).

Table 78 – CR1F

Drive Type		
Type: R/W		**Default: 0x00 on VCC POR**
BIT NO.	**BIT NAME**	**DESCRIPTION**
0	FDD0 DT1	Drive Type Bit 1 for FDD 0.
1	FDD0 DT0	Drive Type Bit 0 for FDD 0.
2	FDD1 DT1	Drive Type Bit 1 for FDD 1.
3	FDD1 DT0	Drive Type Bit 0 for FDD 1.
4	FDD2 DT1	Drive Type Bit 1 for FDD 2.
5	FDD2 DT0	Drive Type Bit 0 for FDD 2.
6	FDD3 DT1	Drive Type Bit 1 for FDD 3.
7	FDD3 DT0	Drive Type Bit 0 for FDD 3.

Table 79 – Drive Type Encoding

DRIVE TYPE		**DRVDEN0**	**DRVDEN1**	
DT0	**DT1**			**DRIVE TYPE DESCRIPTION**
0	0	DENSEL	DRATE0	4/2/1 MB 3.5” 2/1 MB 5.25” FDDS 2/1.6/1 MB 3.5” (3-MODE)
0	1	DRATE1	DRATE0	
1	0	nDENSEL	DRATE0	PS/2
1	1	DRATE0	DRATE1	

CR20

CR20 can only be accessed in the configuration state and after the CSR has been initialized to 20H. CR20 is used to select the base address of the floppy disk controller (FDC). The FDC base address can be set to 96 locations on 8 byte boundaries from 100H - 3F8H. To disable the FDC set ADR9 and ADR8 to zero. Set CR20.[1:0] to 00b when writing the FDC Base Address.

FDC Address Decoding: address bits A[15:10] must be ‘000000’ to access the FDC registers. A[3:0] are decoded as 0XXXb.

Table 80 – CR20

FDC Base Address		
Type: R/W		Default: 0x3C on VCC POR
BIT NO.	**BIT NAME**	**DESCRIPTION**
0	Reserved	Read Only. A read returns 0.
1	Reserved	Read Only. A read returns 0.
2	ADR4	FDC Base Address bits for decoder.
3	ADR5	
4	ADR6	
5	ADR7	
6	ADR8	
7	ADR9	

CR21
CR21 can only be accessed in the configuration state and after the CSR has been initialized to 21H. CR21 is the Floppy on Parallel Port Pin register.

Table 81 – CR21

FDC on PP/EPP Timeout Select				
Type: R/W				Default: 0x00 on VCC POR
BIT NO.	**BIT NAME**	**DESCRIPTION**		
0,1	**FDC_PP**	**FDC on Parallel Port Pin**		
		BIT1	**BIT0**	**DESCRIPTION**
		0	0	Bits in PP mode Register control the FDC on the parallel port, the FDC_PP pin function is not used.
		0	1	The FDC_PP pin controls the FDC on the PP as follows: (non-inverted polarity) when the pin is low, the parallel port pins are used for a floppy disk controller: drive 0 is on FDC pins, drive 1 is on parallel port pins.
		1	0	The FDC_PP pin controls the FDC on the PP as follows: (non-inverted polarity) when the pin is low, the parallel port pins are used for a floppy disk controller: drive 0 is on parallel port pins and drive 1 is on parallel port pins.
		1	1	Reserved
2	TIMEOUT_SELECT	This bit selects the means of clearing the TIMEOUT bit in the EPP Status register. If the TIMEOUT_SELECT bit is cleared (‘0’), the TIMEOUT bit is cleared on the trailing edge of the read of the EPP Status Register (default). If the TIMEOUT_SELECT bit is set (‘1’), the TIMEOUT bit is cleared on a write of ‘1’ to the TIMEOUT bit.		
3-7	Reserved	Read Only. A read returns 0.		

CR22

The ECP Software Select register CR22 contains the ECP IRQ Select bits and the ECP DMA Select bits. CR22 is part of the ECP DMA/IRQ Software Indicators described in the ECP cnfgB register. CR22 is read/write. Note: all of the ECP DMA/IRQ Software Indicators, including CR22, are software-only. Writing these bits does not affect the ECP hardware DMA or IRQ channels that are configured in CR26 and CR27.

Table 82 - CR22

ECP Software Select Register		
Type: R/W		Default: 0x00 on VCC POR
BIT NO.	**BIT NAME**	**DESCRIPTION**
2:0	ECP DMA Select	ECP DMA software Indicator
5:3	ECP IRQ Select	ECP IRQ Software Indicator
6,7	Reserved	Read Only. A read returns 0.

CR23

CR23 can only be accessed in the configuration state and after the CSR has been initialized to 23H. CR23 is used to select the base address of the parallel port. If EPP is not enabled, the parallel port can be set to 192 locations on 4-byte boundaries from 100H - 3FCH; if EPP is enabled, the parallel port can be set to 96 locations on 8-byte boundaries from 100H - 3F8H. To disable the parallel port, set ADR9 and ADR8 to zero.

Parallel Port Address Decoding: address bits A[15:10] must be '000000' to access the Parallel Port when in Compatible, Bi-directional, or EPP modes. A10 is active when in ECP mode.

Table 83 - CR23

Parallel Port Base Address		
Type: R/W		Default: 0x00 on VCC POR
BIT NO.	**BIT NAME**	**DESCRIPTION**
0	ADR2	Parallel Port Base Address bits for decoder.
1	ADR3	
2	ADR4	
3	ADR5	
4	ADR6	
5	ADR7	
6	ADR8	
7	ADR9	

Table 84 - Parallel Port Addressing Options

EPP ENABLED	ADDRESSING (LOW BITS) DECODE
No	A[1:0] = XXb
Yes	A[2:0] = XXXb

CR24

CR24 can only be accessed in the configuration state and after the CSR has been initialized to 24H. CR24 is used to select the base address of Serial Port 1 (UART1). The serial port can be set to 96 locations on 8-byte boundaries from 100H - 3F8H. To disable Serial Port 1, set ADR9 and ADR8 to zero. Set CR24.0 to 0 when writing the UART1 Base Address.

Serial Port 1 Address Decoding: address bits A[15:10] must be '000000' to access UART1 registers. A[2:0] are decoded as XXXb.

Table 85 - CR24

UART1 Base Address Register		
Type: R/W		**Default: 0x00 on VCC POR**
BIT NO.	**BIT NAME**	**DESCRIPTION**
0	Reserved	Read Only. A read returns 0.
1	ADR3	Serial Port 1 Base Address bits for decoder.
2	ADR4	
3	ADR5	
4	ADR6	
5	ADR7	
6	ADR8	
7	ADR9	

CR25

CR25 can only be accessed in the configuration state and after the CSR has been initialized to 25H. CR25 is used to select the base address of Serial Port 2 (UART2). Serial Port 2 can be set to 96 locations on 8-byte boundaries from 100H - 3F8H. To disable Serial Port 2, set ADR9 and ADR8 to zero. Set CR25.0 to 0 when writing the UART2 Base Address.

Serial Port 2 Address Decoding: address bits A[15:10] must be '000000' to access UART2 registers. A[2:0] are decoded as XXXb.

Table 86 - CR25

UART2 Base Address Register		
Type: R/W		**Default: 0x00 on VCC POR**
BIT NO.	**BIT NAME**	**DESCRIPTION**
0	Reserved	Read Only. A read returns 0.
1	ADR3	Serial Port 2 Base Address bits for decoder.
2	ADR4	
3	ADR5	
4	ADR6	
5	ADR7	
6	ADR8	
7	ADR9	

CR26

CR26 can only be accessed in the configuration state and after the CSR has been initialized to 26H. CR26 is used to select the DMA for the FDC (Bits 4 - 7) and the Parallel Port (bits 0 - 3). Any unselected DMA Request output (DRQ) is in tristate.

Table 87 - CR26

FDC and PP DMA Selection Register		
Type: R/W		Default: 0x00 on VCC POR
BIT NO.	**BIT NAME**	**DESCRIPTION**
3:0	PP DMA Select	These bits are used to select DMA for Parallel Port.
7:4	FDC DMA Select	These bits are used to select DMA for Floppy Disk Controller.

Table 88 - DMA Selection

BITS[3:0] OR BITS[7:4]	DMA SELECTED
0000	RESERVED
0001	DMA1
0010	DMA2
0011	DMA3
0100	RESERVED
....	…. ….
1110	RESERVED
1111	NONE

CR27

CR27 can only be accessed in the configuration state and after the CSR has been initialized to 27H. CR27 is used to select the IRQ for the FDC (Bits 4 - 7) and the Parallel Port (bits 3 - 0). Any unselected IRQ output (registers CR27 - CR29) is in tri-state.

Table 89 - CR27

FDC and PP IRQ Selection Register		
Type: R/W		Default: 0x00 on VCC POR
BIT NO.	**BIT NAME**	**DESCRIPTION**
3:0	PP IRQ Select	These bits are used to select IRQ for Parallel Port.
7:4	FDC IRQ Select	These bits are used to select IRQ for Floppy Disk Controller.

Table 90 – IRQ Encoding

BITS[3:0] OR BITS[7:4]	IRQ SELECTED
0000	NONE
0001	IRQ_1
0010	IRQ_2
0011	IRQ_3
0100	IRQ_4
0101	IRQ_5
0110	IRQ_6
0111	IRQ_7
1000	IRQ_8
1001	IRQ_9
1010	IRQ_10
1011	IRQ_11
1100	IRQ_12
1101	IRQ_13
1110	IRQ_14
1111	IRQ_15

CR28

CR28 can only be accessed in the configuration state and after the CSR has been initialized to 28H. CR28 is used to select the IRQ for Serial Port 1 (bits 7 - 4) and for Serial Port 2 (bits 3 - 0). Refer to the IRQ encoding for CR27 (Table 90). Any unselected IRQ output (registers CR27 - CR29) is in tristate. Shared IRQs are not supported in the LPC47N227.

Table 91 – CR28

UART Interrupt Selection		
Type: R/W		Default: 0x00 on VCC POR
BIT NO.	**BIT NAME**	**DESCRIPTION**
3:0	UART2 IRQ Select	These bits are used to select IRQ for Serial Port 2. See IRQ encoding for CR27 (Table 90).
7:4	UART1 IRQ Select	These bits are used to select IRQ for Serial Port 1. See IRQ encoding for CR27 (Table 90).

Table 92 – UART Interrupt Operation

UART1		UART2		IRQ PINS	
UART1 OUT2 bit	**UART1 IRQ Output State**	**UART2 OUT2 bit**	**UART2 IRQ Output State**	**UART1 Pin State**	**UART2 Pin State**
0	Z	0	Z	Z	Z
1	asserted	0	Z	1	Z
1	de-asserted	0	Z	0	Z
0	Z	1	asserted	Z	1
0	Z	1	de-asserted	Z	0
1	asserted	1	asserted	1	1
1	asserted	1	de-asserted	1	0
1	de-asserted	1	asserted	0	1
1	de-asserted	1	de-asserted	0	0
It is the responsibility of the software to ensure that two IRQ's are not set to the same IRQ number. Potential damage to chip may result. Note: Z = Don't Care.					

CR29

CR29 can only be accessed in the configuration state and after the CSR has been initialized to 29H. CR29 controls the HPMODE bit and is used to select the IRQ mapping (bits 0 - 3) for the IRQIN1 pin. Refer to IRQ encoding for CR27 (Table 90). Any unselected IRQ output (registers CR27 - CR29) is in tristate.

Table 93 – CR29

IRQIN1/HPMODE/SIRQ_CLKRUN_En			
Type: R/W			**Default: 0x80 on VCC POR**
BIT NO.	**BIT NAME**	**DESCRIPTION**	
0-3	IRQIN1	Selects the IRQ for IRQIN1.	
4	HPMODE	**See** FIGURE 2 – INFRARED INTERFACE BLOCK DIAGRAM	
		0	Select IRMODE (default)
		1	Select IRRX3
5	RESERVED	Not Writeable, Reads Return "0"	
7	SIRQ_CLKRUN_EN	Serial IRQ and CLKRUN enable bit. 0 = Disable 1 = Enable (default)	

CR2A

CR2A can only be accessed in the configuration state and after the CSR has been initialized to 2AH. CR2A is used to select the IRQ mapping (bits 0 - 3) for the IRQIN2 pin. Refer to IRQ encoding for CR27 (Table 90). Any unselected IRQ output (registers CR27 - CR29) is in tristate.

Table 94 – CR2A

IRQIN2		
Type: R/W		**Default: 0x00 on VCC POR**
BIT NO.	**BIT NAME**	**DESCRIPTION**
3:0	IRQIN2	Selects the IRQ for IRQIN2.
7:4	Reserved	Read Only. A read returns 0.

CR2B

CR2B can only be accessed in the configuration state and after the CSR has been initialized to 2BH. CR2B is used to set the SCE (FIR) base address ADR[10:3]. The SCE base address can be set to 224 locations on 8-byte boundaries from 100H - 7F8H. To disable the SCE, set ADR10, ADR9 and ADR8 to zero.

SCE Address Decoding: address bits A[15:11] must be '00000' to access SCE registers. A[2:0] are decoded as XXXb.

Table 95 - CR2B

SCE (FIR) Base Address Register		
Type: R/W		Default: 0x00 on VCC POR
BIT NO.	**BIT NAME**	**DESCRIPTION**
0	ADR3	FIR Base Address bits for decoder.
1	ADR4	
2	ADR5	
3	ADR6	
4	ADR7	
5	ADR8	
6	ADR9	
7	ADR10	

CR2C

CR2C can only be accessed in the configuration state and after the CSR has been initialized to 2CH. Bits D[3:0] of this register are used to select the DMA for the SCE (FIR). Bits D[7:4] are Reserved. Reserved bits cannot be written and return 0 when read. Any unselected DMA Request output (DRQ) is in tristate.

Table 96 - CR2C

SCE (FIR) DMA Select Register						
Type: R/W					Default: 0x00 on VCC POR	
BIT NO.	**BIT NAME**	**DESCRIPTION**				
3:0	DMA Select	**BIT3**	**BIT2**	**BIT1**	**BIT0**	**DMA SELECTED**
		0	0	0	0	RESERVED
		0	0	0	1	DMA1
		0	0	1	0	DMA2
		0	0	1	1	DMA3
		0	1	0	0	RESERVED
		.	.	.	.	.
		.	.	.	.	.
		1	1	1	0	RESERVED
		1	1	1	1	NONE
7:4	Reserved	Read Only. A read returns 0.				

CR2D
CR2D can only be accessed in the configuration state and after the CSR has been initialized to 2DH. CR2D is used to set the IR Half Duplex Turnaround Delay Time for the IR port. This value is 0 to 25.5msec in 100µsec increments.

The IRCC v2.0 block includes an 8 bit IR Half Duplex Time-out register in SCE Register Block 5, Address 1 that interacts with configuration register CR2D. These two registers behave like the other IRCC Legacy controls where either source uniformly updates the value of both registers when either register is explicitly written or following a device-level POR. IRCC software resets do not affect these registers.

The IR Half Duplex Time-out is programmable from 0 to 25.5mS in 100µS increments, as follows:

IR HALF DUPLEX TIME-OUT = (CR2D) x 100µS

Table 97 – CR2D

IR Half Duplex Timeout		
Type: R/W		Default: 0x03 on VCC POR
BIT NO.	**BIT NAME**	**DESCRIPTION**
0-7	IR Half Duplex Time Out	These bits are used to set the IR Half Duplex Turnaround Delay Time for the IR port. This value is 0 to 25.5msec in 100µsec increments.

CR2E
CR2E can only be accessed in the configuration state and after the CSR has been initialized to 2EH. CR2E is directly connected to SCE Register Block Three, Address 0x05 in the IRCC v2.0 block.

Table 98 – CR2E

Software Select A		
Type: R/W		Default: 0x00 on VCC POR
BIT NO.	**BIT NAME**	**DESCRIPTION**
0-7	Software Select A	These bits are directly connected to SCE Register Block Three, Address 0x05 in the IRCC v2.0 block.

CR2F
CR2F can only be accessed in the configuration state and after the CSR has been initialized to 2FH. CR2F is directly connected to SCE Register Block Three, Address 0x06 in the IRCC v2.0 block.

Table 99 – CR2F

Software Select B		
Type: R/W		Default: 0x00 on VCC POR
BIT NO.	**BIT NAME**	**DESCRIPTION**
0-7	Software Select B	These bits are directly connected to SCE Register Block Three, Address 0x06 in the IRCC v2.0 block.

CR30
CR30 can only be accessed in the configuration state and after the CSR has been initialized to 30H. CR30 is used to set the Runtime Register Block base address ADR[11:4]. The Runtime Register Block

base address can be set to 240 locations on 16-byte boundaries from 100H – FF0H. To disable Runtime Registers Block, set ADR11 – ADR8 to zero.

SCE Address Decoding: address bits A[15:12] must be '0000' to access Runtime Register Block registers. A[3:0] are decoded as XXXXb.

Table 100 – CR30

Runtime Registers Block Base Address		
Type: R/W		Default: 0x00 on VCC POR
BIT NO.	**BIT NAME**	**DESCRIPTION**
0	ADR4	The bits in this register are used to program the location of the Runtime Register Block Base Address.
1	ADR5	
2	ADR6	
3	ADR7	
4	ADR8	
5	ADR9	
6	ADR10	
7	ADR11	

CR31
CR31 can only be accessed in the configuration state and after the CSR has been initialized to 31H. CR31 is GPIO Direction Register 1 and is used to select the direction of GP10-GP17 pins.

Table 101 – CR31

GPIO Direction Register 1		
Type: R/W		Default: 0x00 on VTR POR
BIT NO.	**BIT NAME**	**DESCRIPTION**
0	GP10	The bits in this register are used to select the direction of the GP10-GP17 pins. 0=Input 1=Output
1	GP11	
2	GP12	
3	GP13	
4	GP14	
5	GP15	
6	GP16	
7	GP17	

CR32
CR32 can only be accessed in the configuration state and after the CSR has been initialized to 32H. CR32 is GPIO Polarity Register 1 and is used to select the polarity of GP10-GP17 pins.

Table 102 – CR32

GPIO Polarity Register 1		
Type: R/W		Default: 0x00 on VTR POR
BIT NO.	**BIT NAME**	**DESCRIPTION**
0	GP10	The bits in this register are used to select the polarity of the GP10-GP17 pins. 0=Non-Inverted 1=Inverted
1	GP11	
2	GP12	
3	GP13	
4	GP14	
5	GP15	
6	GP16	
7	GP17	

CR33
CR33 can only be accessed in the configuration state and after the CSR has been initialized to 33H. CR33 is GPIO Direction Register 2. It is used to select the direction of GP20-GP24 pins, and select alternate function on GP23 and GP12 pins.

Table 103 – CR33

GPIO Direction Register 2		
Type: R/W		Default: 0x00 on VTR POR
BIT NO.	**BIT NAME**	**DESCRIPTION**
0	GP20	These bits are used to select the direction of the GP20-GP24. 0=Input 1=Output
1	GP21	
2	GP22	
3	GP23	
4	GP24	
5	Reserved	Read Only. A read returns 0.
6	GP23 Alternate Function Select	0=GPIO 1=FDC_PP (When this function is selected, the pin must be selected as an input. Polarity is controlled by the polarity bit. If enabled for PME or SMI, the interrupt is generated on either edge.)
7	GP12 Alternate. Function Select	0=GPIO 1=nIO_SMI Note: Selecting the nIO_SMI function with GP12 configured with non-inverted polarity will give an active low output signal. The output type can be programmed for open drain via CR39.

CR34

CR35 can only be accessed in the configuration state and after the CSR has been initialized to 34H. CR34 is GPIO Polarity Register 2. It is used to select the polarity of GP20-GP24 and IO_PME pins, and select alternate function on GP13 and GP14 pins.

Table 104 – CR34

GPIO Polarity Register 2		
Type: R/W		**Default: 0x00 on VTR POR**
BIT NO.	**BIT NAME**	**DESCRIPTION**
0	GP20	These bits are used to select the polarity of the GP20-GP24 pins. 0=Non-Inverted 1=Inverted
1	GP21	
2	GP22	
3	GP23	
4	GP24	
5	nIO_PME Polarity select	This bit is used to select the polarity of the nIO_PME pin. 0=Non-Inverted 1=Inverted Note: configuring this pin function with non-inverted polarity will give an active low output signal. The output type can be either open drain or push-pull. (See CR39).
6	GP13 Alternate Function Select	0=GPIO 1=IRQIN1
7	GP14 Alternate Function Select	0=GPIO 1=IRQIN2

CR35

CR35 can only be accessed in the configuration state and after the CSR has been initialized to 35H. CR35 is GPIO Direction Register 3 and is used to select the direction of GP30-GP37 pins.

Table 105 – CR35

GPIO Direction Register 3		
Type: R/W		**Default: 0x00 on VTR POR**
BIT NO.	**BIT NAME**	**DESCRIPTION**
0	GP30	The bits in this register are used to select the direction of the GP30-GP37 pins. 0=Input 1=Output
1	GP31	
2	GP32	
3	GP33	
4	GP34	
5	GP35	
6	GP36	
7	GP37	

CR36
CR36 can only be accessed in the configuration state and after the CSR has been initialized to 36H. CR36 is GPIO Polarity Register 3 and is used to select the polarity of GP30-GP37 pins.

Table 106 – CR36

GPIO Polarity Register 3		
Type: R/W		Default: 0x00 on VTR POR
BIT NO.	**BIT NAME**	**DESCRIPTION**
0	GP30	The bits in this register are used to select the polarity of the GP30-GP37 pins. 0=Non-Inverted 1=Inverted
1	GP31	
2	GP32	
3	GP33	
4	GP34	
5	GP35	
6	GP36	
7	GP37	

CR37
CR37 can only be accessed in the configuration state and after the CSR has been initialized to 37H. CR37 is GPIO Direction Register 4 and is used to select the direction of GP40-GP47 pins.

Table 107 – CR37

GPIO Direction Register 4		
Type: R/W		Default: 0x00 on VTR POR
BIT NO.	**BIT NAME**	**DESCRIPTION**
0	GP40	The bits in this register are used to select the direction of the GP40-GP47 pins. 0=Input 1=Output
1	GP41	
2	GP42	
3	GP43	
4	GP44	
5	GP45	
6	GP46	
7	GP47	

CR38
CR38 can only be accessed in the configuration state and after the CSR has been initialized to 38H. CR38 is GPIO Polarity Register 4 and is used to select the polarity of GP40-GP47 pins.

Table 108 – CR38

GPIO Polarity Register 4		
Type: R/W		Default: 0x80 on VTR POR
BIT NO.	**BIT NAME**	**DESCRIPTION**
0	GP40	The bits in this register are used to select the polarity of the GP40-GP47 pins. 0=Non-Inverted 1=Inverted
1	GP41	
2	GP42	
3	GP43	
4	GP44	
5	GP45	
6	GP46	
7	GP47	

CR39
CR39 can only be accessed in the configuration state and after the CSR has been initialized to 39H. CR39 is GPIO Output Register and is used to select the output buffer of GP12-GP17, GP20 and nIO_PME pins.

Table 109 – CR39

GPIO Output Register		
Type: R/W		Default: 0x00 on VTR POR
BIT NO.	**BIT NAME**	**DESCRIPTION**
0	GP12	The bits in this register are used to select the output buffer type of the GP12-GP17, GP20 and nIO_PME pins. 0=Push-pull 1=Open Drain
1	GP13	
2	GP14	
3	GP15	
4	GP16	
5	GP17	
6	GP20	
7	nIO_PME	

Logical Device Base I/O Address and Range

Table 110 – I/O Base Address Configuration Register Description

LOGICAL DEVICE	REGISTER INDEX	BASE I/O RANGE (Note 1)	FIXED BASE OFFSETS
FDC	0x20	[0x0100:0x03F8] on 8-byte boundaries	+0 : SRA +1 : SRB +2 : DOR +3 : TDR +4 : MSR/DSR +5 : FIFO +7 : DIR/CCR
Parallel Port	0x23	[0x0100:0x03FC] on 4-byte boundaries (EPP Not supported) or [0x0100:0x03F8] on 8-byte boundaries	+0 : Data/ecpAfifo +1 : Status +2 : Control +400h : cfifo/ecpDfifo/tfifo/cnfgA +401h : cnfgB +402h : ecr
		(all modes supported, EPP is only available when the base address is on an 8-byte boundary)	+3 : EPP Address +4 : EPP Data 0 +5 : EPP Data 1 +6 : EPP Data 2 +7 : EPP Data 3
Serial Port 1	0x24	[0x0100:0x03F8] on 8 byte boundaries	+0 : RB/TB/LSB div +1 : IER/MSB div +2 : IIR/FCR +3 : LCR +4 : MCR +5 : LSR +6 : MSR +7 : SCR
Serial Port 2	0x25	[0x0100:0x03F8] on 8-byte boundaries	+0 : RB/TB/LSB div +1 : IER/MSB div +2 : IIR/FCR +3 : LCR +4 : MCR +5 : LSR +6 : MSR +7 : SCR
	0x2B (FIR/CIR)	[0x100:0x07F8] on 8-byte boundaries	+0 : DR/SCEA/CIRC/IDH/(IRDACR/BOFH) +1 : INTID/SCEB/CIRCR/IDL/BOFL +2 : IER/FIFOT/CIRBR/CID/BWCL +3 : LSR/LSA/VERN/(BWCH/TDSH) +4 : LCA/(IRQL/DMAC)/TDSL +5 : LCB/RDSH +6 : BS/RDSL +7 : MCR

LOGICAL DEVICE	REGISTER INDEX	BASE I/O RANGE (Note 1)	FIXED BASE OFFSETS
Runtime Register Block	0x30	[0x0100:0x0FF0] on 16-byte boundaries	+00 : PME_STS . . . +0F : GP4 (See Table 52 in the Runtime Registers section for Full List)
Config. Port	0x12, 0x13 (Note 2)	[0x0100:0x07FE] On 2-byte boundaries	See Configuration Registers in Table 55. They are accessed through the index and DATA ports located at the Configuration Port address and the Configuration Port address +1 respectively.

Note 2: The Configuration Port is at either 0x02E or 0x04E (for SYSOPT=0 or SYSOPT=1) at power up and can be relocated via CR12 and CR13.

Note A. Logical Device IRQ and DMA Operation

1. IRQ and DMA Enable and Disable: Any time the IRQ or DMA channel for a logical block is disabled by a register bit in that logical block, the IRQ and/or DMA channel is disabled. This is in addition to the IRQ and DMA channel disabled by the Configuration Registers (active bit or address not valid).

a. FDC: For the following cases, the IRQ and DMA channel used by the FDC are disabled.
Digital Output Register (Base+2) bit D3 (DMAEN) set to "0".
The FDC is in power down (disabled).

b. Serial Ports:
Modem Control Register (MCR) Bit D2 (OUT2) - When OUT2 is a logic "0", the serial port interruptis disabled.
Disabling DMA Enable bit, disables DMA for UART2. Refer to the IrCC specification.

c. Parallel Port:
I. SPP and EPP modes: Control Port (Base+2) bit D4 (IRQE) set to "0", IRQ is disabled.
ii. ECP Mode:
(1) (DMA) dmaEn from ecr register. See table below.
(2) IRQ - See table below.

MODE (FROM ECR REGISTER)		IRQ CONTROLLED BY	DMA CONTROLLED BY
000	PRINTER	IRQE	dmaEn
001	SPP	IRQE	dmaEn
010	FIFO	(on)	dmaEn
011	ECP	(on)	dmaEn
100	EPP	IRQE	dmaEn
101	RES	IRQE	dmaEn
110	TEST	(on)	dmaEn

MODE (FROM ECR REGISTER)		IRQ CONTROLLED BY	DMA CONTROLLED BY
111	CONFIG	IRQE	dmaEn

OPERATIONAL DESCRIPTION

Maximum Guaranteed Ratings

Operating Temperature Range ..... 0^oC to $+70^oC$
Storage Temperature Range ..... -55^o to $+150^oC$
Lead Temperature Range ..... Refer to JEDEC Spec. J-STD-020
Positive Voltage on any pin, with respect to Ground ..... V_{CC}+0.3V
Negative Voltage on any pin, with respect to Ground ..... -0.3V
Maximum V_{CC} ..... +7V

Note: Stresses above those listed above could cause permanent damage to the device. This is a stress rating only and functional operation of the device at any other condition above those indicated in the operation sections of this specification is not implied.

Note: When powering this device from laboratory or system power supplies, it is important that the Absolute Maximum Ratings not be exceeded or device failure can result. Some power supplies exhibit voltage spikes on their outputs when the AC power is switched on or off. In addition, voltage transients on the AC power line may appear on the DC output. If this possibility exists, it is suggested that a clamp circuit be used.

DC Electrical Characteristics

($T_A = 0^0C – 70^0C$, V_{CC} = +3.3 V ± 10%)

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	COMMENTS
I Type Input Buffer						
Low Input Level	V_{ILI}			0.8	V	TTL Levels
High Input Level	V_{IHI}	2.0			V	
IS Type Input Buffer						
Low Input Level	V_{ILIS}			0.8	V	Schmitt Trigger
High Input Level	V_{IHIS}	2.2			V	Schmitt Trigger
Schmitt Trigger Hysteresis	V_{HYS}		100		mV	
Input Leakage, I and IS Buffers						
Low Input Leakage	I_{IL}	-10		+10	µA	V_{IN} = 0
High Input Leakage	I_{IH}	-10		+10	µA	$V_{IN} = V_{CC}$

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	COMMENTS
O6 Type Buffer						
Low Output Level	V_{OL}			0.4	V	I_{OL} = 6mA
High Output Level	V_{OH}	2.4			V	I_{OH} = -3mA
IO8 Type Buffer						
Low Output Level	V_{OL}			0.4	V	I_{OL} = 8mA
High Output Level	V_{OH}	2.4			V	I_{OH} = -4mA
Input Leakage Current	I_{LEAK}	-10		+10	µA	V_{IN} = 0 to V_{CC} (Note 1)
O8 Type Buffer						
Low Output Level	V_{OL}			0.4	V	I_{OL} = 8mA
High Output Level	V_{OH}	2.4			V	I_{OH} = -4mA
O12 Type Buffer						
Low Output Level	V_{OL}			0.4	V	I_{OL} = 12mA
High Output Level	V_{OH}	2.4			V	I_{OH} = -6mA
IO12 Type Buffer						
Low Output Level	V_{OL}			0.4	V	I_{OL} = 12mA
High Output Level	V_{OH}	2.4			V	I_{OH} = -6mA
Input Leakage Current	I_{LEAK}	-10		+10	µA	V_{IN} = 0 to V_{CC} (Note 1)
OD12 Type Buffer						
Low Output Level	V_{OL}			0.4	V	I_{OL} = 12mA
Input Leakage Current	I_{LEAK}	-10		+10	µA	V_{IN} = 0 to V_{CC}
OD14 Type Buffer						
Low Output Level	V_{OL}			0.4	V	I_{OL} = 14mA
Input Leakage Current	I_{LEAK}	-10		+10	µA	V_{IN} = 0 to V_{CC}

PARAMETER	SYMBOL	MIN	TYP	MAX	UNITS	COMMENTS
OP14 Type Buffer						
Low Output Level	V_{OL}			0.4	V	I_{OL} = 14mA
High Output Level	V_{OH}	2.4			V	I_{OH} = -14mA
Input Leakage Current	I_{LEAK}	-10		+10	µA	V_{IN} = 0 to V_{CC} (Note 1)
IOP14 Type Buffer						
Low Output Level	V_{OL}			0.4	V	I_{OL} = 14mA
High Output Level	V_{OH}	2.4			V	I_{OH} = -14mA
Input Leakage Current	I_{LEAK}	-10		+10	µA	V_{IN} = 0 to V_{CC} (Note 1)
Backdrive Protect/ChiProtect (All pins excluding LAD[3:0], nLDRQ, nLPCPD, nLFRAME)	I_{IL}			± 10	µA	V_{CC} = 0V V_{IN} = 5.5V Max
5V Tolerant Pins (All pins excluding LAD[3:0], nLDRQ, nLPCPD, nLFRAME) Inputs and Outputs in High Impedance State	I_{IL}			± 10	µA	V_{CC} = 3.3V V_{IN} = 5.5V Max
LPC Bus Pins (LAD[3:0], nLDRQ, nLPCPD, nLFRAME)	I_{IL}			± 10	µA	V_{CC} = 3.3V V_{IN} = 3.6V Max
V_{CC} Supply Current Active	I_{CCI}			25[3]	mA	All outputs open, all inputs in a fixed state (i.e., 0V or 3.3V)
Trickle Supply Voltage	V_{TR}	V_{CC} min -.5V[5]		V_{CC} max	V	V_{CC} must not be greater than .5V above V_{TR}
V_{TR} Supply Current Active	I_{TRI}			0.1[3,4]	mA	All outputs open, all inputs in a fixed state (i.e., 0V or 3.3V)

Note 1: All output leakage's are measured with all pins in high impedance
Note 2: Output leakage is measured with the low driving output off, either for a high level output or a high impedance state.
Note 3: Contact SMSC for the latest values.
Note 4: Max I_{TRI} with V_{CC} = 3.3V (nominal) is 0.1mA.
Max I_{TRI} with V_{CC} = 0V (nominal) is 50 µA.
Note 5: The minimum value given for V_{TR} applies when V_{CC} is active. When V_{CC} is 0V, the minimum V_{TR} is 0V.

CAPACITANCE $T_A = 25^0C$; fc = 1MHz; V_{CC} = 3.3V ±10%

PARAMETER	SYMBOL	LIMITS			UNIT	TEST CONDITION
		MIN	TYP	MAX		
Clock Input Capacitance	C_{IN}			20	pF	All pins except pin under test tied to AC ground
Input Capacitance	C_{IN}			10	pF	
Output Capacitance	C_{OUT}			20	pF	

TIMING DIAGRAMS

For the Timing Diagrams shown, the following capacitive loads are used on outputs.

NAME	CAPACITANCE TOTAL (pF)
SER_IRQ	50
nLAD[3:0]	50
nLDRQ	50
nDIR	240
nSTEP	240
nDS0-1	240
nWDATA	240
PD[0:7]	240
nSTROBE	240
nALF	240
SLCTIN	240
TXD1	50
TXD2	50
nCLKRUN	50

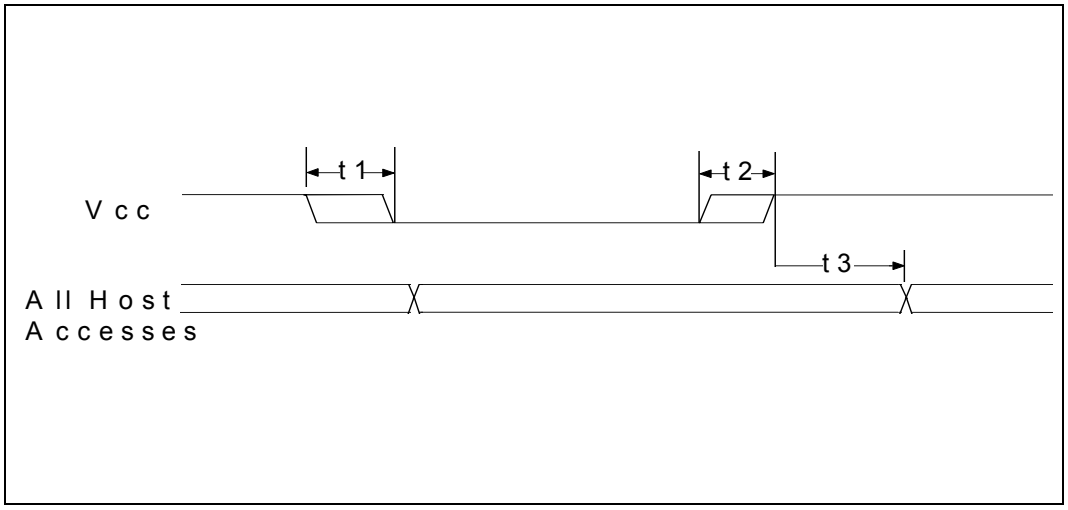


FIGURE 6 - POWER-UP TIMING

NAME	DESCRIPTION	MIN	TYP	MAX	UNITS
t1	Vcc Slew from 2.7V to 0V	300			µs
t2	Vcc Slew from 0V to 2.7V	100			µs
t3	All Host Accesses After Powerup (Note 1)	125		500	µs

Note 1: Internal write-protection period after Vcc passes 2.7 volts on power-up

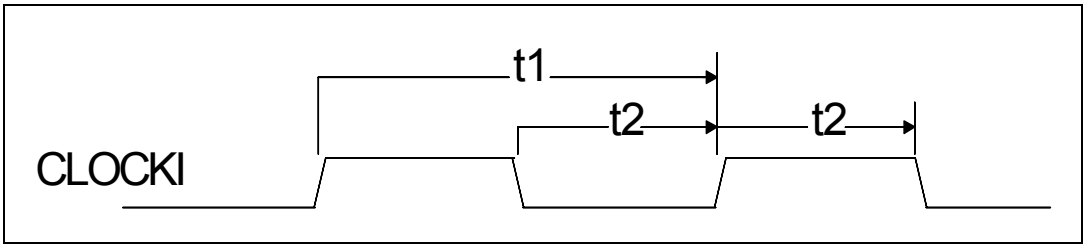


FIGURE 7 - INPUT CLOCK TIMING

NAME	DESCRIPTION	MIN	TYP	MAX	UNITS
t1	Clock Cycle Time for 14.318MHZ		69.84		ns
t2	Clock High Time/Low Time for 14.318MHz	20	35		ns
t1	Clock Cycle Time for 32KHZ		31.25		µs
t2	Clock High Time/Low Time for 32KHz		16.53		µs
	Clock Rise Time/Fall Time (not shown)			5	ns

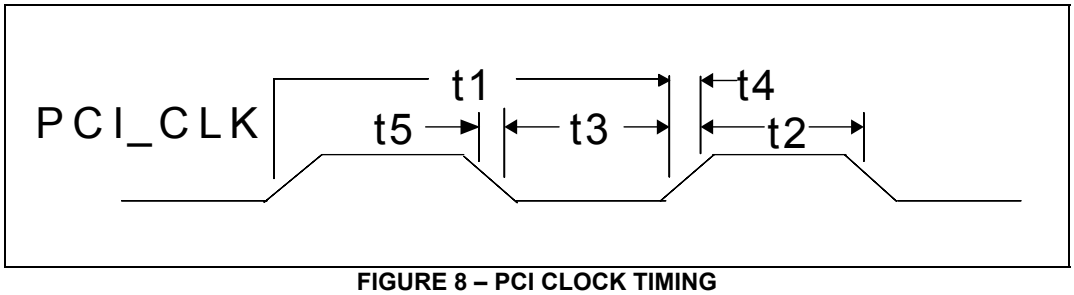


FIGURE 8 – PCI CLOCK TIMING

NAME	DESCRIPTION	MIN	TYP	MAX	UNITS
t1	Period	30		33.3	nsec
t2	High Time	12			nsec
t3	Low Time	12			nsec
t4	Rise Time			3	nsec
t5	Fall Time			3	nsec

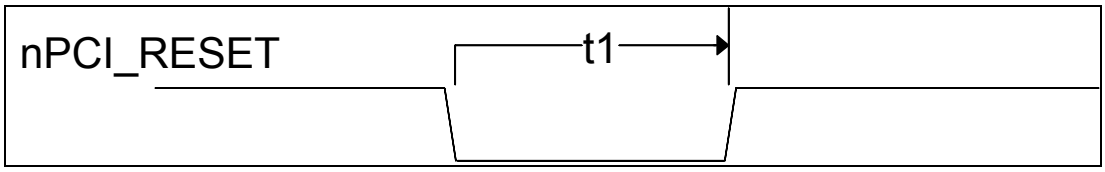


FIGURE 9 - RESET TIMING

NAME	DESCRIPTION	MIN	TYP	MAX	UNITS
t1	nPCI_RESET width	1			ms

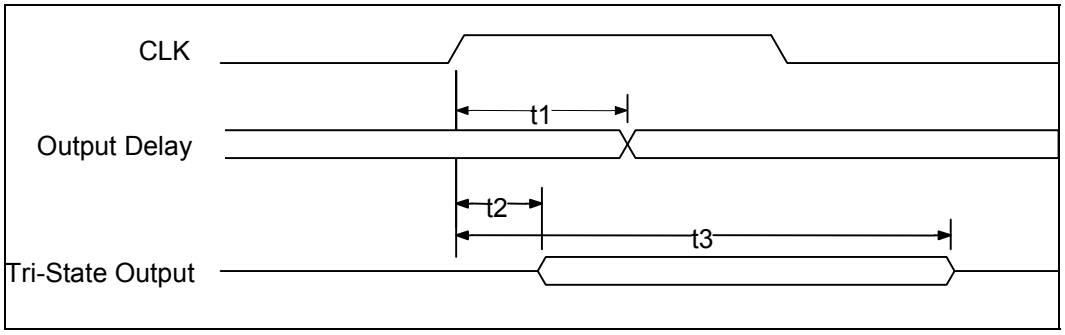


FIGURE 10 – OUTPUT TIMING MEASUREMENT CONDITIONS, LPC SIGNALS

NAME	DESCRIPTION	MIN	TYP	MAX	UNITS
t1	CLK to Signal Valid Delay – Bused Signals	2		11	ns
t2	Float to Active Delay	2		11	ns
t3	Active to Float Delay			28	ns

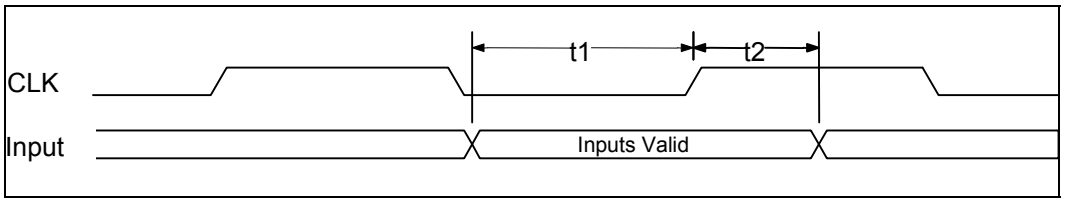
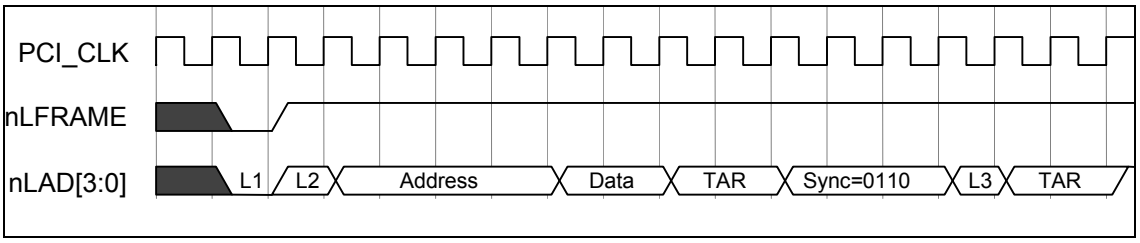


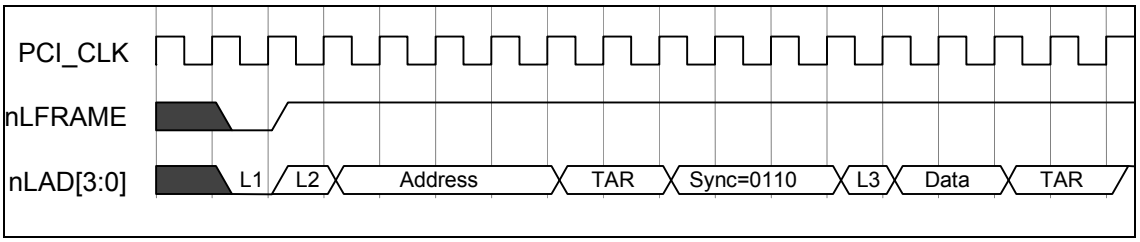
FIGURE 11 – INPUT TIMING MEASUREMENT CONDITIONS, LPC SIGNALS

NAME	DESCRIPTION	MIN	TYP	MAX	UNITS
t1	Input Set Up Time to CLK – Bused Signals	7			ns
t2	Input Hold Time from CLK	0			ns



Note: L1=Start; L2=CYCTYP+DIR; L3=Sync of 0000

FIGURE 12 – I/O WRITE



Note: L1=Start; L2=CYCTYP+DIR; L3=Sync of 0000

FIGURE 13 – I/O READ

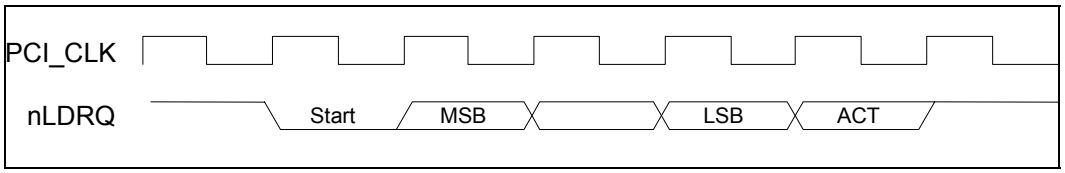
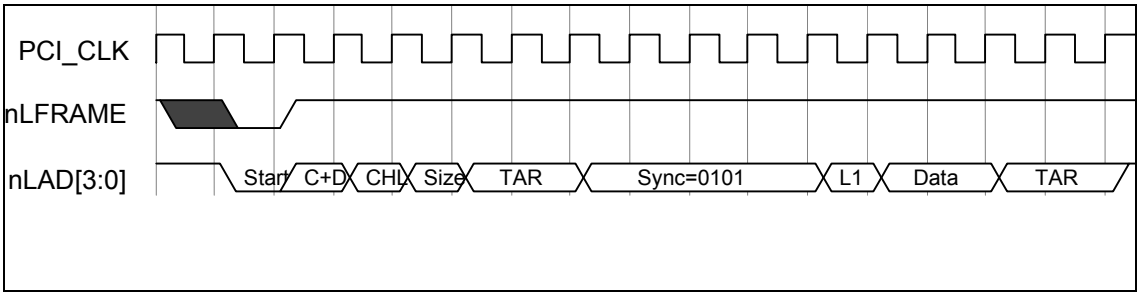
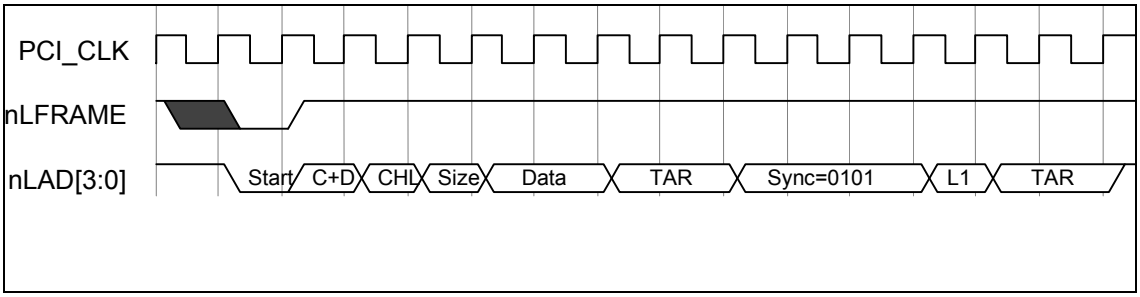


FIGURE 14 – DMA REQUEST ASSERTION THROUGH nLDRQ



Note: L1=Sync of 0000

FIGURE 15 – DMA WRITE (FIRST BYTE)



Note: L1=Sync of 0000

FIGURE 16 – DMA READ (FIRST BYTE)

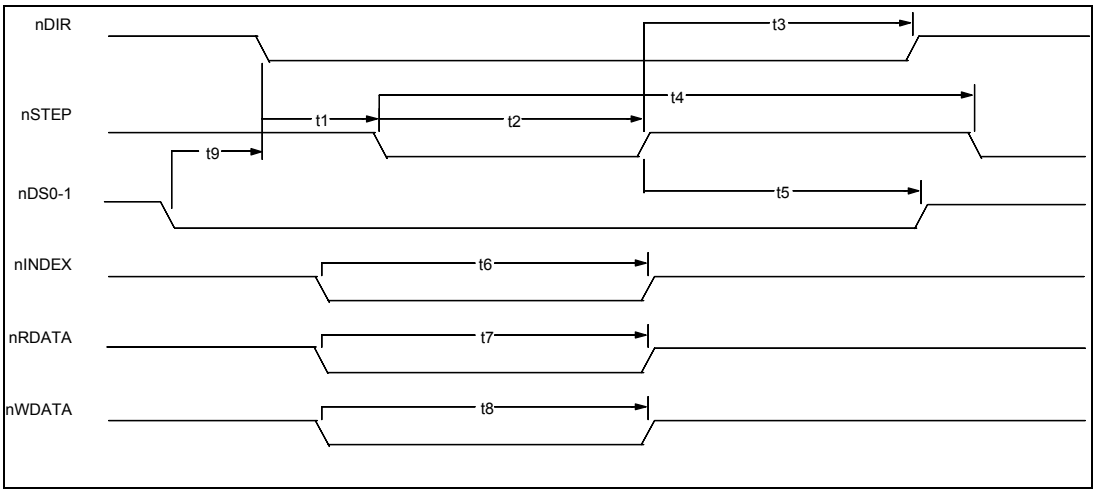


FIGURE 17 – FLOPPY DISK DRIVE TIMING (AT MODE ONLY)

NAME	DESCRIPTION	MIN	TYP	MAX	UNITS
t1	nDIR Set Up to STEP Low		4		X*
t2	nSTEP Active Time Low		24		X*
t3	nDIR Hold Time after nSTEP		96		X*
t4	nSTEP Cycle Time		132		X*
t5	nDS0-1 Hold Time from nSTEP Low (Note)		20		X*
t6	nINDEX Pulse Width		2		X*
t7	nRDATA Active Time Low		40		ns
t8	nWDATA Write Data Width Low		.5		Y*
t9	nDS0-1, Setup Time nDIR Low (Note)	0			ns

*X specifies one MCLK period and Y specifies one WCLK period.
MCLK = 16 x Data Rate (at 500 kb/s MCLK = 8 MHz)
WCLK = 2 x Data Rate (at 500 kb/s WCLK = 1 MHz)
Note: The nDS0-1 setup and hold times must be met by software.

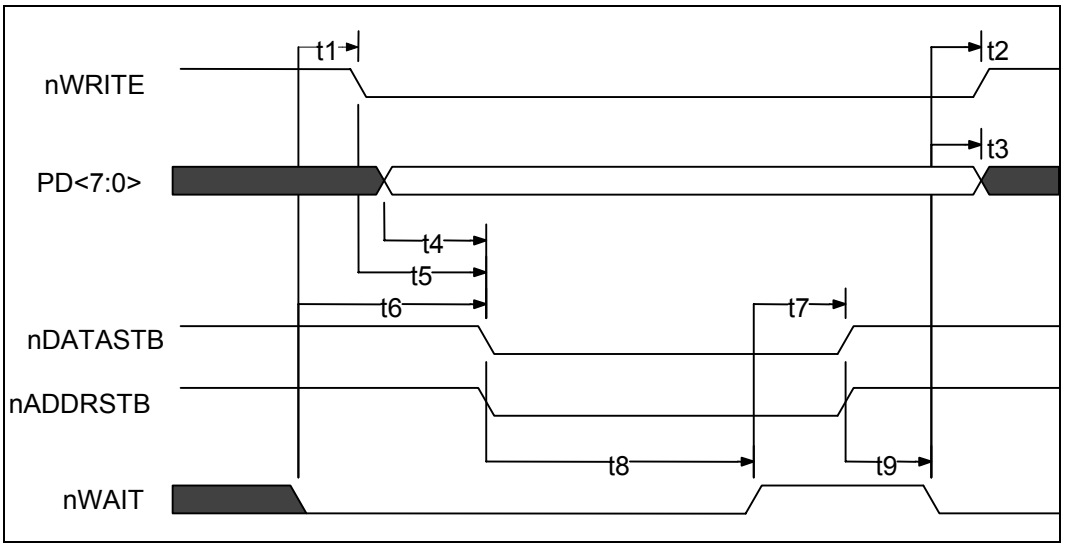


FIGURE 18 – EPP 1.9 DATA OR ADDRESS WRITE CYCLE

NAME	DESCRIPTION	MIN	TYP	MAX	UNITS
t1	nWAIT Asserted to nWRITE Asserted (Note 1)	60		185	ns
t2	nWAIT Asserted to nWRITE Change (Note 1)	60		185	ns
t3	nWAIT Asserted to PDATA Invalid (Note 1)	0			ns
t4	PDATA Valid to Command Asserted	10			ns
t5	nWRITE to Command Asserted	5		35	ns
t6	nWAIT Asserted to Command Asserted (Note 1)	60		210	ns
t7	nWAIT Deasserted to Command Deasserted (Note 1)	60		190	ns
t8	Command Asserted to nWAIT Deasserted	0		10	μs
t9	Command Deasserted to nWAIT Asserted	0			ns

Note 1: nWAIT must be filtered to compensate for ringing on the parallel bus cable. WAIT is considered to have settled after it does not transition for a minimum of 50 nsec.

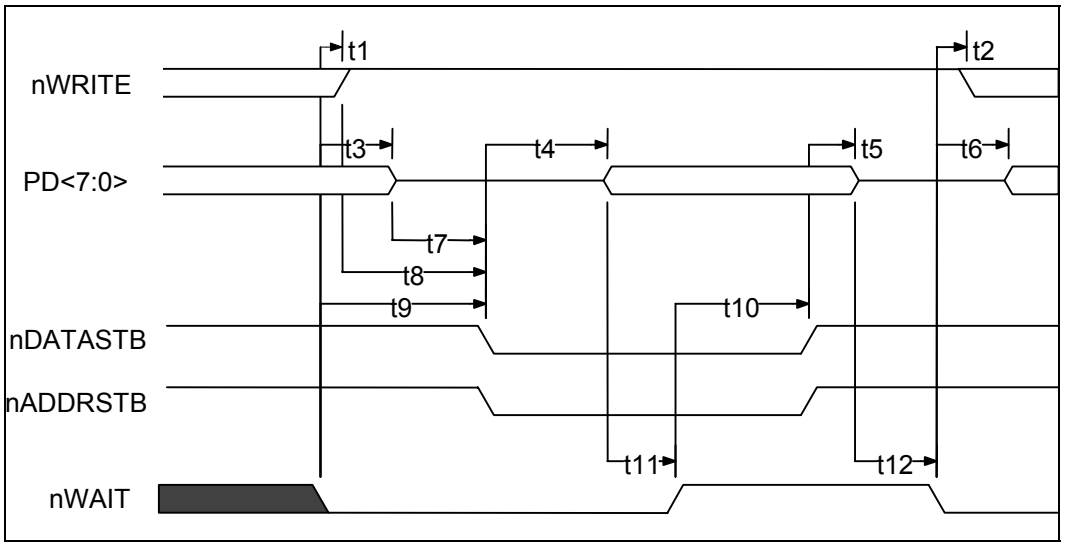


FIGURE 19 – EPP 1.9 DATA OR ADDRESS READ CYCLE

NAME	DESCRIPTION	MIN	TYP	MAX	UNITS
t1	nWAIT Asserted to nWRITE Deasserted	0		185	ns
t2	nWAIT Asserted to nWRITE Modified (Notes 1,2)	60		190	ns
t3	nWAIT Asserted to PDATA Hi-Z (Note 1)	60		180	ns
t4	Command Asserted to PDATA Valid	0			ns
t5	Command Deasserted to PDATA Hi-Z	0			ns
t6	nWAIT Asserted to PDATA Driven (Note 1)	60		190	ns
t7	PDATA Hi-Z to Command Asserted	0		30	ns
t8	nWRITE Deasserted to Command	1			ns
t9	nWAIT Asserted to Command Asserted	0		195	ns
t10	nWAIT Deasserted to Command Deasserted (Note 1)	60		180	ns
t11	PDATA Valid to nWAIT Deasserted	0			ns
t12	PDATA Hi-Z to nWAIT Asserted	0			µs

Note 1: nWAIT is considered to have settled after it does not transition for a minimum of 50 ns.
Note 2: When not executing a write cycle, EPP nWRITE is inactive high.

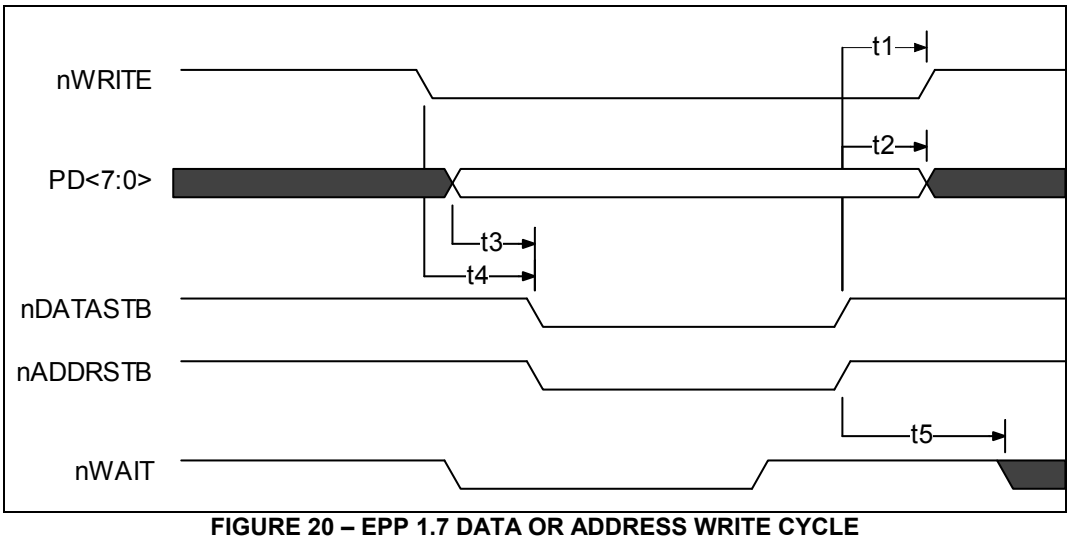


FIGURE 20 – EPP 1.7 DATA OR ADDRESS WRITE CYCLE

NAME	DESCRIPTION	MIN	TYP	MAX	UNITS
t1	Command Deasserted to nWRITE Change	0		40	ns
t2	Command Deasserted to PDATA Invalid	50			ns
t3	PDATA Valid to Command Asserted	10		35	ns
t4	nWRITE to Command	5		35	ns
t5	Command Deasserted to nWAIT Deasserted	0			ns

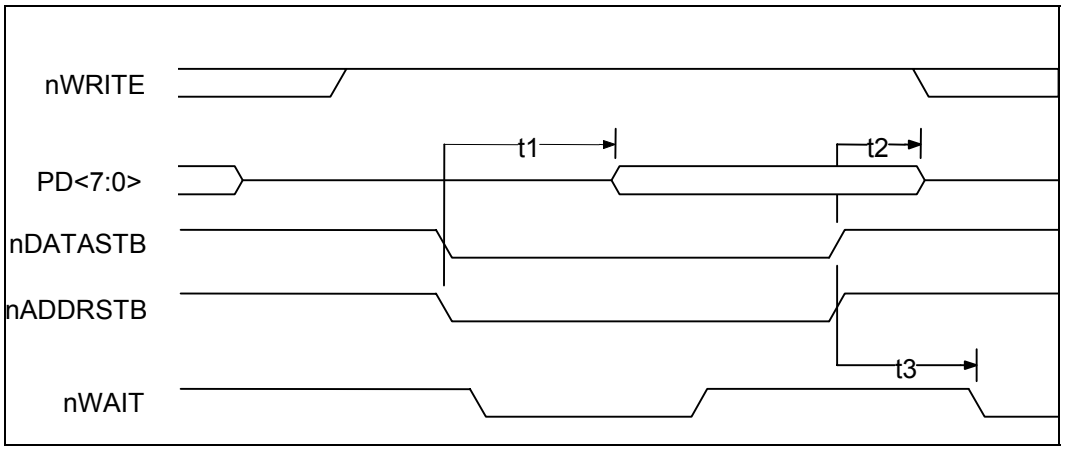


FIGURE 21 – EPP 1.7 DATA OR ADDRESS READ CYCLE

NAME	DESCRIPTION	MIN	TYP	MAX	UNITS
t1	Command Asserted to PDATA Valid	0			ns
t2	Command Deasserted to PDATA Hi-Z	0			ns
t3	Command Deasserted to nWAIT Deasserted	0			ns

Parallel Port FIFO (Mode 101)

The standard parallel port is run at or near the peak 500KBytes/sec allowed in the forward direction using DMA. The state machine does not examine nACK and begins the next transfer based on Busy. Refer to FIGURE 22.

ECP Parallel Port Timing

The timing is designed to allow operation at approximately 2.0 Mbytes/sec over a 15ft cable. If a shorter cable is used then the bandwidth will increase.

Forward-Idle

When the host has no data to send it keeps HostClk (nStrobe) high and the peripheral will leave PeriphClk (Busy) low.

Forward Data Transfer Phase

The interface transfers data and commands from the host to the peripheral using an interlocked PeriphAck and HostClk. The peripheral may indicate its desire to send data to the host by asserting nPeriphRequest.

The Forward Data Transfer Phase may be entered from the Forward-Idle Phase. While in the Forward Phase the peripheral may asynchronously assert the nPeriphRequest (nFault) to request that the channel be reversed. When the peripheral is not busy it sets PeriphAck (Busy) low. The host then sets HostClk (nStrobe) low when it is prepared to send data. The data must be stable for the specified setup time prior to the falling edge of HostClk. The peripheral then sets PeriphAck (Busy) high to acknowledge the handshake. The host then sets HostClk (nStrobe) high. The peripheral then accepts the data and sets PeriphAck (Busy) low, completing the transfer. This sequence is shown in FIGURE 23.

The timing is designed to provide 3 cable round-trip times for data setup if Data is driven simultaneously with HostClk (nStrobe).

Reverse-Idle Phase

The peripheral has no data to send and keeps PeriphClk high. The host is idle and keeps HostAck low.

Reverse Data Transfer Phase

The interface transfers data and commands from the peripheral to the host using an interlocked HostAck and PeriphClk.

The Reverse Data Transfer Phase may be entered from the Reverse-Idle Phase. After the previous byte has beed accepted the host sets HostAck (nALF) low. The peripheral then sets PeriphClk (nACK) low when it has data to send. The data must be stable for the specified setup time prior to the falling edge of PeriphClk. When the host is ready to accept a byte it sets HostAck (nALF) high to acknowledge the handshake. The peripheral then sets PeriphClk (nACK) high. After the host has accepted the data it sets HostAck (nALF) low, completing the transfer. This sequence is shown in FIGURE 24.

Output Drivers

To facilitate higher performance data transfer, the use of balanced CMOS active drivers for critical signals (Data, HostAck, HostClk, PeriphAck, PeriphClk) are used in ECP Mode. Because the use of active drivers can present compatibility problems in Compatible Mode (the control signals, by tradition, are specified as open-collector), the drivers are dynamically changed from open-collector to totem-pole. The timing for the dynamic driver change is specified in then IEEE 1284 Extended Capabilities Port Protocol and ISA Interface Standard, Rev. 1.14, July 14, 1993, available from Microsoft. The dynamic driver change must be implemented properly to prevent glitching the outputs.

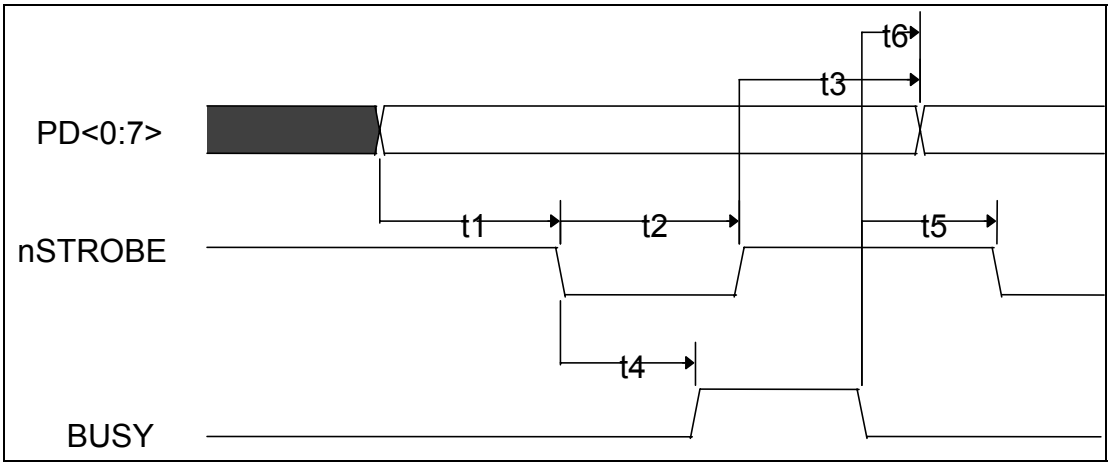


FIGURE 22 – PARALLEL PORT FIFO TIMING

NAME	DESCRIPTION	MIN	TYP	MAX	UNITS
t1	PDATA Valid to nSTROBE Active	600			ns
t2	nSTROBE Active Pulse Width	600			ns
t3	PDATA Hold from nSTROBE Inactive (Note 1)	450			ns
t4	nSTROBE Active to BUSY Active			500	ns
t5	BUSY Inactive to nSTROBE Active	680			ns
t6	BUSY Inactive to PDATA Invalid (Note 1)	80			ns

Note 1: The data is held until BUSY goes inactive or for time t3, whichever is longer. This only applies if another data transfer is pending. If no other data transfer is pending, the data is held indefinitely.

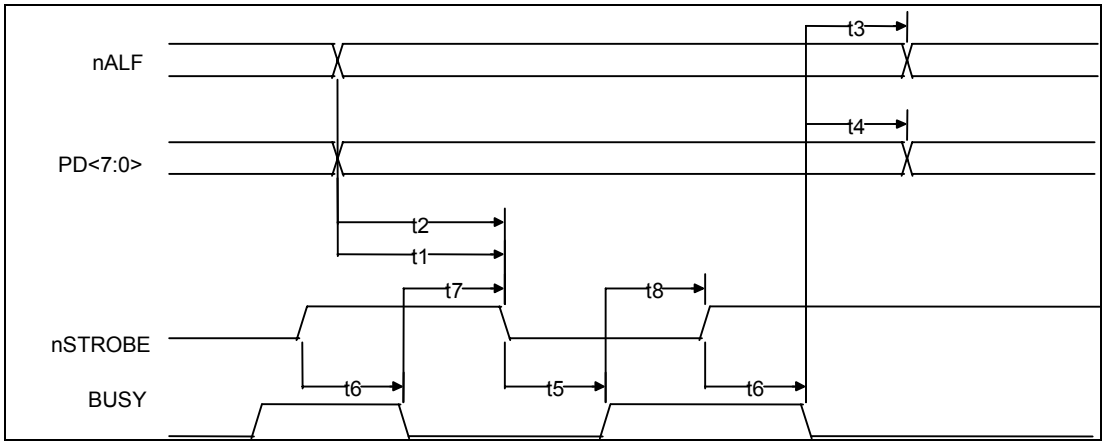


FIGURE 23 - ECP PARALLEL PORT FORWARD TIMING

NAME	DESCRIPTION	MIN	TYP	MAX	UNITS
t1	nALF Valid to nSTROBE Asserted	0		60	ns
t2	PDATA Valid to nSTROBE Asserted	0		60	ns
t3	BUSY Deasserted to nALF Changed (Notes 1,2)	80		180	ns
t4	BUSY Deasserted to PDATA Changed (Notes 1,2)	80		180	ns
t5	nSTROBE Asserted to Busy Asserted	0			ns
t6	nSTROBE Deasserted to Busy Deasserted	0			ns
t7	BUSY Deasserted to nSTROBE Asserted (Notes 1,2)	80		200	ns
t8	BUSY Asserted to nSTROBE Deasserted (Note 2)	80		180	ns

Note 1: Maximum value only applies if there is data in the FIFO waiting to be written out.
Note 2: BUSY is not considered asserted or deasserted until it is stable for a minimum of 75 to 130 ns.

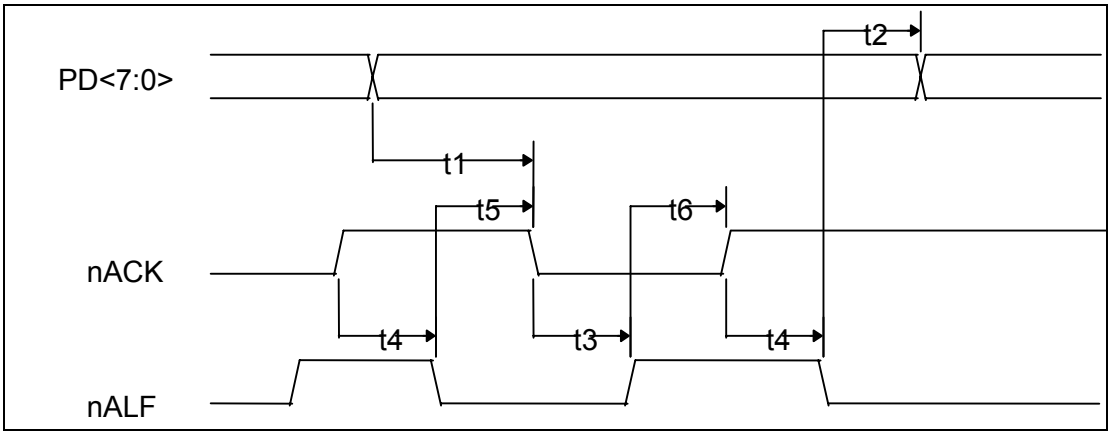
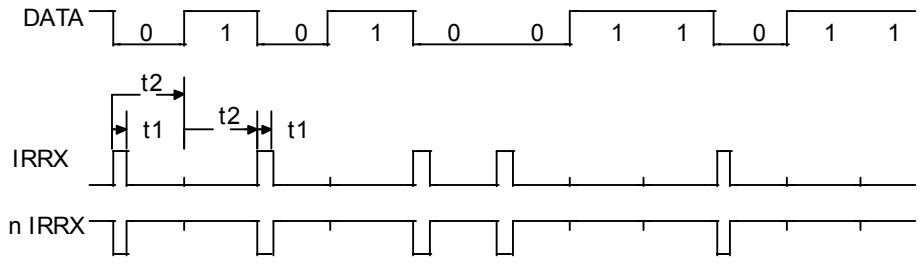


FIGURE 24 - ECP PARALLEL PORT REVERSE TIMING

NAME	DESCRIPTION	MIN	TYP	MAX	UNITS
t1	PDATA Valid to nACK Asserted	0			ns
t2	nALF Deasserted to PDATA Changed	0			ns
t3	nACK Asserted to nALF Deasserted (Notes 1,2)	80		200	ns
t4	nACK Deasserted to nALF Asserted (Note 2)	80		200	ns
t5	nALF Asserted to nACK Asserted	0			ns
t6	nALF Deasserted to nACK Deasserted	0			ns

Note 1: Maximum value only applies if there is room in the FIFO and terminal count has not been received. ECP can stall by keeping nALF low.

Note 2: nACK is not considered asserted or deasserted until it is stable for a minimum of 75 to 130 ns.

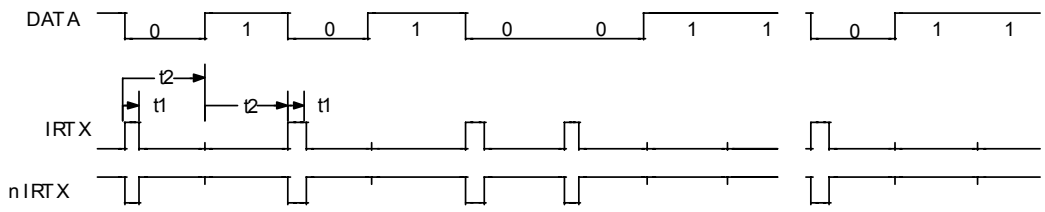


	Parameter	min	typ	max	units
t1	Pulse Width at 115kbaud	1.4	1.6	2.71	µs
t1	Pulse Width at 57.6kbaud	1.4	3.22	3.69	µs
t1	Pulse Width at 38.4kbaud	1.4	4.8	5.53	µs
t1	Pulse Width at 19.2kbaud	1.4	9.7	11.07	µs
t1	Pulse Width at 9.6kbaud	1.4	19.5	22.13	µs
t1	Pulse Width at 4.8kbaud	1.4	39	44.27	µs
t1	Pulse Width at 2.4kbaud	1.4	78	88.55	µs
t2	Bit Time at 115kbaud		8.68		µs
t2	Bit Time at 57.6kbaud		17.4		µs
t2	Bit Time at 38.4kbaud		26		µs
t2	Bit Time at 19.2kbaud		52		µs
t2	Bit Time at 9.6kbaud		104		µs
t2	Bit Time at 4.8kbaud		208		µs
t2	Bit Time at 2.4kbaud		416		µs

Notes:

1. Receive Pulse Detection Criteria: A received pulse is considered detected if the received pulse is a minimum of 1.41µs.
2. IRRX: L5, CRF1 Bit 0 = 1
   nIRRX: L5, CRF1 Bit 0 = 0 (default)

FIGURE 25 - IrDA RECEIVE TIMING

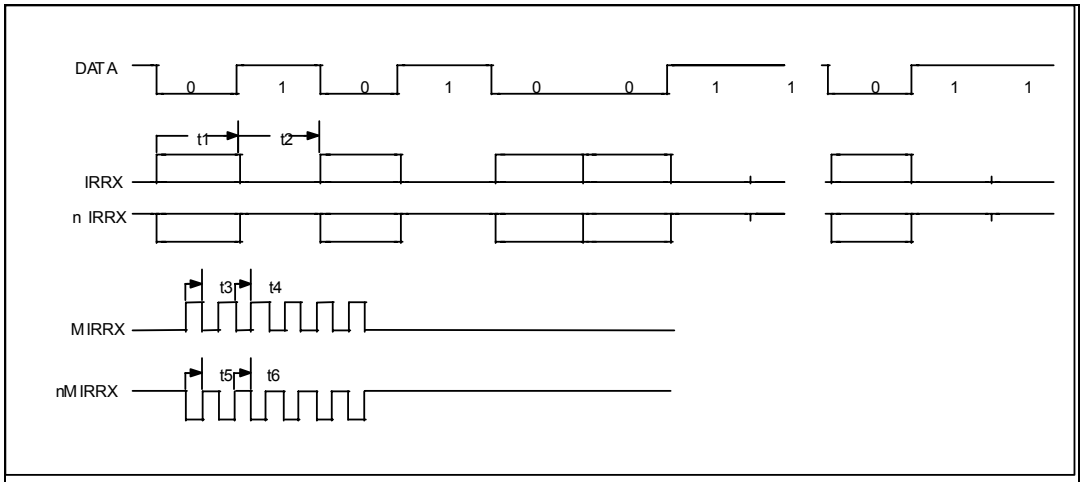


	Parameter	min	typ	max	units
t1	Pulse Width at 115kbaud	1.41	1.6	2.71	µs
t1	Pulse Width at 57.6kbaud	1.41	3.22	3.69	µs
t1	Pulse Width at 38.4kbaud	1.41	4.8	5.53	µs
t1	Pulse Width at 19.2kbaud	1.41	9.7	11.07	µs
t1	Pulse Width at 9.6kbaud	1.41	19.5	22.13	µs
t1	Pulse Width at 4.8kbaud	1.41	39	44.27	µs
t1	Pulse Width at 2.4kbaud	1.41	78	88.55	µs
t2	Bit Time at 115kbaud		8.68		µs
t2	Bit Time at 57.6kbaud		17.4		µs
t2	Bit Time at 38.4kbaud		26		µs
t2	Bit Time at 19.2kbaud		52		µs
t2	Bit Time at 9.6kbaud		104		µs
t2	Bit Time at 4.8kbaud		208		µs
t2	Bit Time at 2.4kbaud		416		µs

Notes:

1. IrDA @ 115k is HPSIR compatible. IrDA @ 2400 will allow compatibility with HP95LX and 48SX.
2. IRTX: L5, CRF1 Bit 1 = 1 (default)
   nIRTX: L5, CRF1 Bit 1 = 0

FIGURE 26 - IRDA TRANSMIT TIMING

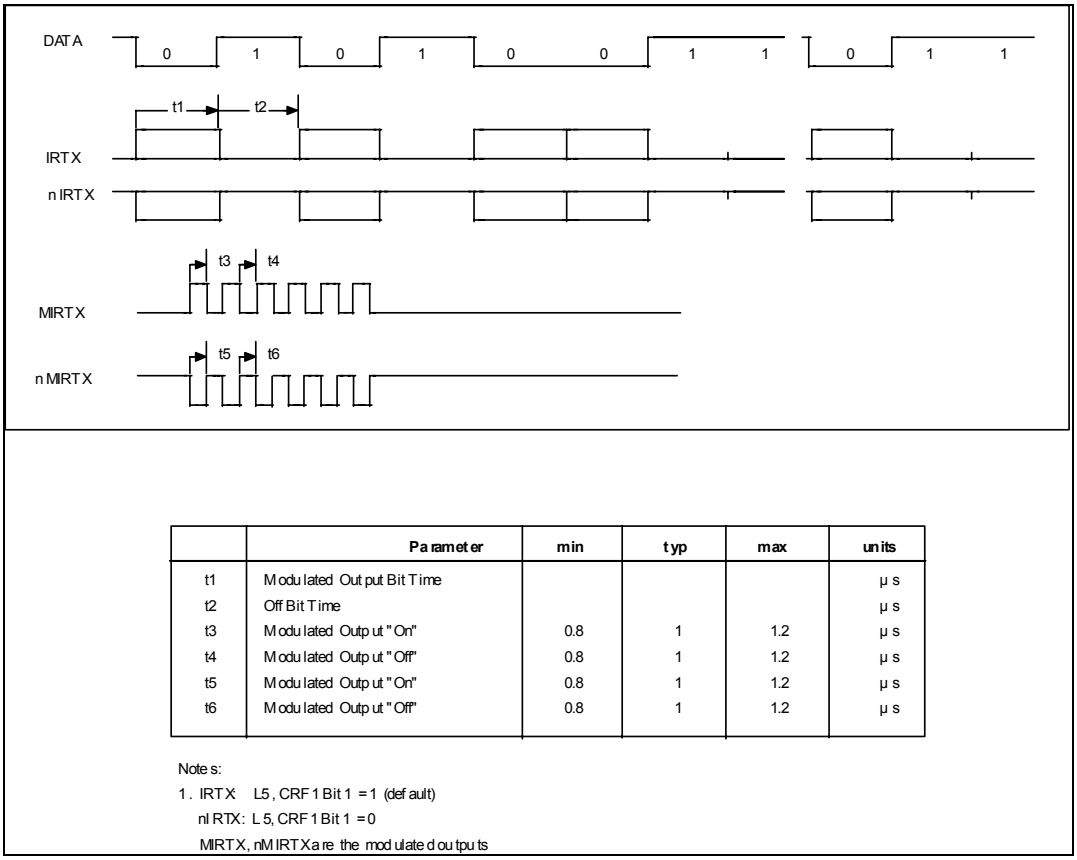


	Parameter	min	typ	max	units
t1	Modulated Output Bit Time				µs
t2	Off Bit Time				µs
t3	Modulated Output "On"	0.8	1	1.2	µs
t4	Modulated Output "Off"	0.8	1	1.2	µs
t5	Modulated Output "On"	0.8	1	1.2	µs
t6	Modulated Output "Off"	0.8	1	1.2	µs

Notes:

1. IRRX: L5, CRF1 Bit 0 = 1
   nIRRX: L5, CRF1 Bit 0 = 0 (default)
   MIRRX, nMIRRX are the modulated outputs

FIGURE 27 – AMPLITUDE SHIFT KEYED IR RECEIVE TIMING



	Parameter	min	typ	max	units
t1	Modulated Output Bit Time				µs
t2	Off Bit Time				µs
t3	Modulated Output "On"	0.8	1	1.2	µs
t4	Modulated Output "Off"	0.8	1	1.2	µs
t5	Modulated Output "On"	0.8	1	1.2	µs
t6	Modulated Output "Off"	0.8	1	1.2	µs

Notes:

1. IRTX: L5, CRF1 Bit 1 = 1 (default)
   nIRTX: L5, CRF1 Bit 1 = 0
   MIRTX, nMIRTX are the modulated outputs

FIGURE 28 – AMPLITUDE SHIFT KEYED IR TRANSMIT TIMING

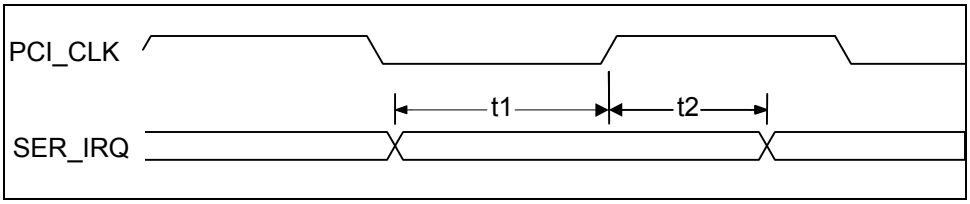


FIGURE 29 – SETUP AND HOLD TIME

NAME	DESCRIPTION	MIN	TYP	MAX	UNITS
t1	SER_IRQ Setup Time to PCI_CLK Rising	7			nsec
t2	SER_IRQ Hold Time to PCI_CLK Rising	0			nsec

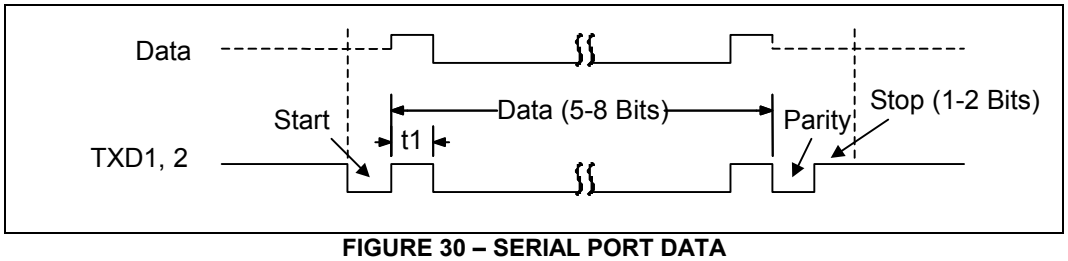


FIGURE 30 – SERIAL PORT DATA

NAME	DESCRIPTION	MIN	TYP	MAX	UNITS
t1	Serial Port Data Bit Time		t_{BR} [1]		nsec

Note 1: t_{BR} is 1/Baud Rate. The Baud Rate is programmed through the divisor latch registers. Baud Rates have percentage errors indicated in the “Baud Rate” table in the “Serial Port” section.

PACKAGE OUTLINES

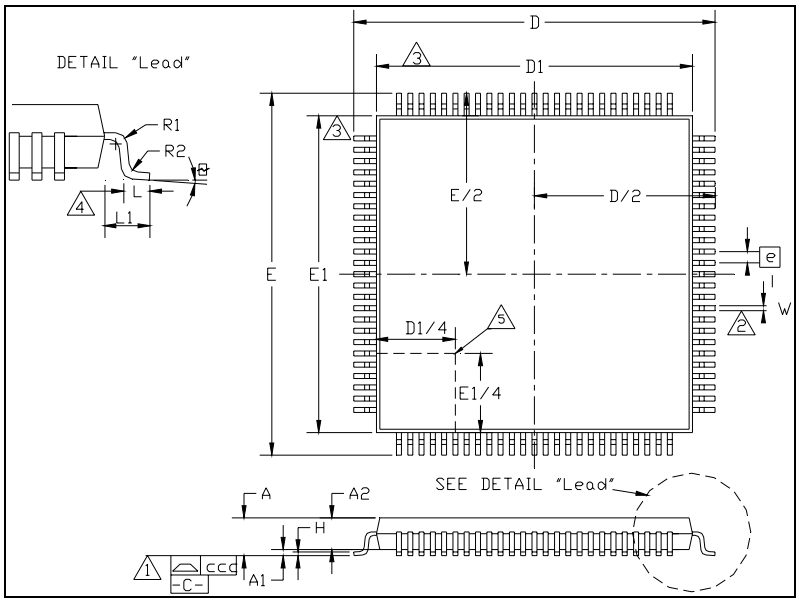


FIGURE 31 – 100 PIN TQFP and 100 PIN TQN (LEAD-FREE) PACKAGE OUTLINE

	MIN	***NOMINAL***	***MAX***	***REMARK***
A	*~*	*~*	*1.60*	*Overall Package Height*
A1	*0.05*	*~*	*~*	*Standoff*
A2	*1.35*	*1.40*	*1.45*	*Body Thickness*
D	*15.80*	*16.00*	*16.20*	*X Span*
D/2	*7.90*	*8.00*	*8.10*	*$^1/_2$ X Span Measure from Centerline*
D1	*13.90*	*14.00*	*14.10*	*X body Size*
E	*15.80*	*16.00*	*16.20*	*Y Span*
E/2	*7.90*	*8.00*	*8.10*	*$^1/_2$ Y Span Measure from Centerline*
E1	*13.90*	*14.00*	*14.10*	*Y body Size*
H	*~*	*~*	*0.20*	*Lead Frame Thickness*
L	*0.45*	*0.60*	*0.75*	*Lead Foot Length from Centerline*
L1	*~*	*1.00*	*~*	*Lead Length*
e		*0.50 Basic*		*Lead Pitch*
θ	*0°*	*~*	*8°*	*Lead Foot Angle*
W	*~*	*0.25*	*~*	*Lead Width*
R1	*~*	*0.20*	*~*	*Lead Shoulder Radius*
R2	*~*	*0.20*	*~*	*Lead Foot Radius*
ccc	~	~	0.0762	Coplanarity *(Assemblers)*
ccc	~	~	0.08	Coplanarity *(Test House)*

Notes:

[1] Controlling Unit: millimeter

[2] Tolerance on the position of the leads is ± 0.04 mm maximum.

[3] Package body dimensions D1 and E1 do not include the mold protrusion.
Maximum mold protrusion is 0.25 mm.

[4] Dimension for foot length L measured at the gauge plane 0.25 mm above the seating plane is 0.78-1.08 mm.

[5] Details of pin 1 identifier are optional but must be located within the zone indicated.

[6] Shoulder widths must conform to JEDEC MS-026 dimension 'S' of a minimum of 0.20mm.

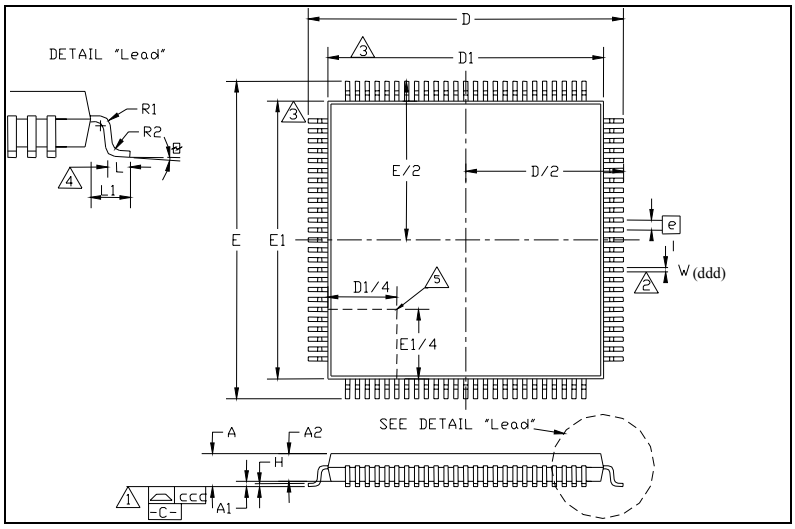


FIGURE 32 – 100 PIN STQFP and 100 PIN STQN (LEAD-FREE) PACKAGE OUTLINE

	MIN	***NOMINAL***	***MAX***	***REMARK***
A	~	~	*1.60*	*Overall Package Height*
A1	*0.05*	~	*0.15*	*Standoff*
A2	*1.35*	*1.40*	*1.45*	*Body Thickness*
D	*13.80*	*14.00*	*14.20*	*X Span*
D/2	*6.90*	*7.00*	*7.10*	*$^1/_2$ X Span Measure from Centerline*
D1	*11.80*	*12.00*	*12.20*	*X body Size*
E	*13.80*	*14.00*	*14.20*	*Y Span*
E/2	*6.90*	*7.00*	*7.10*	*$^1/_2$ Y Span Measure from Centerline*
E1	*11.80*	*12.00*	*12.20*	*Y body Size*
H	0.09	~	0.20	Lead Frame Thickness
L	0.45	0.60	0.75	Lead Foot Length from Centerline
L1	~	1.00	~	Lead Length
e		0.40 Basic		Lead Pitch
θ	0°	3.5°	7°	Lead Foot Angle
W	0.13	0.16	0.23	Lead Width
R1	0.08	~	~	Lead Shoulder Radius
R2	0.08	~	0.20	Lead Foot Radius
ccc	~	~	.0762	Coplanarity *(Assemblers)*
ccc	~	~	0.08	Coplanarity *(Test House)*
ddd	~	~	0.035	True Position Spread (Bent Leads)

Notes:

[1] *Controlling Unit: millimeter*

[2] *Minimum space between protrusion and an adjacent lead is .007 mm.*

[3] *Details of pin 1 identifier are optional but must be located within the zone indicated.*

[4] *Dimension for foot length L measured at the gauge plane 0.25 mm above the seating plane.*

[5] *Shoulder widths must conform to JEDEC MS-026 dimension 'S' of a minimum of 0.20mm.*

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