Description

The IPS2550 is a magnet-free, inductive position sensor IC that can be used for high-speed absolute position sensing in automotive, industrial, medical, and consumer applications. The IPS2550 uses the physical principle of eddy currents to detect the position of a simple metallic target that is moving above a set of coils, consisting of one transmitter coil and two receiver coils.

The three coils are typically printed as copper traces on a printed circuit board (PCB). They are arranged such that the transmitter coil induces a secondary voltage in the two receiver coils, which depends on the position of the metallic target above the coils.

A signal representative of the target's position over the coils is obtained by demodulating and processing the secondary voltages from the receiver coils. The target can be any kind of metal, such as aluminum, steel, or a PCB with a printed copper layer.

The IPS2550 provides two independent output interfaces:

- A high-speed analog interface providing position information in the form of demodulated analog sine/cosine raw data
- An I2C digital interface for diagnostics and programming

The IPS2550 operates at rotation speeds up to 600000 RPM (relating to coil designs using 1 period per turn). An ultra-low propagation delay of 4µs provides high dynamic control for fast spinning motors.

The IPS2550 has been developed according to ISO26262 for implementation in safety-relevant systems up to ASIL C. It can also be used in ASIL D system-level requirements according to ASIL Decomposition rules (i.e. ISO 26262:2018, Part 9, Clause 5") or proper risk analysis by the system integrator.

The IPS2550 is available in a 16-pin exposed pad TSSOP package and qualified for automotive use at -40°C to +160°C ambient temperature.

Available Support

Renesas provides reference designs that demonstrate IPS2550 rotary position sensing applications.

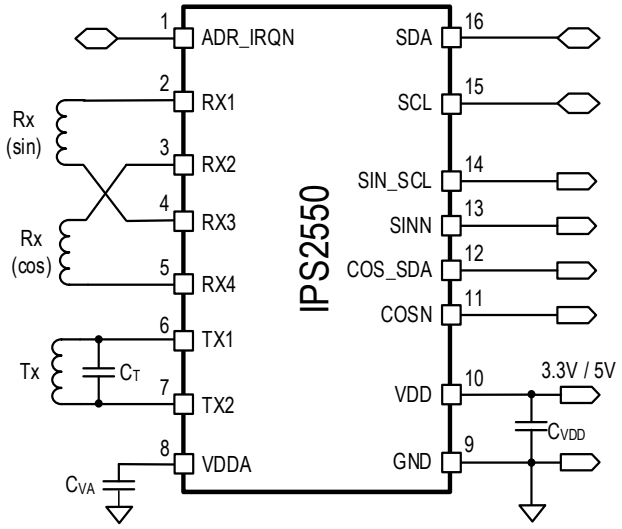
Typical Applications

- Rotor position detection for brushless DC motors; adaptable to any pole pair count
- Replacement of resolvers

Features

- Position sensing based on an inductive principle
- Cost-effective; no magnet required
- Immune to magnetic stray fields; no shielding required
- Suitable for harsh environments and extreme temperatures
- Differential and single-ended sine and cosine outputs
- Automatic gain control with programmable limits
- Nonvolatile user-configurable memory, programmable via I2C interface
- Programmable through analog or digital interface
- Single IC supports on-axis and off-axis rotation, linear motion, and arc motion sensing
- Adaptable to any full-scale angle range through coil design
- High accuracy: ≤ 0.1% full scale (with ideal coils)
- Rotation sensing up to a 360º angle range
- Over-voltage and reverse-polarity protection: ±18V on both supply and output pins
- Facilitates redundant design requirements
- Suitable for implementation in safety-related systems compliant to ISO26262 up to ASIL-C on a single IC and ASIL-D on dual ICs
- Fast diagnostic alarm via interrupt pin
- Wide operation temperature: -40 C up to +160°C
- Supply voltage programmable for 3.3V±0.3V or 5.0V±0.5V
- Small 16-TSSOP exposed pad package (4.4mm ×5.0mm)

Application Circuit Example



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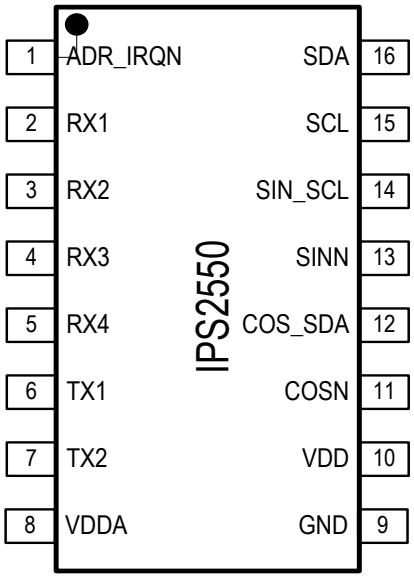
1. Pin Assignments

The IPS2550 is available in a 16-TSSOP 4.4mm × 5.0mm RoHS package with exposed pad RoHS package. It is qualified for an ambient temperature of -40°C to +160°C.

Figure 1. Pin Assignments for 16-TSSOP Package – Top View



2. Pin Descriptions

Table 1. Pin Descriptions

Pin Number	Name	Type	Description	
1	ADR_IRQN	Digital Input/Output	Address-select digital input for I2C interface address selection; push/pull interrupt output (programmable options, see Table 3). Use the pull-up or pull-down resistor R_{ADR} to define the I2C address, see Table 14.	
2	RX1	Analog Input	ASIL-C Configuration Mode (default) : receiver coil 1 (Sine, see Figure 2)	Compatibility Mode: receiver coil 1 (Sine, see Figure 3)
3	RX2		ASIL-C Configuration Mode (default): receiver coil 2 (Cosine, see Figure 2)	Compatibility Mode: receiver coil 1 (inverted sine, see Figure 3)
4	RX3		ASIL-C Configuration Mode (default): receiver coil 1 (inverted sine, see Figure 2)	Compatibility Mode: receiver coil 2 (Cosine, see Figure 3)
5	RX4		ASIL-C Configuration Mode (default): receiver coil 2 (inverted cosine, see Figure 2)	Compatibility Mode: receiver coil 2 (inverted cosine, see Figure 3)
6	TX1	Analog Input/Output	Connect the transmitter coil between the TX1 and TX2 pins. The resonant frequency is adjusted with capacitors C_{Tx1} from TX1 to GND and C_{Tx2} from TX2 to GND as shown in Figure 2 and Figure 3. C_{Tx1} and C_{Tx2} must have the same capacitance value. They can be calculated with Equation 3.	
7	TX2			

Pin Number	Name	Type	Description
8	VDDA	Supply	Internally regulated analog voltage supply, depending on selected VDD supply mode. Connect the capacitor C_{VA} to the GND pin (see Table 6). For 5V operation, see $VDDA_5$ in Table 8, for 3.3V operation, see $VDDA_3$ in Table 7.
9	GND	Supply	Common ground connection.
10	VDD	Supply	External supply voltage. Connect capacitor C_{VDD} to the GND pin (see Table 6).
11	COSN	Analog Output	Buffered analog output; see Table 2.
12	COS_SDA	Analog Output, Digital I/O	Buffered analog output; digital I2C data input/output during Programming Mode; see Table 2.
13	SINN	Analog Output	Buffered analog output; see Table 2.
14	SIN_SCL	Analog Output, Digital Input	Buffered analog output; digital I2C clock input during Programming Mode; see Table 2.
15	SCL	Digital Input	Clock input for digital programming and diagnostic I2C interface. Connect a pull-up resistor R_{SCL} to this pin, see Table 14.
16	SDA	Digital Input/Output	Open drain bi-directional data I/O line for digital programming and diagnostic I2C interface. Connect a pull-up resistor R_{SDA} to this pin, see Table 14.
	Exposed Pad	Heat sink	Heat sink only. It can be connected with short, direct connection to GND (pin #9), or left unconnected. Refer to Figure 4 for details. Do not connect the exposed pad to any other potential than GND.

Table 2. Output Configuration

Pin (See Figure 1)		Output Depending on Mode			Diagnostic State, Program Options			
Pin Number	Pin Name	Analog Differential	Analog Single-Ended	Programming	Disabled	Mode1	Mode2	Mode3
14	SIN_SCL	SIN	SIN	SCL	SIN	SIN	Hi-Z	Hi-Z
13	SINN	SINN	REF	Not used	SINN	Hi-Z	SINN	Hi-Z
12	COS_SDA	COS	COS	SDA	COS	COS	Hi-Z	Hi-Z
11	COSN	COSN	REF	Not used	COSN	Hi-Z	COSN	Hi-Z

[a] Abbreviations used in Table 2:

SIN: Sine channel output, bias voltage = VDD/2

SIN: Inverted sine channel output, bias voltage = VDD/2

COS: Cosine channel output, bias voltage = VDD/2

COSN: Inverted cosine channel output, bias voltage = VDD/2

REF: DC output bias voltage, VDD/2

SCL: Serial clock input for I2C programming

SDA: Serial bi-directional data I/O port for I2C programming

Hi-Z: Output is high ohmic; diagnostics are indicated by external pull-up or pull-down resistors

Table 3. Digital Interface Configuration

Pin (See Figure 1)		Input/Output Depending on Interface Mode [a]	
TSSOP Pin Number	Pin Name	I2C with Address Select	I2C with Interrupt
16	SDA	SDA	
15	SCL	SCL	
1	ADR_IRQN	ADR	IRQN

[a] Abbreviations used in Table 3:

ADR_IRQN: Combined address select input and interrupt output

ADR: Hardware address-select input for I2C Mode (two address options, depending on digital input level at the ADR_IRQN pin)

SDA: Serial bi-directional data I/O port for I2C Modes`

SCL: Serial clock input for I2C Modes

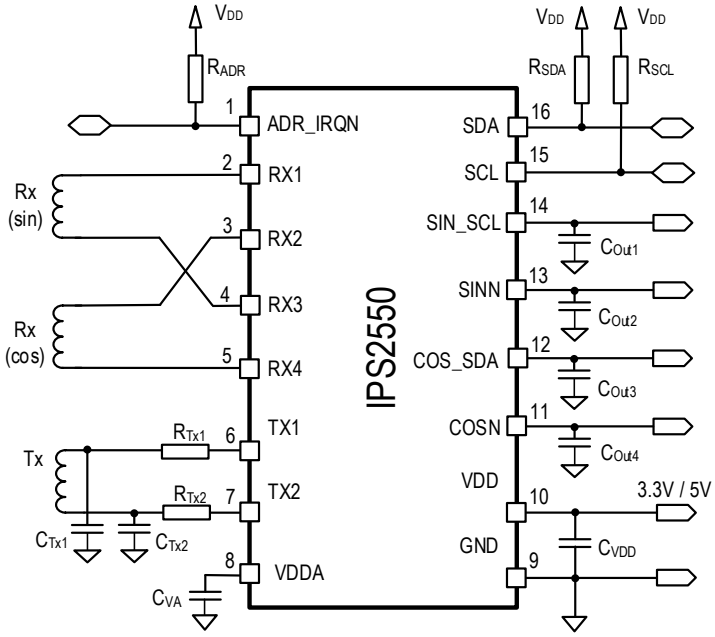
IRQN: Interrupt output

3. Receiver Coil Connection Options

The IPS2550 can be configured in two user-programmable modes related to the connection of the receiver coils:

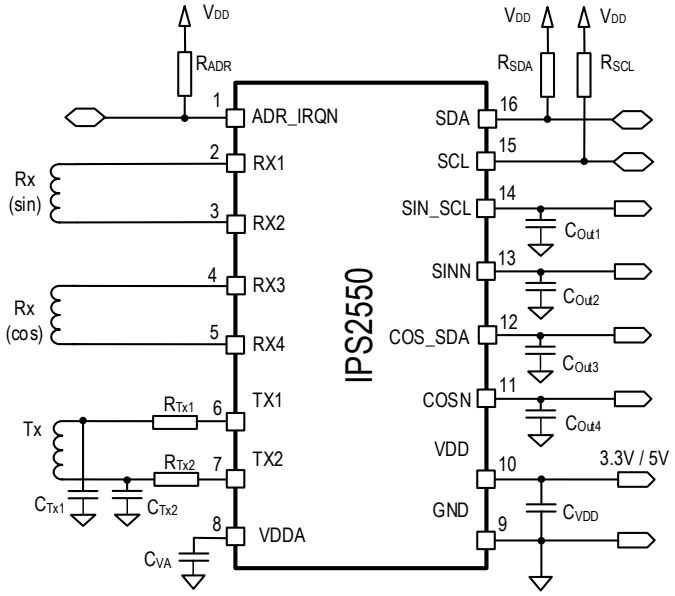
- The ASIL-C Configuration Mode (default) improves the failure detection rate of the chip because it avoids a short circuit of any receiver coil by a short between two neighboring pins.
- The Compatibility Mode (programming option) provides pin-to-pin compatibility with the IPS2200 inductive sensor IC.

Figure 2. LC Oscillator Connection in ASIL-C Configuration with Split TX Capacitors



Configuration in ASIL-C mode with split capacitors $C_{Tx1} = C_{Tx2}$, Tx coil series resistors $R_{Tx1} = R_{Tx2}$ and Output capacitors $C_{Out1} = C_{Out2} = C_{Out3} = C_{Out4}$ for improved EMC performance.

Figure 3. LC Oscillator Connection in Compatibility Mode Configuration with Split TX Capacitors



Configuration in compatibility mode with split capacitors C_{Tx1} = C_{Tx2}, Tx coil series resistors R_{Tx1} = R_{Tx2} and Output capacitors C_{Out1} = C_{Out2} = C_{Out3} = C_{Out4} for improved EMC performance.

The oscillator frequency is determined by the values of coil L and capacitors CTx1 and CTx2 as the following:

Oscillator frequency:

$$f_{TX} = \frac{1}{2\pi\sqrt{\frac{L \times C_{Tx1} \times C_{Tx2}}{C_{Tx1} + C_{Tx2}}}}$$ **Equation 1**

For C_{Tx1} = C_{Tx2} :

$$f_{TX} = \frac{1}{2\pi\sqrt{L\frac{C_{Tx1}}{2}}}$$ **Equation 2**

$$\mathrm{CTx1} = \mathrm{CTx2} = \frac{2}{L(2\pi f_{TX})^2}$$ **Equation 3**

Where:
f_{TX} = Oscillator frequency in MHz
L = Coil impedance in µHenry
C_{Tx1}, C_{Tx2} = Capacitance in µFarad

Note: R_{Tx1} = R_{Tx2} = 22Ohm (typical)

4. Absolute Maximum Ratings

The absolute maximum ratings are stress ratings only. Stresses greater than those listed below can cause permanent damage to the device. Functional operation of the IPS2550 at the absolute maximum ratings is not implied. Exposure to absolute maximum rating conditions could affect device reliability.

All voltage levels refer to GND.

Table 4. Absolute Maximum Ratings

Symbol	Parameter	Conditions	Minimum	Maximum	Units
V_{VDDmax}	External supply voltage	Continuous	-18	18	V
V_{OUT}	SIN_SCL, SINN,COS_SDA and COSN output voltage	Continuous	-18	18	V
V_{RX1}	Receiver coil pin: RX1		-12	12	V
V_{RX2}	Receiver coil pin: RX2				
V_{RX3}	Receiver coil pin: RX3				
V_{RX4}	Receiver coil pin: RX4				
$V_{DIGITAL}$	Digital IO pins: SCL, SDA, ADR_IRQN		-0.3	VDD+0.3	V
V_{Tx1_2}	Transmitter pins, TX1, TX2		-0.3	5.6	V
$V_{VDDAmax}$	VDDA internal LDO output	VDDA is internally regulated with external capacitor to GND. No other connection to external voltages.	For 5V operation, see $VDDA_5$ in Table 8, for 3.3V operation, see $VDDA_3$ in Table 7.		V

Table 5. Electrostatic Discharges (ESD)

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{ESD}	ESD tolerance for all pins: Human Body Model (HBM) 100pF / 1.5kΩ	According to AEC-Q100-002 classification H2	±2			kV
$V_{ESD,OUT}$	ESD tolerance for pins with potential external cable connection: SIN_SCL, COS_SDA, SINN, COSN, ADR_IRQN, VDD (HBM 100pF / 1.5kΩ)	According to AEC-Q100-002 classification H3A	±4			kV
V_{CDM}	ESD tolerance for all pins: Charged-Device Model (CDM)	According to AEC-Q100-011 classification C3B	±500			V
$V_{CDM,C}$	ESD tolerance for corner pins ADR_IRQN, SDA, VDDA, GND (CDM)	According to AEC-Q100-011 classification C3B	±750			V

5. Operating Conditions

Conditions: VDD = 3.3V±0.3V or 5.0V±0.5V , T_{AMB} = -40°C to +160°C, unless otherwise noted.

Table 6. Operating Conditions

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
T_{AMB_TSSOP}	Ambient temperature	16-TSSOP package with exposed pad	-40		160[1]	ºC
T_J	Junction temperature		-40		165	ºC
T_{STOR}	Storage temperature	Unmounted units must be limited to 10 hours at temperatures above 125°C	-55		160	ºC
R_{THJA_TSSOP}	Thermal resistance junction to ambient: 16-TSSOP package with exposed pad. Velocity = 0m/s JEDEC MO-153.	Copper ground planes under exposed pad on 4 layer PCB, 3x3 thermal vias between layers.		35.48		K/W
		Copper ground planes under exposed pad on 2 layer PCB, 3x3 thermal vias between layers.		39.96		
		Without PCB ground plane under exposed pad.		61.26		
R_{THJC_TSSOP}	Thermal resistance junction to case	Junction to bottom of package		6.42		K/W
t_{pup}	Start-up time	Power-on reset (POR) to valid output signal			5	ms
V_{EL}	Input rotational velocity, Electrical speed; sine or cosine periods	Electrical revolutions per minute			600000	rpm
		Input frequency			10	kHz
$V_{VDDA\_TH\_H}$	Power-on reset (POR), high threshold	The device is activated when VDDA increases above this threshold			2.49	V
$V_{VDDA\_TH\_L:}$	Power-on reset, low threshold	The device is deactivated when VDDA decreases below this threshold	2.08			V
$VDDA_{POR\_HYST}$	Power-on reset hysteresis	At VDDA pins		110		mV
I_{VDDA}	VDDA short circuit current limitation	VDDA must be connected to a capacitor C_{VA}. No other external load allowed at this pin.	40		85	mA
I_{CC}	Current consumption	Without coils, no load	5		12	mA
		Programmable transmitter coil drive current (depending on inductance of the transmitter coil)	For values, refer to Table 9.			mA
C_{VA}	Capacitor from VDDA pin to GND			100		nF
C_{VDD}	Capacitor from VDD pin to GND	Nominal value	70			nF

[1] Ambient temperature above 155°C limited to 120 hours over lifetime.

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
INL_{uv3V}	Accuracy, 3.3V Mode, VDD= under-voltage alarm level to 3.0V	With ideal sinusoidal input signals, $150mV_{pk-pk}$ Differential output mode, Transmitter frequency = 3.5MHz AGC = on Channel swapping = 0ff			±0.2	% FS [a]
INL_{3V}	Accuracy, 3.3V Mode, VDD= 3.0 to 3.6V				±0.1	% FS
INL_{ov3V}	Accuracy, 3.3V Mode, VDD= 3.6V to over-voltage alarm level				±0.2	% FS
INL_{uv5V}	Accuracy, 5V Mode, VDD= under-voltage alarm level to 4.5V				±0.2	% FS
INL_{5V}	Accuracy, 5.0V Mode, VDD= 4.5 to 5.5V				±0.1	% FS
INL_{ov5V}	Accuracy, 5.0V Mode, VDD= 5.5V to over-voltage alarm level				±0.2	% FS

[a] % FS = percent of full scale = accuracy in % per period, where 100% is the angle range of one electrical period. For rotary multi-period designs, one electrical period = 360° (one full turn) divided by the number of periods per turn, see examples in section 20.

6. Ambient Temperature Range

The minimum ambient temperature for the IPS2550 is -40°C.

The maximum ambient temperature depends on the following factors:

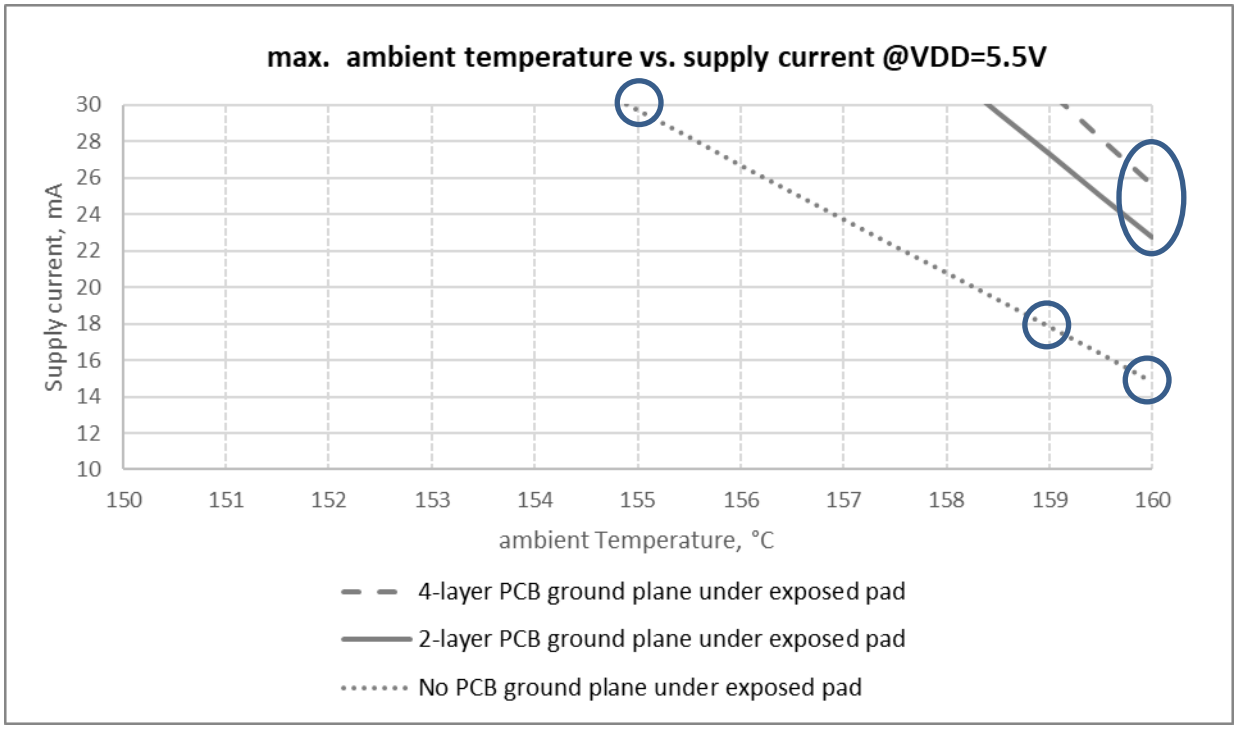
- The maximum junction temperature, see Table 6 for details.
- The supply current. The total power consumption of the chip depends on the supply voltage, the internal supply current, and the user programmable transmitter coil current. The programmable transmitter coil current is shown in Table 9 and the internal circuit current consumption is shown in Table 6.
- The minimum usable coil current in a given application. Typically, smaller coils require more transmitter coil current and larger coils can operate with less coil current. Typical coil designs in the range of 25mm to 30mm coil diameter can require approximately 3mA to 5mA coil current, respectively around 12mA to 14mA supply current. The IPS2550 can drive as high as 20mA of transmitter coil current.
- The temperature range of the supplier part qualification. The IPS2550 is qualified for -40°C to +160°C ambient temperature.
- The thermal resistance of the package in combination with a copper ground plane area on the PCB.

The maximum supply current at VDD = 5.5V versus the ambient temperature with different PCB layers and no airflow cooling is shown in the circled areas of Figure 4. For example, the maximum supply current (internal current + transmitter coil current) at $T_{ambient}$ = 160°C for a PCB with copper ground plane under the exposed pad is 25.6mA for a 4-layer PCB and 22.8mA for a 2-layer PCB. The ground plane is assumed having minimum the same rectangular area as the exposed pad and copied to all layers with a 3x3 array of interconnect vias between each layer.

Note: ignore the small half circles extended at each short side of the exposed pad on the package drawing at the end of this document, they do not need to be copied to the PCB ground plane.

Without copper ground plane(s) under the exposed pad, the maximum current consumption at 160°C ambient temperature is 14.8mA. If the maximum ambient temperature is less than 155°C and the maximum current consumption is below 29.7mA, no PCB ground planes are needed. If the maximum supply current is below 18mA, no PCB ground planes are needed up to an ambient temperature of 159°C

Figure 4. Maximum Supply Current vs Ambient Temperature, with and without Ground Plane



7. Electrical Characteristics

The following electrical specifications are valid for the operating conditions as specified in Table 6: (T_{AMB} is -40°C to 160°C).

Table 7. IPS2550 Electrical Characteristics, 3.3V Mode

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
VDD_3	Supply voltage		3.0	3.3	3.6	V
$V3_{OVR}$	Over-voltage detection, VDD rising	An over-voltage alarm is created if VDD rises above this limit	3.7	3.86	4.1	V
$V3_{OVF}$	Over-voltage detection, VDD falling	An over-voltage alarm is cleared if VDD falls below this limit	3.65	3.79	4.0	V
$V3_{OVH}$	Over-voltage detection hysteresis			70		mV
$V3_{UVR}$	Under-voltage detection, VDD falling	An under-voltage alarm is created if VDD falls below this limit	2.65	2.75	2.90	V
$V3_{UVF}$	Under-voltage detection, VDD rising	An under-voltage alarm is cleared if VDD rises above this limit	2.70	2.85	3.00	V
$V3_{UVH}$	Under-voltage detection hysteresis			100		mV
$VDDA_3$	Analog supply voltage	Internally regulated. Connect capacitor C_{VA} = 100nF between VDDA and GND (see Table 6)	2.85	3.0	3.1	V

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
$V3VDDA_{UVF}$	VDDA under-voltage detection	An under-voltage alarm is created if VDDA falls below these limits.	2.59		2.80	V
$V3VDDA_{UVRr}$	VDDA under-voltage detection	An under-voltage alarm is cleared if VDDA rises above these limits.	2.63		2.85	V
$V3VDDA_{UVH}$	VDDA Under-voltage detection hysteresis			45		mV

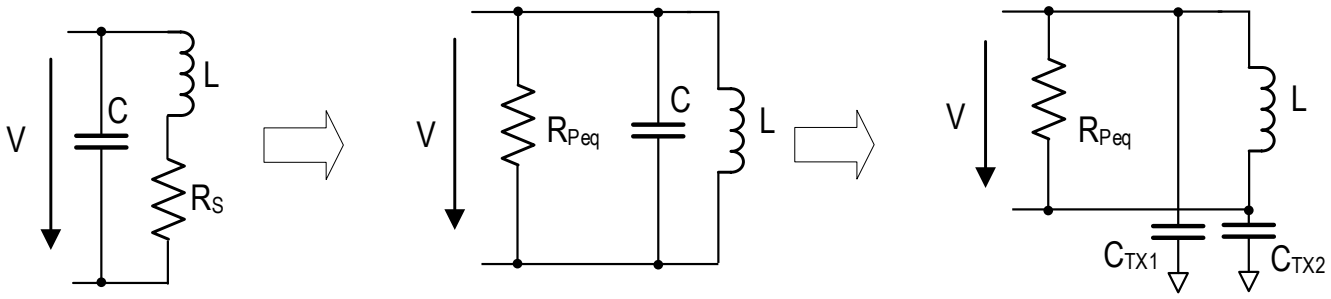
Table 8. IPS2550 Electrical Characteristics, 5.0V Mode

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
VDD_5	Supply voltage		4.5	5.0	5.5	V
$V5_{OVR}$	Over-voltage detection, VDD rising	An over-voltage alarm is created if VDD rises above this limit	5.60	5.84	6.10	V
$V5_{OVF}$	Over-voltage detection, VDD falling	An over-voltage alarm is cleared if VDD falls below this limit	5.55	5.76	6.05	V
$V5_{OVH}$	Over-voltage detection hysteresis			80		mV
$V5_{UVR}$	Under-voltage detection, VDD falling	An under-voltage alarm is created if VDD falls below this limit	4.10	4.33	4.45	V
$V5_{UVF}$	Under-voltage detection, VDD rising	An under-voltage alarm is cleared if VDD rises above this limit	4.20	4.40	4.49	V
$V5_{UVH}$	Under-voltage detection hysteresis			70		mV
$VDDA_5$	Analog supply voltage	Internally regulated. Connect a capacitor C_{VA} = 100nF between VDDA and GND (see Table 6)	3.9	4.0	4.1	V
$V5VDDA_{UVF}$	VDDA under-voltage detection	A VDDA under-voltage alarm is triggered when VDDA falls below these limits.	3.50		3.79	V
$V5VDDA_{UVRr}$	VDDA under-voltage detection	A VDDA under-voltage alarm is cleared if VDDA rises above these limits.	3.60		3.87	V
$V5VDDA_{UVH}$	VDDA Under-voltage detection hysteresis			65		mV

Table 9. LC Oscillator Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
R_{Peq}	Equivalent parallel resistance of the LC resonant circuit	See Equation 4	250			Ω
f_{LC}	Excitation frequency	LC oscillator frequency is determined by external components L and C.	2.0		5.6	MHz
V_{TX_P}	LC oscillator amplitude	Peak-to-peak voltage; pins TX1 vs. TX2; all modes. Adjustable by coil current.		6	11	Vpp
I_{LC}	Programmable transmitter coil drive current	Equivalent DC current. Programmable, depending on transmitter coil inductance.	0	3	20	mA
R_{Tx1},R_{Tx2}	TX Series resistor	For reduced EMC emission		22		Ω

Figure 5. Parallel Resonator Circuit



The equivalent parallel resistance R_{Peq} of the LC oscillator can be calculated using Equation 4. It defines the minimum loss resistance that the oscillator can drive for safe operation.

Note: for improved EMC performance, it is recommended to split capacitor C into two equal capacitors with double capacitance, connected to GND: $C_{TX1} = C_{TX2} = 2C$. See also Figure 2 and Figure 3 for further details.

$$R_{Peq} = \frac{1}{R_S} \times \frac{L}{C}$$

Equation 4

Where

R_{Peq} Equivalent parallel resistance of the LC oscillator.

R_S Serial resistance of the transmitter coil at the transmitter frequency.

L Coil reactance at the resonant frequency.

C Capacitance of the parallel capacitor

Note that the capacitor losses are not included in the equation, since in case of C0G or NP0 ceramics they can be neglected.

Table 10. Coil Receiver Front-End Specifications

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{RX}	Receiver coil amplitude.	Input signal full range to maintain AGC target levels: 3.0V p-p AGC target, gain boost bit disabled	25		1500	mV_{pp}
		Input signal full range to maintain AGC target levels: 3.0V p-p AGC target, gain boost bit enabled	13		780	
		Input signal full range to maintain AGC target levels: 1.8V p-p AGC target, gain boost bit disabled	15		920	
		Input signal full range to maintain AGC target levels: 1.8V p-p AGC target, gain boost bit enabled	8		470	
A_{IN_mm}	Maximum amplitude mismatch correction	Programmable individual gain mismatch correction of Receiver coil signals (SIN and COS)	13		20	%
	Amplitude mismatch step size		0.1		0.15	%
$A_{IN\_OFFSET\_POS\%}$	Maximum positive input offset correction.	Differential input offsets of sine or cosine signal, percentage of transmitter coil amplitude.	+0.17		+0.23	%
$A_{IN\_OFFSET\_NEG\%}$	Maximum negative input offset correction.		-0.25		-0.17	%
$A_{IN\_OFFSET\_mV}$	Input offset correction range at typical oscillator amplitude (see Table 9).		-7.5		7.5	mV
OFF_{CORR_RES}	Input offset correction step size			0.0015		%
R_{Rx}	Coil receiver DC input resistance	Common mode to GND		20		kΩ
		Differential		100		kΩ
C_{RX1}	Receiver input filter capacitors	For improved EMC immunity		100		pF
C_{RX2}						
C_{RX3}						
C_{RX4}						

Table 11. Automatic Gain Control (AGC)

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
$VOUT_{AGC1}$	Output signal amplitude, single ended, AGC enabled	Program option1, for 3.3V Mode and 5V mode (default)	1.4	1.8	2.2	V_{PP}
VM_{AGC1W}	AGC1, no-switching window	AGC1 signal magnitude window, in which gain setting is not changed	200	207	218	mV
$VOUT_{AGC2}$	Output signal amplitude, single ended, AGC enabled	Program option2, for 5V mode	2.6	3.0	3.4	V_{PP}
VM_{AGC2W}	AGC2, no-switching window	AGC2 signal magnitude window, in which gain setting is not changed	195	201	208	mV
$GAIN_{AFE}$	Overall gain adjustment range, sine and cosine signal channel	Default setting	2		120	V/V
		With gain boost bit set	4		240	
AGCAttack	AGC attack time, increase/decrease in same direction			10		µs
AGCDecay	AGC decay time	AGC reversing direction, programmable decay time		0 30 100 300		ms
t_{swap}	Channel swapping cadence	Channel swapping functional safety feature enabled, programmable cadence time		10 50 100 200		µs

Table 12. Diagnostic Checks

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
t_{fail}	Failure reaction time, (time to flag an error condition at the ADR_IRQN pin)	Chip internal diagnostic checks			500	µs
t_{oc_assert}	Debounce time for switching off the analog output amplifiers in case of over-current	If the load current on any analog output exceeds the current limit (I_{OvL}), all four analog outputs are switched off (tri-state) after this time. [a]	135		t_{fail}	µs
t_{cm_assert}	Debounce time for switching off the analog output amplifiers in case of output common mode failure	If the common mode voltage on any analog output exceeds the V_{CM} limit (DC_{OFF_AL}), all four analog outputs are switched off (tri-state) after this time. [b]	40		t_{fail}	µs
$t_{oc\_deassert}$	Debounce time for temporary release of analog outputs after over-current failure	Following an over-current switch-off condition, all outputs are turned on again after this time	4.61	4.68	4.75	ms
$t_{cm\_deassert}$	Debounce time for temporary release of analog outputs after output common mode failure	Following an output common mode switch-off condition, all outputs are turned on again after this time	see $t_{oc\_deassert}$			ms
$R_{\_open\_th}$	Resistance of Rx coil, open coil detection	Rx coil error flag activated	91		154	kΩ
$R_{\_short\_GND}$	External resistance from any coil input to GND, short-to-ground detection	Rx coil error flag activated	68		117	kΩ
$R_{\_short\_VDD}$	External resistance from any coil input to VDD, short to VDD detection	Rx coil error flag activated; VDD = 3.0 to 5.5V	14		233	kΩ
$R_{\_short\_th}$	Rx coil error flag cleared	Rx coil error flag cleared	50		130	kΩ
DC_{OFF_AL}	DC common mode output offset alarm limits	Absolute value relative to VDD/2. Output offset alarm flag activated.	75		195	mV

[a] Over-current durations shorter than these limits are ignored.

[b] Common Mode failure durations shorter than these limits are ignored.

Table 13. Back-End Specification, Analog Outputs SIN_SCL, SINN, COS_SDA, COSN

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
$V3_{OUT}$	Analog output range, 3.3V option	-1.5mA ≤ I_{OUT} ≤ 1.5mA	GND + 0.4		VDD – 0.4	V
$V5_{OUT}$	Analog output range, 5V option	-2.5mA ≤ I_{OUT} ≤ 2.5mA				
VDD_{OUT_CM}	Output DC offset voltage, common mode voltage	All modes, Deviation from VDD/2	-35	0	35	mV
$DC_{OFFDRIFT}$	DC offset voltage drift	Over temperature range	-50		50	µV/°C

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
I_{OUT3}	Output current; 3.3V option	Voltage change ±6mV relative to no load	-3		+3	mA
I_{OUT5}	Output current; 5V option	Voltage change ±10mV relative to no load	-5		+5	mA
I_{OVL}	Output overload current	Short circuit current limit	15		30	mA
Noise	Device output noise	Maximum gain, no output filtering, shorted coil inputs		2	5	mV_{rms}
C_{OUT1}	Output filter capacitors	For improved EMC immunity, placed close to IC output			47	nF
C_{OUT2}						
C_{OUT3}						
C_{OUT4}						

Table 14. Digital I2C Control Interface, Pins SDA and SCL

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{IH}	High level input voltage, all modes	IRQN address select input, SCL clock input, SDA data input	0.7•VDD		VDD+0.3	V
V_{IL}	Low level input voltage, all modes		-0.3		0.3•VDD	V
I_{LEAK}	Input leakage current	VDD = 0V to 5.5V	-8		1.5	µA
$V_{I\_STR\_hyst}$	Hysteresis of Schmitt trigger input	SCL clock input	0.1			V
V_{OL_SDA}	SDA low level output voltage, open drain	3mA sink current	0		0.4	V
I_{OL_SDA}	SDA Low level output current	V_{OL} = 0.4V, VDD=5.5V, R_P=2kΩ	3			mA
C_{IN}	Capacitance of SDA/SCL pin	Pad and ESD protection			10	pF
f_{SCL}	SCL clock frequency		0		100	kHz
t_{LOW}	LOW period of SCL clock		4.7			µs
t_{HIGH}	HIGH period of SCL clock		4.0			µs
t_R	Rise time SDA/SCL	V_{IHmin} to V_{ILmax}			1	µs
t_F	Fall time SDA/SCL	V_{IHmax} to V_{ILmin}			0.3	µs
C_B	External capacitive load for each bus line				400	pF
R_{SDA}, R_{SCL}	External pull-up resistor at pins SDA and SCL	Resistor value and capacitive load on these pins are limiting the maximum clock frequency	1.8	4.7		kΩ
R_{ADR}	External resistor at pin ADR_IRQN for I2C address selection	Pull-up or pull-down, depending on I2C address setting.	1.8	4.7		kΩ

Table 15. I2C Interface via Analog Outputs

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{IH}	SIN_SCL/COS_SDA high level input voltage		0.7•VDD		VDD+0.3	V
V_{IL}	SIN_SCL/COS_SDA low level input voltage		-0.3		0.3•VDD	V
$V_{I\_STR\_hyst}$	Hysteresis of Schmitt trigger inputs, SIN_SCL and COS_SDA		0.1			V
$V_{OL\_COS\_SDA}$	COS_SDA low level output voltage, open-drain	3mA sink current	0		0.4	V
$I_{OL\_COS\_SDA}$	COS_SDA Low level output current	V_{OL} = 0.4V, VDD=5.5V, R_P=1.8kΩ	3			mA
I_{IN}	SIN_SCL/COS_SDA input leakage current	VDD = 0V to 5.5V	-1.5		8	µA
C_{IN}	Capacitance of SCL and SDA pins	Pad and ESD protection			10	pF
f_{SCL}	SCL clock frequency		4		25	kHz
t_{LOW}	LOW period of SCL clock		20		125	µs
t_{HIGH}	HIGH period of SCL clock		20		125	µs
t_F	Fall time SIN_SCL/COS_SDA	V_{IHmin} to V_{ILmax}		0.8	1.2	µs
C_B	External capacitive load for SIN_SCL and COS_SDA				47	nF
t_{PEU}	Program Entry window after POR	First time window to start sending unlock command	1.5		5	ms
t_{PW}	Program Start window after Unlock	Second time window to complete first programming command			75	ms
R_{PU}	External pull-up resistors	Optional; for diagnostic indication	See Table 24			kΩ
		Optional; during programming on pins SIN_SCL and COS_SDA	1.8			kΩ
R_{PD}	External pull-down resistors	Optional; for diagnostic indication	See Table 25			kΩ

Table 16. Digital I2C Control Interface, Pin ADR_IRQN

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
V_{IH}	ADR_IRQN High level input voltage		0.7•VDD		VDD+0.3	V
V_{IL}	ADR_IRQN Low level input voltage		-0.3		0.3•VDD	V
$V_{I\_STR\_hyst}$	Hysteresis Schmitt trigger input		0.1			V
I_{LEAK}	Input leakage current		-8		1.5	µA
V_{OH}	ADR_IRQN high level output voltage	ADR_IRQN configured as interrupt pin	0.8•VDD		VDD+0.3	V
V_{OL}	ADR_IRQN low level output voltage		-0.3		0.2•VDD	V

Table 17. Nonvolatile Memory

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
DR_{NVM}	Data retention	According to AEC Q100		> 100 at 25°C >15 at 100°C		Years
t_{Wr_NVM}	Write temperature	Allowed ambient temperature range for read and write access	-40		135	°C
t_{Rd_NVM}	Read temperature		-40		160	°C
C_{Wr_NVM}	Endurance[a]	Over product lifetime			1000	NVM Write Cycles
C_{Rd_NVM}	Read Cycles		$5x\ 10^{11}$	$1x\ 10^{12}$		NVM Read events

[a] Verified number of program/erase cycles. Qualified with 2000 cycles

8. Circuit Description

The IPS2550 sensor circuit consists of one transmitter coil and two receiver coils, which are typically designed as traces on a printed circuit board. The two receiver coils have a sinusoidal shape and are shifted by 90° with respect to each other; refer to Figure 7 and Figure 8 for typical coil shapes. A metal target is placed above the coil arrangement.
Circuit signal flow:

1. The IPS2550 drives AC current into the transmitter coil and generates an alternating magnetic field.
2. The magnetic field induces voltages in the receiver coils. Without a metallic target, due to the balanced, anti-serial connection of their segments, the voltages are compensated to achieve zero output at each pair of terminals.
3. If a metal target is placed above the coils:
   a. The magnetic field induces eddy currents on the surface of the metal target.
   b. The eddy currents generate a counter magnetic field, thus reducing the total flux density underneath.
   c. The voltage induced in the receiver coil areas underneath the target is reduced, creating an imbalance in the anti-serial coil segment voltages
   d. An output voltage occurs on the terminals, changing amplitude and polarity with the target position.

4. The IPS2550 IC performs a synchronous demodulation of the received signals, and then filters and outputs them for external signal processing.

Due to the 90° phase shift of the two receiver coils, the output signals also have a 90° phase shift in relation to the target position, generating ratiometric sine and cosine signals. The signals can be converted into an absolute position, for example by applying an arctangent operation of Vsin and Vcos.

$$Position = \arctan\left(\frac{V_{sin}}{V_{cos}}\right)$$ **Equation 5**

8.1 Overview

Figure 6. Response of the IPS2550

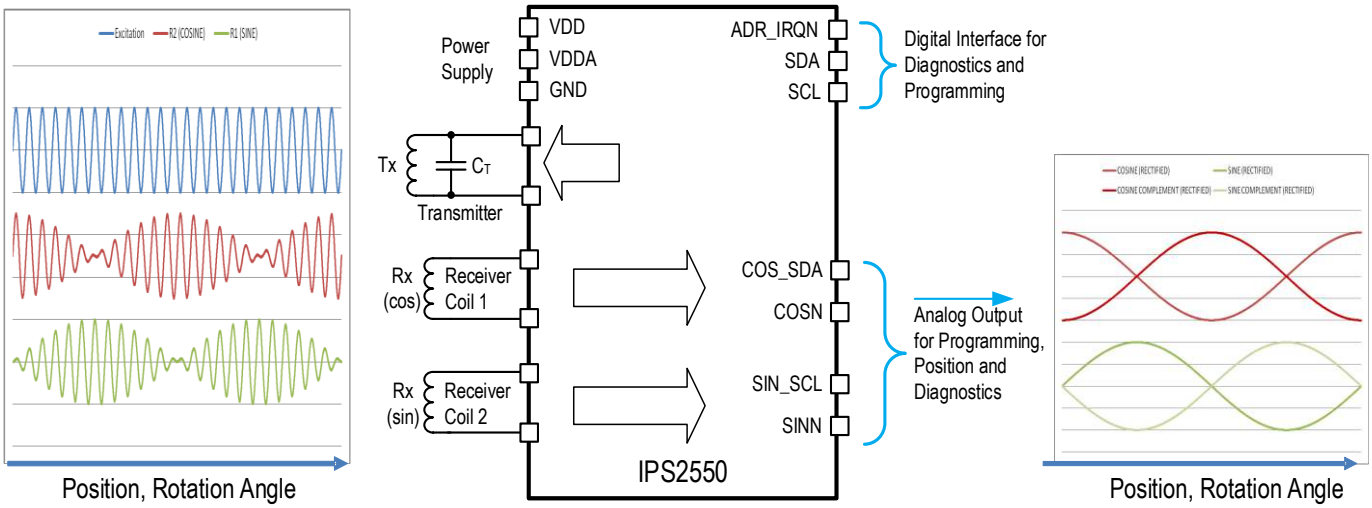


Figure 7 shows an example of a linear motion sensor with one transmitter coil (tx loop) and two receiver coils:

1. Sine Loop = Sin Loop 1 + Sin Loop 2

   and

2. Cosine Loop = Cos Loop 1 + Cos Loop 2.
   Note: the Cosine loop is shifted relative to the Sine Loop, so Cos Loop 1 is split into two halves:
   Cos Loop1 = Cos Loop 1a and Cos Loop 1b

Due to the alternating clockwise and counterclockwise winding direction of each segment in a loop (for example RxCos = clockwise Cos Loop1 + counterclockwise Cos Loop 2), the induced voltages in each segment have alternating opposite polarity.

$$V_{Sin\ Loop1} = -V_{Sin\ Loop2} \quad \textbf{Equation 6}$$

$$V_{Cos\ Loop1} = -V_{Cos\ Loop2} \quad \textbf{Equation 7}$$

If no target is present, the secondary voltages cancel each other:

$$V_{Sin} = V_{Sin\ Loop1} + V_{Sin\ Loop2} = 0V \quad \textbf{Equation 8}$$

$$V_{Cos} = V_{Cos\ Loop1} + V_{Cos\ Loop2} = 0V \quad \textbf{Equation 9}$$

With a target placed above the coils, the secondary voltage induced in the covered area is lower than the secondary voltage without a target above it.

$$V_{Sin\ Loop1} \neq -V_{Sin\ Loop2} \quad \textbf{Equation 10}$$

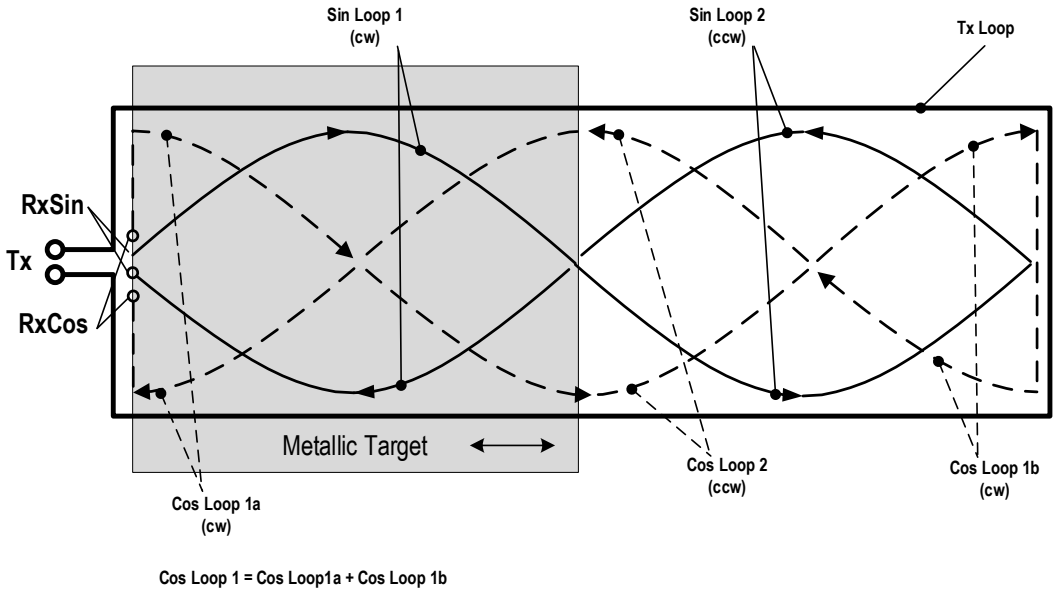
$$V_{Cos\ Loop1} \neq -V_{Cos\ Loop2} \quad \textbf{Equation 11}$$

This creates an imbalance of the secondary voltage segments, and thus, a secondary voltage $\neq 0V$ is generated, depending on the location of the target.

$$V_{Sin} = V_{Sin\ Loop1} + V_{Sin\ Loop2} \neq 0V \quad \textbf{Equation 12}$$

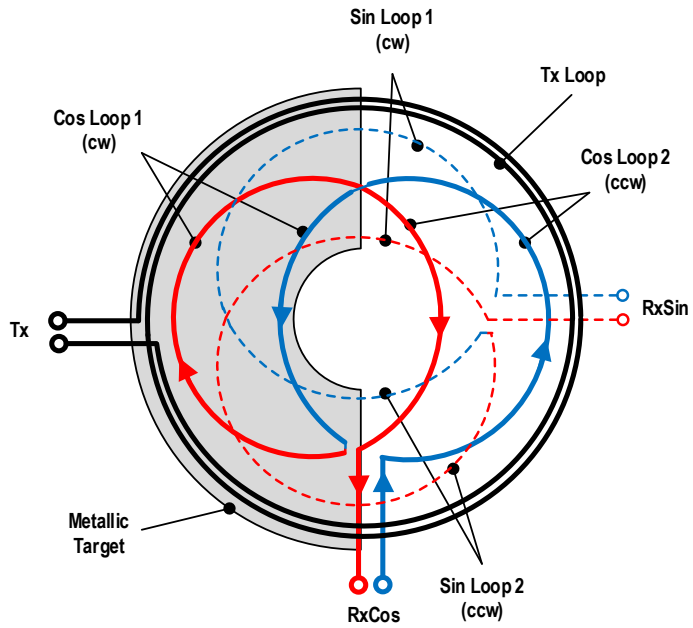
$$V_{Cos} = V_{Cos\ Loop1} + V_{Cos\ Loop2} \neq 0V \quad \textbf{Equation 13}$$

Figure 7. Coil Design for a Linear Motion Sensor



The same principles shown for the linear motion sensor in Figure 7 can be applied to an arc or rotary sensor as shown in Figure 8.

Figure 8. Coil Design for a 360° Rotary Sensor



9. Sampling Rate, Resolution, Output Data Rate, and Propagation Delay

Since the IPS2550 uses analog signal processing (no ADC), there is no sampling rate and the resolution is virtually infinite.

Due to the internal filtering and demodulation processes, there is a short signal propagation delay between analog input and output signals. This delay is factory trimmed to a fixed value, independent of the transmitter oscillation frequency.

Table 18. Propagation Delay

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
t_{PD_trim}	Propagation delay of receiver input signals 1 and 2 at Sine and Cosine outputs.	Factory trimmed; at room temperature over specified supply voltage range	3.8	4	4.2	µs
t_{PD_tc}	Propagation delay temperature drift	over specified operating temperature range	1.8	2.2	2.65	ns/°C

10. Output Modes

Figure 9. Output Signals: Sine-Cosine Analog Differential Mode

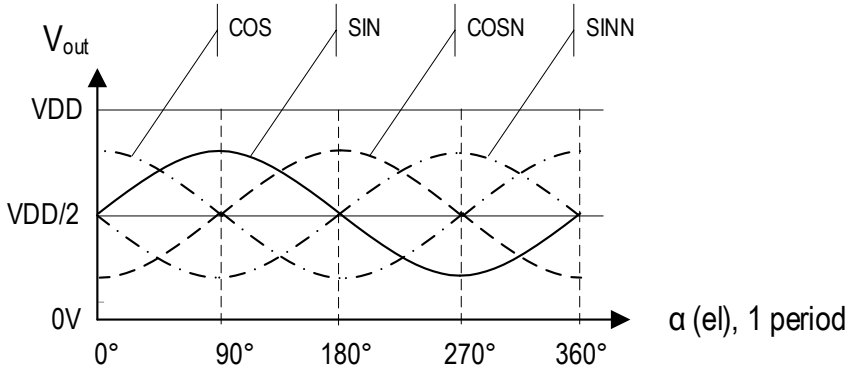
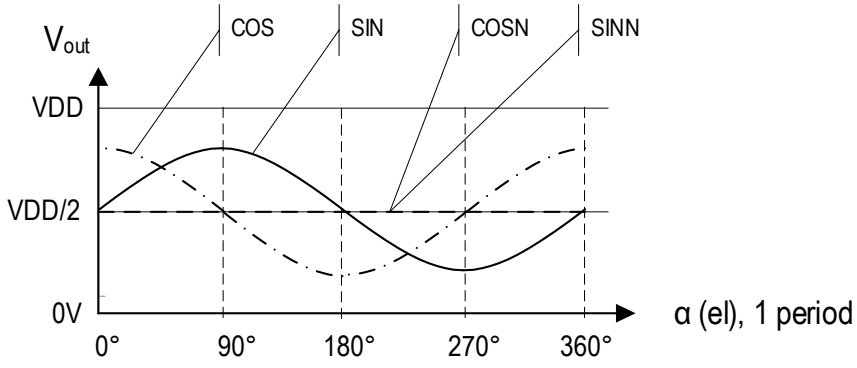


Figure 10. Output Signals: Sine-Cosine Analog Single-Ended Mode



11. Operating at High Speed

The IPS2550 uses analog signal processing, so it can handle inputs signals at very high speed. The input signal can have a frequency of up to 10kHz, which is equivalent to 600000 RPM (electrical phases per minute). Even higher frequencies and therefore higher speeds are possible, but with reduced performance and signal amplitude.

The mechanical rotor speed can be calculated with Equation 14:

$$rpm(mech) = \frac{rpm\ (el)}{coil\ periods}$$ **Equation 14**

Where

rpm (mech) Rotation speed of the rotor (and target) in revolutions per minute

rpm (el) Maximum electrical input frequency of the sensor in rpm (electrical)
= 600000 electrical periods per minute (rpm)
= 10000 electrical periods per second = 10 kHz

coil periods Number of electrical periods per turn
= number of coil periods per 360° circle
= number of metal target segments

For example, Figure 30 shows a design for a 6 pole motor (having 3 pole pairs) using a 3-periodic coil design.

The maximum mechanical rotation speed of this motor is calculated according to Equation 15.

$$\frac{600\text{krpm(el)}}{3} = 200\text{krpm(mech)}$$ **Equation 15**

Table 19. Output Modes and Maximum Speed

	SIN/COS Output Mode	Maximum Rotor Speed
Target Design (metal / no metal)	Sine, Cosine Cycles per Revolution	Mechanical Speed
1 × (180° / 180°)	1 × 360°	600krpm
2 × (90° / 90°)	2 × 180°	300krpm
3 × (60° / 60°)	3 × 120°	200krpm
4 × (45° / 45°)	4 × 90°	150krpm
6 × (30° / 30°)	6× 60°	100krpm
8 × (22.5° / 22.5°)	8 × 45°	75krpm
10 × (18° / 18°)	10 × 36°	60krpm
…	1 cycle per target	600krpm / targets per wheel

12. Digital Diagnostics and Programming Interfaces

In order to program the IPS2550 and to enable fast diagnostics without interrupting the analog high speed signal path, an additional I2C digital serial interface is available.

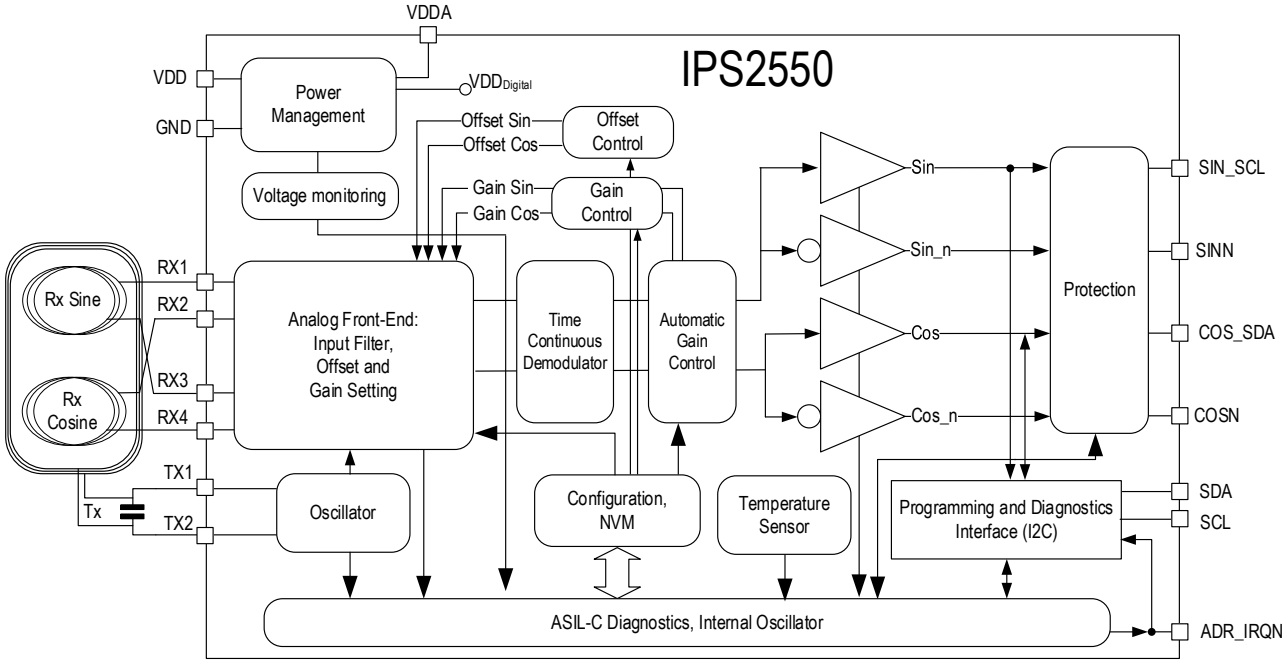
The I2C interface can be operated in two modes:

- I2C interface with address select (default)
- I2C interface with interrupt (programming option)

13. Block Diagram

Figure 11 shows the block diagram of the IPS2550.

Figure 11. Block Diagram



The main building blocks include the following:

- Power management: Power-on-reset (POR) circuit; low drop-out (LDO) regulators for analog and digital supplies.
  - Over-voltage and under-voltage monitoring for VDD, VDDA and internal voltage VDDDigital
- Oscillator: Generation of the transmitter coil signal.
- Analog front-end: Input filter, offset, and gain control for the receive signals.
  - Offset control: Correction of offsets at the receiver coil inputs RX1-RX2 and RX3-RX4.
  - Gain setting: Correction of amplitude mismatch between receiver coil input signals Rx1-RX2 and RX3-RX4.
- Time Continuous Demodulator: Converting RF amplitude modulated position signal to LF demodulated position signal.
- Gain control: Correction of amplitude mismatch from RX1/RX2 and RX3/RX4 input signals.
- Automatic Gain Control: Overall automatic adjustment of sine and cosine channel gain.
- Configuration, NVM: Nonvolatile storage of factory and user-programmable settings.

- Programming and Diagnostics Interface: Available over SIN and COS analog output interface and as a separate I2C interface.
- Temperature Sensor: Monitoring the chip temperature.
- ASIL-C Diagnosis, Internal Oscillator: Internal diagnosis of critical blocks to ensure functional safety. The factory trimmed Internal Oscillator is used for chip-internal timings and as a time base for the Transmitter frequency measurement
- 4 buffered analog/digital outputs with over-voltage and reverse-polarity protection.
- There are three interface options for the SIN_SCL, SINN, COS_SDA, and COSN pins (see Table 2):
  - Differential analog output.
  - Single-ended analog output with reference.
  - Programming

14. Detailed Block Descriptions

Refer to the block diagram in Figure 11 for an illustration of the following blocks.

14.1 Power Management

The IPS2550 can be operated with a power supply at either VDD = 3.3V ±0.3V or VDD = 5.0V ±0.5V. An internal LDO generates the supply voltages for the analog and digital circuits. The analog supply (VDDA) is buffered by an external capacitor C_{VA}. The digital power supply is connected internally only.

VDD is over-voltage and reverse-polarity protected and constantly monitored for over-voltage or under-voltage.

14.2 LC Oscillator

The LC oscillator generates the RF magnetic field for the sensor. It operates in the frequency range of ~2MHz to 5MHz.The frequency is adjusted by external components L (the transmitter coil) and C (external capacitor). See Table 9 for further details.

The IPS2550 accepts a large range of coil inductance, and the coil drive current is user programmable.

The LC oscillator is continuously checked for the correct frequency or failures such as open/short circuits or an oscillator failure.

14.3 Analog Signal Path

For maximum speed, the IPS2550 uses two parallel analog signal channels: one for sine and one for cosine and all-analog signal processing.

14.3.1 Rx Coil Diagnostics

The receiver coils Rx Sine and Rx Cosine are continuously checked for open/short circuits to ground, shorts to VDD, and shorts to the opposite coil. As shown in Figure 2 and Figure 3, the receiver coils can be connected in the following two ways:

- ASIL C connection: preventing possible short-circuit of receiver coils due to a short of two neighboring pins.
- Compatibility connection: providing pin-to-pin compatibility to the industrial grade IPS2200.

14.3.2 Receiver Signal Low-Pass Filter

The receive signal is an amplitude-modulated signal where the carrier frequency is the frequency of the LC oscillator and the signal amplitude is representative of the target position. In a rotating system, the LF signals are sine and cosine shaped, where one period of the LF signal is equivalent to one period of the coil shape. See section 20 for examples of coil designs and their corresponding LF signal.

In a first step, the amplitude-modulated signals are low-pass filtered to suppress possible RF electromagnetic disturbances.

14.3.3 Offset and Gain Matching

After the signals are filtered, the RF signal is corrected for a possible offset and amplitude mismatch, originating from imperfect coil designs. The amount of offset and fine gain correction can be user programmed to a fixed value in the NVM or corrected on-the-fly in embedded applications; see section 15.1 for further details.

14.3.4 Demodulation

The time-continuous demodulator removes the carrier from the input signal, generating the demodulated LF signal.

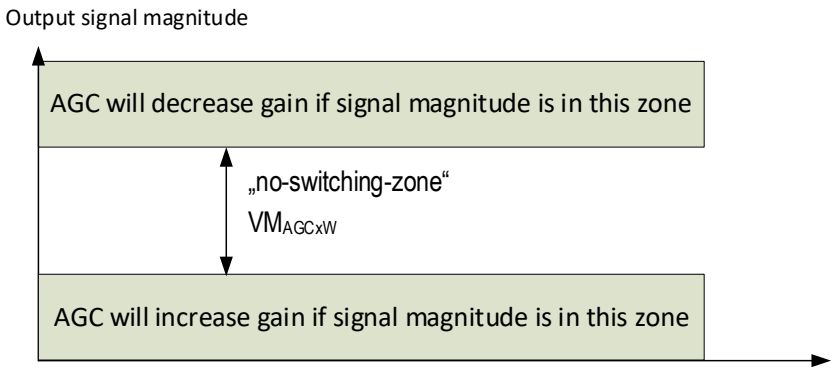
14.3.5 Automatic Gain Control (AGC)

The signal magnitude strength of the demodulated signal, $M = \sqrt{V sin^2 + V cos^2}$, is permanently monitored and compared against a nominal range, which is programmable in two options (see Table 11). The AGC will automatically adjust the receiver gain to bring the output signal magnitude into the “no-switching zone” .

The AGC can also be enabled to generate an alarm if the receiver gain is outside a programmable range, for example to indicate that the receiver input signals are too strong or too weak.

Figure 12. AGC Magnitude ranges

See Table 11 for detailed levels



14.4 Signal Channel Swapping

An effective method to improve the detection of internal gain errors is a Renesas patent-pending signal channel swapping feature, available as a configuration option. When enabled, the chip periodically swaps the sine and cosine signal channels between the two analog signal paths. By applying this method, any gain mismatch between sine and cosine signal channels is immediately detectable at the analog signal outputs, even in static (non-rotating) operation.

14.5 Output Buffers

The four analog signals (sine, inverted sine, cosine and inverted cosine) are individually buffered at the corresponding output pins.

The buffer outputs are over-voltage and reverse-polarity protected and checked for shorts to ground, shorts to VDD, or common-mode voltage disruption. In the diagnostic state, if enabled, the buffers are turned off, allowing diagnostics indication by the external MCU through external pull-up or pull-down resistors.

14.6 Temperature Sensor

The IPS2550 features an internal chip temperature sensor to generate an alarm in the event of an over-temperature event. The temperature sensor has two levels of alarm:

1. The junction temperature exceeds the warning threshold: a diagnostics alarm is generated, the output buffers for SIN_SCL, COS_SDA, SINN, COSN are turned off to reduce the power consumption.
2. The junction temperature exceeds a critical alarm level. In addition, as a programming option, the LC oscillator can also be turned off to further reduce the power consumption.

Table 20. Internal Chip Temperature Sensor Characteristics

Symbol	Parameter	Conditions	Minimum	Typical	Maximum	Units
T_{OVT_WARN}	Over-temperature warning threshold		175	180	185	°C
T_{OVT_ERR}	Over-temperature error threshold		180	185	190	°C
ACC_{TS}	Temperature sensor absolute accuracy		-10		+10	ºC
T_{HYST}	Temperature hysteresis		8	10	12	ºC

15. ECU Connection Options

Note: In Figure 13, Figure 14, and Figure 15, the various connection options between the IPS2550 and the electric control unit (ECU) are shown.

The IPS2550 must be programmed properly to match to the correct VDD voltage supply level (3.3V or 5.0V).

15.1 Embedded vs. Remote Connection

In an embedded connection, both the sensor and microcontroller (MCU) are mounted on the same printed circuit board (PCB). In these applications, the number of connections between the two chips is not critical. The MCU can take advantage of the separate digital I2C interface to constantly monitor the diagnostic registers without interrupting the analog signal flow or to change offset or gains on-the-fly.

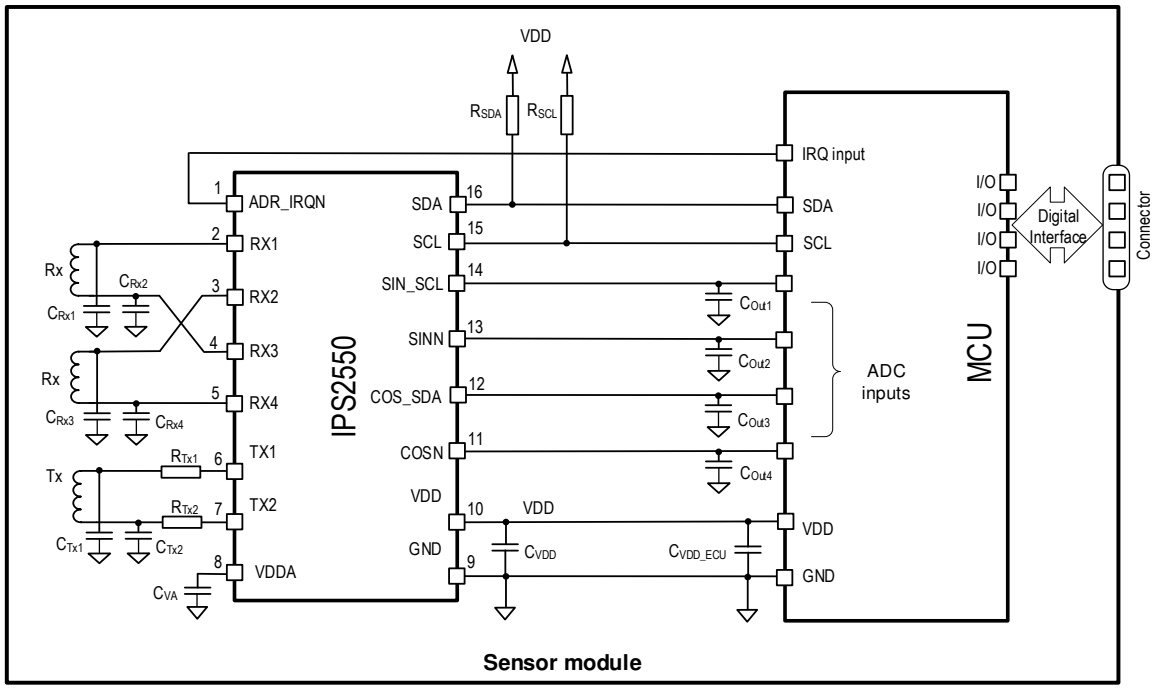
ADR_IRQ Pin is used in IRQ mode for diagnosis.

When using the digital interface pins, SDA and SCL, IPS2550 and ECU must share the same VDD voltage supply level in order to match the digital high and low signal levels.

The circuit diagram, shown in Figure 13, include external components required for improved EMC performance in embedded operation.

Note: Capacitors C_{Out1} to C_{Out4} depend on ADC input specifications of the connected MCU.

Figure 13. Embedded Application: Sensor and MCU are on the same PCB



In a remote application, the sensor module is separate from the ECU, connected by a cable. For cost efficiency, the number of wires on the cable and the number of connector pins should be kept as small as possible, typically four wires (VDD, GND, Sine, Cosine) for single-ended configuration and six wires (VDD, GND, Sine, Inverted Sine, Cosine, Inverted Cosine) for differential configuration.

In an error case, the analog outputs are switched to tristate mode; a diagnostic state is indicated by either pushing the output voltage to VDD using pull-up resistors (as shown in Figure 14) or by pulling the output voltage to ground, using pull-down resistors (as shown in Figure 15).

See 18.2 for further details on diagnostic indication.

The circuit diagrams, shown in Figure 14 and Figure 15 include external components required for improved EMC performance in remote operation.

Figure 14. Remote Application with Pull-Up Resistors for Diagnosis

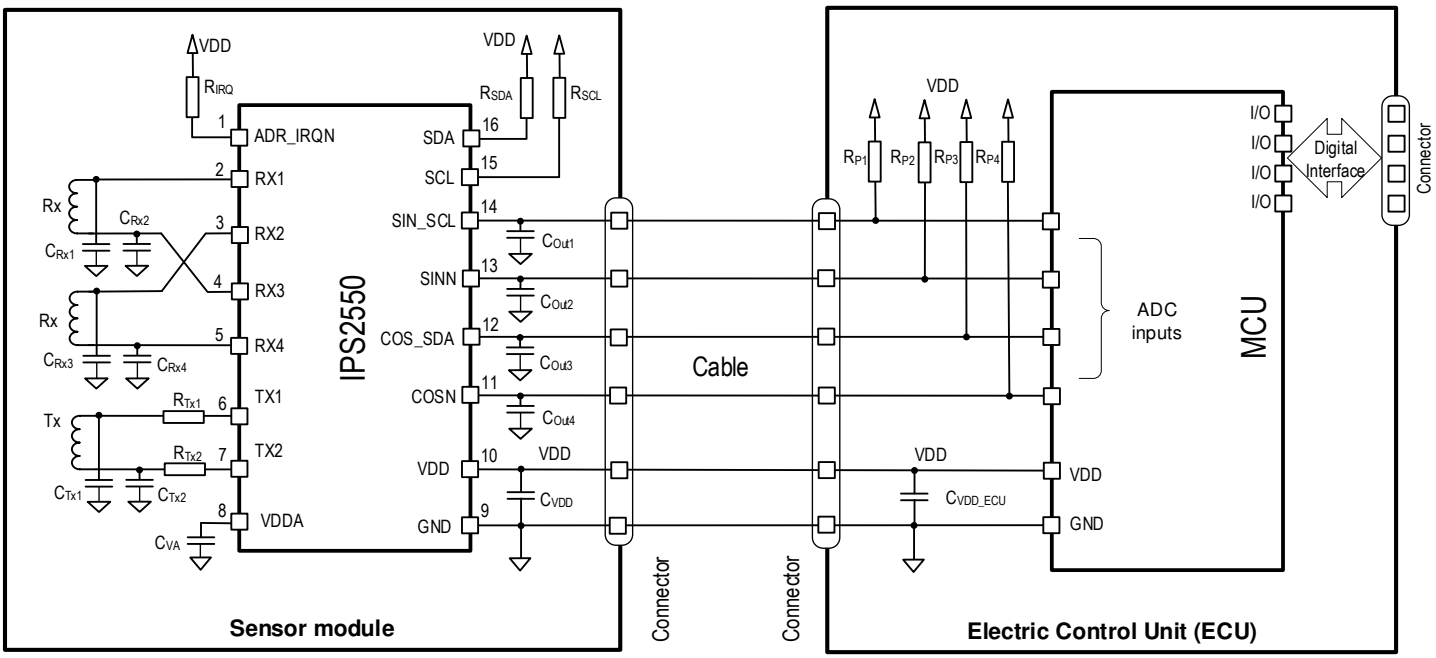
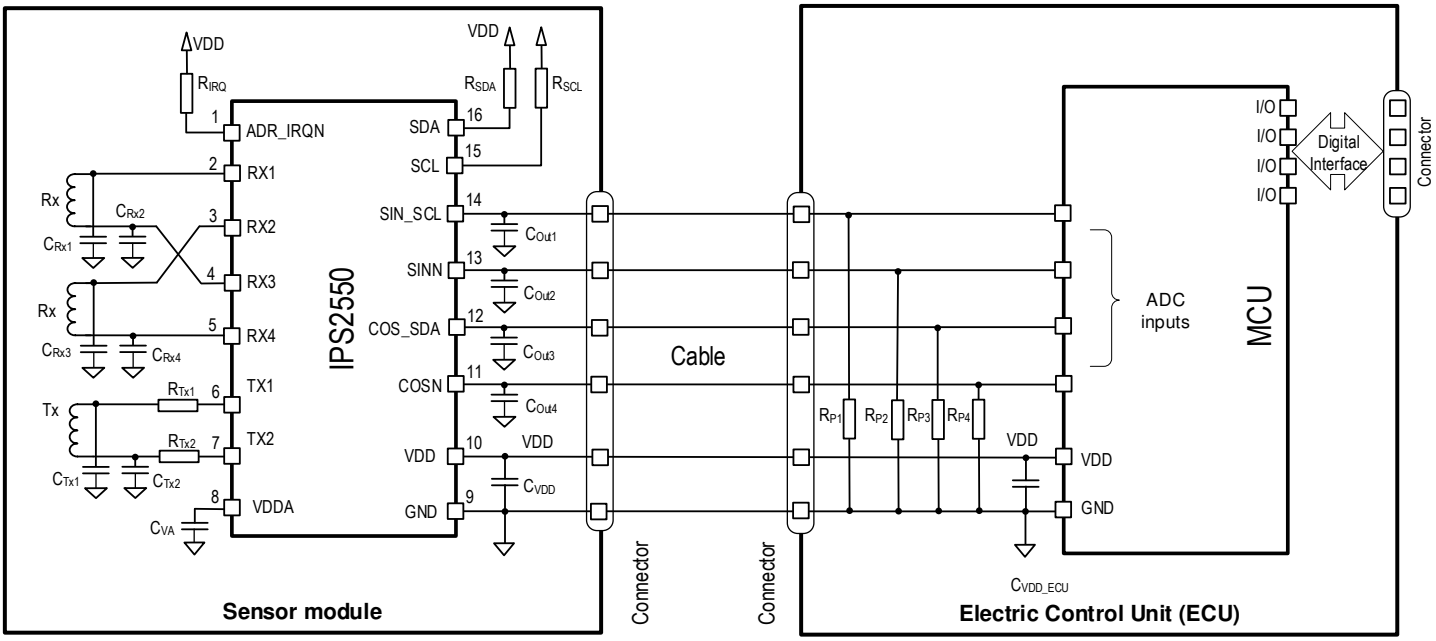


Figure 15. Remote Application with Pull-Down Resistors for Diagnosis



15.2 Supply Voltage Operation: 3.3V or 5V

The IPS2550 can be programmed to operate with either a 3.3V ±0.3V or VDD = 5.0V ±0.5V supply voltage, the default is 5V. Refer to section 0 for changing the default supply voltage."

15.3 I2C Interface

The IPS2550 includes a standard I2C interface. The I2C address is programmable. In addition, the ADR_IRQN pin can be programmed as either an I2C address selection pin or as an interrupt output (IRQN) pin when using the I2C interface (see Table 3). The IPS2550 is configured as an I2C slave; several slaves can be connected in parallel on the I2C bus. A detailed description of the programming features is available in the *IPS2550 User Programming Manual.*

Two wires, serial data (SDA, pin 16) and serial clock (SCL, pin 15), carry information between the devices connected to the bus. Both SDA and SCL are connected to the positive supply voltage VDD via an external pull-up resistor. When the bus is free, both lines are high. The output stages of devices connected to the bus must have an open-drain or open-collector to perform the wired-AND function.

An external master (host controller) initiates a transfer, generates clock signals, and terminates a transfer. The implementation supports the I2C slave function, which is addressed by the master and supports the I2C bus specification version 2.1.

Since the analog outputs might contain passive filters or EMC capacitors, the rise and fall times might be longer compared to the digital I2C interface. Therefore, the I2C clock rate during programming of the IPS2550 over the analog outputs must be adapted accordingly.

15.3.1 I2C with Address Selection (Default)

When the IPS2550 is programed to use the I2C interface with address selection, the ADR_IRQN pin is used to select the I2C slave address by hardware pin strapping.

By default, the ADR_IRQN pin (#1) is used to define the IPS2550 I2C slave address by hardware pin strapping.

The status of this pin is mirrored in I2C address Bit A3 and the inverted status of this pin is mirrored in I2C address Bit A0 of the 7-bit I2C address (see Figure 16).

The default setting of I2C address bit is A4 =1.

If ADR_IRQN is tied to Ground, the IPS2550 default slave address is 001**0**00**1** (binary) = 0x11 (Hex), while if this pin is connected to VDD, the I2C address is set to 001**1**00**0** (binary) = 0x18 (Hex).

I2C address selection through hardware pin strapping can be disabled and a fixed I2C address can be defined in the NVM address bits A6…A3 (see further details in the *IPS2550 Programming Guide* document).

Table 21 shows the different options for selecting the I2C address by combinations of pin addressing and NVM address register setting.

I2C address bits A3 to A6 can be configured in the NVM for an individual I2C address, allowing up to 14 devices to be addressed in parallel. See the *IPS2550 Programming Guide* document for more information.

Table 21. I2C Address Selection Options in NVM

I2C Address Selection Mode	A6	A5	A4	A3	A2	A1	A0
Default setting	0	0	1	Pin#1	0	0	Pin#1 inverted
User programmable range, with I2C address selection by pin #1	001 to 110 (binary)			Pin#1	0	0	Pin#1 inverted
User programmable range, with fixed I2C address	0001 to 1110 (binary)				0	0	0

Figure 16. I2C Address Select Bits

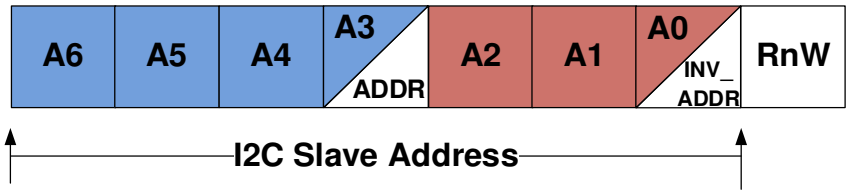
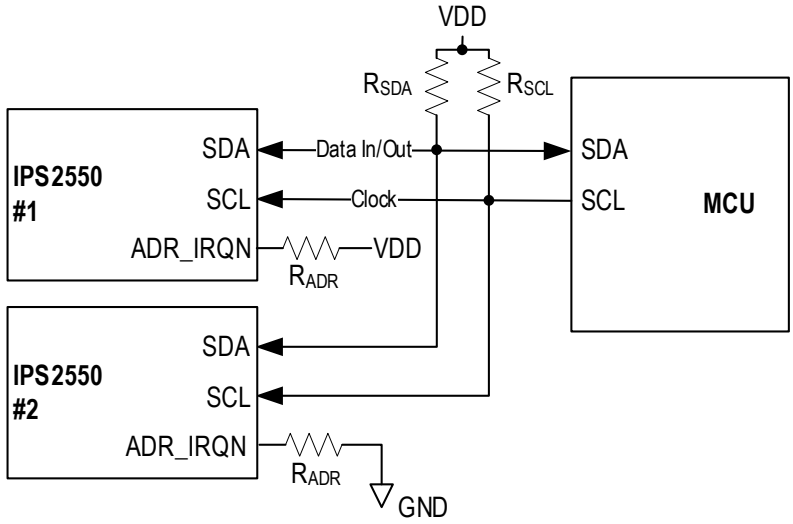


Figure 17. I2C Interface with Address Select

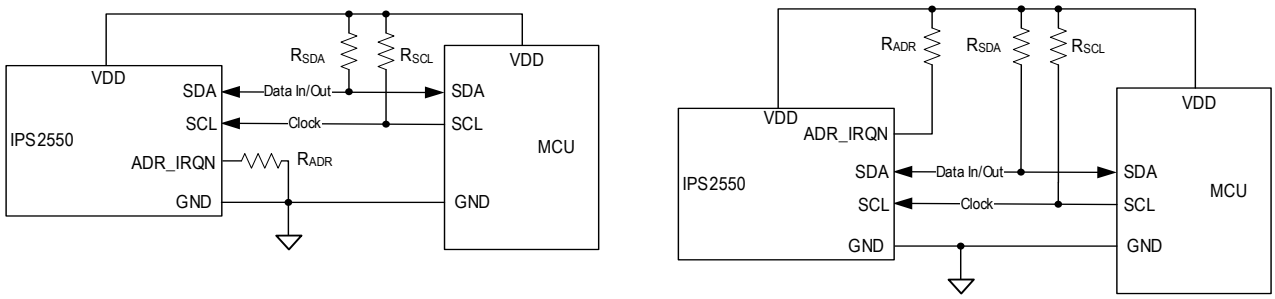


15.3.2 Avoiding a Parasitic Path through ADR_IRQN Pin during Loss of GND or Loss of VDD

In safety critical applications, a loss of ground or VDD must be monitored and reacted to in case of failure. Cases for a loss of the GND or VDD wire in a remote application and their proper diagnostic configuration are shown in Figure 25.

If the ADR_IRQN pin is used for selecting the I2C address through hardware pin strapping, it is recommended not to connect it directly to VDD or GND. Connected it to VDD or GND with a resistor R_{ADR} (see Figure 18 and Table 14) to avoid parasitic supply currents flowing through the ADR_IRQN pin in case of broken GND or VDD wires that might put the chip in an undefined state.

Figure 18. I2C Interface with Address Selection by Hardware Pin Strapping Through ADR_IRQN Pin



15.3.3 I2C Interface with Interrupt (Programming Option)

When the IPS2550 is programed to use the I2C interface with the interrupt function, it operates as a standard I2C interface. The I2C address is programmable. In addition, the ADR_IRQN pin is used as an interrupt output for fast signaling of a diagnostic event.

Figure 19. I2C Interface Configuration with Interrupt on a Single Slave

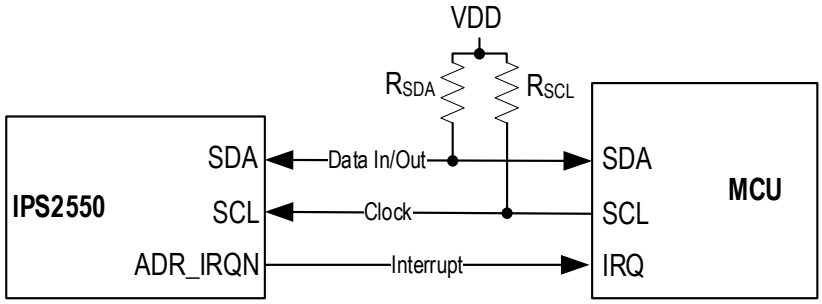
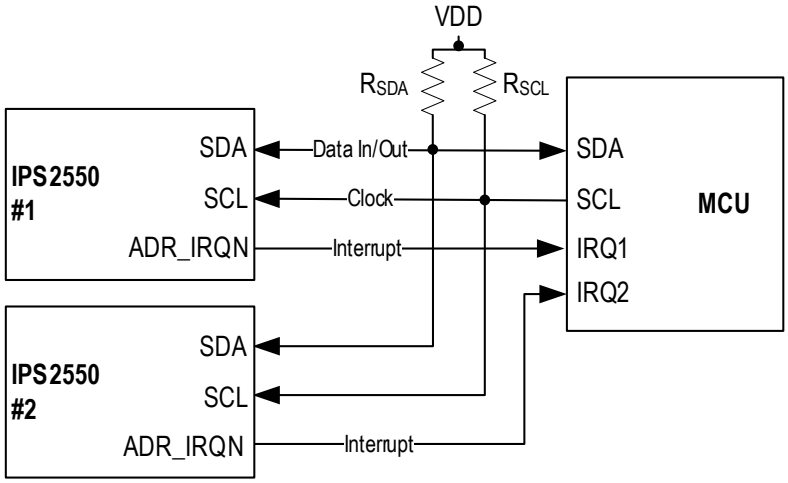


Figure 20. I2C Interface Configuration with Multi-slave Interrupt

Note: In this mode, several I2C slaves are connected in parallel. Note that each I2C slave must have an individual I2C address.



For a detailed description of the I2C interface, refer to the *IPS2550 Programming Guide.*

16. Over-Voltage Protection

16.1 I/O Protection

In order to meet the automotive requirements for over-voltage and reverse-polarity protection on both the output and power supply pins, the IPS2550 includes several protection and diagnosis features:

1. Protection against short circuit of the output pins SIN, SINN, COS, and COSN to GND or to VDD
2. Over-voltage and reverse-polarity protection:
   a. On supply pin VDD to GND
   b. On analog output pins SIN, SINN, COS, and COSN to GND

17. Programming Options

The IPS2550 family offers a variety of programming options. The main programming functions are described in Table 22.

The IPS2550 can be accessed and programmed in one of two ways:

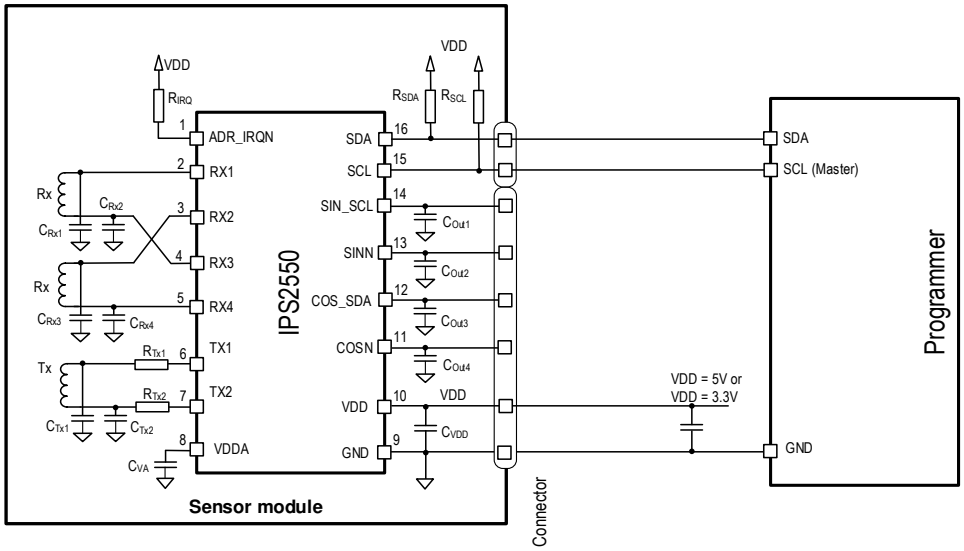
- Over the I2C interface pins SDA and SCL
- Through the analog outputs SIN_SCL and COS_SDA

Note: For programming details, see the *IPS2550 Programming Guide*, which is available from Renesas on request.

The I2C interface, available at pins SDA and SCL, allows simultaneous access to the internal registers and on-the-fly modification of gain and offset settings without interruption of the analog output signals. The IPS2550 can also be programmed via this interface in the same way using a standard I2C protocol; see Figure 21.

Note that the SDA and SCL pins do not contain internal pull-up resistors. If this interface is used, external pull-up resistors need to be installed, either on the sensor module or externally.

Figure 21. Programming the IPS2550 over the I2C Interface



In some cases, particularly in remote applications, where the number of connector pins and wires is kept at a minimum and where permanent access to the internal registers is not needed, it is also possible to program the IPS2550 over two analog outputs (SIN_SCL and COS_SDA; see Figure 22).

This method is typically used for end-of-line programming for a final, assembled sensor module, where the digital interface pins SDA and SCL are no longer accessible.

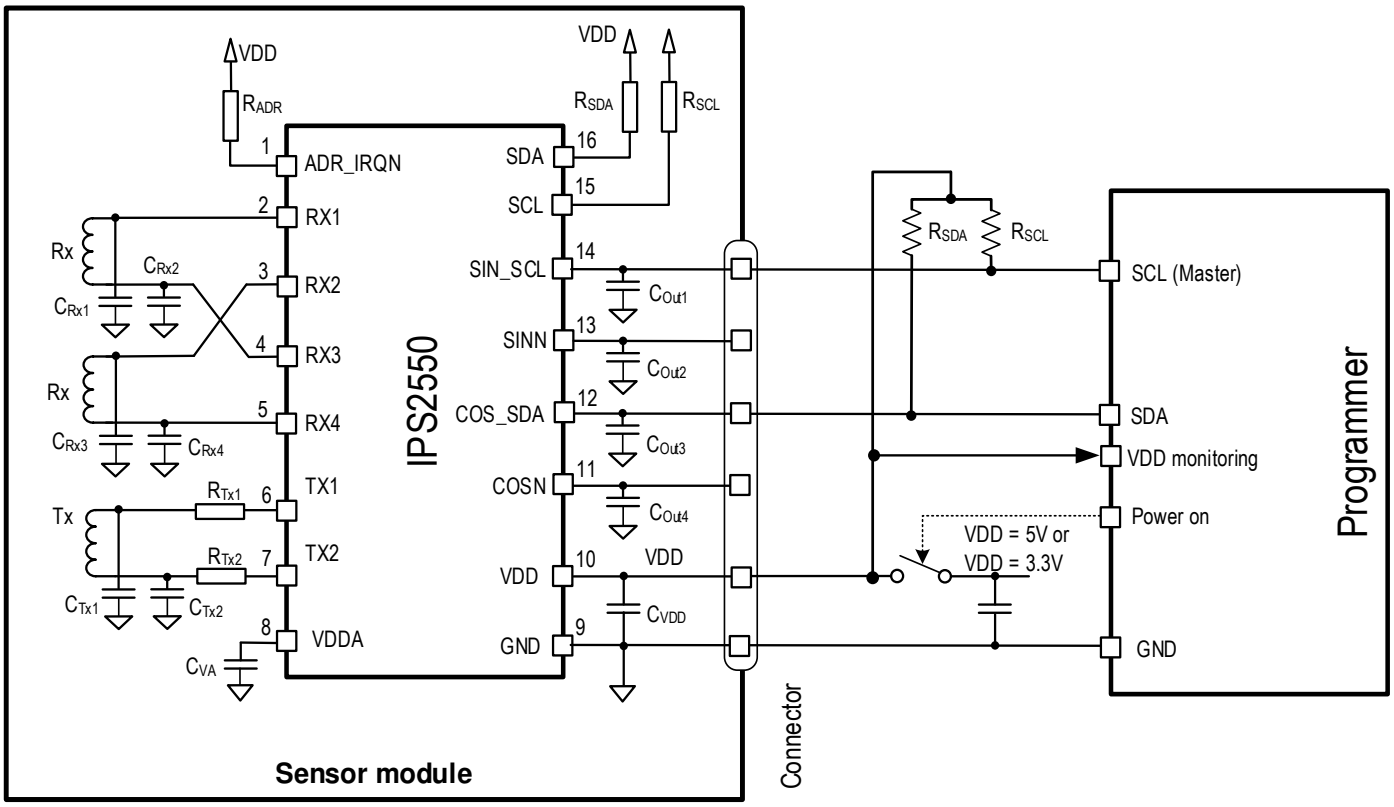
In order to avoid unintentional programming of the IPS2550, a few safety locks are implemented:

- The programming enable window is open for a few milliseconds after power-up. If there is no external enable command sent within this time window, the IPS2550 resumes normal power up.
- Following this first level of enabling programming mode, another password must be sent within a second, longer window to unlock Programming Mode. See the *IPS2550 Programming Guide* document for details.
- After programming, the chip can be locked for further writing, and in addition it can also be locked for reading. Once the chip is locked, it cannot be unlocked (Cyber Security feature).

Since the analog outputs could contain external passive EMC filters that will slow down the data rate, the programmer must also be able to run at lower speeds.

In order to hit the programming time window after power-up, the programmer must be able to sense the VDD ramp-up of the IPS2550. Optionally, the programmer can actively cycle the power for the IPS2550 as illustrated in Figure 22.

Figure 22. End of Line Programming of the IPS2550 Through the Analog Outputs



Note: For improved EMC and ESD performance, do not leave unused I2C interface pins floating. Connect the SCL and SDA pins to VDD using series resistors R_{SDA} and R_{SCL}, see Table 14 for recommended component values.

17.1 Programming the Device to Use the Other Supply Voltage Option

The IPS2550 can be programmed for two operation supply voltages: 3.3V ±0.3V or VDD = 5.0V ±0.5V.

If an IPS2550 that is programmed for 5V supply is connected to a 3.3V supply, it will remain in a (5V) under-voltage state and not boot up. However, in this state, the NVM Programming Mode can be enabled, so the chip can be re-programmed to a 3.3V supply voltage. After a power-on-reset, the IPS2550 will re-boot as a 3.3V device and operate normally in a 3.3V environment.

If an IPS2550 that is programmed for 3.3V supply is connected to a 5V supply, it will start-up, flag a (3.3V) over-voltage alarm, and enter the diagnostic state. However, despite the alarm, Programming Mode can still be enabled, so the IPS2550 can be re-programmed to 5V supply voltage. After a power-on-reset, the IPS2550 will re-boot as a 5V device and operate normally in a 5V environment.

17.2 Lock Feature (Cyber Security)

The IPS2550 contains a lock bit option, which can be set by the user. The lock feature is user selectable for write lock only or read+write lock. Once the write lock bit or write+read lock bit is set, no further writing to the IPS2550 is possible. A locked IPS2550 cannot be unlocked.

Note: The detailed IPS2550 Programming Guide is available from Renesas on request.

17.3 Programming Options

Table 22. Programming Options Overview

Function	Programming Option
Supply voltage range	3.3V ±0.3V or 5.0V ±0.5V, alarm levels
High speed interface	Sine/cosine differential or single-ended
Digital diagnostic and programming interface	I2C with address select or I2C with interrupt
I2C interface	Slave address, I2C mode with address select or with interrupt
Diagnostic signaling on high speed analog interface	Analog output pins are high ohmic in diagnostic state. (SIN, COS) and (SINN, COSN) can be enabled/disabled separately
Security lock function	Access to internal registers of the device can be set to read-only or R/W lock
Receiver overall gain	Overall gain coarse adjustment
Sine, cosine channel gain	Amplitude mismatch correction, fine adjustment
Sine, cosine offset	Pre-adjustment of input offsets
Transmitter oscillator	Bias current, optimization of coil performance
Time base counter	Measurement of transmitter oscillator frequency, and upper/lower frequency alarm
Interrupt	Enable/disable/clear interrupt events
Automatic gain control	Upper/lower gain limit

18. Functional Safety and Diagnostics

18.1 Functional Safety ASIL and ISO Compliance

The IPS2550 has been developed according to ISO26262 as a Safety Element out of Context (SEooC) for implementation in safety relevant systems up to ASIL C for a single IC and ASIL D for dual, redundant ICs, using internal and external safety mechanisms.

Integration of IPS2550 products into safety-related applications requires a safety analysis performed by the user.

Internal safety mechanisms include, but are not limited to, the following:

- Detection of broken or shorted receive or transmitter coils
- Under-voltage and over-voltage detection
- Broken-chip detection
- Data integrity checks (ECC and parity)
- Silicon chip over-temperature detection
- Detection of output buffer failures

See Table 26 for additional IPS2550 safety features.

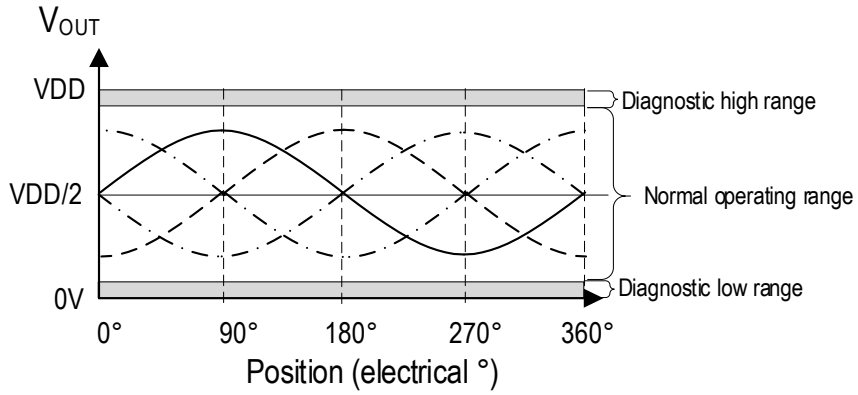
External safety mechanisms must be performed by the receiving microcontroller unit (MCU). They include, but are not limited to, the following:

- Cable harness checks (open, short to GND, short to VDD)
- Plausibility and failure checks of the sine and cosine signals (offset, amplitude, phase)
- Position output synchronicity (for systems using dual ICs)

18.2 Diagnostic Mode Indication through Analog Outputs

In addition to the diagnostic flag indication through the I2C interface and interrupt output pins, the IPS2550 offers diagnostic indication through the analog output pins by putting them in diagnostic mode. This diagnostic mode is indicated by an output voltage that is outside the normal operating range, see Figure 23.

Figure 23. Operating Range and Diagnostic Range



When the AGC is enabled, the normal operating range is:

- VDD/2 ±1.5V = 1.0 to 4.0V for 5V mode
- VDD/2 ±900mV = 0.75 to 2.55V for 3.3V mode or 5V mode (default)

When the AGC is disabled, the operating output voltage range is not limited and defined by the input voltage multiplied by the total gain in the signal path. Note that the gain has to be set correctly otherwise the output voltage moves into the diagnostic ranges.

The limits for the diagnostic ranges are defined by the user. Typical diagnostic ranges are:

- Diagnostic low $\leq$ 3 to 5% VDD
- Diagnostic high $\geq$ 95 to 97%VDD.

For the IPS2550, the output voltage in diagnostic mode depends on the error condition and the value of the external pull-up or pull-down resistors, see section 18.2.1.2 details.

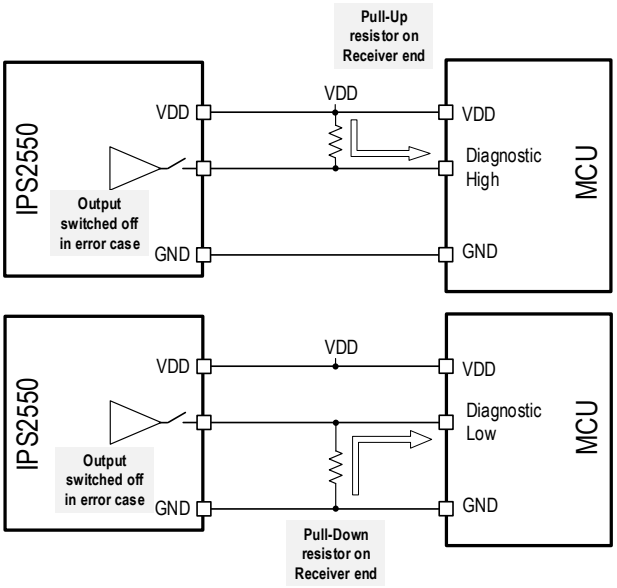
The IPS2550 provides the following options for diagnostics indication through the analog outputs:

- Diagnostics indication on output pins disabled
- Diagnostics only on SIN_SCL and COS_SDA pins
- Diagnostics only on SINN and COSN pins
- Diagnostics on all four analog output pins

Each individually checked error can be enabled or disabled for diagnostics indication.

If diagnostic is enabled and an error occurs, the selected outputs are switched off. By connecting external pull-up or pull-down resistors, the output voltage is either pulled towards VDD into the Diagnostic high range or pulled towards GND into the Diagnostic low range, see Figure 24.

Figure 24. Selection of Diagnostic Range



Note that during programming through the analog outputs using the I2C interface, the SIN_SCL and COS_SDA pins need to be connected to external pull-up resistors. If the Sensor module includes on-board pull-down resistors, the external pull-up resistors for programming must be selected properly to provide adequate high levels that does not exceed the load current on the outputs. Therefore, if the IPS2550 is to be programmed on module level, for example for end-of-line calibration, the use of pull-up resistors for diagnostics indication is recommended.

18.2.1 Shorted and Broken Wire Detection

A failure from a broken or shorted wire occurs when the sensor is connected-to a control unit (MCU, ECU) by a cable.

18.2.1.1 Shorted Wires

Shorts between Ground, Signal and Supply wires can be safely detected, as shown in Table 23:

Table 23. Detection of Shorts between Wires

Cable connections	Supply	Output	Ground
Supply	Short between two supplies. Only applicable for isolated, redundant sensor IC supplies. Must be monitored and controlled by the external power supply unit supplying the sensors.	Short between Supply and Output. Output switches off when the output current exceeds the over-current threshold. Diagnostic state depends on whether pull-up or pull-down resistors are installed at the receiver side.	Short between Supply and Ground. Over-current in the supply line. Must be monitored and controlled by the external power supply unit supplying the sensor.
Output	Short between Output and Supply. Output switches off when the output current exceeds the over-current threshold. Diagnostic state depends on whether pull-up or pull-down resistors are installed at the receiver side.	Short between two different outputs. Outputs switch off when their output current exceeds the over-current threshold. Diagnostic state depends on whether pull-up or pull-down resistors are installed at the receiver side.	Short between Output and Ground. Output switches off when the output current exceeds the over-current threshold. Diagnostic state depends on whether pull-up or pull-down resistors are installed at the receiver side.
Ground	Short between Ground and Supply. Over-current in the supply line. Must be monitored and controlled by the external power supply unit supplying the sensor.	Short between Ground and Output. Output switches off when the output current exceeds the over-current threshold. Diagnostic state depends on whether pull-up or pull-down resistors are installed at the receiver side.	Short between two Ground wires. Only applicable for isolated, redundant sensor IC supplies. Must be monitored and controlled by the external power supply unit supplying the sensors”

18.2.1.2 Broken Wires

Most of the broken Supply, broken GND, or analog output signal connection errors are easily detectable by monitoring the DC voltage levels at the analog output pins, see the uncritical error cases on Figure 25 (“OUT” = SIN_SCL, SINN, COS_SDA or COSN). In case of a diagnostic error or broken signal wire, the DC voltage level at the affected pin is pulled into the diagnostic range (diagnostic high or diagnostic low) through the external pull-up or pull-down resistors.

For the following cases, a parasitic current inside the IPS2550 may cause unwanted, too high voltage drops across the pull-up or pull-down resistors and may not indicate the error condition properly :

- a broken VDD Supply wire with external pull-up resistors at the receiving end, see Figure 25, top right :
  A parasitic current flows from VDD on the receiver end → external pull-up resistor → analog output pin of the IPS2550→ device internal parasitic path to GND.
- a broken GND wire with external pull-down resistors at the receiving end see Figure 25, bottom right :
  A parasitic current flows from VDD on the IPS2550 → device internal parasitic path to output pin → external pull-down resistor → GND

For these special cases, the maximum resistance value for these resistors must be selected according to the required diagnostic range, see Table 24 and Table 25.

Figure 25. Parasitic Currents on Analog Outputs with Broken VDD or Broken GND Lines

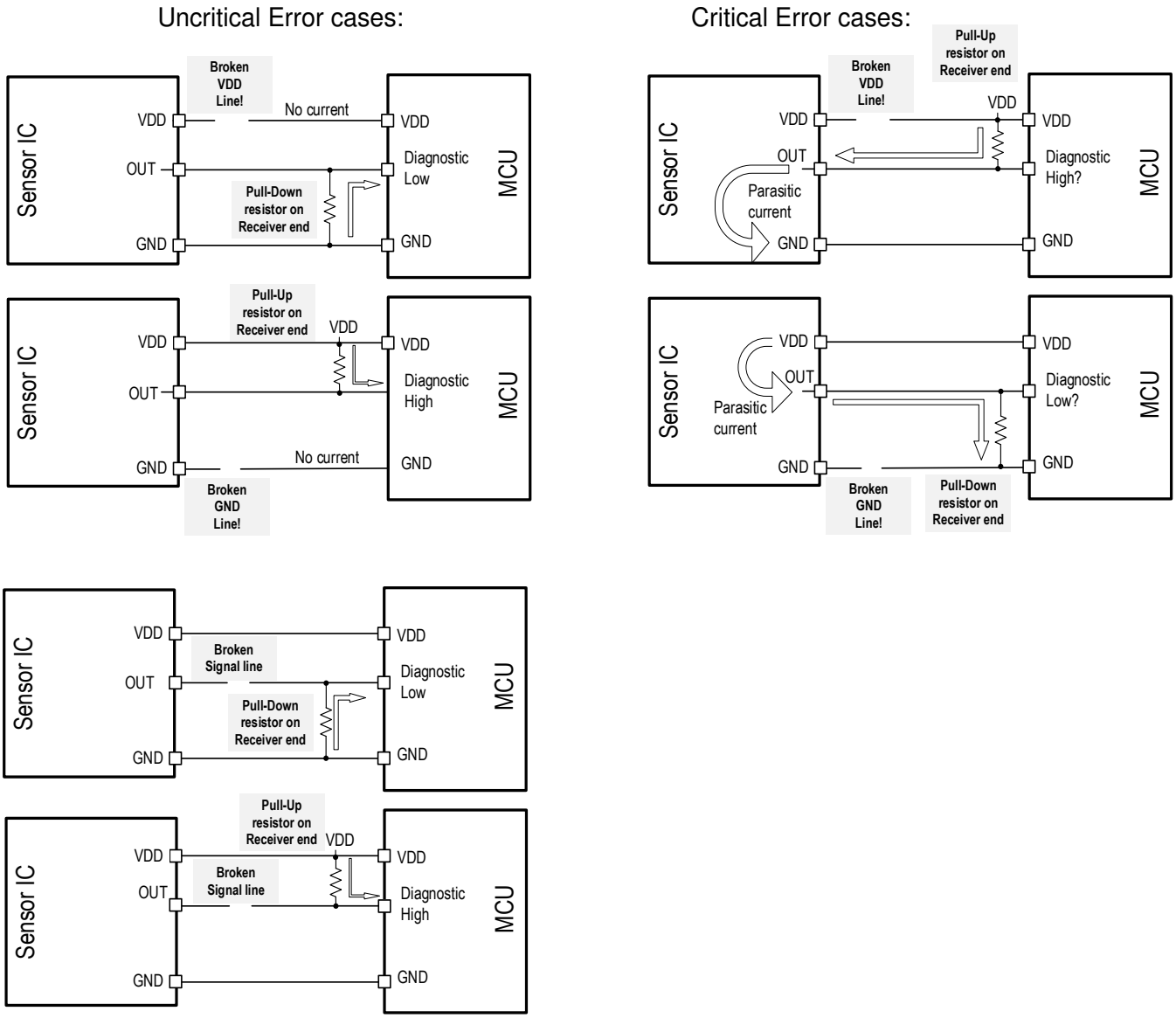


Table 24. Diagnostic Levels with Pull-Up Resistors

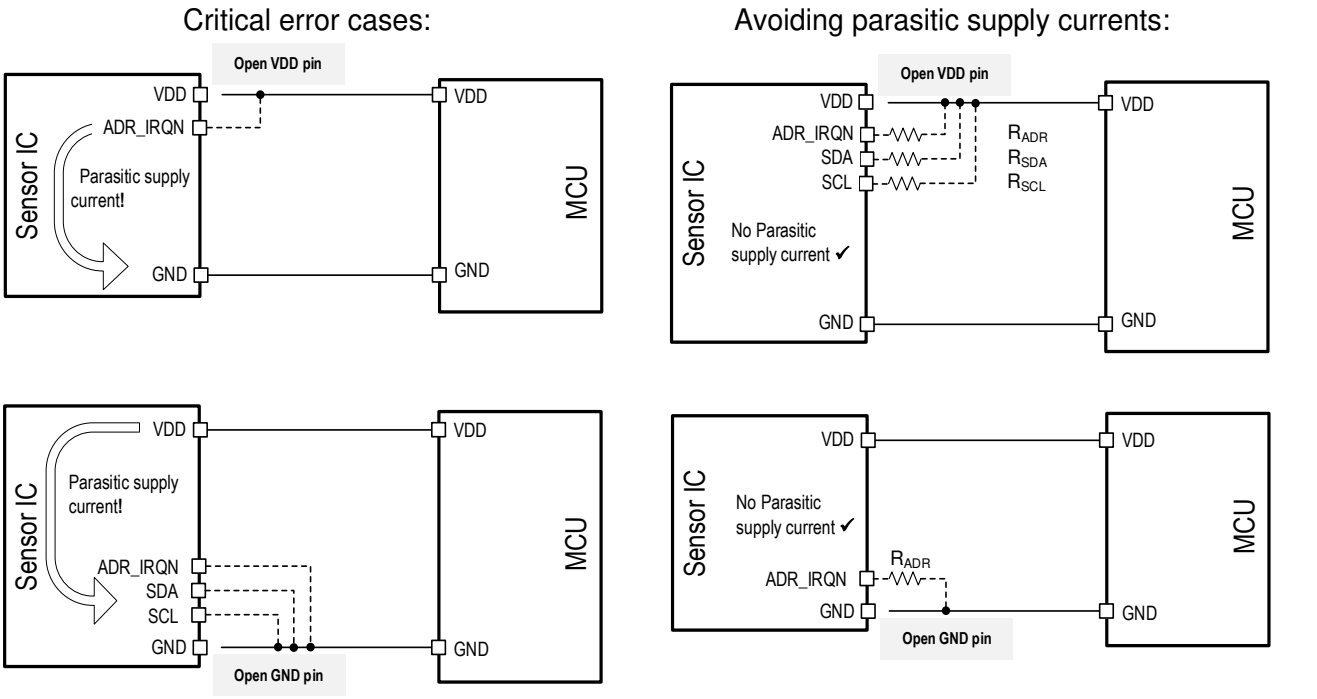
Diagnostic Level	>95% VDD	>96% VDD	>97%VDD	Unit
Error indication during normal operation	≤10			kΩ
Broken GND line	Not critical, see the uncritical error cases on Figure 25			kΩ
Broken VDD line, 5V mode	≤4.7	≤3.82	≤2.84	kΩ
Broken VDD line, 3.3V mode	≤3.96	≤3.2	≤2.4	kΩ

Table 25. Diagnostic Levels with Pull-Down Resistors

Diagnostic level	<3% VDD	<4% VDD	<5%VDD	Unit
Error indication during normal operation	≤10			kΩ
Broken VDD line	Not critical, see the uncritical error cases on Figure 25			kΩ
Broken GND line, 5V mode	≤1.48	≤2.0	≤2.56	kΩ
Broken GND line, 3.3V mode	≤1.65	≤2.23	≤2.85	kΩ

Another potential parasitic supply current path resulting from an open GND pin or open VDD pin may occur when the ADR_IRQN, SDA or SCL pins are directly connected to VDD or GND, see critical error cases on Figure 26. To avoid such parasitic supply currents, connect these pins to VDD or GND via a resistor, see avoiding parasitic supply currents on Figure 26. The specifed values for R_{ADR}, R_{SDA} and R_{SCL} are shown in Table 14.

Figure 26. Parasitic Supply Currents through ADR_IRQN, SDA and SCL Pins



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18.3 Diagnostic Features

The diagnostics described in Table 26 are performed on the chip level and are flagged in corresponding registers if a fault detection occurs. Each of these diagnostic functions can be enabled or disabled to generate an interrupt event at the ADR_IRQN output. In addition, an interrupt event can also be signaled through the high speed interface pins (SIN, SINN, COS, COSN; see Table 2) by putting them into the diagnostic state.

Alarm types marked as “Static” will remain set while the error persists and are cleared only by power-on-reset (POR); alarm types marked as “Temporary” will be cleared when the source of the error is removed.

Diagnostic flags marked as “Continuous” are continuously tested; diagnostic flags marked as “Start-up” are checked at start-up only.

Table 26. Diagnostic Features

Diagnostic Flag	Type	Active	Description
VDD over-voltage	Temporary	Continuous	If the external supply voltage exceeds the maximum limit, this flag is asserted. To avoid a flag toggling, a comparator hysteresis is implemented. See Table 7 for alarm levels in 3.3V Mode and Table 8 for alarm levels in 5V Mode.
VDD under-voltage	Temporary	Continuous	If the external supply voltage falls short of the minimum limit, this flag is asserted. To avoid flag toggling, a comparator hysteresis is implemented. See Table 7 for alarm levels in 3.3V Mode or Table 8 for alarm levels in 5V Mode.
VDDA under-voltage	Temporary	Continuous	Under-voltage condition at VDDA. See Table 7 for alarm levels in 3.3V Mode or Table 8 for alarm levels in 5V Mode.
Data access failure	Temporary	Continuous	Chip internal failure.
Protocol integrity failure	Temporary	Continuous	Failure in the I2C data transfer.
Shadow register DED	Static	Continuous	Shadow register bank double-bit error detection (DED).
Shadow register SED	Temporary	Continuous	Shadow register bank single-bit error detection (SED). Each single-bit error detection triggers a single-bit error correction (SEC) of the register output.
Nonvolatile memory DED	Static	Start-up	NVM double-bit error detection. Each individual addressed word is checked and flagged for bit error.
Nonvolatile memory SED	Temporary	Start-up	NVM single-bit error detection. Each individual addressed word is checked and flagged for bit errors. Each single-bit error detection will automatically trigger a single-bit error correction (SEC) of the NVM output.
LC oscillator frequency failure	Temporary	Continuous	This flag is set when the LC oscillator frequency is out of range. The frequency range is programmable.
LC oscillator general failure	Temporary	Continuous	This flag is set when the LC oscillator stops running.
Internal oscillator failure	Static	Continuous	Failure of the chip internal oscillator.
Internal bus failure	Temporary	Continuous	Chip internal failure.
IRQN watchdog failure	Static	Continuous	A cyclic interrupt request can be initiated by starting a watchdog counter. Once the timer is expired, the interrupt flag is asserted and the timer will be restarted. The timer can be stopped by resetting the watchdog value to zero.
Mechanical damage	Static	Continuous	The chip is checked for mechanical damage (cracks in the silicon).
Output buffer failure	Temporary	Continuous	This flag is set when the mean value of analog outputs (SIN+SINN) or (COS+COSN) differs from (VDD/2) by more than specified limits, see parameter DC_{OFF_AL} in Table 12. This error always turns off the analog outputs, regardless of the analog output diagnostics mode.
	Static		If the output buffer failure condition still persists after eight temporary buffer failure checks, all four analog outputs are permanently turned off to avoid overheating of the chip and the static output buffer failure flag is set. This state can be cleared by power-on-reset or by clearing the static output buffer failure flag through the I2C interface.

Diagnostic Flag	Type	Active	Description
Output buffer overload	Temporary	Continuous	This flag is set when the load current on one or more analog output buffers is above the over-current limit (I_{OVL}). After a debounce time t_{oc_assert} , all four outputs are switched off (tri-state). A temporary output overload check is performed following debounce time $t_{oc\_deassert}$: the outputs are turned on and the over-current condition is asserted again. See Table 12 and Table 13 for parameters.
	Static		If the output overload condition still persists after 8 temporary output overload checks, all four analog outputs are permanently turned off to avoid overheating of the chip and the static output buffer overload flag is set. This state can be cleared by power-on-reset or by clearing the static output buffer overload flag through the I2C interface.
Receiver coils failure	Temporary	Continuous	This flag is set if one of the following malfunctions of the receiver coils occurs: short between coils, short to GND, short to VDD, open coil.
Transmitter coil failure	Temporary	Continuous	This flag is set if there is failure at the transmitter coil.
Junction temperature warning/failure	Temporary	Continuous	Over-temperature warning or failure of the chip internal temperature sensor.
Internal supply failure	Static	Continuous	Failure of the chip's internal supply voltages.
AGC error	Temporary	Continuous	This flag is set when the gain of the AGC has reached user programmed limits.
Internal digital error	Static	Continuous	Error of the internal digital circuit.
BIST diagnostics error	Static	Start-up	Failure of self-test mechanisms.

18.4 Internal Register and Memory Errors

For all registers, volatile and nonvolatile memories, an error correcting code (ECC) is implemented, allowing 2-bit error detection and 1-bit error correction. An alarm flag is set when an ECC error occurs.

18.5 LC Oscillator Frequency Out of Range

The typical LC oscillator frequency ranges from ~2MHz to 5MHz, between the medium-wave radio band (0.52MHz to 1.73MHz) and the short-wave radio band (5.8MHz to 6.3MHz). Due to the use of external components (printed inductor and discrete capacitor), the transmitter oscillation frequency will change over temperature, mainly depending on the temperature coefficient of the discrete capacitor (see C_T in the application circuit on page 1, C_{Tx1} and C_{Tx2} in Figure 2 and Figure 3).

Recommendation: Use a capacitor with a low temperature coefficient.

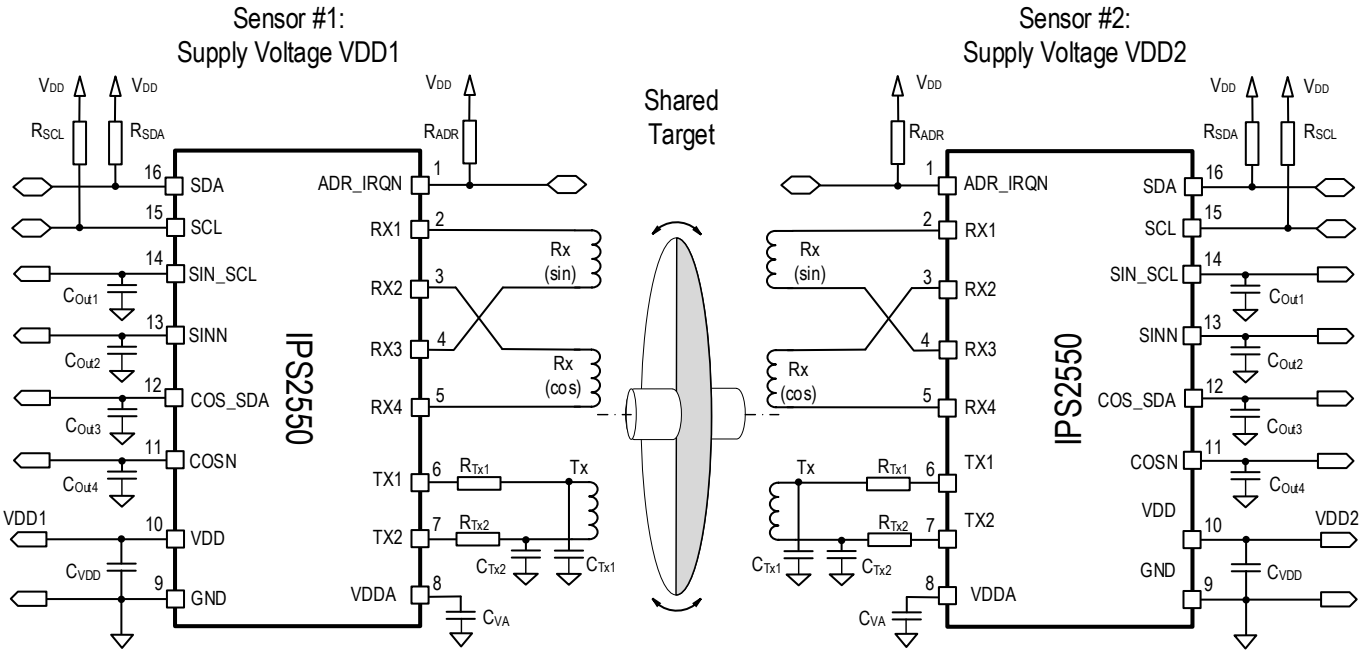
In order to ensure that the oscillation frequency is within the boundaries of a given application, the oscillation frequency of the transmitter oscillator is internally measured and stored as a proportional value in a register. The user can select upper and lower limits for these register values that will create an alarm flag when the oscillation frequency is outside of these programmable boundaries.

19. Redundant Connections

In applications requiring extended reliability, a redundant set-up using two separate IPS2550 circuits can be used, as shown in Figure 27. Physically, they share the same target and share the same coil area but are electrically isolated from one another with the transmitter and receiver coils placed at different PCB layers.

Depending on the coil design, the two transmitter coils can be magnetically coupled with each other. For fail-safe operation, the ideal coupling between the two transmitter coils needs to be evaluated in each case.

Figure 27. Application Diagram: Dual Redundant Sensors, Dual Supply



20. Application Examples

Typical coil and target arrangements are shown in Figure 28 to Figure 31: As examples, rotary designs for 1 × 360°, 2 × 180°, 3 × 120° and 4 × 90° are shown. Many other combinations (essentially any *n* x 360/*n*) are possible, where *n* is an integer number.

For example, in sensor designs for brushless DC rotor position feedback, *n* could be the number of pole pairs on the rotor. In such cases, the output signal of the IPS2550 would be one electric period per each pole pair.

Note that multi-periodic designs improve the mechanical accuracy, compared to a one-periodic coil design. A 4-periodic coil design (4 × 90°) has a typical mechanical accuracy of ±0.2% per 90° = ±0.18°

Figure 28. Coil Design and Signal Output for a 360° Rotary Sensor

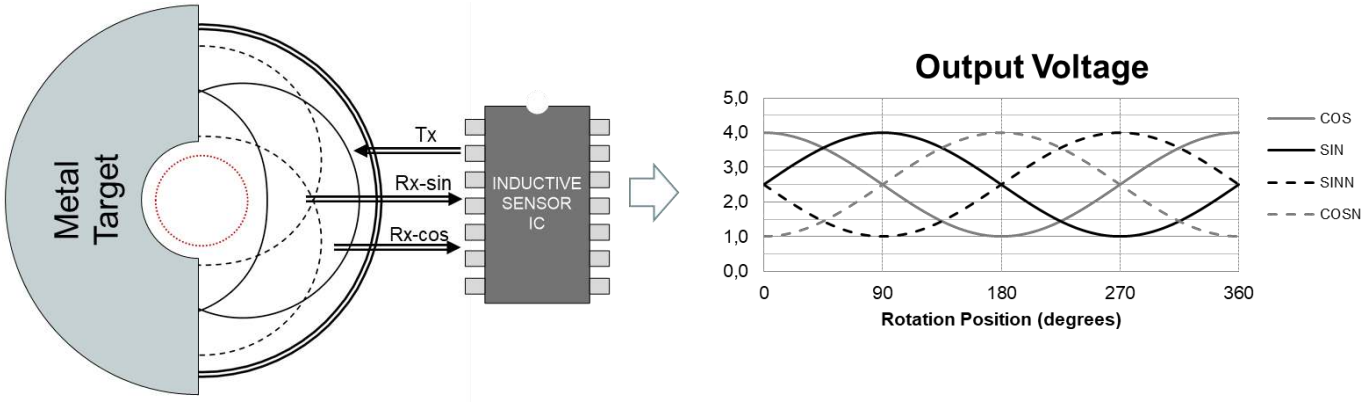


Figure 29. Coil Design and Signal Output for a 2 × 180° Rotary Sensor

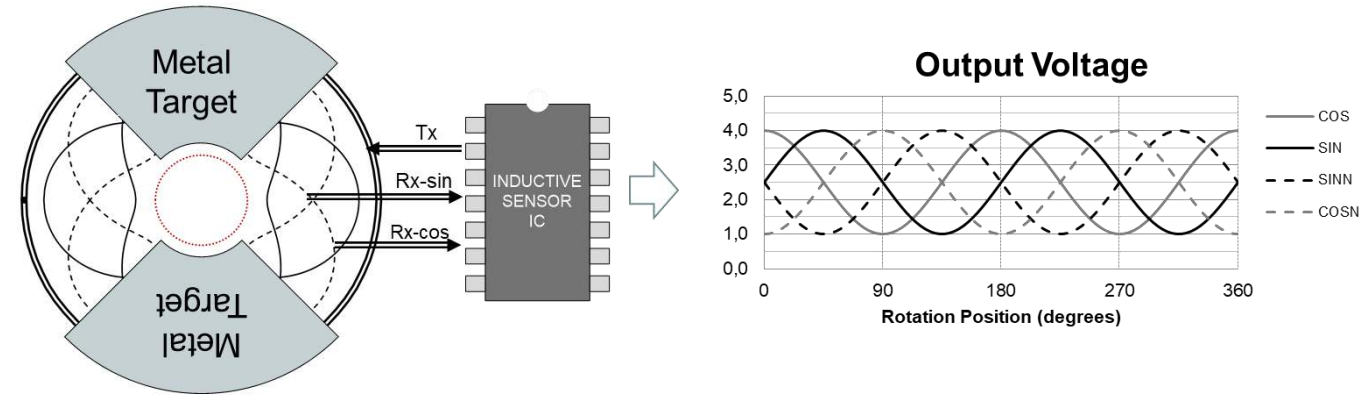


Figure 30. Coil Design and Signal Output for a 3 × 120° Rotary Sensor

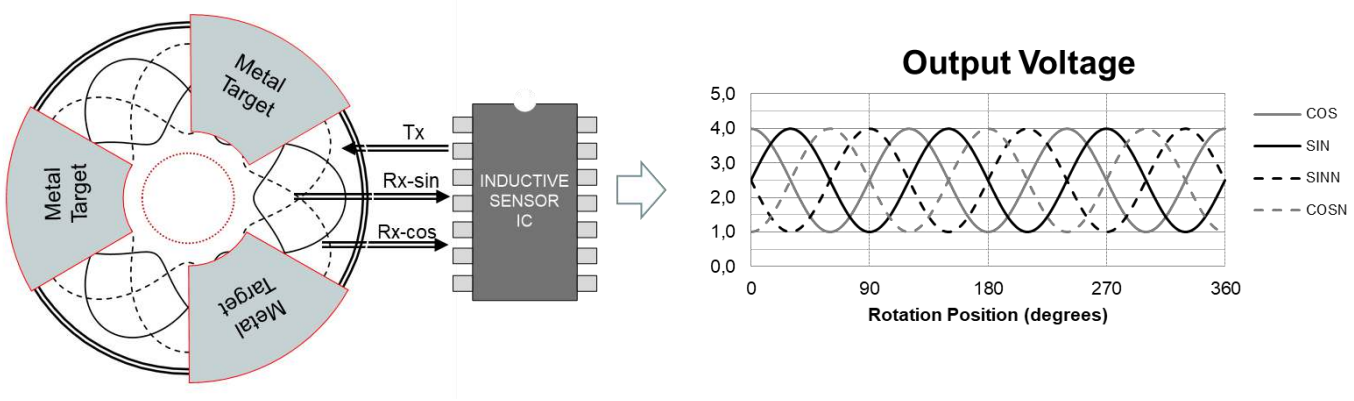
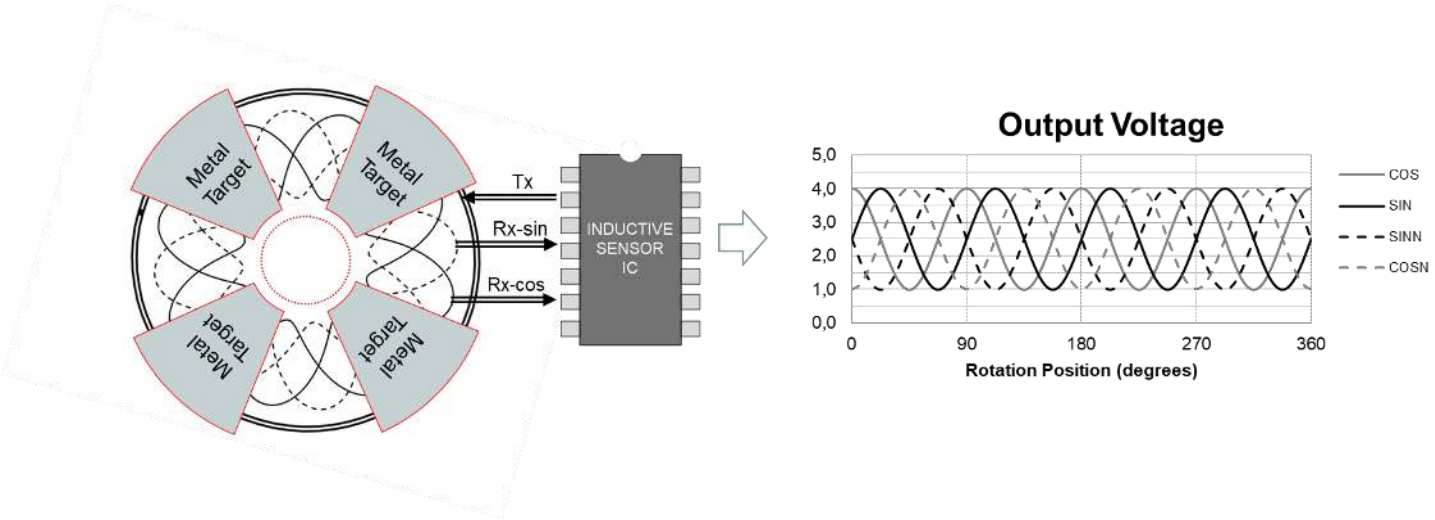


Figure 31. Coil Design and Signal Output for a 4 × 90° Rotary Sensor



21. Electromagnetic Compatibility (EMC)

Guidelines for EMC compliant circuit designs are available in a separate document “IPS2550 EMC recommendations” on request.

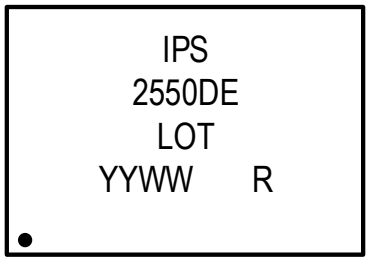
22. 16-TSSOP Package Outline Drawings

The package outline drawings are appended at the end of this document and are accessible from the link below. The package information is the most current data available.

https://www.renesas.com/sg/en/document/psc/16-tssop-package-outline-drawing-50-x-44-mm-body-epad-27-x-33-mm-065mm-pitch-eng16p3

23. Marking Diagram

23.1 Marking of Production Parts



Line 1: First characters of part code (IPS); “ES” is added for engineering samples
Line 2: Next four characters of the part code (2550) followed by
D = Design revision
E = Operation temperature range, Extended automotive
Line 3: “LOT” = Lot number
Line 4: “YYWW” = Manufacturing date:
YY = last two digits of manufacturing year
WW = manufacturing week
R = RoHS compliant statement

24. Ordering Information

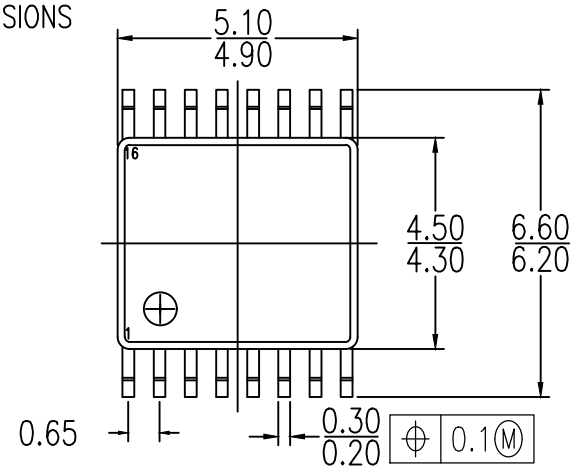
Orderable Part Number	Description and Package	MSL Rating	Carrier Type	Temperature
IPS2550DE1R	16-TSSOP with exposed pad, 4.4 ×5.0 mm	1	13” Reel, 4000 parts / reel	-40° to +160°C
IPS2550STKIT	IPS2550 Starter Kit including USB communication board, IPS2550 sensor module and connection cables			

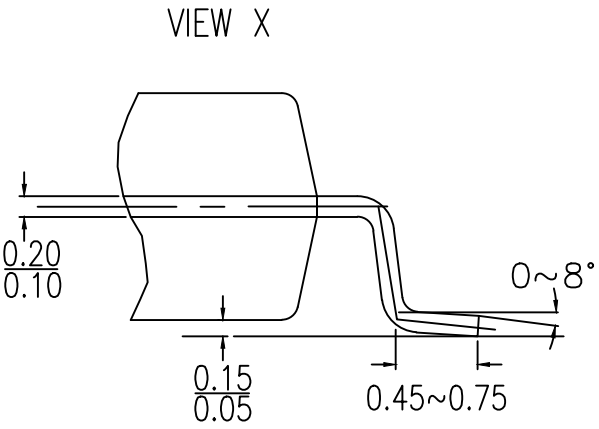
25. Revision History

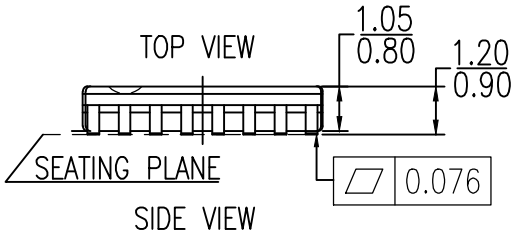
Revision Date	Description of Change
June 20, 2022	• Updated, functional safety statement on page 1 • 3.3V supply range definition: 3.3V ±0.3V • I2C default interface connection updated • Output common mode failure description updated • Section 18.2.1.2: broken wires • More detailed specification of propagation delay, Table 18 • AGC, chapter 14.3.5 updated: added Figure 12, updated Table 11 • Figure 7 to Figure 10, Figure 14, Figure 15, Figure 17 to Figure 20, Figure 22, Figure 25, Figure 26, Table 12, Table 14,Table 17, Table 21,Table 26 updated
January 11, 2022	• Parameter descriptions V_{IH} V_{IL} corrected in • Table 15 and Table 16 • COS Signal labeling corrected in Figure 28 to Figure 31
September 14, 2021	Reference updated in Programming Options section
September 8, 2021	Added description of output buffer overload protection in Table 12 and Table 26
June 24, 2021	Minor corrections throughout the document
June 2, 2021	Section 15.3.2 updated with hardware pin strapping information.
January 26, 2021	Initial release

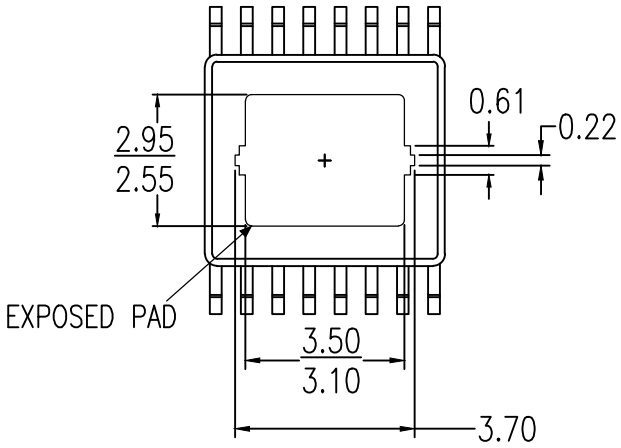
BASED ON JEDEC JEP95: MO-153

1. DIMENSIONS



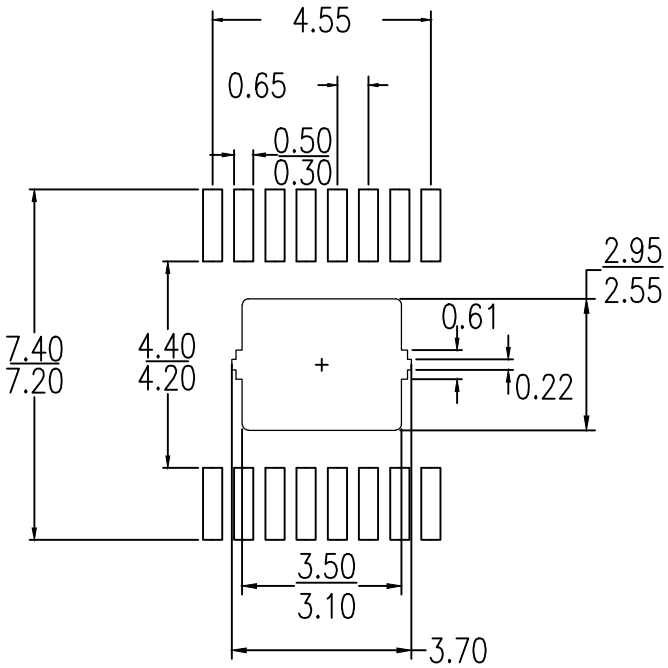






2. WEIGHT ≤ 0.05 g
3. BODY MATERIAL LOW STRESS EPOXY
4. LEAD MATERIAL Cu-ALLOY
5. LEAD FINISH SOLDER PLATING
6. LEAD FORM Z-BENDS

* WITHOUT MOLD FLASH
DIMENSIONS IN MILLIMETERS



LAND PATTERN DIMENSIONS

NOTE:
1. ALL DIMENSIONS ARE IN MILLIMETERS

Package Revision History		
Date Created	Rev No.	Description
Aug 27, 2021	Rev 03	Turn Off AutoCad SHX Software Setting
Aug 13, 2021	Rev 02	Update Exposed pad tolerance.
April 2, 2020	Rev 01	Update Epad Shape.
Dec 4, 2019	Rev 00	Initial Release

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