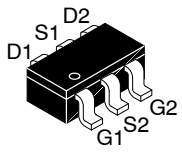
# Field Effect Transistor - Dual, N & P-Channel, Enhancement Mode

# NDC7001C




**TSOT23 6−Lead**
**SUPERSOT−6**
**CASE 419BL**

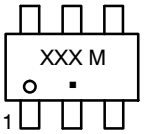
## General Description

These dual N & P−Channel Enhancement Mode Field Effect Transistors are produced using **onsemi**'s proprietary, high cell density, DMOS technology. This very high density process has been designed to minimize on−state resistance, provide rugged and reliable performance and fast switching. These device is particularly suited for low voltage, low current, switching, and power supply application.

## Features

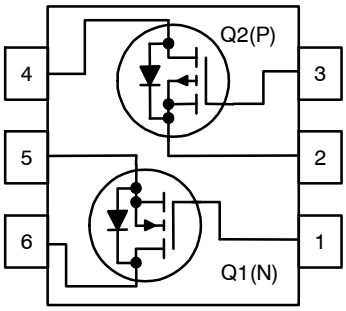
- Q1 0.51 A, 60 V
  $R_{DS(ON)}$ = 2 Ω @ $V_{GS}$ = 10 V
  $R_{DS(ON)}$ = 4 Ω @ $V_{GS}$ = 4.5 V
- Q2 –0.34 A, 60 V
  $R_{DS(ON)}$ = 5 Ω @ $V_{GS}$ = –10 V
  $R_{DS(ON)}$ = 7.5 Ω @ $V_{GS}$ = –4.5 V
- High Saturation Current
- High Density Cell Design for Low $R_{DS(ON)}$
- Proprietary SUPERSOT™ −6 Package Design Using Copper Lead Frame for Superior Thermal and Electrical Capabilities
- This is a Pb−Free Device

## MARKING DIAGRAM




XXX = Specific Device Code
M = Date Code
▪ = Pb−Free Package

## PINOUT




## ORDERING INFORMATION

See detailed ordering and shipping information on page 8 of this data sheet.

## ABSOLUTE MAXIMUM RATINGS ($T_A$ = 25°C unless otherwise noted)

| Symbol | Parameter | | Q1 | Q2 | Unit |
|---|---|---|---|---|---|
| $V_{DSS}$ | Drain−Source Voltage | | 60 | −60 | V |
| $V_{GSS}$ | Gate−Source Voltage | | ±20 | ±20 | V |
| $I_D$ | Drain Current | − Continuous (Note 1a) | 0.51 | −0.34 | A |
| | | − Pulsed | 1.5 | −1 | A |
| $P_D$ | Power Dissipation for Single Operation | (Note 1a) | 0.96 | | W |
| | | (Note 1b) | 0.9 | | W |
| | | (Note 1c) | 0.7 | | W |
| $T_J$, $T_{STG}$ | Operating and Storage Temperature Range | | −55 to +150 | | °C |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

## THERMAL CHARACTERISTICS

| Symbol | Parameter | Ratings | Unit |
|---|---|---|---|
| $R_{\theta JA}$ | Thermal Resistance, Junction to Ambient (Note 1a) | 130 | °C/W |
| $R_{\theta JC}$ | Thermal Resistance, Junction to Case (Note 1) | 60 | °C/W |

**ELECTRICAL CHARACTERISTICS** ($T_A$ = 25°C unless otherwise noted)

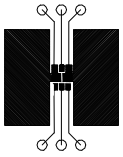
| Symbol | Parameter | | Test Conditions | | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | | | | |
| $BV_{DSS}$ | Drain–Source Breakdown Voltage | | $V_{GS}$ = 0 V, $I_D$ = 250 μA<br>$V_{GS}$ = 0 V, $I_D$ = –250 μA | *Q1*<br>*Q2* | 60<br>–60 | –<br>– | –<br>– | V |
| $\frac{\Delta BV_{DSS}}{\Delta T_J}$ | Breakdown Voltage Temperature Coefficient | | $I_D$ = 250 μA,Ref. to 25°C<br>$I_D$ = –250 μA,Ref. to 25°C | *Q1*<br>*Q2* | –<br>– | 67<br>–57 | –<br>– | mV/°C |
| $I_{DSS}$ | Zero Gate Voltage Drain Current | | $V_{DS}$ = 48 V, $V_{GS}$ = 0 V<br>$V_{DS}$ = –48 V, $V_{GS}$ = 0 V | *Q1*<br>*Q2* | –<br>– | –<br>– | 1<br>–1 | μA |
| $I_{GSSF}$ | Gate–Body Leakage, Forward | | $V_{GS}$ = 20 V, $V_{DS}$ = 0 V | *All* | – | – | 100 | nA |
| $I_{GSSR}$ | Gate–Body Leakage, Reverse | | $V_{GS}$ = –20 V, $V_{DS}$ = 0 V | *All* | – | – | –100 | nA |
| **ON CHARACTERISTICS** (Note 2) | | | | | | | | |
| $V_{GS(th)}$ | Gate Threshold Voltage | *Q1* | $V_{DS}$ = $V_{GS}$, $I_D$ = 250 μA | | 1 | 2.1 | 2.5 | V |
| | | *Q2* | $V_{DS}$ = $V_{GS}$, $I_D$ = –250 μA | | –1 | –1.9 | –3.5 | |
| $\frac{\Delta V_{GS(th)}}{\Delta T_J}$ | Gate Threshold Voltage Temperature Coefficient | *Q1* | $I_D$ = 250 μA, Referenced to 25°C | | – | –3.8 | – | mV/°C |
| | | *Q2* | $I_D$ = –250 μA, Ref. to 25°C | | – | 3.2 | – | |
| $R_{DS(on)}$ | Static Drain–Source On–Resistance | *Q1* | $V_{GS}$ = 10 V, $I_D$ = 0.51 A<br>$V_{GS}$ = 4.5 V, $I_D$ = 0.35 A<br>$V_{GS}$ = 10 V, $I_D$ = 0.51 A, $T_J$ = 125°C | | –<br>–<br>– | 1<br>2<br>1.7 | 2<br>4<br>3.5 | Ω |
| | | *Q2* | $V_{GS}$ = –10 V, $I_D$ = –0.34 A<br>$V_{GS}$ = – 4.5 V, $I_D$ = –0.25 A<br>$V_{GS}$ = –10 V, $I_D$ = –0.34 A, $T_J$ = 125°C | | –<br>–<br>– | 1.2<br>1.5<br>1.9 | 5<br>7.5<br>10 | |
| $I_{D(on)}$ | On–State Drain Current | *Q1* | $V_{GS}$ = 10 V, $V_{DS}$ = 10 V | | 1.5 | – | – | A |
| | | *Q2* | $V_{GS}$ = –10 V, $V_{DS}$ = –10 V | | –1 | – | – | |
| $g_{FS}$ | Forward Transconductance | *Q1* | $V_{DS}$ = 10 V, $I_D$ = 0.51 A | | – | 380 | – | mS |
| **DYNAMIC CHARACTERISTICS** | | | | | | | | |
| $C_{iss}$ | Input Capacitance | *Q1* | For *Q1*:<br>$V_{DS}$ = 25 V, $V_{GS}$ = 0 V<br>f = 1.0 MHz | | – | 20 | – | pF |
| | | *Q2* | | | – | 66 | – | |
| $C_{oss}$ | Output Capacitance | *Q1* | For *Q2*:<br>$V_{DS}$ = –25 V, $V_{GS}$ = 0 V<br>f = 1.0 MHz | | – | 11 | – | pF |
| | | *Q2* | | | – | 13 | – | |
| $C_{rss}$ | Reverse Transfer Capacitance | *Q1* | | | – | 4.3 | – | pF |
| | | *Q2* | | | – | 6 | – | |
| $R_G$ | Gate Resistance | *Q1* | $V_{GS}$ = 15 mV, f = 1.0 MHz | | – | 11.2 | – | Ω |
| | | *Q2* | | | – | 11.2 | – | |
| **SWITCHING CHARACTERISTICS** (Note 2) | | | | | | | | |
| $t_{d(on)}$ | Turn–On Delay Time | *Q1* | For *Q1*:<br>$V_{DS}$ = 25 V, $I_{DS}$ = 1 A<br>$V_{GS}$ = 10 V, $R_{GEN}$ = 6 Ω | | – | 2.8 | 5.6 | ns |
| | | *Q2* | | | – | 3.2 | 6.4 | |
| $t_r$ | Turn–On Rise Time | *Q1* | For *Q2*:<br>$V_{DS}$ = –25 V, $I_{DS}$ = –1 A<br>$V_{GS}$ = –10 V, $R_{GEN}$ = 6 Ω | | – | 8 | 16 | ns |
| | | *Q2* | | | – | 10 | 20 | |
| $t_{d(off)}$ | Turn–Off Delay Time | *Q1* | | | – | 14 | 26 | ns |
| | | *Q2* | | | – | 8 | 16 | |
| $t_f$ | Turn–Off Fall Time | *Q1* | | | – | 4 | 8 | ns |
| | | *Q2* | | | – | 1 | 2 | |
| $Q_g$ | Total Gate Charge | *Q1* | For *Q1*:<br>$V_{DS}$ = 25 V, $I_{DS}$ = 0.51 A<br>$V_{GS}$= 10 V, $R_{GEN}$ = 6 Ω | | – | 1.1 | 1.5 | nC |
| | | *Q2* | | | – | 1.6 | 2.2 | |
| $Q_{gs}$ | Gate–Source Charge | *Q1* | For *Q2*:<br>$V_{DS}$ = –25 V, $I_{DS}$ = –0.35 A<br>$V_{GS}$ = –10 V, $R_{GEN}$ = 6 Ω | | – | 0.2 | – | nC |
| | | *Q2* | | | – | 0.3 | – | |
| $Q_{gd}$ | Gate–Drain Charge | *Q1* | | | – | 0.4 | – | nC |

**ELECTRICAL CHARACTERISTICS** ($T_A$ = 25°C unless otherwise noted) (continued)

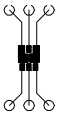
| Symbol | Parameter | | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| **DRAIN–SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS** | | | | | | | |
| $I_S$ | Maximum Continuous Drain–Source Diode Forward Current | | *Q1* | – | – | 0.51 | A |
| | | | *Q2* | – | – | –0.34 | |
| $V_{SD}$ | Drain–Source Diode Forward Voltage | *Q1* | $V_{GS}$ = 0 V, $I_S$ = 0.51 A (Note 2) | – | 0.8 | 1.2 | V |
| | | *Q2* | $V_{GS}$ = 0 V, $I_S$ = –0.34 A (Note 2) | – | –0.8 | –1.4 | |
| $t_{rr}$ | Diode Reverse Recovery Time | *Q1* | $I_F$ = 0.51 A, $d_{iF}/d_t$ = 100 A/μs | – | 18 | – | nS |
| | | *Q2* | $I_F$ = –0.34 A, $d_{iF}/d_t$ = 100 A/μs | – | 16 | – | |
| $Q_{rr}$ | Diode Reverse Recovery Charge | *Q1* | $I_F$ = 0.51 A, $d_{iF}/d_t$ = 100 A/μs | – | 16 | – | nC |
| | | *Q2* | $I_F$ = –0.34 A, $d_{iF}/d_t$ = 100 A/μs | – | 11 | – | |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

1. $R_{\theta JA}$ is the sum of the junction–to–case and case–to–ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a. 130°C/W when mounted on a 0.125 $in^2$ pad of 2 oz. copper.



b. 140°C/W when mounted on a .005 $in^2$ pad of 2 oz. copper.

c. 180°C/W when mounted on a minimum pad.

Scale 1:1 on letter size paper

2. Pulse Test: Pulse Width < 300 μs, Duty cycle < 2.0 %.

## TYPICAL CHARACTERISTICS: N−CHANNEL

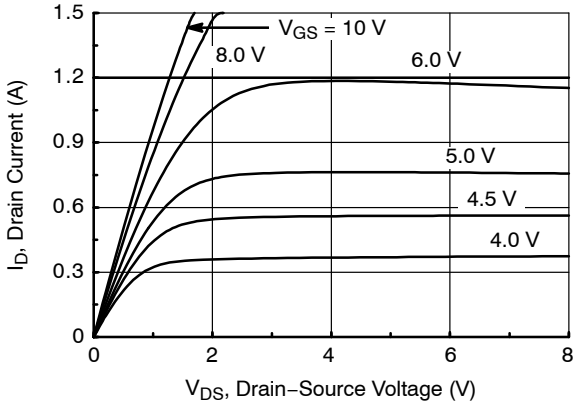



**Figure 1. On−Region Characteristics**

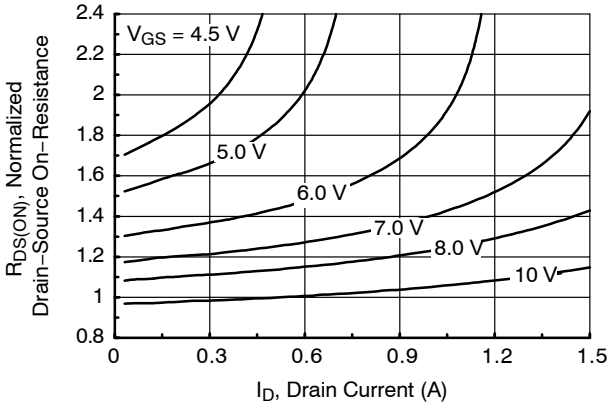



**Figure 2. On−Resistance Variation with Drain Current and Gate Voltage**

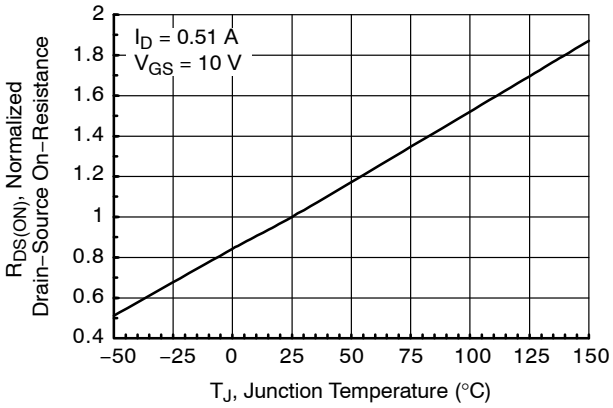



**Figure 3. On−Resistance Variation with Temperature**

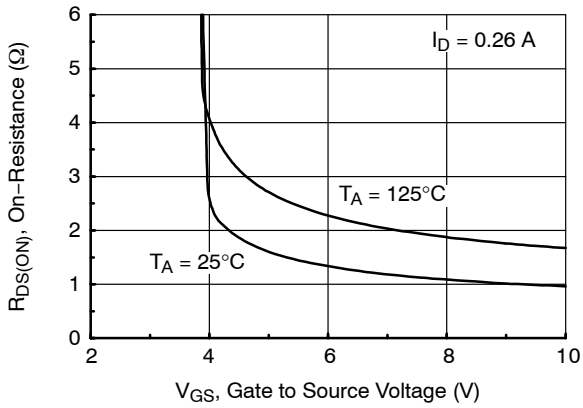



**Figure 4. On−Resistance Variation with Gate−to−Source Voltage**

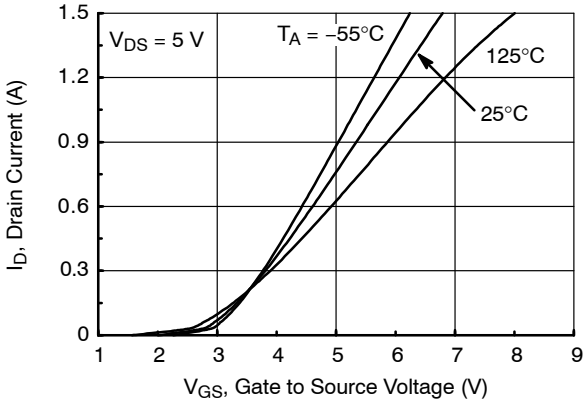



**Figure 5. Transfer Characteristics**

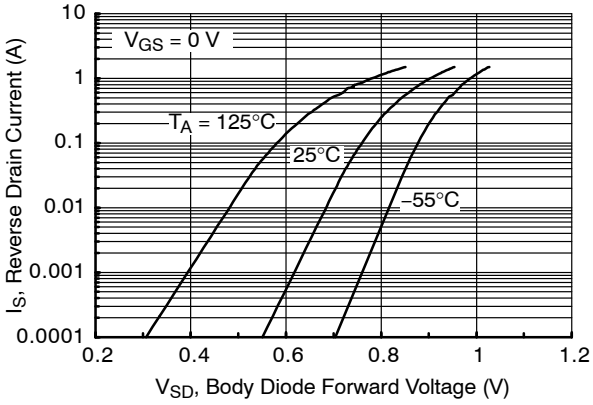



**Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature**

## TYPICAL CHARACTERISTICS: N−CHANNEL (continued)

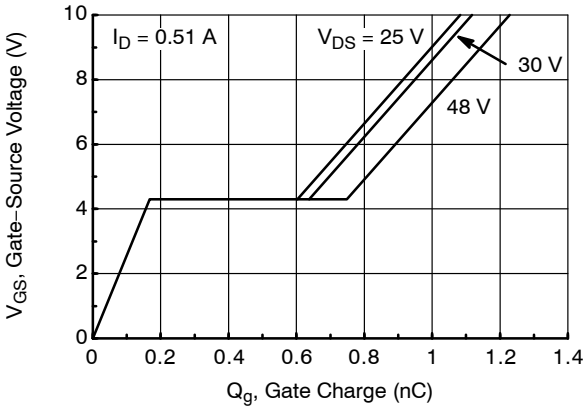



**Figure 7. Gate Charge Characteristics**

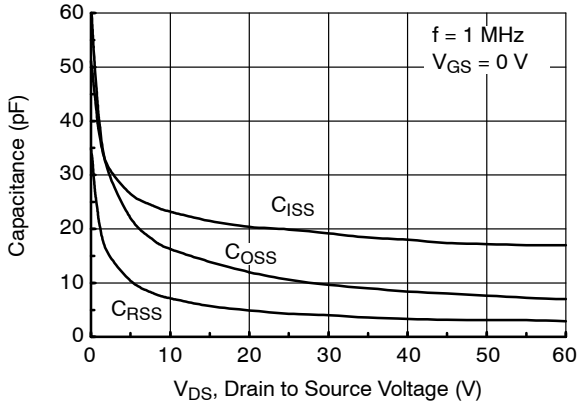



**Figure 8. Capacitance Characteristics**

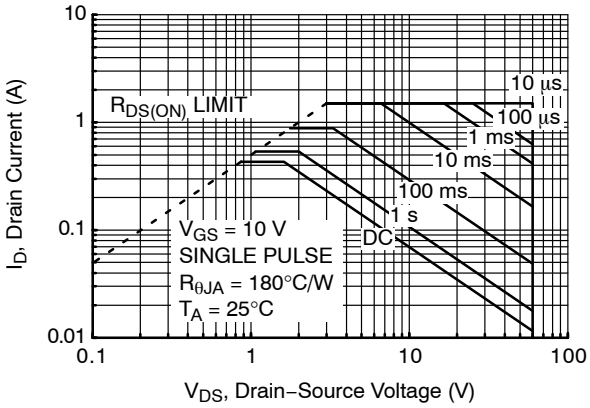



**Figure 9. Maximum Safe Operating Area**

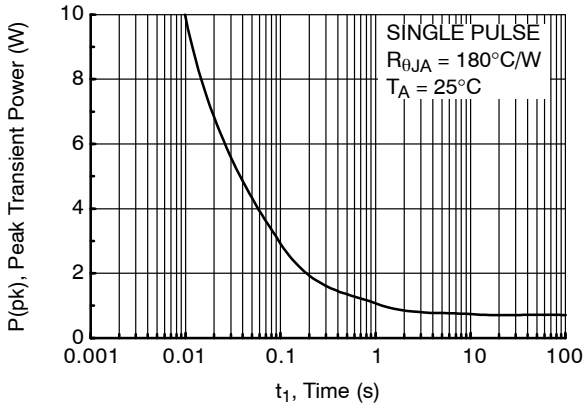



**Figure 10. Single Pulse Maximum Power Dissipation**

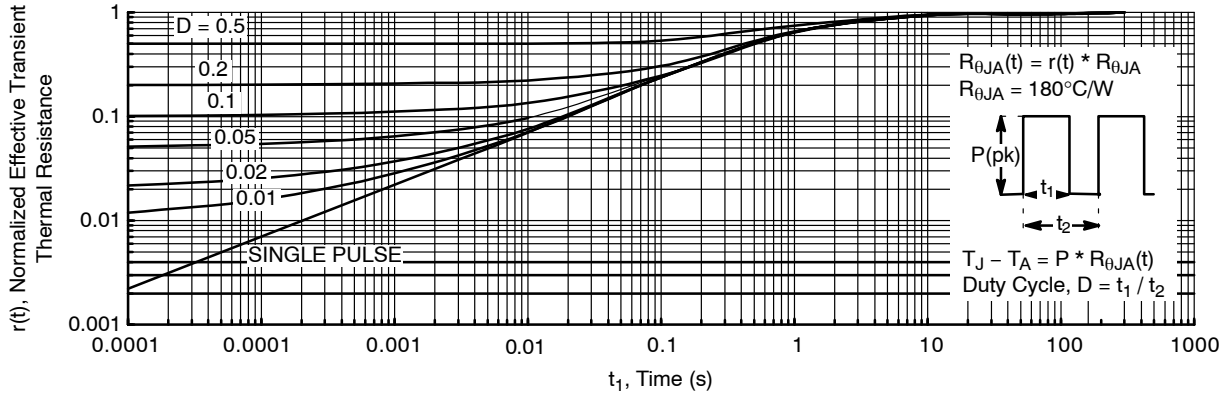



**Figure 11. Transient Thermal Response Curve**

(Note: Thermal characterization performed using the conditions described in Note 1c. Transient thermal response will change depending on the circuit board design.)

## TYPICAL CHARACTERISTICS: P−CHANNEL

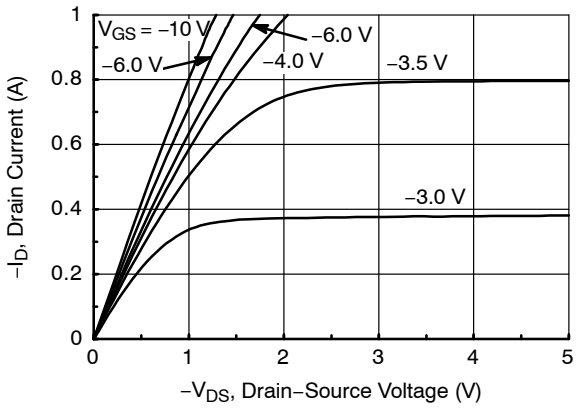



**Figure 12. On−Region Characteristics**

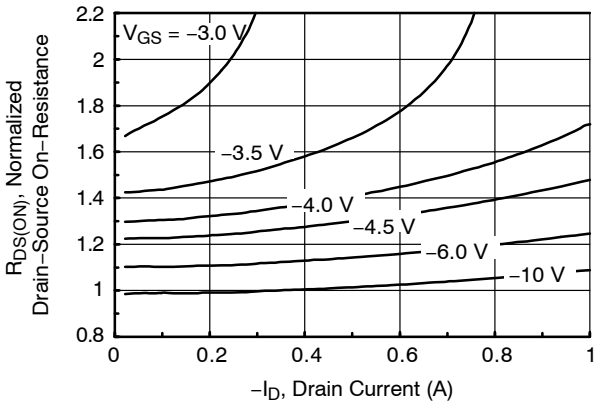



**Figure 13. On−Resistance Variation with Drain Current and Gate Voltage**

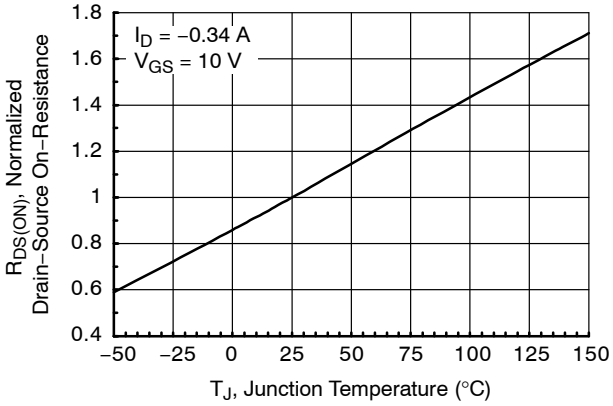



**Figure 14. On−Resistance Variation with Temperature**

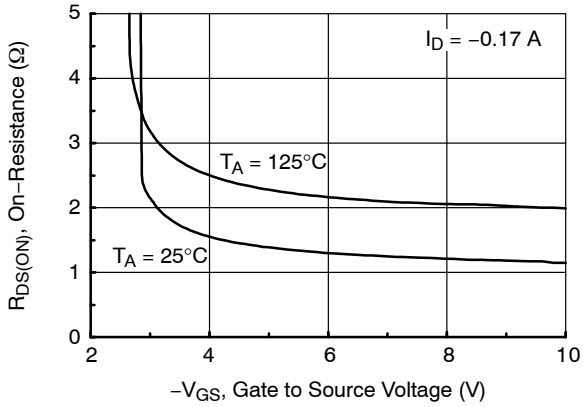



**Figure 15. On−Resistance Variation with Gate−to−Source Voltage**

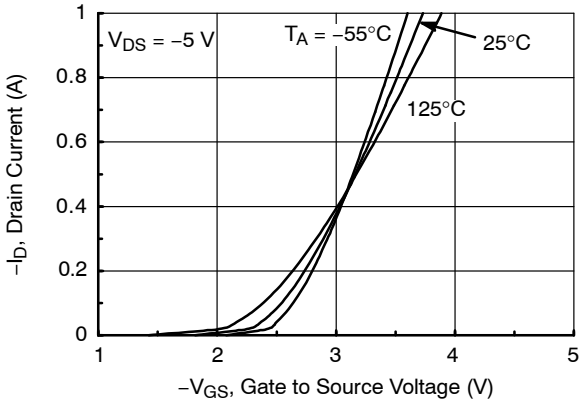



**Figure 16. Transfer Characteristics**

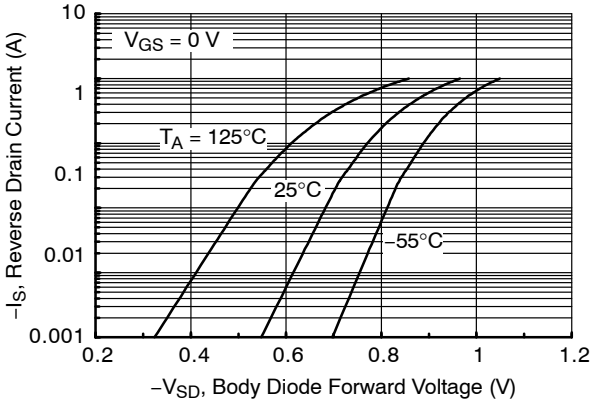



**Figure 17. Body Diode Forward Voltage Variation with Current and Temperature**

## TYPICAL CHARACTERISTICS: P−CHANNEL (continued)

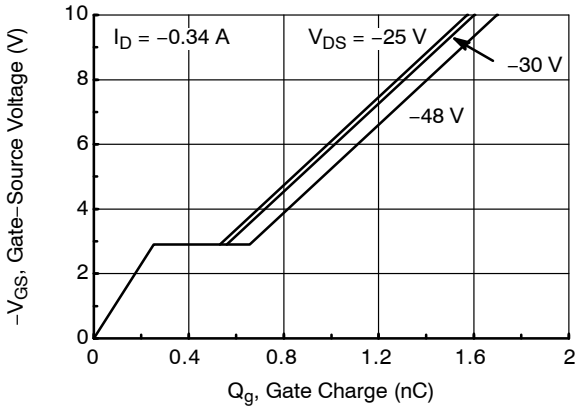



**Figure 18. Gate Charge Characteristics**

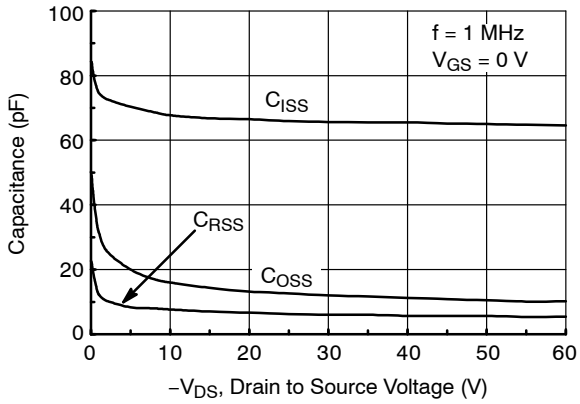



**Figure 19. Capacitance Characteristics**

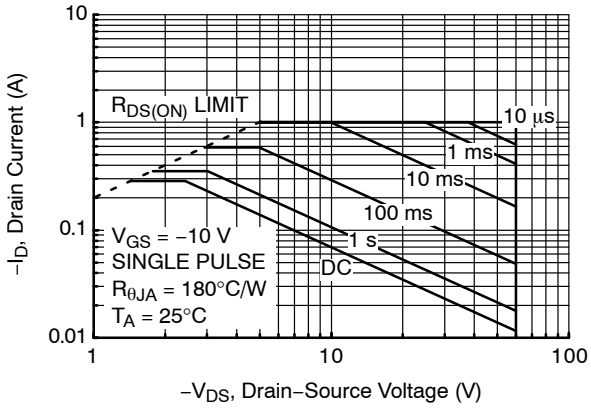



**Figure 20. Maximum Safe Operating Area**

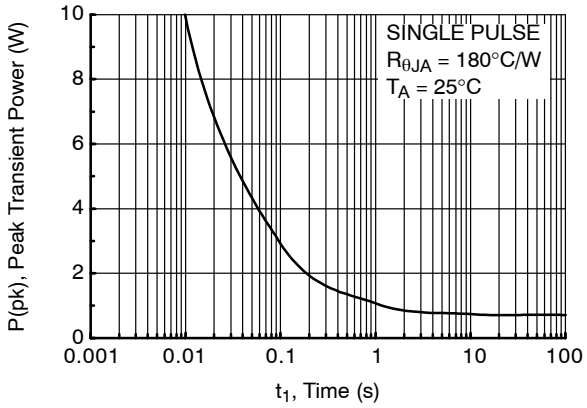



**Figure 21. Single Pulse Maximum Power Dissipation**

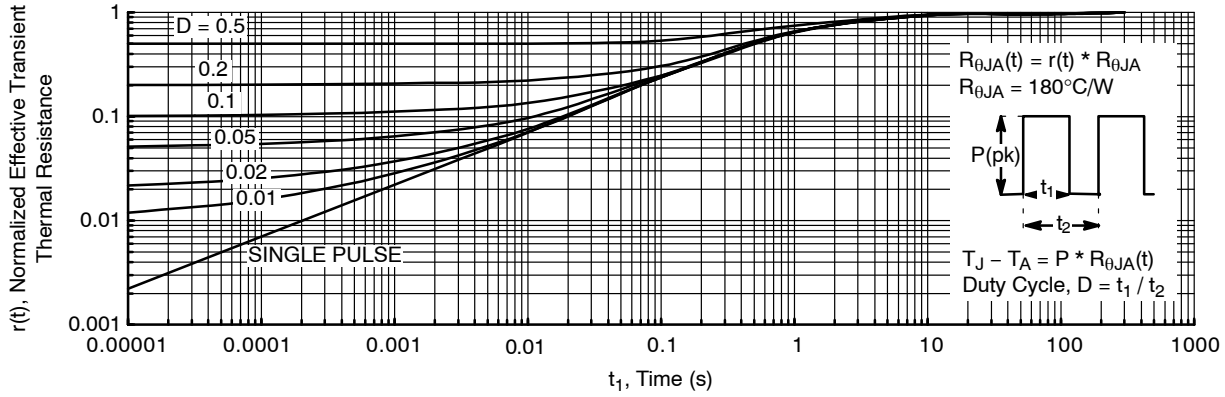



**Figure 22. Transient Thermal Response Curve**

(Note: Thermal characterization performed using the conditions described in Note 1c. Transient thermal response will change depending on the circuit board design.)

## ORDERING INFORMATION

| Device | Device Marking | Package Type | Reel Size | Tape Width | Shipping† |
|---|---|---|---|---|---|
| NDC7001C | .01 | TSOT−23−6<br>(Pb−free) | 7” | 8 mm | 3000 / Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

# MECHANICAL CASE OUTLINE
## PACKAGE DIMENSIONS

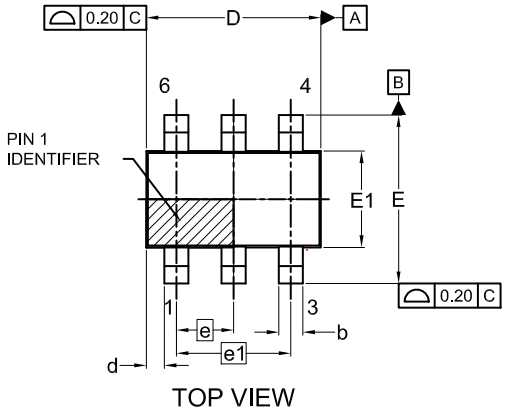
ON Semiconductor®

1

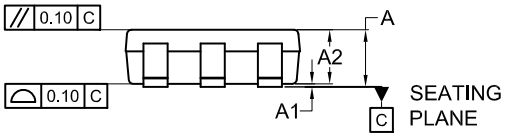
**SCALE 2:1**

**TSOT23 6−Lead**
CASE 419BL
ISSUE A

DATE 31 AUG 2020

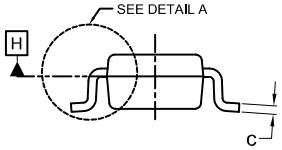



TOP VIEW

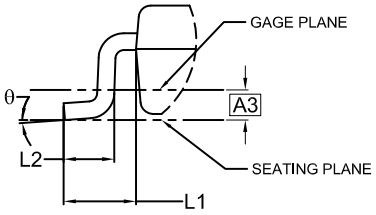



FRONT VIEW

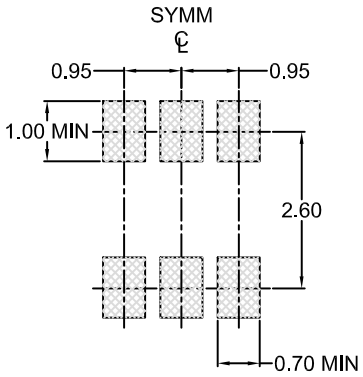
NOTE 4




SIDE VIEW




DETAIL A




LAND PATTERN
RECOMMENDATION

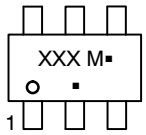
*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.25MM PER END. DIMENSIONS D AND E1 ARE DETERMINED AT DATUM H.
4. SEATING PLANE IS DEFINED BY THE TERMINALS. "A1" IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.

| DIM | MILLIMETERS | | |
|---|---|---|---|
| | MIN. | NOM. | MAX. |
| A | 0.90 | 1.00 | 1.10 |
| A1 | 0.00 | 0.05 | 0.10 |
| A2 | 0.70 | 0.85 | 1.00 |
| A3 | | 0.25 BSC | |
| b | 0.25 | 0.38 | 0.50 |
| c | 0.10 | 0.18 | 0.26 |
| D | 2.80 | 2.95 | 3.10 |
| d | | 0.30 REF | |
| E | 2.50 | 2.75 | 3.00 |
| E1 | 1.30 | 1.50 | 1.70 |
| e | | 0.95 BSC | |
| e1 | | 1.90 BSC | |
| L1 | | 0.60 REF | |
| L2 | 0.20 | 0.40 | 0.60 |
| θ | 0° | --- | 10° |

**GENERIC MARKING DIAGRAM***




XXX = Specific Device Code
M = Date Code
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present. Some products may not follow the Generic Marking.

| | | |
|---|---|---|
| **DOCUMENT NUMBER:** | **98AON83292G** | Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped “CONTROLLED COPY” in red. |
| **DESCRIPTION:** | **TSOT23 6−Lead** | **PAGE 1 OF 1** |

## ADDITIONAL INFORMATION

**TECHNICAL PUBLICATIONS**:
**Technical Library:** www.onsemi.com/design/resources/technical−documentation
**onsemi Website:** www.onsemi.com

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