

## FJ4B01100L1

## Single P-channel MOS FET

For Load switching circuits

### ■ Features

- Low Drain-source ON resistance:  $R_{ds(on)}$  typ. = 68 m $\Omega$  ( $V_{GS} = -2.5$  V)
- CSP (Chip Size Package)
- RoHS compliant (EU RoHS / MSL:Level 1 compliant)

### ■ Marking Symbol: 1D

### ■ Packaging

Embossed type (Thermo-compression sealing) : 1 000 pcs / reel (standard)

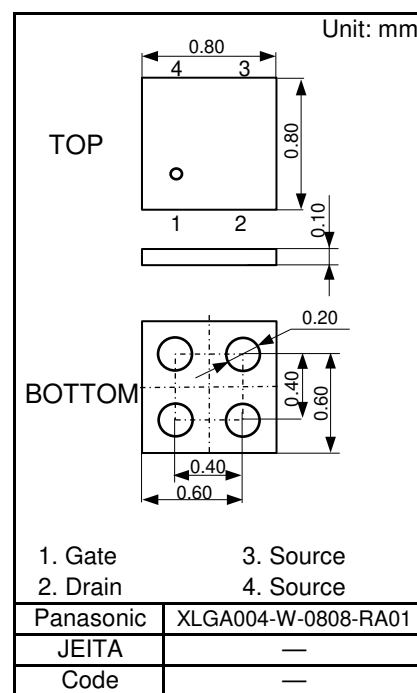
### ■ Absolute Maximum Ratings $T_a = 25$ °C

Parameter	Symbol	Rating	Unit
Drain-Source Voltage	VDS	-12	V
Gate-Source Voltage	VGS	$\pm 8$	V
Drain Current	ID1 <sup>*1</sup>	-2.2	A
	ID2 <sup>*2</sup>	-3.3	
	ID3 <sup>*3</sup>	-4.1	
Peak Drain Current	IDp1 <sup>*1*4</sup>	-17	A
	IDp2 <sup>*2*4</sup>	-26	
	IDp3 <sup>*3*4</sup>	-32	
Power Dissipation	PD1 <sup>*1</sup>	0.36	W
	PD2 <sup>*2</sup>	0.82	
	PD3 <sup>*3</sup>	1.3	
Channel Temperature	Tch	150	°C
Operating Ambient Temperature	Topr	-40 ~ +85	°C
Storage Temperature	Tstg	-55 ~ +150	°C

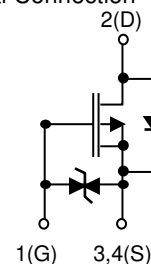
Note \*1 FR4 board (25.4mm×25.4mm×t1.0mm), Min Cu 36mm<sup>2</sup> Copper

\*2 FR4 board (25.4mm×25.4mm×t1.0mm), Full Cu

\*3 Ceramic substrate (70mm×70mm×t1.0mm)

\*4 t = 10  $\mu$ s, Duty Cycle < 1%

### ■ Internal Connection



**■ Electrical Characteristics** Ta = 25 °C ± 3 °C

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Drain-Source Breakdown Voltage	VDSS	ID = -1 mA, VGS = 0	-12			V
Zero Gate Voltage Drain Current	IDSS	VDS = -12 V, VGS = 0			-10	μA
Gate-Source Leakage Current	IGSS	VGS = ±8 V, VDS = 0 V			±10	μA
Gate Threshold Voltage	Vth	ID = -1.2 mA, VDS = -10 V	-0.3		-1.0	V
Drain-Source ON Resistance	RDS(on)	ID = -1.5 A, VGS = -4.5 V		57	74	mΩ
		ID = -1.5 A, VGS = -2.5 V		68	90	
		ID = -0.2 A, VGS = -1.8 V		82	139	
		ID = -0.1 A, VGS = -1.5 V		97	290	
Input Capacitance <sup>*1</sup>	Ciss	VDS = -10 V		459		pF
Output Capacitance <sup>*1</sup>	Coss	VGS = 0		85		
Reverse Transfer Capacitance <sup>*1</sup>	Crss	f = 1MHz		75		
Turn-on delay time <sup>*1,*2</sup>	td(on)	VDD = -6 V VGS = 0 to -4.5 V ID = -1.0 A		8		ns
Rise time <sup>*1,*2</sup>	tr			11		
Turn-off delay time <sup>*1,*2</sup>	td(off)			59		
Fall time <sup>*1,*2</sup>	tf			10		
Total Gate Charge <sup>*1</sup>	Qg	VDD = -6 V		7		nC
Gate to Source Charge <sup>*1</sup>	Qgs	VGS = -4.5 V		0.75		nC
Gate to Drain Miller Charge <sup>*1</sup>	Qgd	ID = -1.0 A		0.95		nC
Body Diode Forward Voltage	VF(D-S)	IF = -0.2A, VGS = 0V		-0.7	-1.2	V

Note Measuring methods are based on JAPANESE INDUSTRIAL STANDARD JIS C 7030 Measuring methods for transistors.

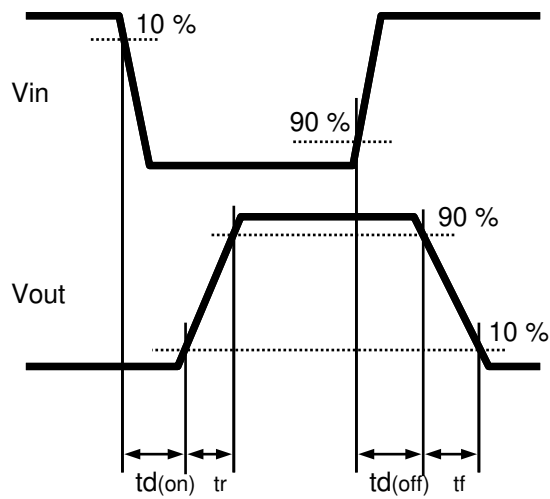
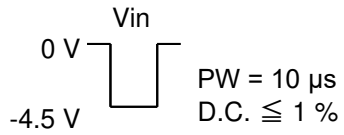
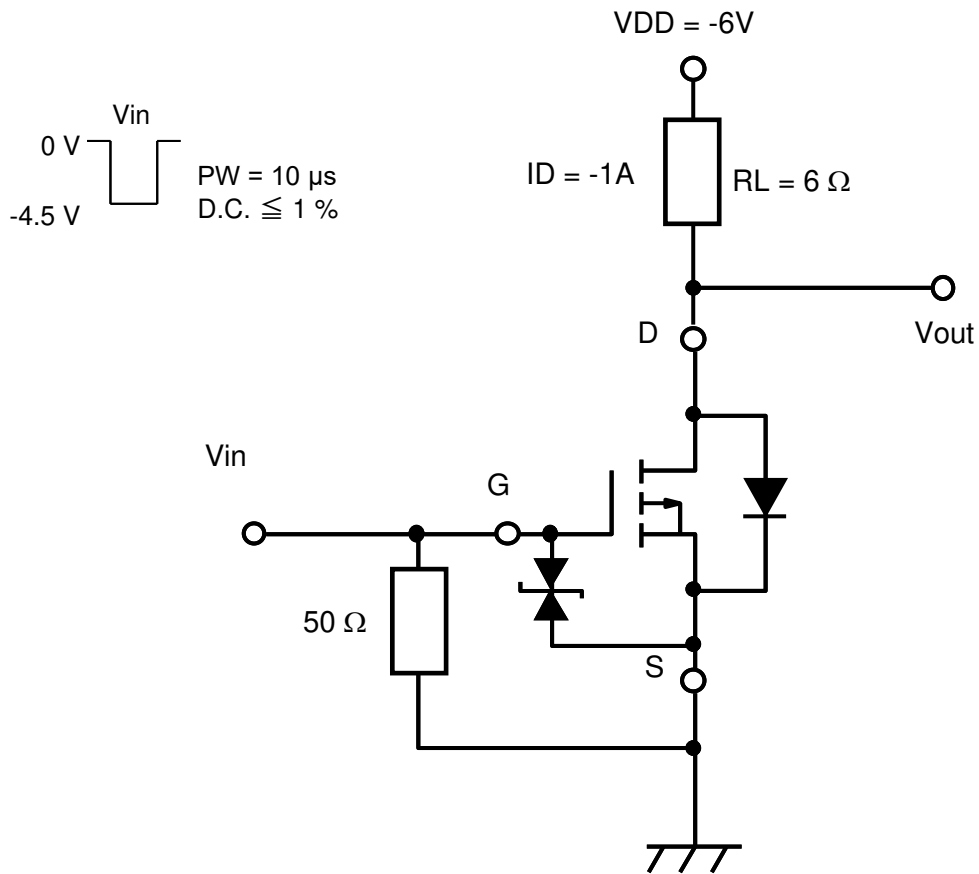
\*1 Guaranteed by design, not subject to production testing

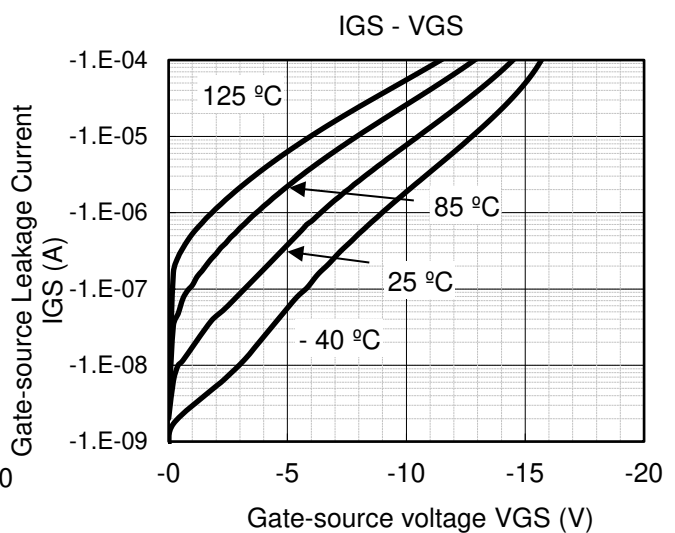
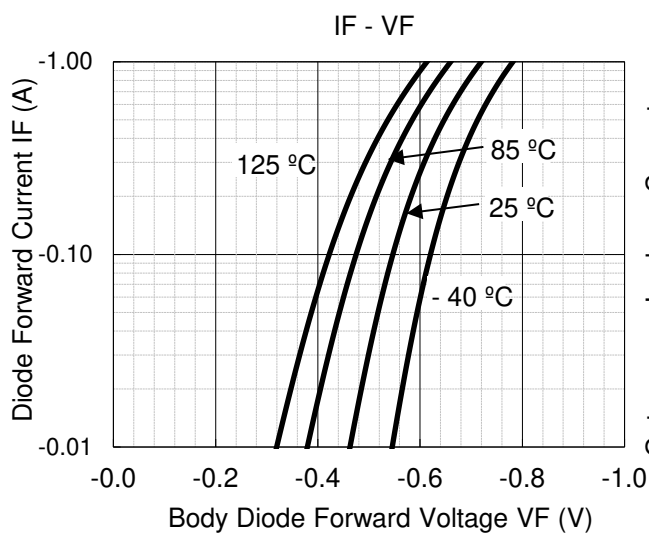
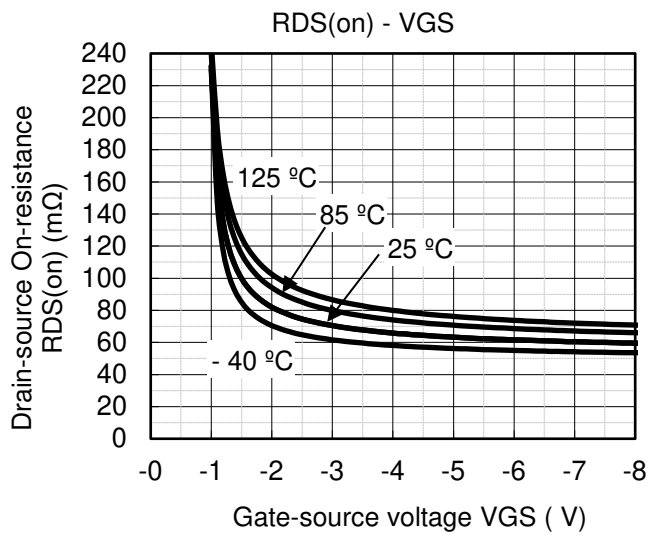
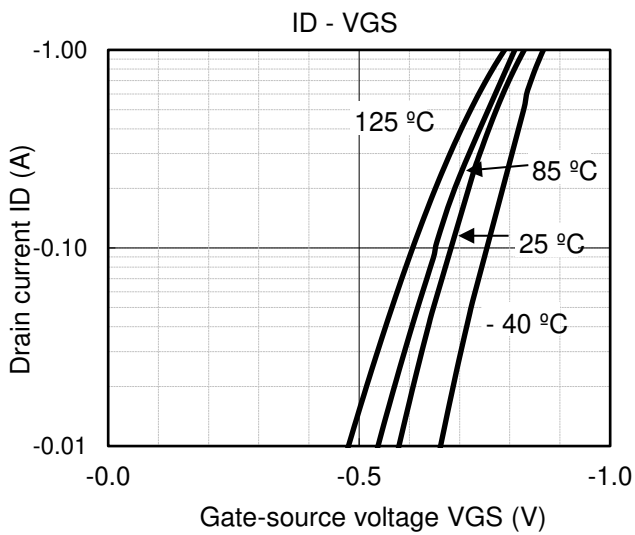
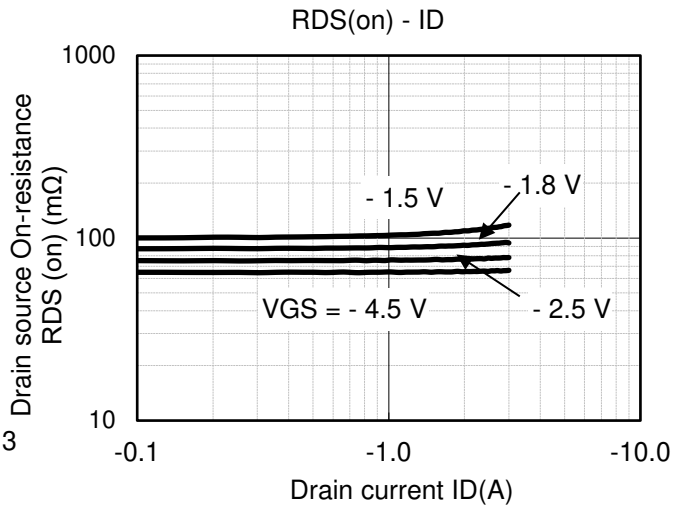
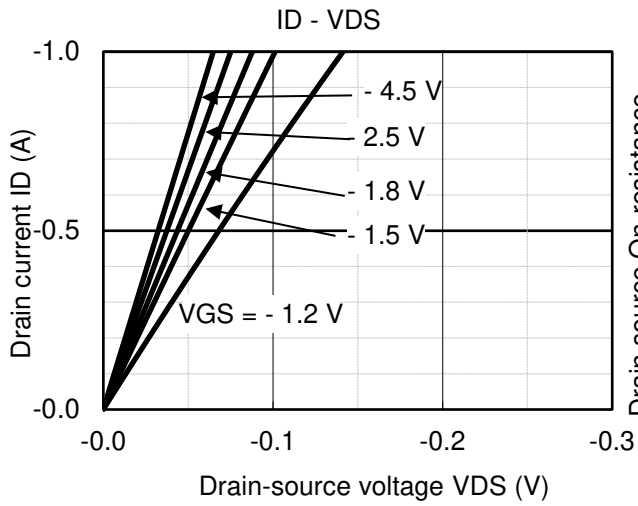
\*2 Measurement circuit for Turn-on delay time / Rise time / Turn-off delay time / Fall time

**■ Electrical State Discharge Characteristics**

Standard	Test Type	Symbol	Conditions	Class	Value	Unit
AEC-Q101-001	Human body model	HBM	C = 100 pF, R = 1.5 kΩ	H1C	>1k to ≤ 2k	V
	Machine model	MM	C = 200 pF, R = 0 Ω	M2	>100 to ≤ 200	V

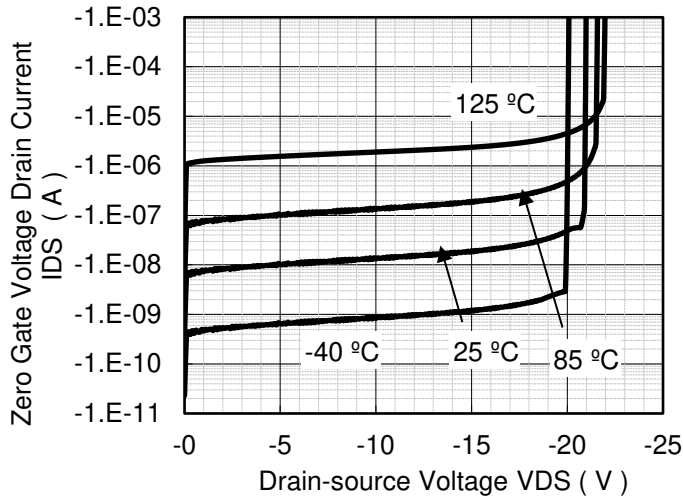
Note2: Measurement circuit



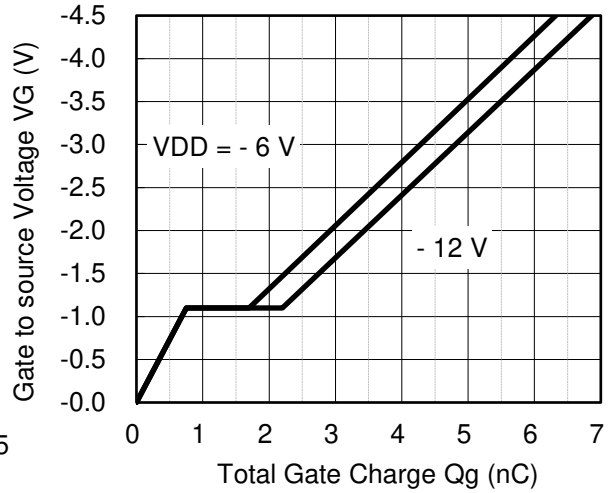




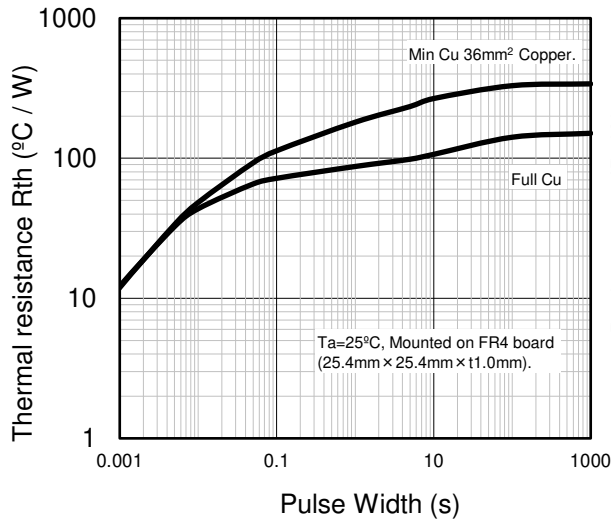
IDS - VDS



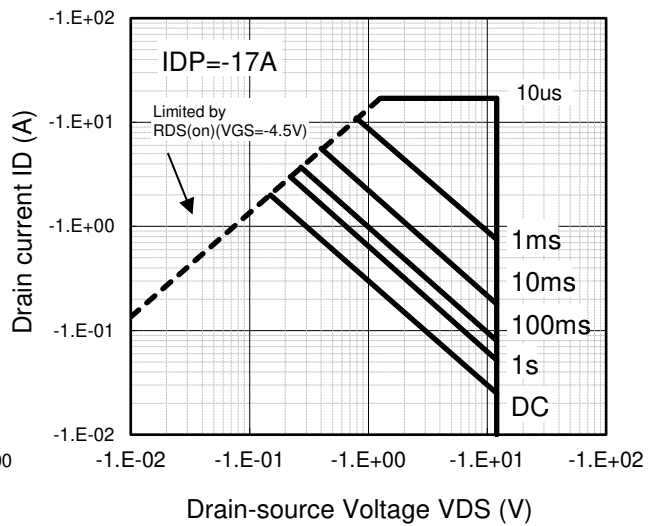
Dynamic Input/Output Characteristics



Rth - tsw

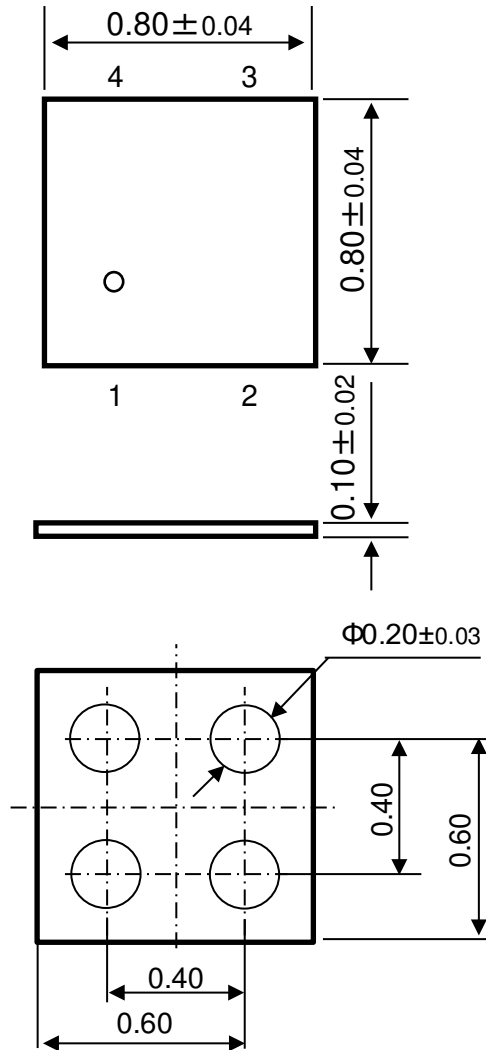


Safe Operating Area



■ XLGA004-W-0808-RA01

Unit: mm



■ Land Pattern (Reference)

