



# 320-MHz 1:7 PECL to PECL/CMOS Buffer

## Features

- DC to 320-MHz operation
- 50-ps output-output skew
- 30-ps cycle-cycle jitter
- 2.5V power supply
- LVPECL input @ 320-MHz Operation
- One LVPECL output @ 320-MHz Operation
- Four LVCMOS/LVTTL outputs @ 250 MHz/160 MHz
- Two LVCMOS/LVTTL outputs @ 250 MHz/80 MHz
- 45% to 55% output duty cycle
- Output divider control
- Output enable/disable control
- Operating temperature range: 0°C to +85°C
- 24-pin TSSOP

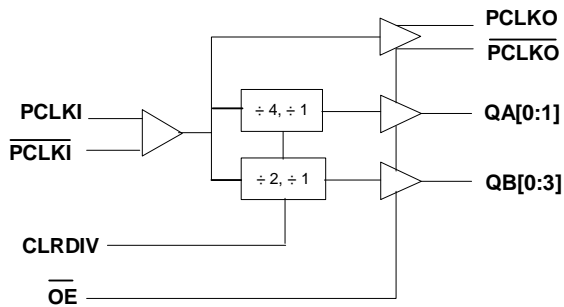
## Description

The CY2PD817 is a low-voltage LVPECL-to-LVPECL and LVCMOS fanout buffer designed for servers, data communications, and clock management.

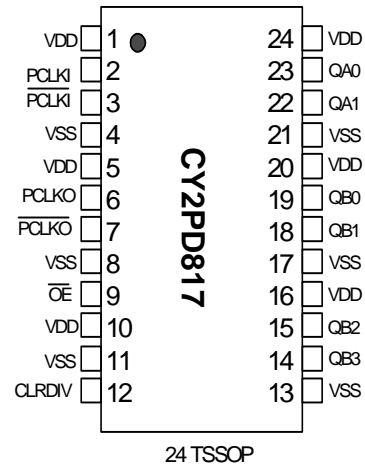
The CY2PD817 is ideal for applications requiring mixed differential and single-ended clock distribution. This device accepts an LVPECL input reference clock and provides one LVPECL and six LVCMOS/LVTTL output clocks. The outputs are partitioned into three banks of one, two, and four outputs. The LVPECL output is a buffered copy of the input clock while the LVCMOS outputs are divided by 1, 2, and 4. When CLRDIV is set HIGH, the output dividers are set to 1. In this mode, the maximum input frequency is limited to 250 MHz.

When  $\overline{OE}$  is set HIGH, the outputs are disabled in a High-Z state.

### Block Diagram



### Pin Configuration



**Pin Description<sup>[1]</sup>**

Pin	Name	I/O	Type	Description
2	PCLKI	I, PD	LVPECL	LVPECL reference clock input
3	PCLKI	I, PU/PD	LVPECL	LVPECL reference clock input
6	PCLKO	O	LVPECL	LVPECL clock output
7	PCLKO	O	LVPECL	LVPECL clock output
23, 22	QA[1,0]	O	LVC MOS	Bank A, LVC MOS clock outputs
14, 15, 18, 19	QB[3:0]	O	LVC MOS	Bank B, LVC MOS clock outputs
12	CLR DIV	I, PD	LVC MOS	Clear divider input. See functional <i>Table 1</i>
9	OE	I, PD	LVC MOS	Output enable/disable input. See functional <i>Table 1</i>
1, 5, 10, 16, 20, 24	VDD	Supply	VDD	2.5V power supply <sup>[2]</sup>
4, 8, 11, 13, 17, 21	VSS	Supply	Ground	Common ground

**Table 1. Functional Table**

Control	Default	0	1
CLR DIV	0	Bank A = ÷4, Bank B = ÷2	Bank A = ÷1, Bank B = ÷1
OE	0	All outputs are enabled	All outputs are three-stated

**Absolute Maximum Conditions**

Parameter	Description	Condition	Min.	Max.	Unit
V <sub>DD</sub>	DC Supply Voltage		-0.5	3.3	V
V <sub>DD</sub>	DC Operating Voltage	Functional	2.375	2.625	V
V <sub>IN</sub>	DC Input Voltage	Relative to V <sub>SS</sub> , with or V <sub>DD</sub> applied	-0.5	V <sub>DD</sub> + 0.5	V
V <sub>OUT</sub>	DC Output Voltage	Relative to V <sub>SS</sub>	-0.5	V <sub>DD</sub> + 0.5	V
V <sub>TT</sub>	Output termination Voltage	LVC MOS outputs	V <sub>DD</sub> / 2		V
		LVPECL output	V <sub>DD</sub> - 2		
LU	Latch Up Immunity	Functional	200	-	mA
R <sub>PS</sub>	Power Supply Ripple	Ripple Frequency < 100 kHz	-	150	mVp-p
T <sub>S</sub>	Temperature, Storage	Non-functional	-65	+150	°C
T <sub>A</sub>	Temperature, Operating Ambient	Functional	0	+85	°C
T <sub>J</sub>	Temperature, Junction	Functional	-	+150	°C
∅ <sub>JC</sub>	Dissipation, Junction to Case	Functional	-	42	°C/W
∅ <sub>JA</sub>	Dissipation, Junction to Ambient	Functional	-	105	°C/W
ESD <sub>H</sub>	ESD Protection (Human Body Model)		2000	-	V
FIT	Failure in Time	Manufacturing test	10		ppm

**Notes:**

1. PU = Internal pull up, PD = Internal pull down.
2. A 0.1-μF bypass capacitor should be placed as close as possible to each positive power pin (< 0.2"). If these bypass capacitors are not close to the pins their high frequency filtering characteristics will be cancelled by the lead inductance of the trace.

**DC Electrical Specifications** ( $V_{DD} = 2.5V \pm 5\%$ ,  $T_A = 0^\circ C$  to  $+85^\circ C$ )

Parameter	Description	Condition	Min.	Typ.	Max.	Unit
$V_{PP}$	Input Peak-Peak Voltage	PCLKI, PCLKI	250	–	$V_{DD} - 1.3$	mV
$V_{CMR}$	Input Common Mode Range	PCLKI, PCLKI	1.0	–	$V_{DD} - 0.6$	V
$V_{IL}$	Input Voltage, Low	OE, CLRDIV	–0.30	–	0.7	V
$V_{IH}$	Input Voltage, High		1.7	–	$V_{DD} + 0.3$	V
$V_{OL}$	Output Voltage, Low	PCLKO, PCLKO, $50\Omega$ to $V_{TT}$	0.2	–	0.8	V
$V_{OH}$	Output Voltage, High	PCLKO, PCLKO, $50\Omega$ to $V_{TT}$	$V_{DD} - 1.2$	–	$V_{DD} - 0.4$	V
$V_{OL}$	Output Voltage, Low <sup>[3]</sup>	$I_{OL} = 16$ mA, QA, QB	–0.3	–	0.6	V
$V_{OH}$	Output Voltage, High <sup>[3]</sup>	$I_{OH} = -16$ mA, QA, QB	1.8	–	$V_{DD} + 0.3$	V
$I_{IL}$	Input Current, Low <sup>[4]</sup>	$V_{IL} = V_{SS}$	–	–	–20	$\infty$ A
$I_{IH}$	Input Current, High <sup>[4]</sup>	$V_{IH} = V_{DD}$	–	–	100	$\infty$ A
$I_{DDQ}$	Quiescent Supply Current	$V_{IN} = 0V$ , outputs disabled	–	2.5	3.5	mA
$I_{DD}$	Dynamic Supply Current	Outputs loaded @ 250 MHz	–	250	–	mA
$C_{IN}$	Input Pin Capacitance		–	4	–	pF
$C_{OUT}$	Output Pin Capacitance		–	4	–	pF
$Z_{OUT}$	Output Impedance	QA, QB	–	25	–	$\Omega$

**AC Electrical Specifications** ( $V_{DD} = 2.5V \pm 5\%$ ,  $T_A = 0^\circ C$  to  $+85^\circ C$ )<sup>[5, 6]</sup>

Parameter	Description	Condition	Min.	Typ.	Max.	Unit
$f_{in}$	Input Frequency	CLRDIV = 0	0	–	320	MHz
		CLRDIV = 1	–	–	250	
$V_{PP}(AC)$	Input Peak-Peak Voltage	PCLKI, PCLKI	500	–	1000	mV
$V_{CMR}(AC)$	Input Common Mode Range	PCLKI, PCLKI	1.2	–	$V_{DD} - 0.6$	V
$f_{refDC}$	Reference Input Duty Cycle		40	–	60	%
$f_{max}$	Output Frequency	PCLKO, PCLKO	0	–	320	MHz
		Bank B, CLRDIV = 0	0	–	160	
		Bank A, CLRDIV = 0	–	–	80	
		Bank A, Bank B, CLRDIV = 1	–	–	250	
$t_r, t_f$	Output Rise/Fall Time	20% to 80%, PCLKO, PCLKO	200	–	700	ps
		0.6V to 1.8V, QA, QB	0.1	–	1.2	ns
DC	Output Duty Cycle, $DC_{REF} = 50\%$	Bank A/Bank B	45	–	55	%
		LVPECL Output, $f_{max} < 300$ MHz	45	–	55	
		LVPECL Output, $f_{max} > 300$ MHz	40	–	60	
$t_{sk}(O)$	Output-to-Output Skew	Skew within Bank	–	50	75	ps
		BankA to BankB Skew	–	150	200	
		PECL Output to all Banks Skew	–	200	250	
$T_{PLH}$	Propagation Delay	PCLKI to PCLKO	–	–	7	ns
		PCLKI to QA/QB	–	–	7	
$T_{PHL}$	Propagation Delay	PCLKI to PCLKO	–	–	7	ns
		PCLKI to QA/QB	–	–	7	
$t_{Qoff}$	Output Disable Time	OE to any output	–	3	6	ns
$t_{Qon}$	Output Enable Time	OE to any output	–	3	6	ns
$t_{JIT}(CC)$	Cycle-to-Cycle Jitter	LVPECL output	–	30	75	ps
		LVTTTL output	–	–	50	

**Notes:**

- Driving  $50\Omega$  parallel terminated transmission line to a termination voltage of  $V_{TT}$ .
- Inputs have pull-down resistors that affect the input current.
- AC characteristics apply for parallel output termination to  $V_{TT}$ . Parameters are guaranteed by characterization and are not 100% tested.
- AC test are measured with  $f_{in} = 250$  MHz at  $V_{DD}/2$  unless otherwise specified.

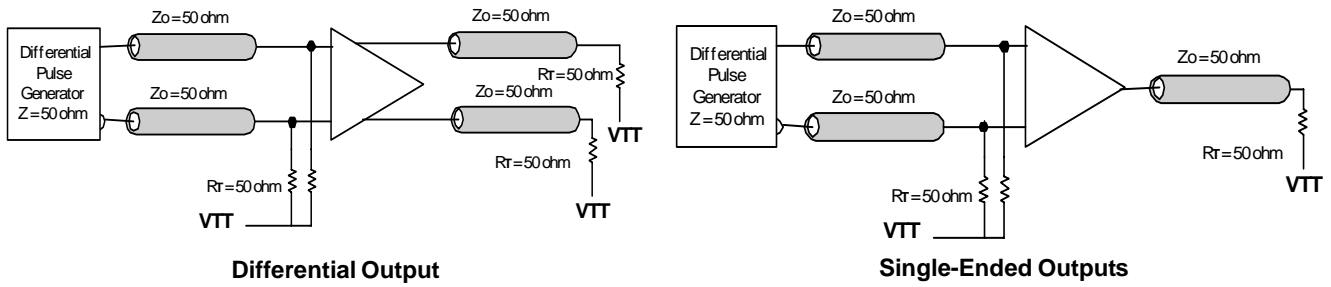


Figure 1. CY2PD817 Test Reference

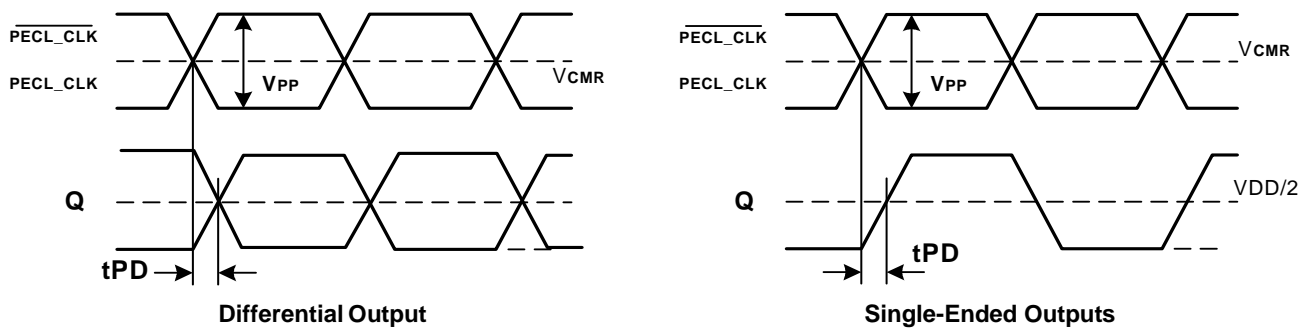


Figure 2. Propagation Delay (TPD) Test Reference

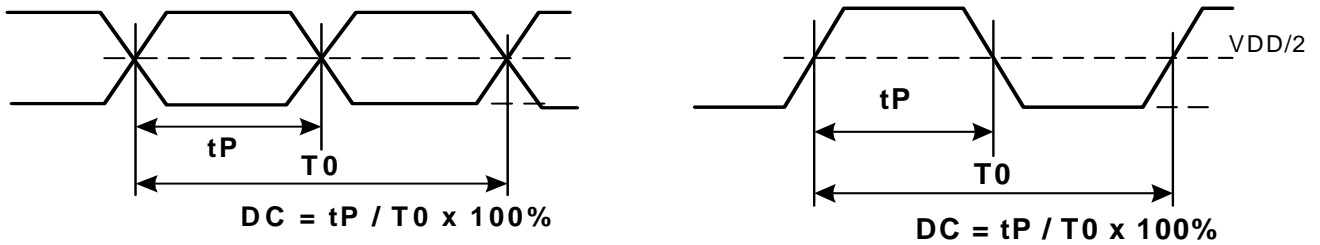


Figure 3. Output Duty Cycle

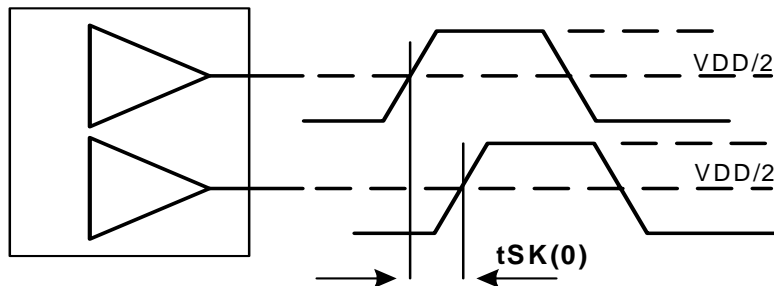
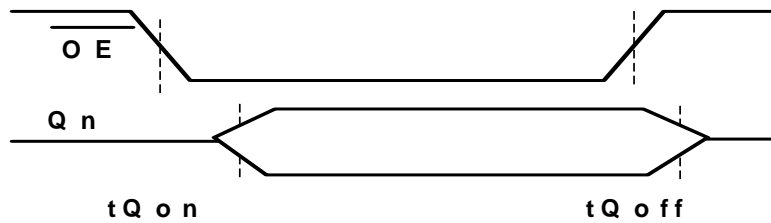
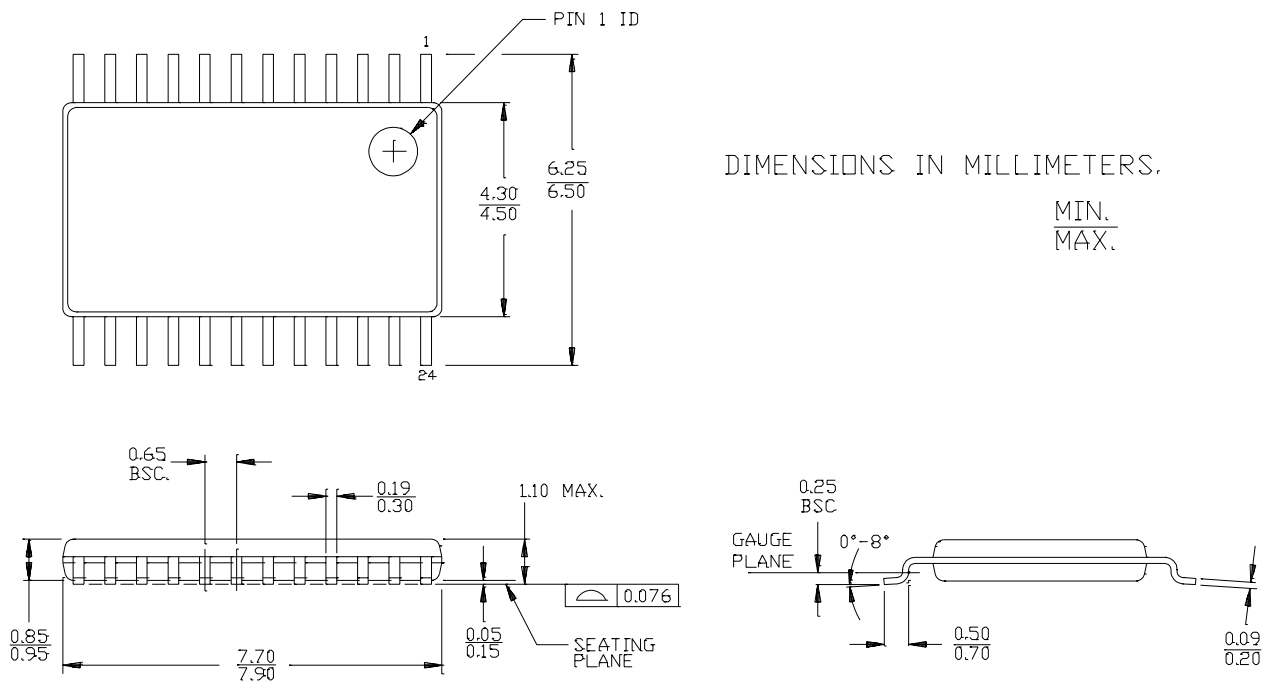


Figure 4. Output-Output Skew


**Figure 5. Output Enable/Disable Time**
**Ordering Information**

Part Number	Package Type	Product Flow
CY2PD817ZC	24-pin TSSOP	Commercial, 0°C to +85°C
CY2PD817ZCT	24-pin TSSOP – Tape and Reel	

**Package Drawing and Dimensions**
**24-lead Thin Shrink Small Outline Package (4.40-mm Body) Z24**


51-85119-\*\*

All product and company names mentioned in this document are the trademarks of their respective holders.

**Document History Page**

Document Title: CY2PD817 320-MHz 1:7 PECL to PECL/CMOS Buffer  
Document Number: 38-07574

REV.	ECN NO.	Issue Date	Orig. of Change	Description of Change
**	129024	08/29/03	RGL	New Data Sheet