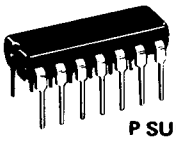
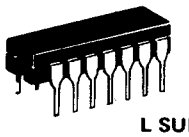
# MTTL III INTEGRATED CIRCUITS FROM MOTOROLA MTTL III

## MC3000 Series (0 to +75°C)/MC74H00
## MC3100 Series (−55 to +125°C)/MC54H00

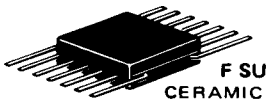
ISSUE A



P SUFFIX
PLASTIC PACKAGE
CASE 646



L SUFFIX
CERAMIC PACKAGE
CASE 632



F SUFFIX
CERAMIC PACKAGE
CASE 607

MTTL III integrated circuits comprise a family of transistor-transistor logic designed for general purpose digital applications. The family has a high operating speed (30-50 MHz clock rate), good external noise immunity, high fan-out, and the capability of driving lines up to 600 pF capacitance.

### FUNCTIONS AND CHARACTERISTICS ($V_{CC}$ = 5.0 V, $T_A$ = 25°C)

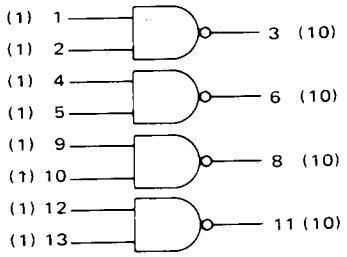
| Function | Type ① | | Loading Factor Each Output | Propagation Delay ns typ | Power Dissipation mW typ/pkg |
|---|---|---|---|---|---|
| | Case 605, 607, 632 0 to +70°C | Case 607, 632 −55°C to +125°C | | | |
| Quad 2-Input NAND Gate | MC3000(74H00) | MC3100(54H00) | 10 | 6.0 | 88 |
| Quad 2-Input AND Gate | MC3001 | MC3101 | 10 | 9.0 | 112 |
| Quad 2-Input NOR Gate | MC3002 | MC3102 | 10 | 6.0 | 122 |
| Quad 2-Input OR Gate | MC3003 | MC3103 | 10 | 9.0 | 150 |
| Quad 2-Input NAND Gate (Open Collector) | MC3004(74H01) | MC3104(54H01) | 10 | 8.0 | 88 |
| Triple 3-Input NAND Gate | MC3005(74H10) | MC3105(54H10) | 10 | 6.0 | 66 |
| Triple 3-Input AND Gate | MC3006(74H11) | MC3106(54H11) | 10 | 9.0 | 84 |
| Triple 3-Input NAND Gate (Open Collector) | MC3007 | Mc3107 | 10 | 8.0 | 66 |
| Hex Inverter | MC3008(74H04) | MC3108(54H04) | 10 | 6.0 | 140 |
| Hex Inverter | MC3009(74H05) | MC3109(54H05) | 10 | 8.0 | 90 |
| Dual 4-Input NAND Gate | MC3010(74H20) | MC3110(54H20) | 10 | 6.0 | 44 |
| Dual 4-Input AND Gate | MC3011(74H21) | MC3111(54H21) | 10 | 9.0 | 56 |
| Dual 4-Input NAND Gate (Open Collector) | MC3012(74H22) | MC3112(54H22) | 10 | 8.0 | 44 |
| 8-Input NAND Gate | MC3015 | MC3115 | 10 | 8.0 | 22 |
| 8-Input NAND Gate | MC3016(74H30) | MC3116(54H30) | 10 | 8.0 | 22 |
| Expandable Dual 2-Wide 2-Input AND-OR-INVERT Gate | MC3020(74H50) | MC3120(54H50) | 10 | 6.0 | 62.5 |
| Quad 2-Input Exclusive OR Gate | MC3021 | MC3121 | 8 | 14 | 100 |
| Quad 2-Input Exclusive NOR Gate | MC3022 | MC3122 | 8 | 14 | 85 |
| Dual 2-Wide 2-Input AND-OR-INVERT Gate | MC3023(74H51) | MC3123(54H51) | 10 | 6.0 | 62.5 |
| Dual 4-Input NAND Buffer Gate | MC3024(74H40) | MC3124(54H40) | 30 | 6.0 | 90 |
| Dual 4-Input NAND Power Gate | MC3025 | MC3125 | 20 | 6.0 | 70 |
| Dual 4-Input AND Power Gate | MC3026 | MC3126 | 20 | 9.0 | 90 |
| Dual 3-Input 3-Output AND Series Terminated Line Driver | MC3028 | MC3128 | * | 9.0 | 56 |
| Dual 3-Input 3-Output NAND Series Terminated Line Driver | MC3029 | MC3129 | * | 6.0 | 44 |
| Expandable 4-Wide 2-2-2-3 Input AND-OR Gate | MC3031(74H52) | MC3131(54H52) | 10 | 10 | 87.5 |
| Expandable 4-Wide 2-2-2-3 Input AND-OR-INVERT Gate | MC3032(74H53) | MC3132(54H53) | 10 | 7.0 | 40 |
| AND Input J-K Flip-Flop | MC3051 | MC3151 | 10 | f = 50 MHz | 50 |
| AND Input JJ-KK Flip-Flop | MC3052 | MC3152 | 10 | f = 40 MHz | 75 |
| Dual Type D Flip-Flop | MC3060 | MC3160 | 10 | f = 30 MHz | 120 |
| Dual J-K Flip-Flop | MC3061 | MC3161 | 10 | f = 50 MHz | 100 |
| Dual J-K Flip-Flop | MC3062 | MC3162 | 10 | f = 50 MHz | 100 |

① F suffix denotes Flat Package, L suffix denotes Dual In-Line Ceramic Package, P suffix denoates Plastic Package, (i.e., MC3000F = Flat Package, MC3000L = Ceramic Package, MC3000P = Plastic Package).

*Direct Output = 10 minus the number of resistor-terminated outputs being used.

## GATES

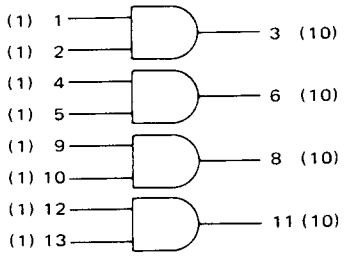
### MC3000/MC3100
### Quad 2-Input NAND Gate
### MC74H00/54H00




$3 = \overline{1 \cdot 2}$

$t_{pd}$ = 6.0 ns typ
$P_D$ = 88 mW typ/pkg

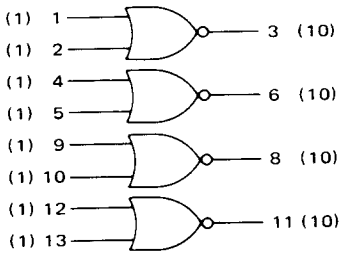
### MC3001/MC3101
### Quad 2-Input AND Gate




$3 = 1 \cdot 2$

$t_{pd}$ = 9.0 ns typ
$P_D$ = 112 mW typ/pkg

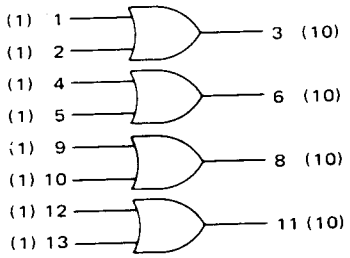
### MC3002/MC3102
### Quad 2-Input NOR Gate




$3 = \overline{1 + 2}$

$t_{pd}$ = 6.0 ns typ
$P_D$ = 122 mW typ/pkg

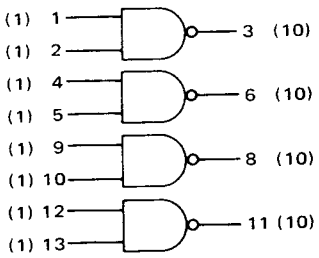
### MC3003/MC3103
### (74H32)/(54H32)
### Quad 2-Input OR Gate




$3 = 1 + 2$

$t_{pd}$ = 9.0 ns typ
$P_D$ = 150 mW typ/pkg

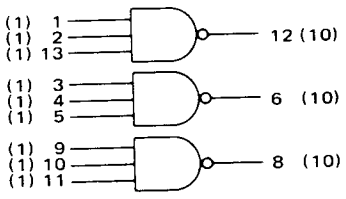
### MC3004/MC3104
### (74H01)/(54H01)
### Quad 2-Input NAND Gate
### (Open Collector)




$3 = \overline{1 \cdot 2}$

$t_{pd}$ = 8.0 ns typ
$P_D$ = 88 mW typ/pkg

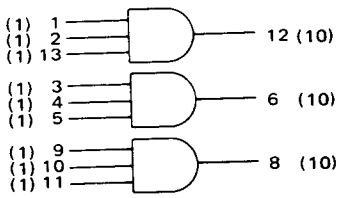
### MC3005/MC3105
### Triple 3-Input NAND Gate
### MC74H10/54H10




$12 = \overline{1 \cdot 2 \cdot 13}$

$t_{pd}$ = 6.0 ns typ
$P_D$ = 66 mW typ/pkg

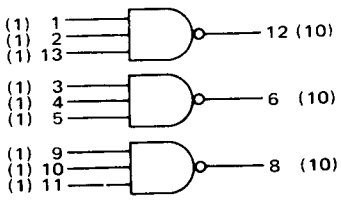
### MC3006/MC3106
### Triple 3-Input AND Gate
### MC74H11/MC54H11




$12 = 1 \cdot 2 \cdot 13$

$t_{pd}$ = 9.0 ns typ
$P_D$ = 84 mW typ/pkg

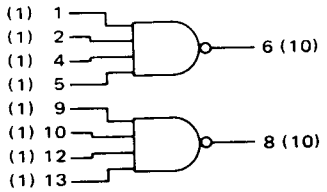
### MC3007/MC3107
### Triple 3-Input NAND Gate
### (Open Collector)




$12 = \overline{1 \cdot 2 \cdot 13}$

$t_{pd}$ = 8.0 ns typ
$P_D$ = 66 mW typ/pkg

### MC3010/MC3110
### Dual 4-Input NAND Gate
### MC74H20/MC54H20




$6 = \overline{1 \cdot 2 \cdot 4 \cdot 5}$

$t_{pd}$ = 6.0 ns typ
$P_D$ = 44 mW typ/pkg

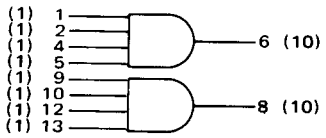
(continued

Numbers at ends of terminals represent pin numbers.
Numbers in parenthesis indicate loading.

$V_{CC}$ = Pin 14, Gnd = Pin 7.

## GATES (continued)

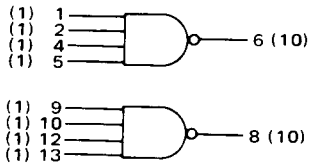
### MC3011/MC3111
### Dual 4-Input AND Gate
### MC74H21/MC54H21




$6 = 1 \bullet 2 \bullet 4 \bullet 5$

$t_{pd}$ = 9.0 ns typ
$P_D$ = 56 mW typ/pkg

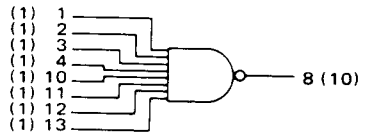
### MC3012/MC3112
### Quad 4-Input NAND Gate
### (Open Collector)
### MC74H22/MC54H22




$6 = \overline{1 \bullet 2 \bullet 4 \bullet 5}$

$t_{pd}$ = 8.0 ns typ
$P_D$ = 44 mW typ/pkg

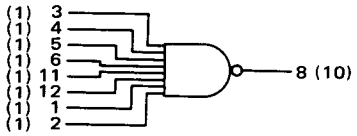
### MC3015/MC3115
### 8-Input NAND Gate




$8 = \overline{1 \bullet 2 \bullet 3 \bullet 4 \bullet 10 \bullet 11 \bullet 12 \bullet 13}$

$t_{pd}$ = 8.0 ns typ
$P_D$ = 22 mW typ/pkg

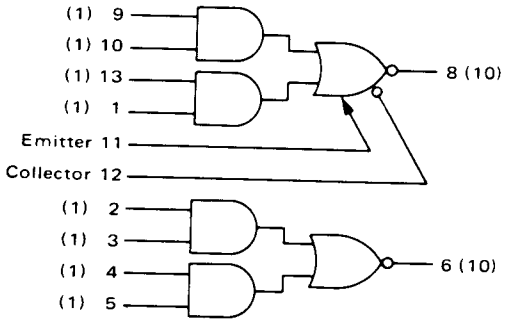
### MC3016/MC3116
### 8-Input NAND Gate
### MC74H30/MC54H30




$8 = \overline{3 \bullet 4 \bullet 5 \bullet 6 \bullet 11 \bullet 12 \bullet 1 \bullet 2}$

$t_{pd}$ = 8.0 ns typ
$P_D$ = 22 mW typ/pkg

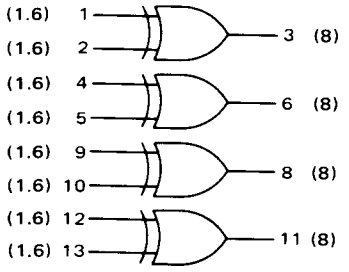
### MC3020/MC3120
### Expandable Dual 2-Wide 2-Input
### AND-OR-INVERT Gate
### MC74H50/MC54H50




$8 = \overline{(9 \bullet 10) + (13 \bullet 1) + (\text{Expanders})}$

$t_{pd}$ = 6.0 ns typ
$P_D$ = 62.5 mW typ/pkg

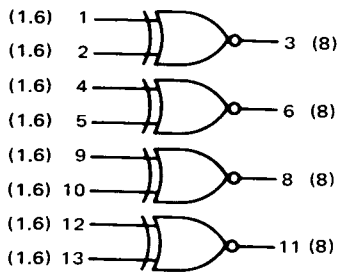
### MC3021/MC3121
### Quad 2-Input
### Exclusive OR Gate




$3 = 1 \bullet \bar{2} + \bar{1} \bullet 2$

$t_{pd}$ = 14 ns typ
$P_D$ = 100 mW typ/pkg

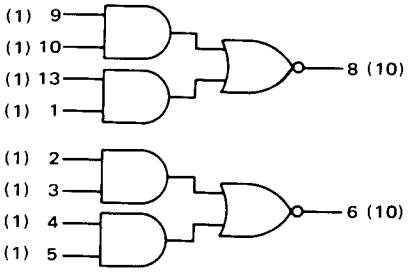
### MC3022/MC3122
### Quad 2-Input
### Exclusive NOR Gate




$3 = \bar{1} \bullet \bar{2} + 1 \bullet 2$

$t_{pd}$ = 14 ns typ
$P_D$ = 85 mW typ/pkg

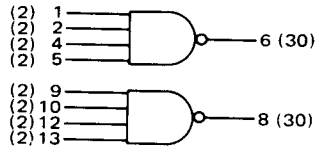
### MC3023/MC3123
### Dual 2-Wide 2-Input
### AND-OR-INVERT Gate
### MC74H51/Mc54H51




$8 = \overline{(9 \bullet 10) + (13 \bullet 1)}$

$t_{pd}$ = 6.0 ns typ
$P_D$ = 62.5 mW typ/pkg

### MC3024/MC3124
### Dual 4-Input NAND
### Buffer Gate
### MC74H40/Mc54H40




$6 = \overline{1 \bullet 2 \bullet 4 \bullet 5}$

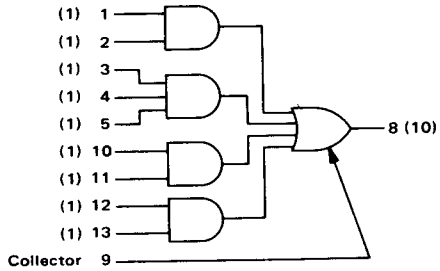
typ = 6.0 ns typ
$P_D$ = 90 mW typ/pkg

(continued)

# MTTL III LOGIC DIAGRAMS

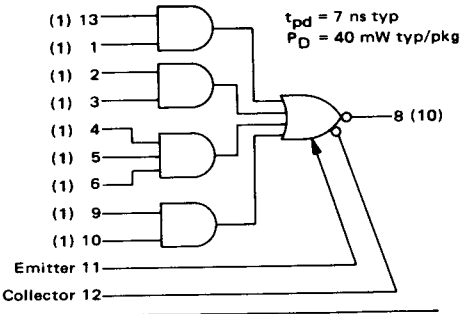
## GATES (continued)

### MC3031/MC3131
**Expandable 4-Wide 2-2-2-3-Input AND-OR Gate**
**MC74H52/MC54H52**




$t_{pd}$ = 10 ns typ
$P_D$ = 87.5 mW typ/pkg

### MC3032/MC3132
**Expandable 4-Wide 2-2-2-3-Input AND-OR-INVERT Gate**
**MC74H53/MC54H53**

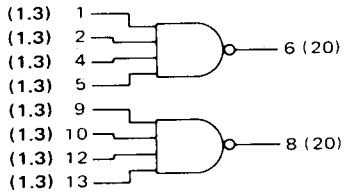



$t_{pd}$ = 7 ns typ
$P_D$ = 40 mW typ/pkg

$8 = \overline{(13 \cdot 1) + (2 \cdot 3) + (4 \cdot 5 \cdot 6) + (9 \cdot 10) + (\text{Expanders})}$

## POWER GATES

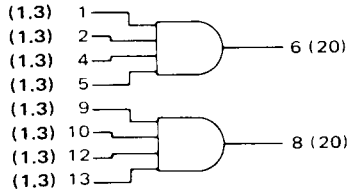
### MC3025/MC3125
**Dual 4-Input NAND Power Gate**




$6 = \overline{1 \cdot 2 \cdot 4 \cdot 5}$

$t_{pd}$ = 6.0 ns typ
$P_D$ = 70 mW typ/pkg

### MC3026/MC3126
**Dual 4-Input AND Power Gate**

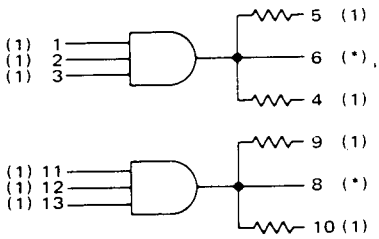



$6 = 1 \cdot 2 \cdot 4 \cdot 5$

$t_{pd}$ = 9.0 ns typ
$P_D$ = 90 mW typ/pkg

## LINE DRIVERS

### MC3028/MC3128
**Dual 3-Input 3-Output AND Series Terminated Line Driver**

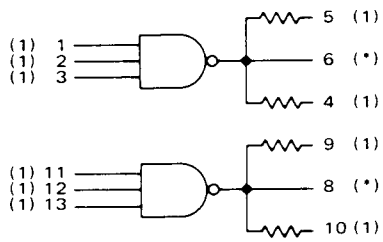



$4, 5, 6, = 1 \cdot 2 \cdot 3$

$t_{pd}$ = 9.0 ns typ
$P_D$ = 56 mW typ/pkg

*8 MINUS THE NUMBER OF RESISTOR-TERMINATED OUTPUTS BEING USED.

### MC3029/MC3129
**Dual 3-Input 3-Output NAND Series Terminated Line Driver**



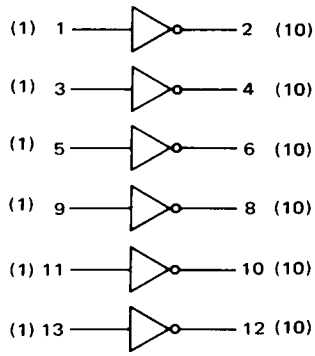

$4, 5, 6 = \overline{1 \cdot 2 \cdot 3}$

$t_{pd}$ = 6.0 ns typ
$P_D$ = 44 mW typ/pkg

*8 MINUS THE NUMBER OF RESISTOR-TERMINATED OUTPUTS BEING USED.

# INVERTERS

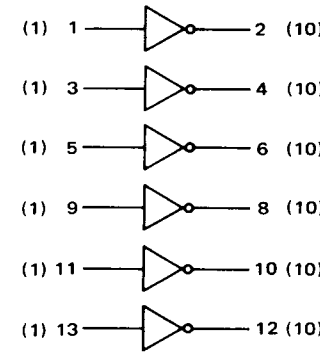
## MC3008/MC3108
## Hex Inverter
## MC74H04/Mc54H04




$2 = \overline{1}$

$t_{pd}$ = 6.0 ns typ
$P_D$ = 140 mW typ/pkg

## MC3009/MC3109
## Hex Inverter
## Open Collector
## MC74H05/MC54H05

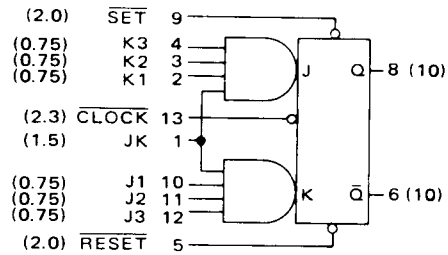



$2 = \overline{1}$

$t_{pd}$ = 8.0 ns typ
$P_D$ = 90 mW typ/pkg

# FLIP-FLOPS

## MC3051/MC3151
## AND J-K Flip-Flop

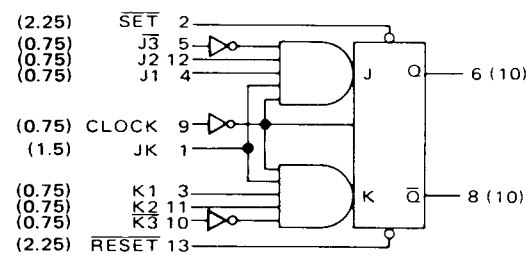



where
J = J1 • J2 • J3 • JK
K = K1 • K2 • K3 • JK

f = 50 MHz
$P_D$ = 50 mW typ/pkg

| J | K | $Q^n$ | $Q^{n+1}$ |
|---|---|---|---|
| 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 |
| 0 | 1 | 0 | 0 |
| 0 | 1 | 1 | 0 |
| 1 | 0 | 0 | 1 |
| 1 | 0 | 1 | 1 |
| 1 | 1 | 0 | 1 |
| 1 | 1 | 1 | 0 |

## MC3052/MC3152
## AND Input JJ-K$\overline{K}$ Flip-Flop




Where:
J = J1 • J2 • $\overline{J3}$ • JK
K = K1 • K2 • $\overline{K3}$ • JK

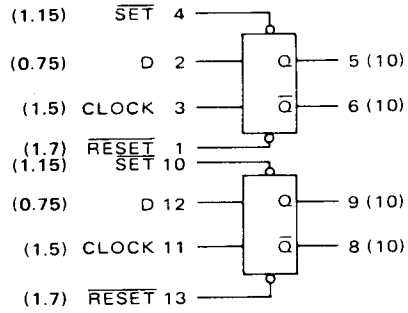
f = 40 MHz
$P_D$ = 75 mW typ/pkg

| J | K | $Q_n$ | $Q_{n+1}$ |
|---|---|---|---|
| 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 |
| 0 | 1 | 0 | 0 |
| 0 | 1 | 1 | 0 |
| 1 | 0 | 0 | 1 |
| 1 | 0 | 1 | 1 |
| 1 | 1 | 0 | 1 |
| 1 | 1 | 1 | 0 |

# MTTL III LOGIC DIAGRAMS

## FLIP-FLOPS (continued)

### MC3060/MC3160
### Dual Type D Flip-Flop



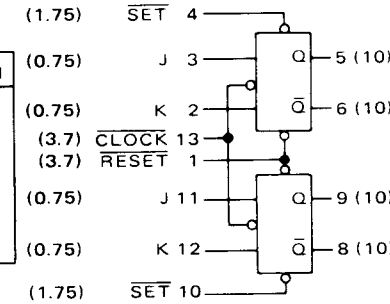

| D | $Q_n$ | $Q_{n+1}$ |
|---|---|---|
| 0 | 0 | 0 |
| 0 | 1 | 0 |
| 1 | 0 | 1 |
| 1 | 1 | 1 |

$Q_{n+1} = D_n$

f = 30 MHz
$P_D$ = 120 mW typ/pkg

### MC3061/MC3161
### Dual J-K Flip-Flop

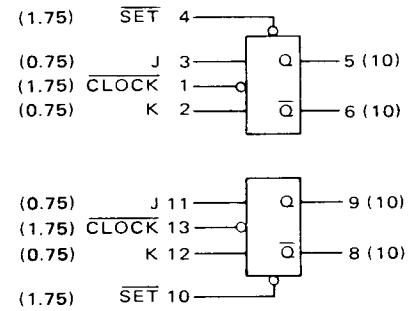
| J | K | $Q_n$ | $Q_{n+1}$ |
|---|---|---|---|
| 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 |
| 0 | 1 | 0 | 0 |
| 0 | 1 | 1 | 0 |
| 1 | 0 | 0 | 1 |
| 1 | 0 | 1 | 1 |
| 1 | 1 | 0 | 1 |
| 1 | 1 | 1 | 0 |




f = 50 MHz
$P_D$ = 100 mW typ/pkg

### MC3062/MC3162
### Dual J-K Flip-Flop

| J | K | $Q_n$ | $Q_{n+1}$ |
|---|---|---|---|
| 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 |
| 0 | 1 | 0 | 0 |
| 0 | 1 | 1 | 0 |
| 1 | 0 | 0 | 1 |
| 1 | 0 | 1 | 1 |
| 1 | 1 | 0 | 1 |
| 1 | 1 | 1 | 0 |




f = 50 MHz
$P_D$ = 100 mW typ/pkg