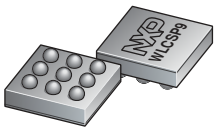


PCA9410/9410A

3.0 MHz, 500 mA, DC-to-DC boost converter

Rev. 1 — 5 August 2016 Product data sheet

1. General description

The PCA9410 and PCA9410A are highly efficient 3.0 MHz, 500 mA, step-up DC-to-DC converters. They convert input voltages from 2.5 V to 5.25 V to a fixed output voltage of 5.0 V.

These devices are optimized for battery-powered applications. High efficiency of up to 94 % enables an extended battery life in all portable designs. Step-up operation at a switching frequency of 3 MHz allows using 1 μH inductor or smaller.

2. Features and benefits

- Efficiency up to 94 %
- ± 3 % output voltage accuracy at nominal and static conditions
- ± 3 % output voltage accuracy over full current, voltage and temperature range
- $V_{IN} \geq V_O$, (Pass-Through Mode Operation)
- Load disconnect
- Current-mode controller
- Soft start function for limiting inrush current with true load disconnect
- Overcurrent and over-temperature protection
- The PCA9410 totally disconnects input to output when disabled
- The PCA9410A connects input to output when disabled
- Wafer-Level Chip-Size Package (WLCSP) with 0.4 mm pitch; allows for the use of a smaller antenna, or for greater signal strength

3. Applications

- Smartphones
- NFC terminals

4. Ordering information

Table 1. Ordering information

Type number	Topside mark	Package		
		Name	Description	Version
PCA9410UK	P10	WLCSP9	wafer-level chip-size package; 9 bumps; body 1.24 × 1.24 × 0.525 mm	-
PCA9410AUK	10A	WLCSP9	wafer-level chip-size package; 9 bumps; body 1.24 × 1.24 × 0.525 mm	-

4.1 Ordering options

Table 2. Ordering options

Type number	Orderable part number	Package	Packing method	Minimum order quantity	Temperature
PCA9410UK	PCA9410UKZ	WLCSP9	REEL 7" Q1/T1 *SPECIAL MARK CHIPS DP	3000	T_{amb} = −40 °C to +85 °C
PCA9410AUK	PCA9410AUKZ	WLCSP9	REEL 7" Q1/T1 *SPECIAL MARK CHIPS DP	3000	T_{amb} = −40 °C to +85 °C

5. Block diagram

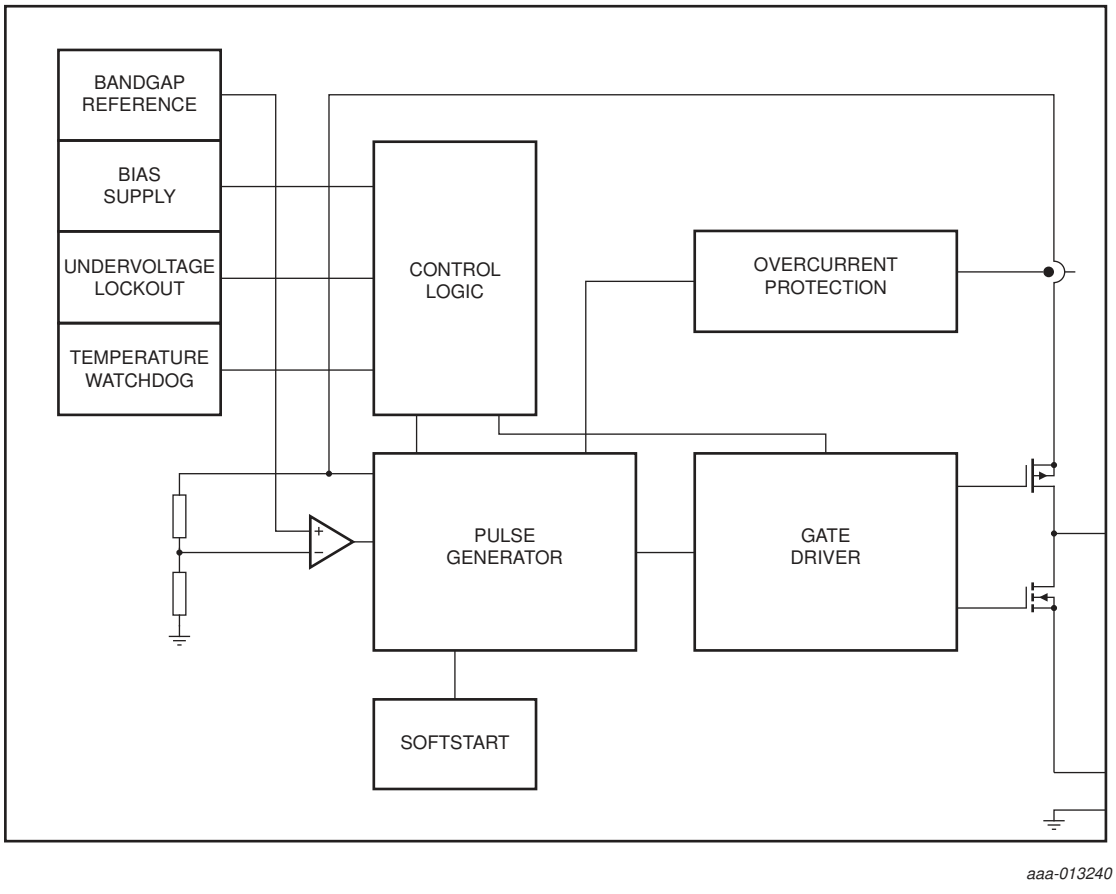
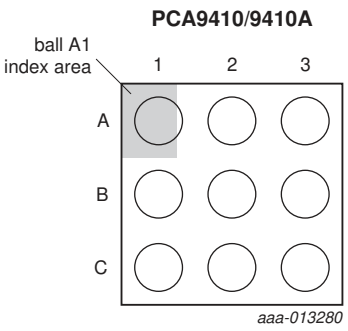


Fig 1. Block diagram

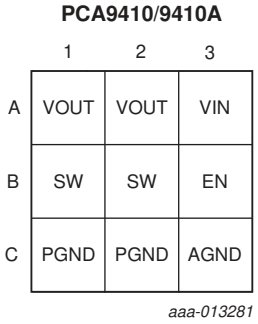
6. Pinning information

6.1 Pinning



Transparent top view

Fig 2. Pin configuration WLCSP9 package



Transparent top view

Fig 3. Ball mapping for WLCSP9

6.2 Pin description

Table 3. Pin description

Symbol	Pin	Description
VOUT	A1, A2	Output voltage. This pin is the output voltage terminal; connect directly to C_{OUT}.
VIN	A3	Input voltage. Connect to Li-Ion battery input power source.
SW	B1, B2	Switching node. Connect to inductor.
EN	B3	Enable. Used to enable/disable the device; HIGH = enabled. Non-A version: EN low = total disconnect A version: EN low = forced pass through
PGND	C1, C2	Power ground. This is the power return for the IC. C_{OUT} capacitor should be returned with the shortest path possible to these pins.
AGND	C3	Analog ground. This is the signal ground reference for the IC. All voltage levels are measured with respect to this pin; connect to PGND at a single point. The AGND pin should be flooded over by the ground plane that is connecting the PGND pins to both the input caps and the output caps.

7. Functional description

The step-up converter (Figure 4) generates a regulated constant output voltage.

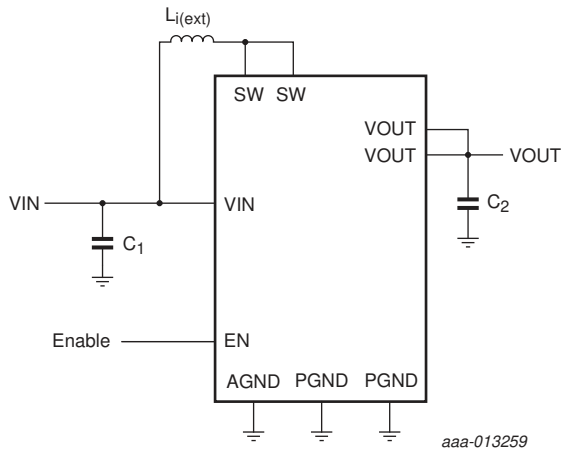


Fig 4. Typical DC-to-DC application

7.1 Enable (EN) pin

EN pin enables the boost converter when HIGH. However the effect of the EN when LOW has two methods of operation, depending on which device is used.

PCA9410 device: the EN pin when LOW causes the part to go into a total disconnect mode from input to output.

PCA9410A device: EN pin when LOW forces the part into Pass Through mode where the output voltage is the same as the input voltage. This device emulates a conventional boost converter (without the voltage drop of the internal diode).

When the EN pin is pulled HIGH it should be held HIGH for at least 500 μs for the device to properly initialize. This is for getting the forced Pass Through mode set up properly. Shorter pulses may cause unpredictable behavior.

Table 4. Operating modes

Mode	Description	Invoked when
LIN	linear start-up	$V_{IN} > V_{OUT}$
SS	boost soft-start	$V_{IN} < V_{OUT} < V_{OUT(TARGET)}$
BST	boost operating mode	$V_{OUT} = V_{OUT(TARGET)}$
PT	pass-through mode	$V_{IN} > V_{OUT(TARGET)}$ or in the advanced part when EN is pulled LOW

7.1.1 Pass-Through (PT) mode

With both devices, the device automatically transitions from Boost Mode to Pass-Through Mode if V_{IN} goes above the V_{OUT} target. In Pass-Through Mode, the device provides a very low impedance path from V_{IN} to V_{OUT}. Entry to the Pass-Through Mode is triggered

by condition where $V_{IN} > V_{OUT}$ target. Pass-Through Mode exit is triggered when V_{OUT} going down reaches the target V_{OUT} voltage. During Automatic Pass-Through Mode, the PMOS overcurrent protection remains enabled.

In the PCA9410A, user can force the device in Forced Pass-Through Mode through the EN pin. If the EN pin is pulled HIGH, the device starts operating in Boost Mode. Once the EN pin is pulled LOW, the device is forced into Pass-Through Mode. To disable the device, the input supply voltage must be removed. The device cannot start-up in Forced Pass-Through Mode. During start-up, keep the EN pulled HIGH for 500 µs, before pulling it LOW and putting the device into Forced Pass-Through Mode. The EN pin has an internal pull-down resistor (see Figure 5 for the sequence).

Table 5. Enable

EN logic level	Description Non-A	Description A
LOW	Power-down isolated output	Forced pass-through
HIGH	Boost mode	Boost mode

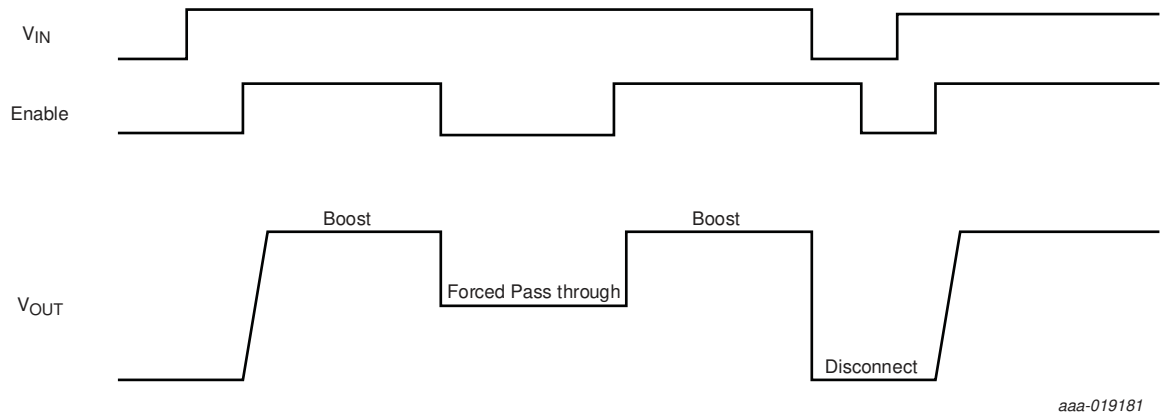


Fig 5. Forced pass-through

7.2 Inrush current limiter (soft start)

The PCA9410 and PCA9410A have an integrated pre-charge circuit that prevents large inrush currents when input voltage is applied. This inrush is accompanied with a current limit that shuts down the device, and runs a delay timer then attempts a restart.

Once the output voltage reaches the input voltage the soft start function is enabled to limit the maximum current in boost time and to reduce an input voltage dip. Therefore the system has a turn-on procedure which starts up step-by-step and limits the inrush current via a duty cycle control up to the maximum current capability.

7.3 Thermal protection

The PCA9410 and PCA9410A have an integrated thermal protection. The protection circuit senses the internal temperature of the chip and switches off the integrated PMOS power switch transistor when temperature reaches 150 °C. After the temperature returns to a safe value 20 °C below the shutdown temperature, the system restarts in the pre-charge phase.

7.4 Overcurrent protection

Overcurrent protection circuit senses the current through the integrated PMOS. If the diagnostic circuit detects an overcurrent, the system switches off the PMOS and NMOS to break the current flow, and a 20 ms timeout is started. Once the 20 ms timeout expires, the part restarts in the pre-charge phase.

8. Limiting values

Table 6. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{IN}	voltage on pin IN		−0.5	+6.0	V
V_i	input voltage	on pin EN	−0.3	V_{IN} + 0.3 V, up to +6.0 V	V
V_O	output voltage	on pins SW, OUT	−0.5	+6.0	V
P_{tot}	total power dissipation	[1]			
T_{stg}	storage temperature		−65	+150	°C
T_j	junction temperature		−40	+125	°C
T_{amb}	ambient temperature		−40	+85	°C
V_{ESD}	electrostatic discharge voltage	human body model (JESD22-001)	−2	+2	kV

[1] Internally limited

9. Recommended operating conditions

Table 7. Operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{IN}	voltage on pin IN		2.5	-	5.25	V
V_i	input voltage	on pin EN	−0.3	-	V_{IN}	V
C_1	external input capacitance	V_{IN} = 4.8 V [1]	2.0	4.2	-	µF
C_2	external output capacitance	V_O = 5 V [1]	3.0	4.2	10	µF
$L_{i(ext)}$	external input inductance	[1]	0.47	1	2.2	µH

[1] This is the capacitance at 5 V bias. Check application section for more details.

10. Static characteristics

Table 8. Static characteristics

At recommended input voltages and T_{amb} = −40 °C to +85 °C; voltages are referenced to GND (ground = 0 V); unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Input voltage and input current						
V_{IN}	input voltage		2.5	3.6	5.25	V
I_Q	supply current	EN = 0 V	-	3.0	10.0	µA
		EN = 1.8 V, V_{IN} = 2.5 V	-	36	-	mA
		EN = 1.8 V, V_{IN} = 4.8 V	-	11	-	mA
		EN = 1.8 V, V_{IN} = 5.25 V	-	3.57	-	mA
Output voltage and output current						
V_{OUT}	output voltage	$I_O \geq$ 15 mA	4.85 (−3 %)	5.0	5.15 (+3 %)	V
$I_{OUT(lim)}$	output current limit	EN = HIGH	0.5	-	-	A
$f_{o(boost)}$	boost output frequency		2.91	3	3.09	MHz
$V_{th(r)(UVLO)}$	rising threshold voltage on V_{IN} UVLO		1.9	2.1	2.3	V
$V_{th(f)(UVLOhyst)}$	falling UVLO hysteresis		70	-	120	mV
$V_{o(noise\_p\text{-}p\_coh)}$	V_o coherent peak-to-peak noise	100 kHz to 1.5 MHz, V_{IN} < 4.8 V			2	mV
		12 MHz to 15 MHz, V_{IN} < 4.8 V			2	mV
$V_{o(noise\_rms)}$	V_o rms noise (incoherent noise)	100 kHz to 1.5 MHz, V_{IN} < 4.8 V			660	µV rms
		12 MHz to 15 MHz, V_{IN} < 4.8 V			660	µV rms
Control input and timing						
V_{IH}	HIGH-level input voltage	pins EN	1.16	-	-	V
V_{IL}	LOW-level input voltage	pins EN	-	-	0.4	V
$t_{startup}$	start-up time		-	500	600	µS
Over-temperature protection						
T_{sd}	shutdown temperature		-	150	-	°C
$T_{sd(hys)}$	hysteresis of shutdown temperature		-	20	-	°C
Switches						
R_{DSon}	drain-source on-state resistance	N-channel FET	-	70	-	mΩ
		P-channel FET	-	80	-	mΩ
I_L	leakage current	V_{IN} = 3.6 V; EN = LOW	0	0.051	10	µA
$R_{pd(en\_low)}$	enable pull down	EN = LOW	450	640	800	kΩ
$I_{(ena\text{-}pulldown)}$	enable pull down current	EN = HIGH, VIN ≥ 2.5 V	-	100	-	nA

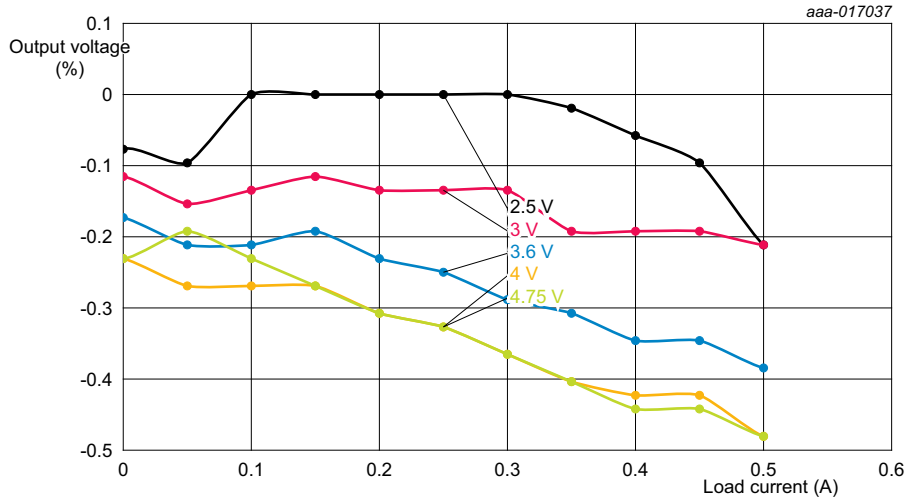


Fig 6. Output regulation vs Iload and V_{IN}

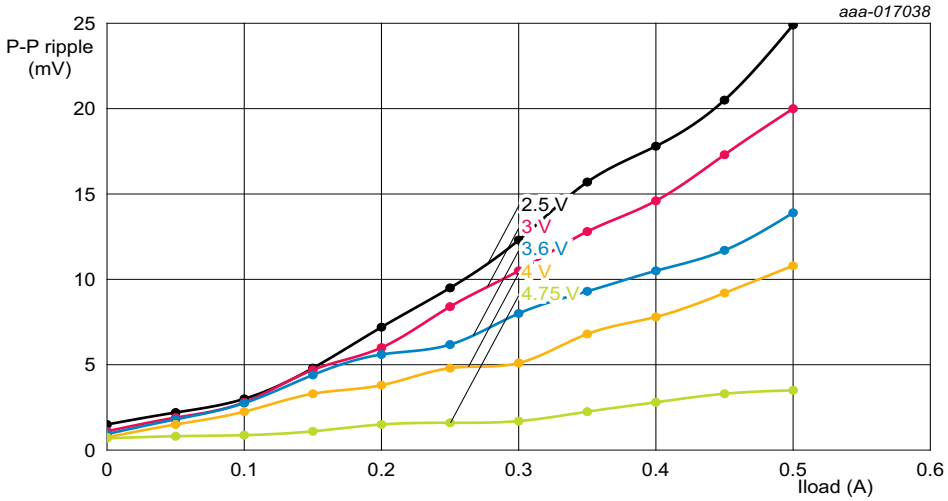


Fig 7. Output ripple vs Iload and V_{IN}

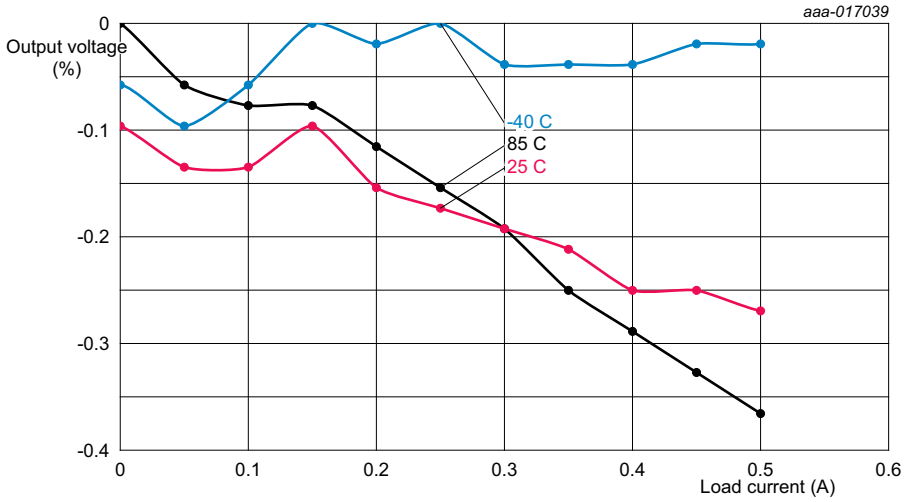


Fig 8. Output regulation vs Iload and temp (V_{IN} = 3.6 V)

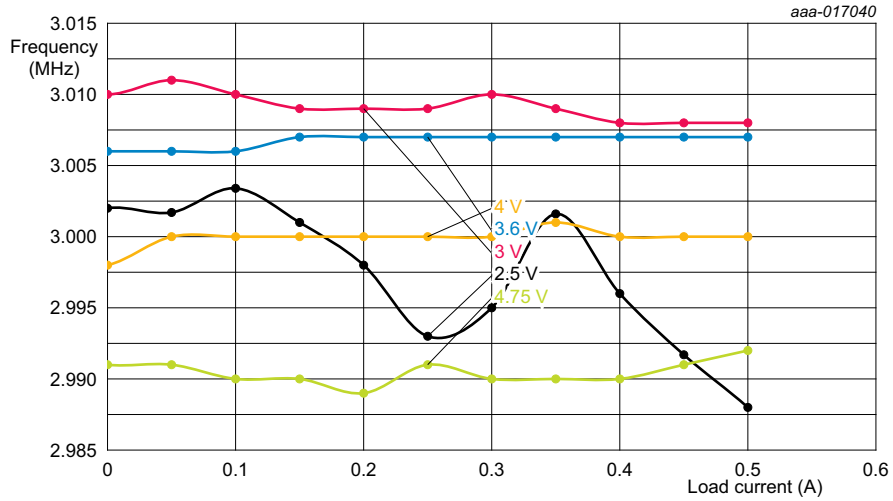


Fig 9. Frequency vs load current and V_{IN}

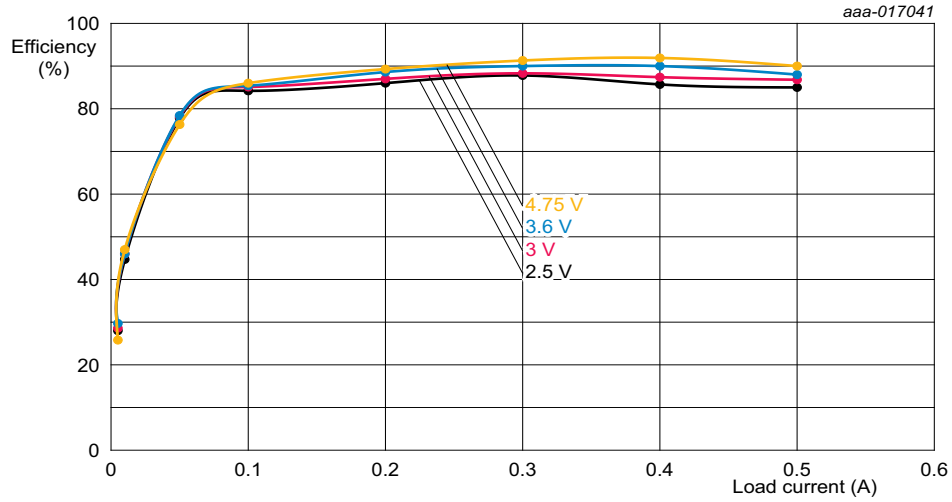


Fig 10. Efficiency vs Iload and V_{IN}

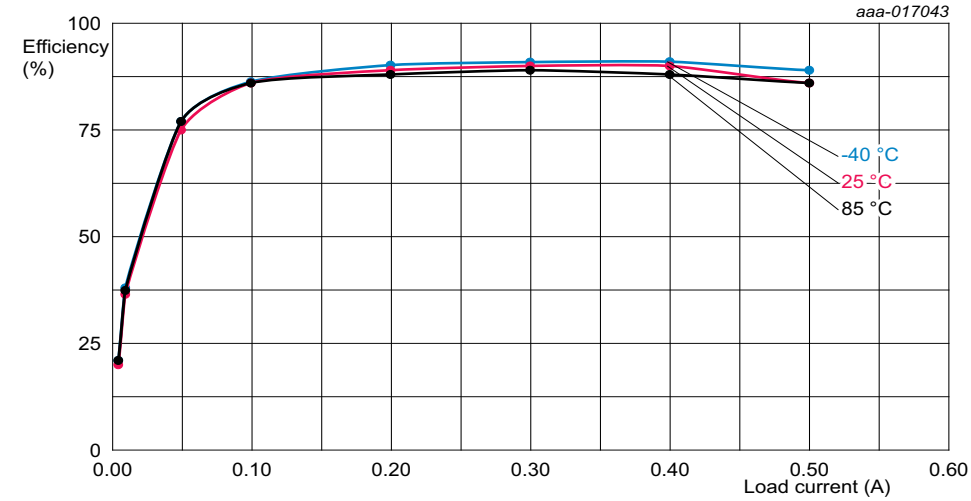


Fig 11. Efficiency vs Iload and temp (V_{IN} = 3.6 V)

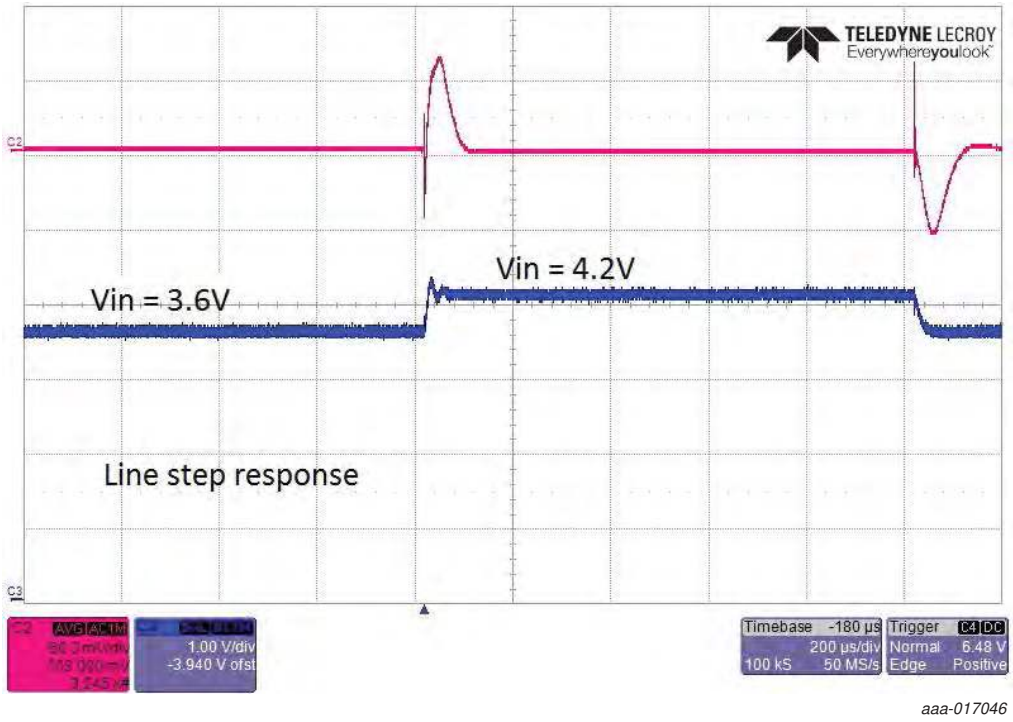


Fig 12. Line step response

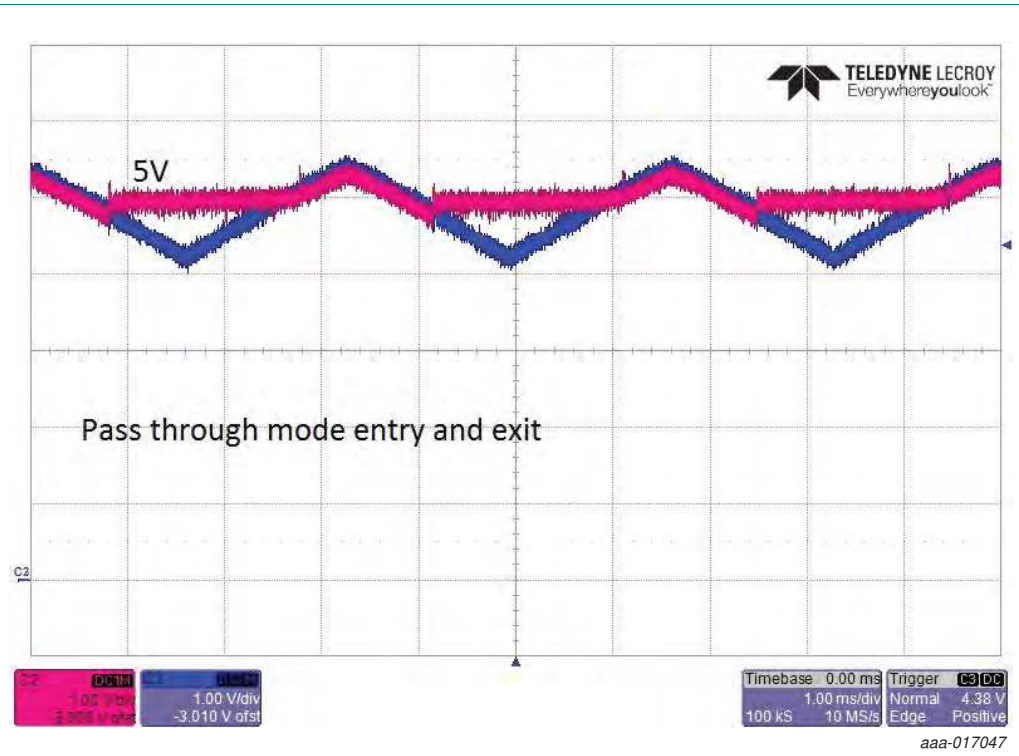


Fig 13. Pass through

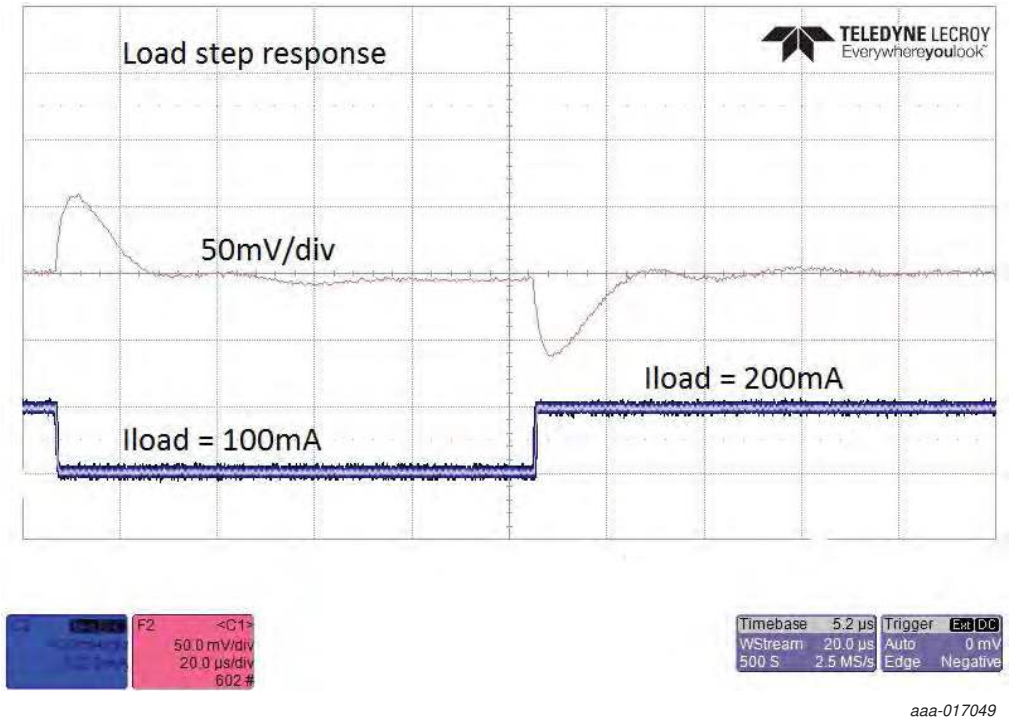


Fig 14. Load step

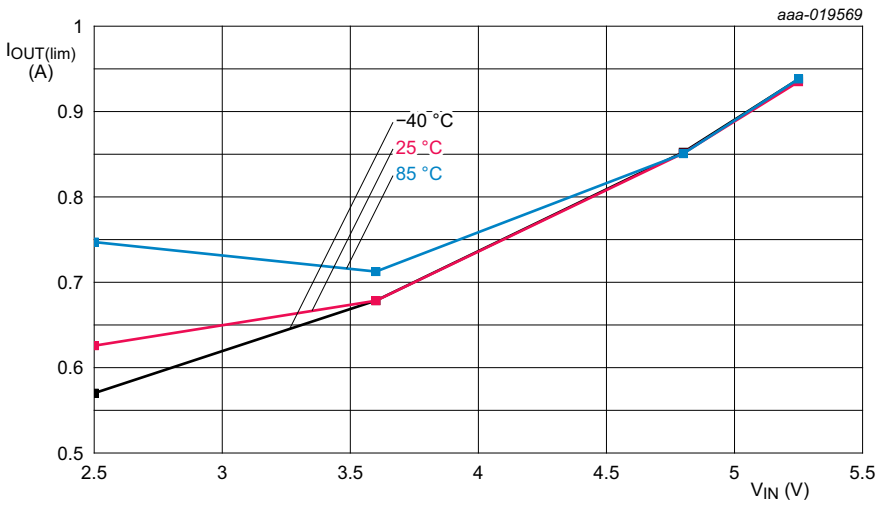


Fig 15. Typical load current capability vs V_{IN} and temp

11. Application information

11.1 Overcurrent protection

Conventional Boost convertors have no output current limit protection. Additionally they have a phantom power path made up of the inductor and output diode connecting the input directly to the output; this causes an inrush of current when power is applied. The PCA9410 has extra provisions to prevent the inrush current and output current limit problems.

To implement these protections this device has a start-up state machine. This machine includes a two-stage pre-charge of the output circuitry:

- Stage 1, Inrush control: a 1 A current source is turned on providing a path from input to output while a voltage comparator and a timer1 are active. If the output voltage doesn't reach V_{IN} - 200 mV within 1 ms, the device goes into the fault state. If the output voltage reaches 200 mV below the input voltage first the state machine advances to the boost mode soft start state.
- Stage 2, Boost Soft-Start: Starting from $V_{OUT} = V_{IN}$, the output will ramp up to V_{OUT} target. The PMOS current limit will be enabled during this stage.

The current levels are implemented through the synchronous rectifier transistor properties and drive states.

11.2 Thermal shutdown

A thermal shutdown state shuts out all other states out until the device has cooled to the (HiTemp – Thysteresis) turn back on temperature, and then it enters the fault state.

11.3 Fault recovery

When a fault occurs, the device has a fault state that disables the output for 20 ms. After the 20 ms timeout, the device will attempt a restart starting from the inrush state.

11.4 Enable delay

Once the device has been running and gets disabled, it cannot be re-enabled until the output voltage discharges down to the input voltage. The device has an internal pull-down to accomplish this, however in the absence of any external load this will take 3 ms. Any external load will shorten the time it takes to get re-enabled.

11.5 Connection diagram

The DC-to-DC converter requires an external inductor and two decoupling capacitors.

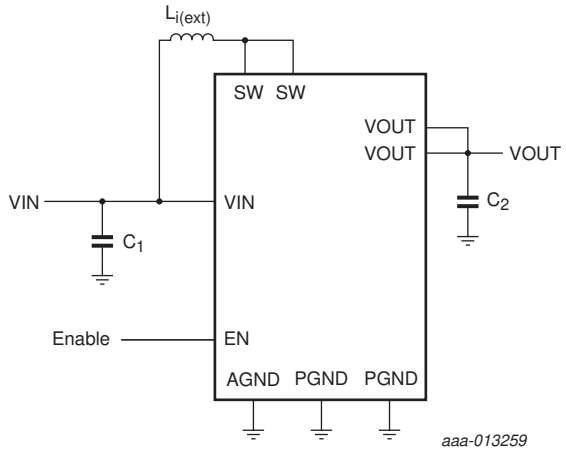


Fig 16. Simple DC-to-DC application diagram

11.6 Recommended inductors

In order to ensure proper operation of the step-up DC-to-DC converter an inductor with a sufficient inductance and sufficient saturation current value needs to be used. Recommended inductance is 1 μH. Using this recommended 0603 inductor puts a 300 mA current limit on the circuit; this inductor has a 800 mA saturation current. For more output current a larger, higher saturation current inductor will be required according to Figure 17. The saturation current of the inductor has to be properly chosen for the input voltage and load current range. The lower the input voltage the higher the input current for a given load current. Once the saturation current of the inductor is reached, the ferromagnetic core of the inductor will show a rapid nonlinear behavior and the output current capability of the circuit will drop significantly.

Table 9. Recommended inductors

Inductor	Manufacturer	Product	Parameter	Package size
L	Abracon	ASMPH-0603-1R0M-T	1 μH	0603

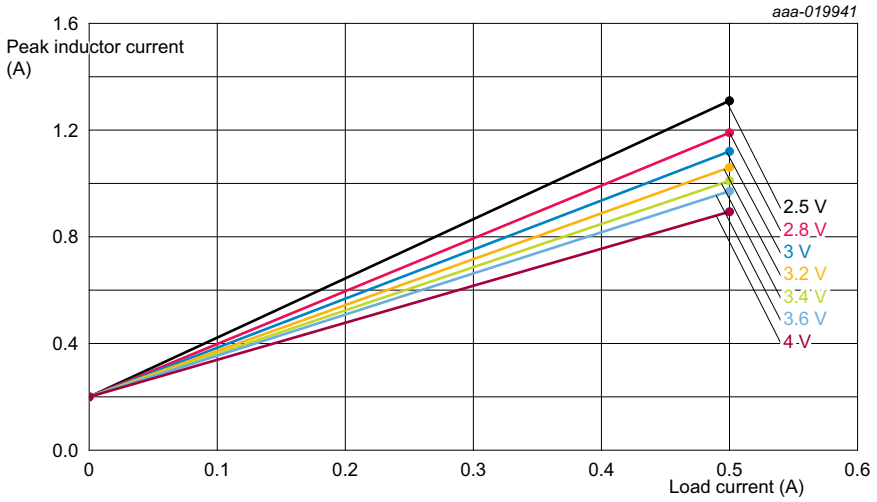


Fig 17. Inductor peak current vs Iload and V_{IN}

11.7 Input capacitor

To eliminate unwanted voltage transients at the input, place an input decoupling capacitor of at least 2.2 μF as close as possible to the input pin. Due to the voltage dependence of the capacitor, care should be taken that the effective capacitance of 2 μF is available at input voltages up to 5.25 V. To ensure best performance, it is recommended to use a capacitor with a low Equivalent Series Resistance (ESR). When using a capacitor with X5R or X7R dielectric keep in mind that the capacitance drops significantly with voltage, thus a 22 μF cap will actually only have 4.2 μF at 5 V as shown in Table 10.

Table 10. Recommended input capacitors

Manufacturer	Product	Parameter	Package size
Samsung	CL05A106MQ5NUNC	10 μf 6.3 V, 2.5 μF at 5 V	0402
TDK	C1608X5R0J226M080AC	22 μf at 6.3 V, 4.2 μF at 5 V	0603

11.8 Output capacitor

Because of the narrow voltage-dependent capacitance spread, high temperature stability and low ESR at high frequencies, it is recommended to use the dielectric X7R or X5R. The rated capacitance of the output capacitor will be much greater than the actual capacitance at the 5 V output voltage. The device requires at least 3 μF of output capacitance at its rated output voltage for suppression of ringing, overshoot, as well as for loop stability. We recommend a 22 μF 6.3 V capacitor that is actually a 4.2 μF capacitor when biased at 5 V.

Table 11. Recommended output capacitors

Cap	Manufacturer	Product	Parameter	Package size
C_2	TDK	C1608X5R0J226M080AC	22 μF 6.3 V, 4.2 μF at 5 V	0603

When the space on the application board allows, it is recommended to use two capacitors instead of a single large value. The reason is that the equivalent series inductance reduces to half when using two capacitors with the same value and this helps the capacitors to work more efficiently against high frequency noise where it can be reduced by a factor of 2. The minimum capacitance needed can either be obtained with a single 22 μF capacitor or two 10 μF capacitors when the space allows and lower noise is targeted; keep in mind that the bulk capacitance at the output voltage needs to be greater than 3.0 μF for control loop stability, and two large capacitors will have superior performance when compared with two smaller capacitors. The boost factor, output current, switching frequency and the desired peak to peak ripple limit define the minimum capacitance needed.

The duty cycle (D) needed with 90 % efficiency at a worst case of 2.5 V V_{IN}.

$$D = 1 - \frac{Eff \times V_{IN}}{V_{OUT}} \quad (1)$$

For the minimum input voltage 2.5 V and 5 V output voltage → D = 0.55

Using the simplified correlation between the current ($I_{OUT(max)}$), ripple (V_{ripple}), duty cycle (D) and switching frequency (f_{sw}) the minimum C_{out} capacitance can be calculated as follows:

$$C_{OUT(min)} = I_{OUT(max)} \times \frac{D}{f_{sw} \times V_{ripple}} \quad (2)$$

With a sample set of values: I_{out} = 300 mA, D = 0.55, f_{sw} = 3 MHz, V_{ripple} = 20 mV

$C_{OUT(min)}$ = 2.75 μF (This is not the nominal value at 0 V bias, it is the derated value at 5 V bias).

This value presumes that the ESR and ESL of the capacitor is negligible and the path output-capacitor-ground is as short as possible. Compensating for the listed factors, the minimum output capacitance is specified at 3.0 μf at 5 V. How much the capacitance degrades at high bias voltage is supplier dependent and especially when 0402 size capacitors are chosen the voltage dependence should be taken into consideration.

11.9 Layout of the PCB

The most critical layout constraint of this circuit is that the output Cap C2 be placed as close to the IC as possible. Use short wide traces to connect this capacitor to the IC. See below for an example of the layout detailing the IC and the output capacitor. The connection from switch pin to the inductor should have minimum capacitance to GND.

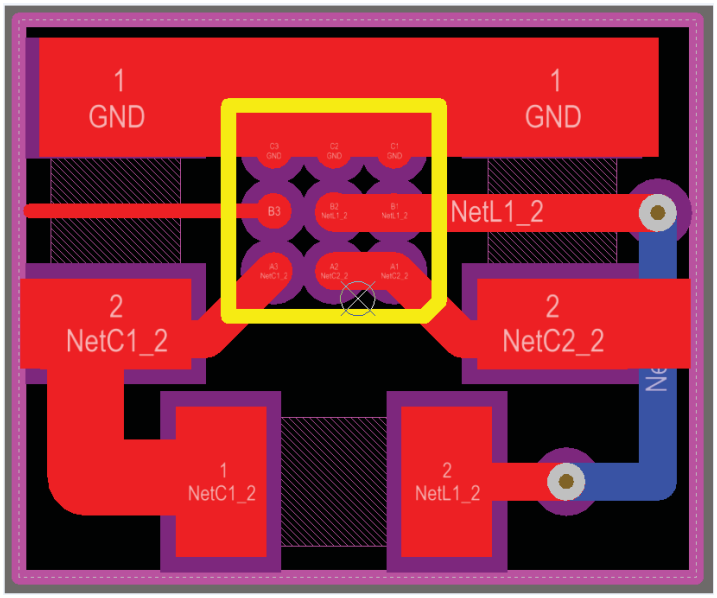
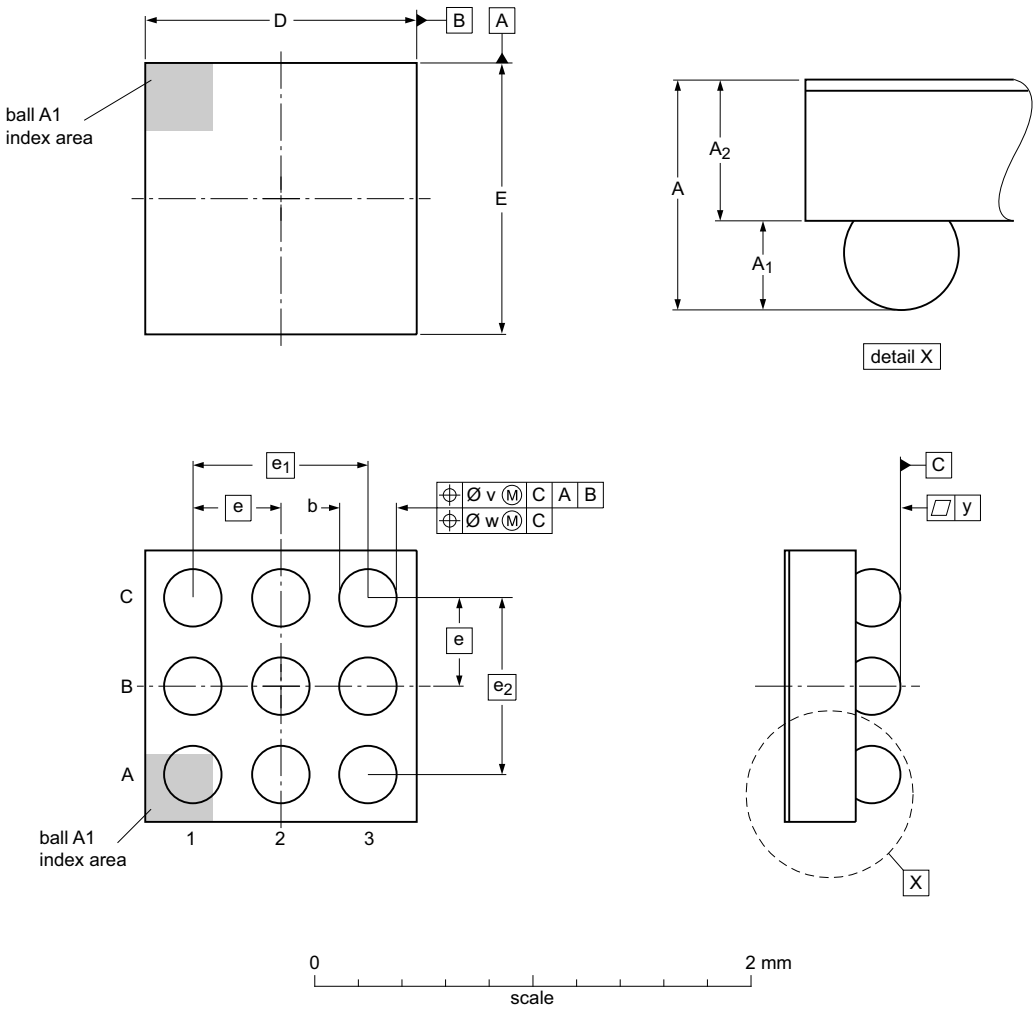


Fig 18. Layout of PCB

12. Package outline

WLCSP9: wafer level chip-scale package; 9 bumps; 1.24 x 1.24 x 0.525 mm (backside coating included) **PCA9410**



Dimensions (mm are the original dimensions)

Unit		A	A_1	A_2	b	D	E	e	e_1	e_2	v	w	y
mm	max	0.565	0.23	0.350	0.29	1.27	1.27						
	nom	0.525	0.20	0.325	0.26	1.24	1.24	0.4	0.8	0.8	0.15	0.05	0.05
	min	0.485	0.17	0.300	0.23	1.21	1.21						

Note: Backside coating 25 µm

wlcsp9_pca9410_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
PCA9410						~~14-09-01~~ 15-07-23

Fig 19. Package outline WLCSP9

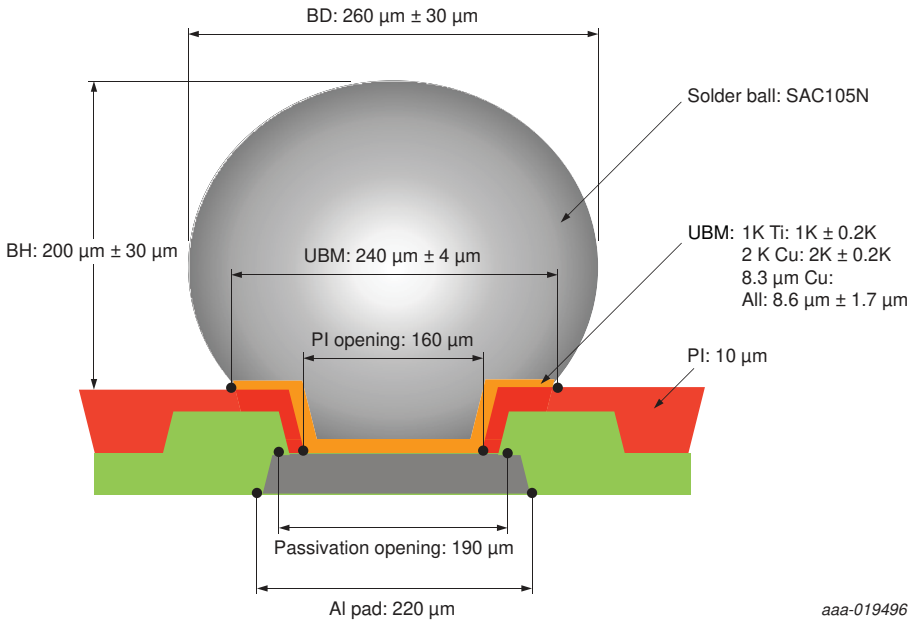


Fig 20. WLCSP9 Under Ball Metal (UBM) structure

13. Soldering of WLCSP packages

13.1 Introduction to soldering WLCSP packages

This text provides a very brief insight into a complex technology. A more in-depth account of soldering WLCSP (Wafer Level Chip-Size Packages) can be found in application note *AN10439 "Wafer Level Chip Scale Package"* and in application note *AN10365 "Surface mount reflow soldering description"*.

Wave soldering is not suitable for this package.

All NXP WLCSP packages are lead-free.

13.2 Board mounting

Board mounting of a WLCSP requires several steps:

1. Solder paste printing on the PCB
2. Component placement with a pick and place machine
3. The reflow soldering itself

13.3 Reflow soldering

Key characteristics in reflow soldering are:

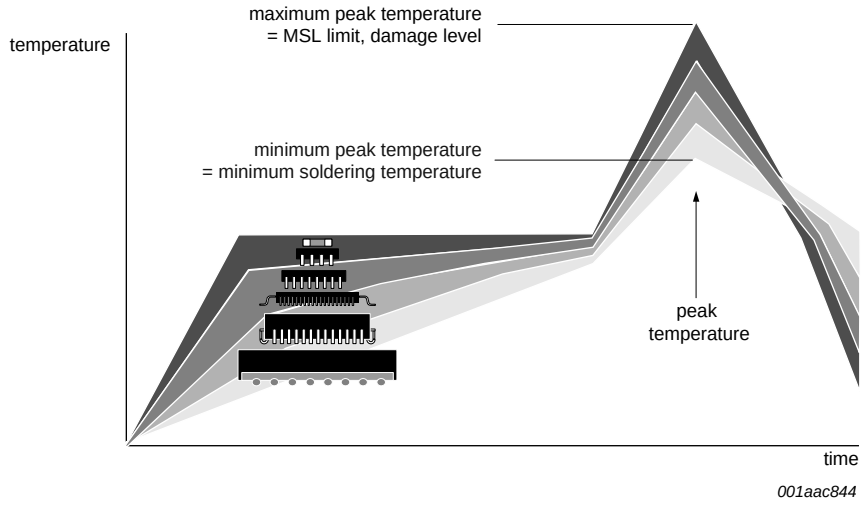
- Lead-free versus SnPb soldering; note that a lead-free reflow process usually leads to higher minimum peak temperatures (see Figure 21) than a SnPb process, thus reducing the process window
- Solder paste printing issues, such as smearing, release, and adjusting the process window for a mix of large and small components on one board
- Reflow temperature profile; this profile includes preheat, reflow (in which the board is heated to the peak temperature), and cooling down. It is imperative that the peak temperature is high enough for the solder to make reliable solder joints (a solder paste characteristic) while being low enough that the packages and/or boards are not damaged. The peak temperature of the package depends on package thickness and volume and is classified in accordance with Table 12.

Table 12. Lead-free process (from J-STD-020D)

Package thickness (mm)	Package reflow temperature (°C)		
	Volume (mm^3)		
	< 350	350 to 2000	> 2000
< 1.6	260	260	260
1.6 to 2.5	260	250	245
> 2.5	250	245	245

Moisture sensitivity precautions, as indicated on the packing, must be respected at all times.

Studies have shown that small packages reach higher temperatures during reflow soldering, see Figure 21.



MSL: Moisture Sensitivity Level

Fig 21. Temperature profiles for large and small components

For further information on temperature profiles, refer to application note *AN10365 "Surface mount reflow soldering description"*.

13.3.1 Stand off

The stand off between the substrate and the chip is determined by:

- The amount of printed solder on the substrate
- The size of the solder land on the substrate
- The bump height on the chip

The higher the stand off, the better the stresses are released due to TEC (Thermal Expansion Coefficient) differences between substrate and chip.

13.3.2 Quality of solder joint

A flip-chip joint is considered to be a good joint when the entire solder land has been wetted by the solder from the bump. The surface of the joint should be smooth and the shape symmetrical. The soldered joints on a chip should be uniform. Voids in the bumps after reflow can occur during the reflow process in bumps with high ratio of bump diameter to bump height, i.e. low bumps with large diameter. No failures have been found to be related to these voids. Solder joint inspection after reflow can be done with X-ray to monitor defects such as bridging, open circuits and voids.

13.3.3 Rework

In general, rework is not recommended. By rework we mean the process of removing the chip from the substrate and replacing it with a new chip. If a chip is removed from the substrate, most solder balls of the chip will be damaged. In that case it is recommended not to re-use the chip again.

Device removal can be done when the substrate is heated until it is certain that all solder joints are molten. The chip can then be carefully removed from the substrate without damaging the tracks and solder lands on the substrate. Removing the device must be done using plastic tweezers, because metal tweezers can damage the silicon. The surface of the substrate should be carefully cleaned and all solder and flux residues and/or underfill removed. When a new chip is placed on the substrate, use the flux process instead of solder on the solder lands. Apply flux on the bumps at the chip side as well as on the solder pads on the substrate. Place and align the new chip while viewing with a microscope. To reflow the solder, use the solder profile shown in application note *AN10365 "Surface mount reflow soldering description"*.

13.3.4 Cleaning

Cleaning can be done after reflow soldering.

14. References

[1] **IEC60134 —** Rating systems for electronic tubes and valves and analogous semiconductor devices

[2] **IEC61340-3-1 —** Method for simulation of electrostatic effects - Human body model (HBM) electrostatic discharge test waveforms

[3] **JESD22-A115C —** Electrostatic Discharge (ESD) Sensitivity Testing Machine Model (MM)

[4] **NX2-00001 —** NXP Semiconductors Quality and Reliability Specification

[5] **AN10365 —** NXP Semiconductors application note "Surface mount reflow soldering description"

15. Revision history

Table 13. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PCA9410 v.1.1	20160805	Product data sheet	-	PCA9410 v.1
Modifications:	• Deleted Figure 12 Startup			
PCA9410 v.1	20151008	Product data sheet	-	-

16. Legal information

16.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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