DAC8564/65 Evaluation Module

This user's guide describes the characteristics, operation, and the use of the DAC8564/65 evaluation module. It covers all pertinent areas involved to properly use this EVM board along with the devices that it supports. The physical PCB layout, schematic diagram, and circuit descriptions are included.

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1 EVM Overview

This section gives a general overview of the DAC8564/65 evaluation module (EVM) and describes some of the factors that must be considered in using this module.

1.1 Features

This EVM features the DAC8564 or the DAC8565 digital-to-analog converters (DAC). The DAC8564/65EVM is a simple evaluation module designed as a quick and easy way to evaluate the functionality and performance of the 16-bit high-resolution, quad-channel, and serial input DAC with a built-in 2.5-V internal reference that is enabled by default. This EVM features a serial interface to communicate with any host microprocessor or TI DSP-based system.

Although the DAC was designed for single-supply operation, a bipolar output range is also possible by properly configuring the output operational amplifier, U2, circuit. This is discussed in detail in section 3.2.3. In addition, the external operational amplifier is also installed as an option to provide output signal conditioning or boost capacitive load drive and for other output mode requirement desired. The external output operational amplifier only supports one DAC output at a time.

A +5-V precision voltage reference is provided via U3 as well as a provision to apply user's choice of reference supply via TP2 and TP3 test points. These reference supplies are optional voltage references provided externally in case it is necessary to evaluate the DAC8564/65 with external reference circuits. The external +5-V reference source for $V_{REF}H$ can be selected via JMP8 jumper configuration.

The EVM also has a provision for possibly experimenting with different circuit loads on the reference of the DAC8564/65. These are available through R25 and C14.

1.2 Power Requirements

The following sections describe the power requirements of this EVM.

1.2.1 Supply Voltage

The DC power supply requirement for this DAC8564/65EVM (AVDD and IOVDD) is selectable between +3.3 V and +5 V via jumper headers (JMP7 and JMP17). The AVDD supply of +3.3 VA comes from J3A-8 whereas the +5 VA comes from J3A-3 terminal. The IOVDD supply of +3.3 VD comes from J3A-9 whereas the +5 VD comes from J3A-10 terminal. These power supply voltages are referenced to ground through the J3A-6 and J3A-5 terminals, respectively. The VCC and VSS supplies are only used by the U2 and U4 operational amplifiers as well as the U3 voltage reference, which ranges from +15 V to –15 V maximum and connects through J3A-1 and J3A-2 terminals, respectively. All the analog power supplies are referenced to analog ground through J3A-6 terminal.

The negative rail of the output operational amplifier, U2, can be selected between VSS and AGND via JMP10 jumper. The external operational amplifier is installed as an option to provide output signal conditioning or for other output mode requirement that is desired by the user.

CAUTION

To avoid potential damage to the EVM board, ensure that the correct cables are connected to their respective terminals as labeled on the EVM board.

Stresses greater than the maximum listed voltage ratings may cause permanent damage to the device.

1.2.2 Reference Voltage

The DAC8564/65 is equipped with a +2.5-V internal reference that is enabled by default. The +2.5-V internal reference can be measured from its $V_{REF}H$ pin, which can be used to source other devices that requires +2.5-V reference. Because the DAC8564/65's internal reference is enabled by default, care should be taken to ensure that the JMP8 is open and JMP9 is shorted between pins 1 and 2. Otherwise, inaccurate performance or damage to the part can result. Provided that the external voltage that is applied to the $V_{REF}H$ pin does not exceed the applied voltage in the V_{DD} pin, and it does not exceed 100 mA of sourcing current, the DAC8564/65 should not be damaged. It is not recommended to leave the external voltage applied on the $V_{REF}H$ pin if the internal reference is not disabled. The external reference source must be disconnected immediately and the EVM power must be recycled to ensure the correct performance of the device.

The +5-V precision voltage reference is provided as an optional reference source to supply the external voltage reference for the DAC through REF02, U3. This reference voltage is selectable via jumper, JMP8. When shorting pins 1 and 2, the +5-V reference is selected whereas shorting pins 2 and 3 selects user preferred reference. The jumper, JMP9 must be shorted between pins 1 and 2 in order for the $V_{REF}L$ pin of the DAC to be properly grounded.

The +5-V reference voltage goes through an adjustable 100-kΩ potentiometer, R15, in series with 20-kΩ R16, to allow the user to adjust the reference voltage to its desired settings. The voltage reference is then buffered through U4A as seen by the device under test. The REF02 precision reference is powered by V_{CC} (+15 V) through J3A-1 terminal.

CAUTION

When applying an external voltage reference through TP2 or J4A-20, ensure that it does not exceed the applied AVDD. Otherwise, this can permanently damage the DAC8564/65, U1, device under test.

1.3 EVM Basic Functions

This EVM is designed primarily as a functional evaluation platform to test certain functional characteristics of the DAC8564/65 digital-to-analog converter. Functional evaluation of the installed DAC device can be accomplished with the use of any microprocessor, TI DSP, or a signal/waveform generator.

The headers J2A (top side) and J2B (bottom side) are pass-through connectors provided to allow the control signals and data required to interface a host processor or waveform generator to the DAC8564/65EVM using a custom-built cable.

An adapter interface board (5-6k adapter interface) is also available to fit and mate with TI's C5000™ and C6000™ DSP Starter Kit (DSK). This makes it unnecessary to build a custom cable. In addition, the Precision Analog Application group of Texas Instruments has other interface boards that are designed to connect to and interface with this EVM as well. For more details or information regarding the 5-6k adapter interface board or the other interface platforms, call Texas Instruments or send an email to dataconvapps@list.ti.com.

The DAC outputs can be monitored through the selected pins of J4A header connector. The outputs can be switched through each of their respective jumpers, JMP11, JMP12, JMP13, and JMP14 for the stacking purposes. The stacking of multiple EVMs allows a total of eight (DAC8564/65) DAC channels to be used provided that the frame synchronization signal, $\overline{\text{SYNC}}$, is unique for each EVM board stacked. The $\overline{\text{SYNC}}$ signal can be selected for each EVM board via jumper JMP18.

In addition, the option of selecting the DAC output to be fed to the non-inverting side of the output operational amplifier, U2, is also possible by using a jumper across the selected pins of J4A. The output operational amplifier, U2, must be first configured correctly for the desired waveform characteristic (see section 3 of this user's guide manual).

A block diagram of the EVM is shown in Figure 1.

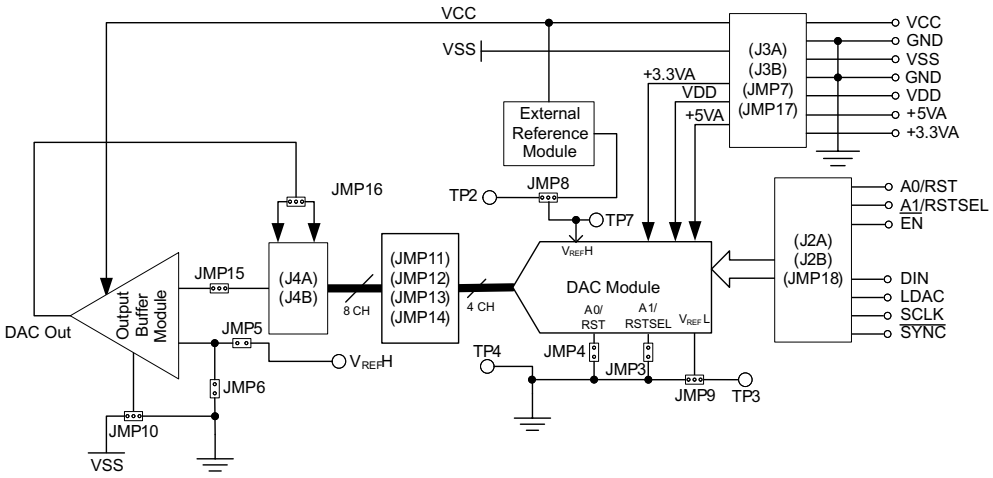


Figure 1. DAC8564/65 EVM Block Diagram

2 PCB Design and Performance

This section talks about the layout design of the PCB thereby describing the physical and mechanical characteristics of the EVM, as well as a brief description of the EVM test performance procedure performed. The list of components used on this evaluation module is also included in this section.

2.1 PCB Layout

The DAC8564/65 EVM is designed to preserve the performance quality of the DAC, device under test, as specified in the data sheet. Carefully analyzing the EVM's physical restrictions and the given or known elements that contributes to the EVM's performance degradation is the key to a successful design implementation. These obvious attributes that diminish the performance of the EVM can be easily addressed during the schematic design phase, by properly selecting the right components and building the circuit correctly. The circuit must include adequate bypassing, identifying and managing the analog and digital signals, and understanding the components mechanical attributes.

The obscure part of the design is the layout process in which limited knowledge and inexperience can easily present a problem. The main concern is primarily with component placement and the proper routing of signals. The bypass capacitors must be placed as close as possible to the pins, and the analog and digital signals must be properly separated from each other. The power and ground plane is very important and must be carefully considered in the layout process. A solid plane is ideally preferred but sometimes impractical. Therefore, when solid planes are not possible, a split plane does the job as well. When considering a split plane design, analyze the component placement and carefully split the board into its analog and digital sections starting from the device under test. The ground plane plays an important role in controlling the noise and other effects that otherwise contributes to the error of the DAC output. To ensure that the return currents are handled properly, route the appropriate signals only in their respective sections, meaning that the analog traces should only lay directly above or below the analog section and the digital traces in the digital section. Minimize the length of the traces but use the biggest possible trace width allowable in the design. These design practices discussed can be seen in the following illustrations.

The DAC8564/65EVM board is constructed on a four-layer printed-circuit board using a copper-clad FR-4 laminate material. The printed-circuit board has a dimension of 43,1800 mm (1.7000 inch) × 82,5500 mm (3.2500 inch), and the board thickness is 1,5748 mm (0.062 inch). Figure 2 through Figure 8 show the individual artwork layers.

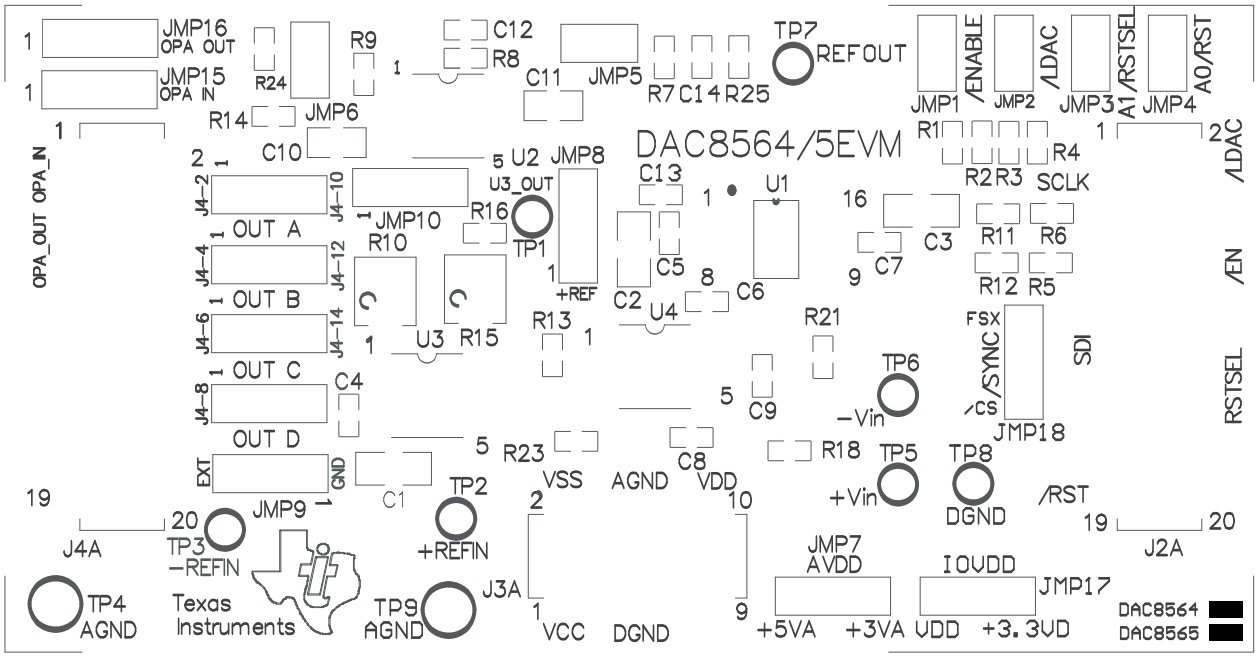


Figure 2. Top Silkscreen

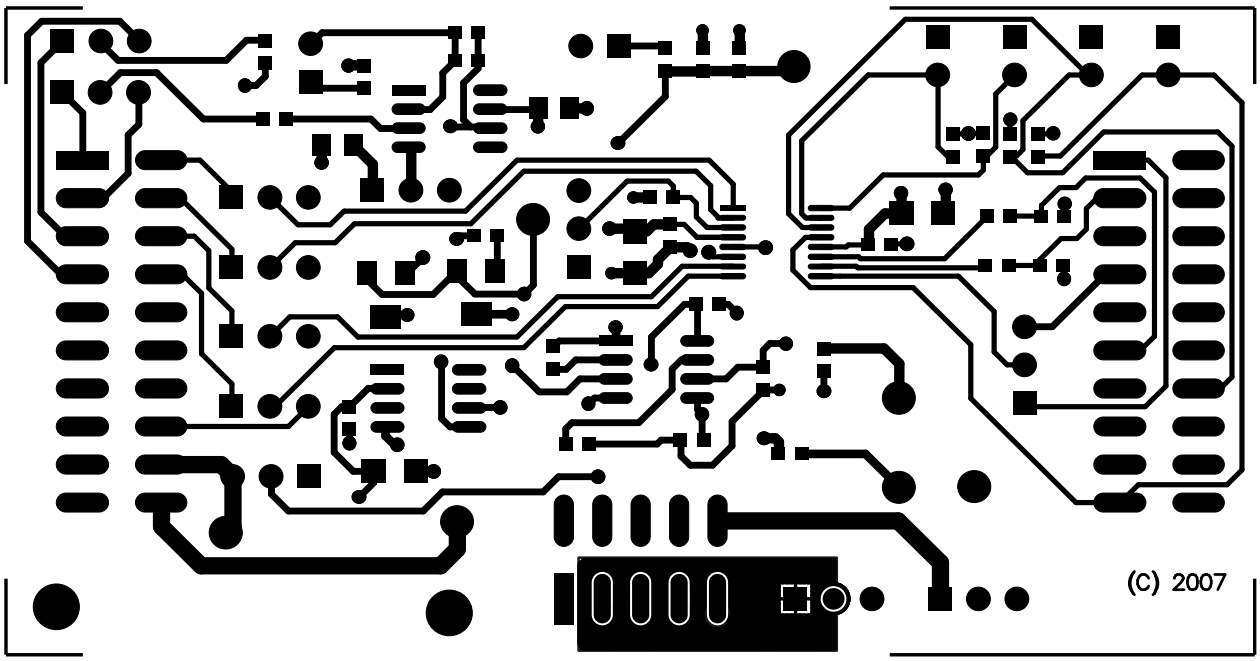


Figure 3. Layer 1 (Top Signal Plane)

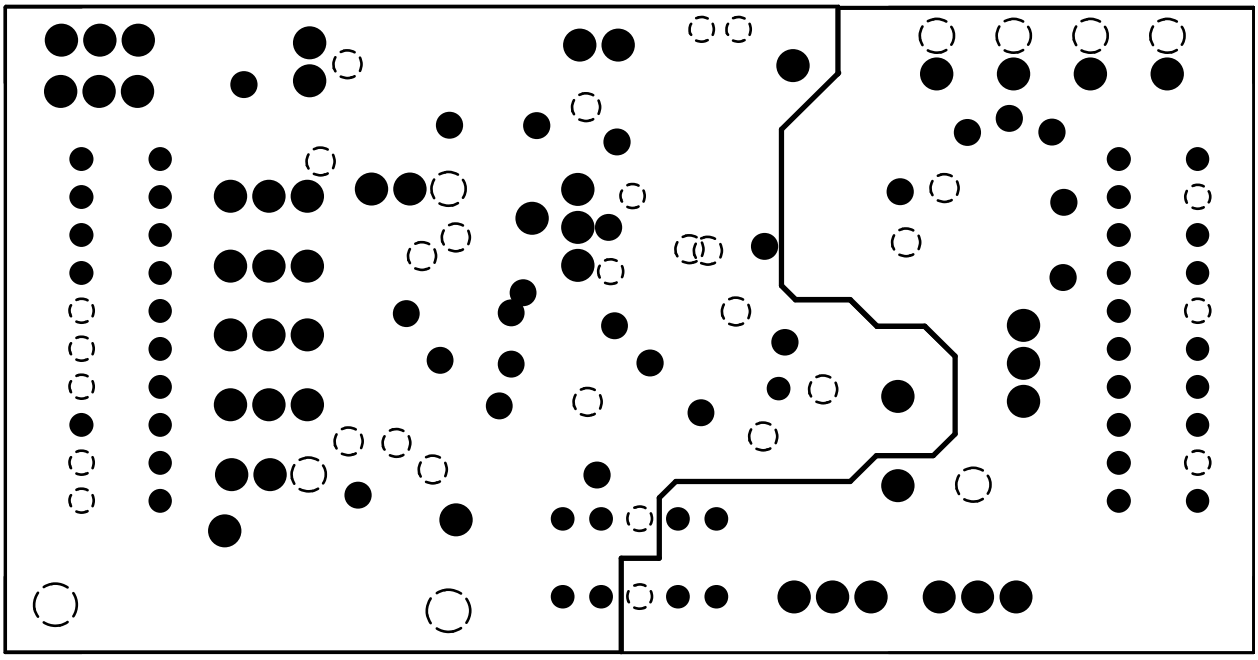


Figure 4. Layer 2 (Ground Plane)

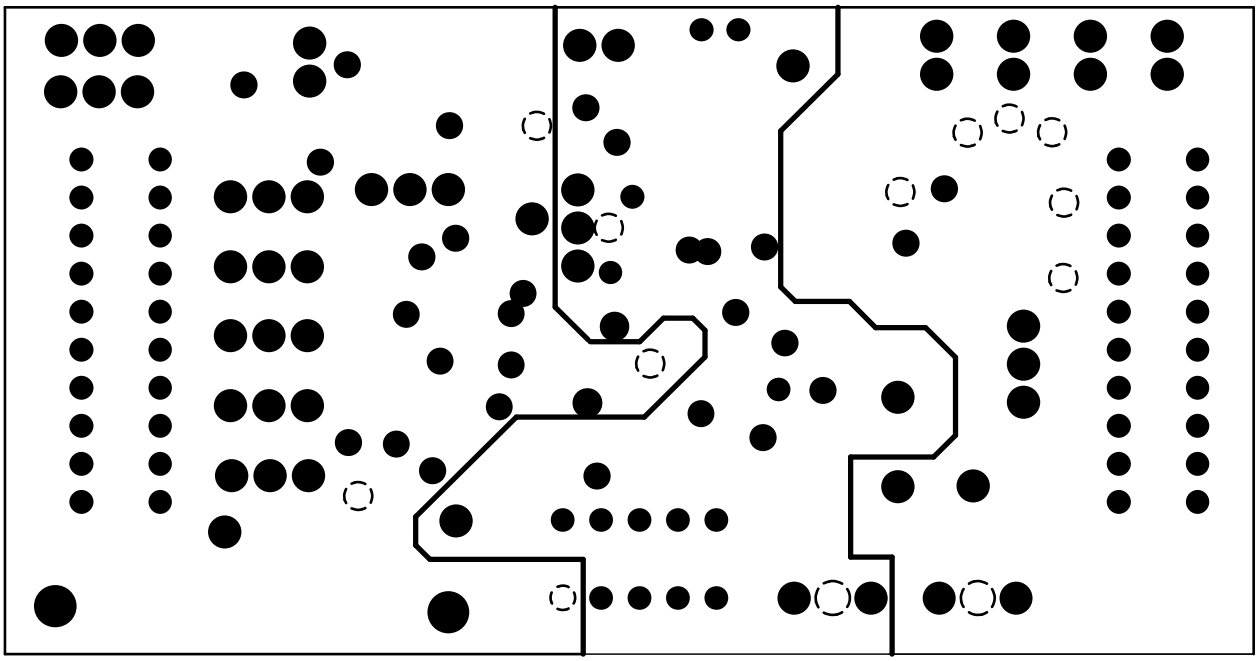


Figure 5. Layer 3 (Power Plane)

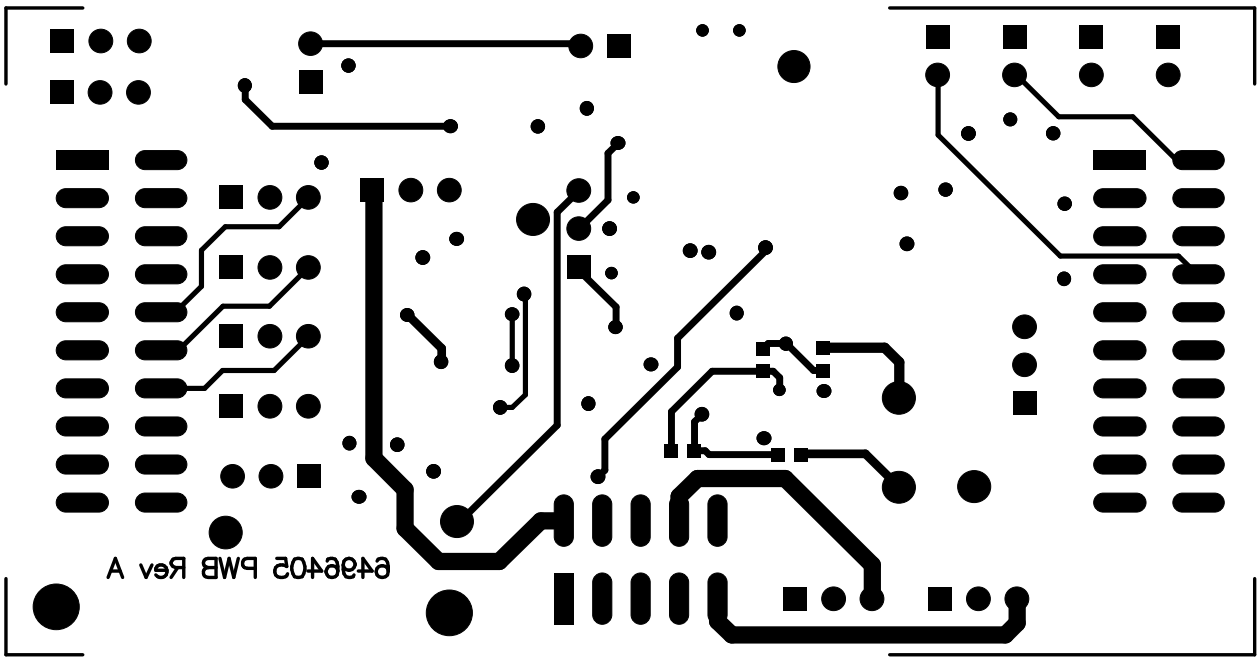


Figure 6. Layer 4 (Bottom Signal Plane)

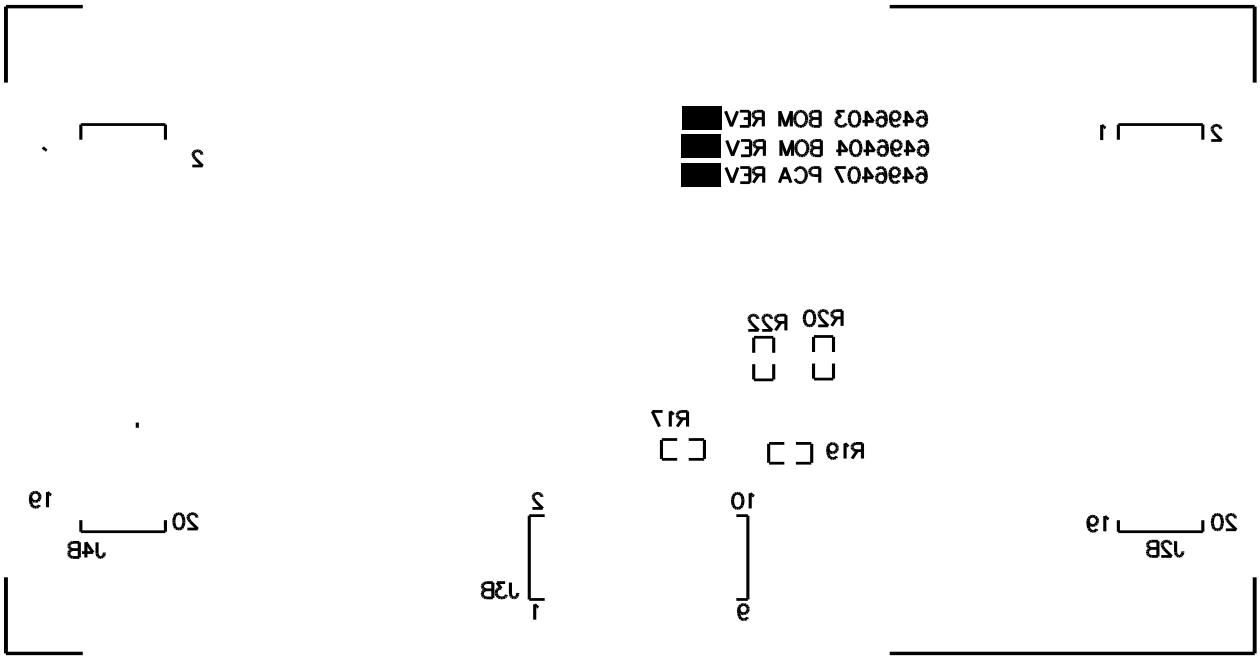


Figure 7. Bottom Silkscreen

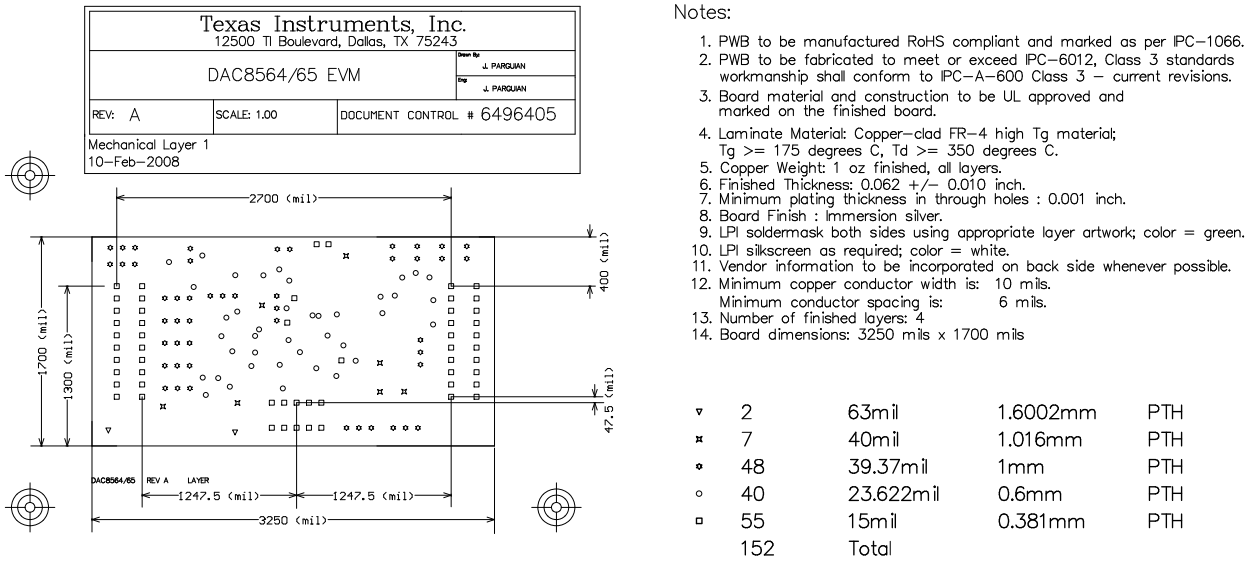


Figure 8. Drill Drawing

2.2 EVM Performance

The EVM performance test is performed using a high-density DAC bench test board, an Agilent 3458A digital multimeter, and a personal computer (PC) running the LabVIEW™ software. The EVM board is tested for all codes of 65535 and the device under test (DUT) is allowed to settle for 1 ms before the meter is read. This process is repeated for all codes to generate the measurements for INL and DNL.

Figure 9 through Figure 15 shows the INL and DNL characteristic plots for each DAC channels of the DAC8564 and the DAC8565, respectively.

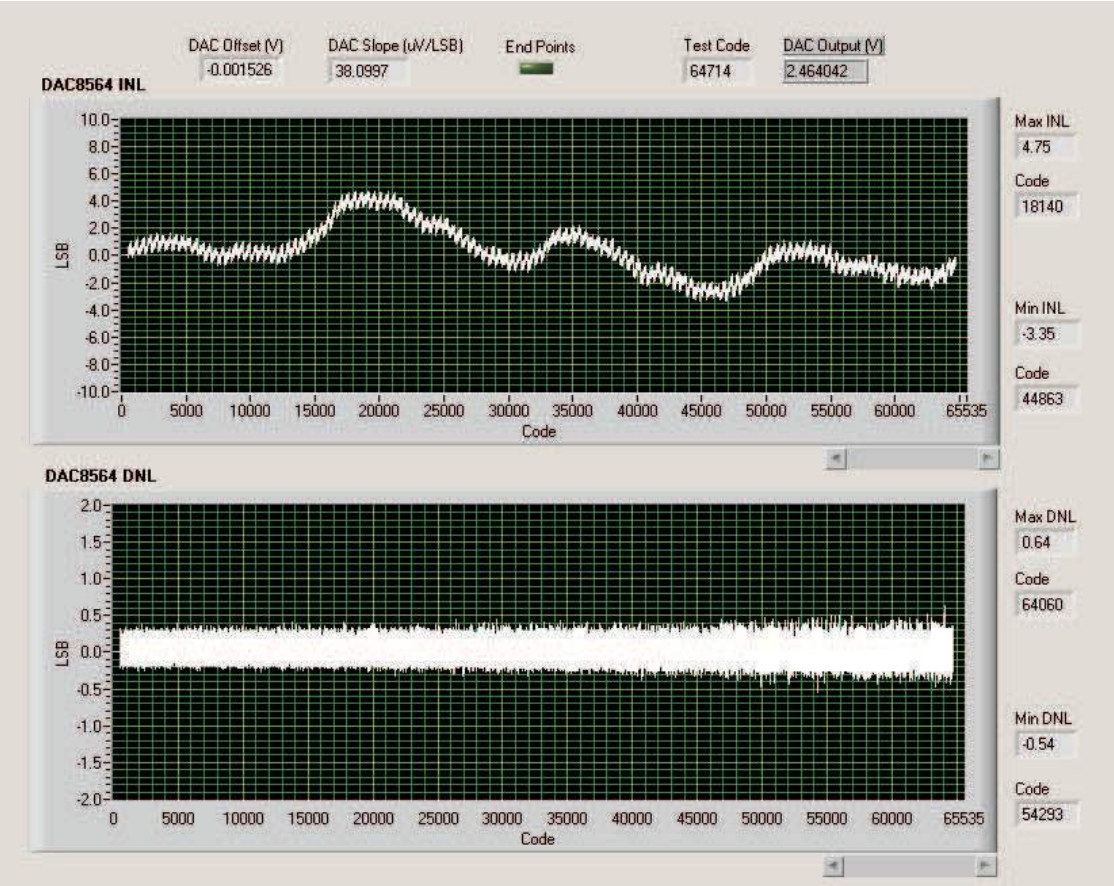


Figure 9. DAC8564 Channel A INL and DNL Characteristic Plot

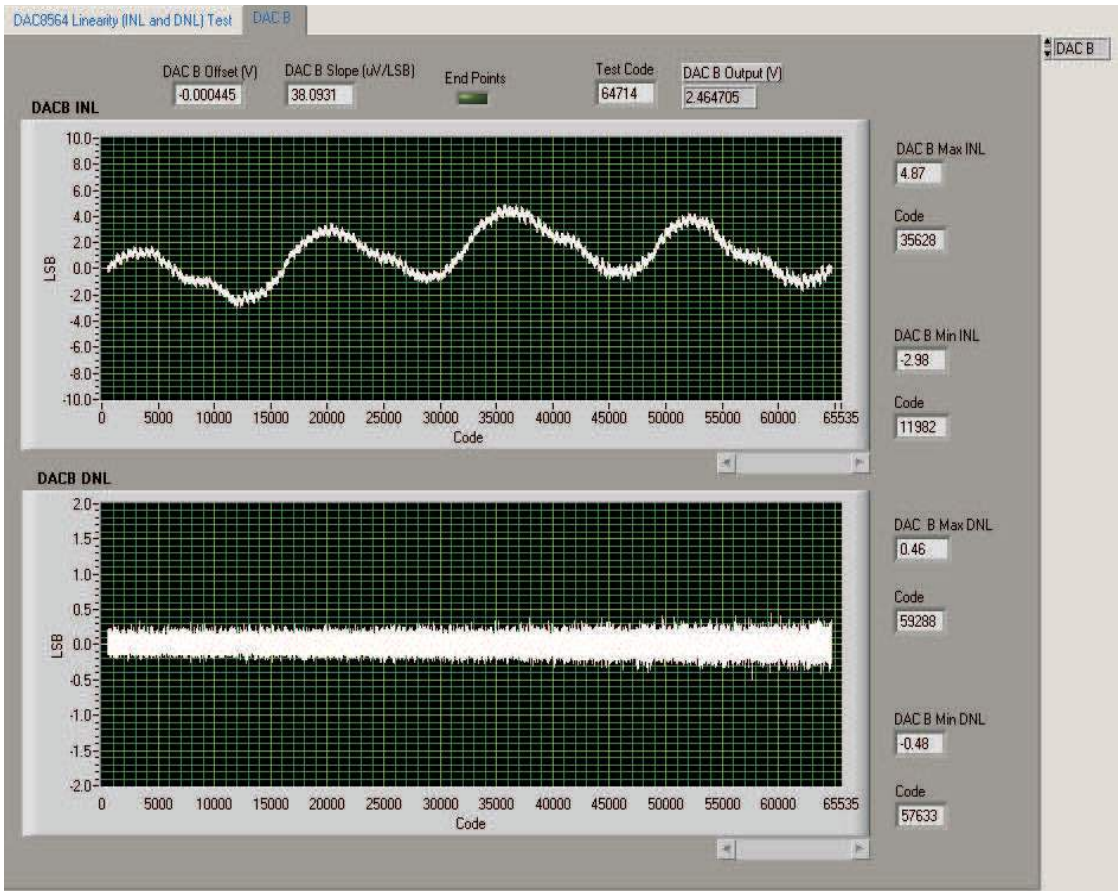


Figure 10. DAC8564 Channel B INL and DNL Characteristic Plot

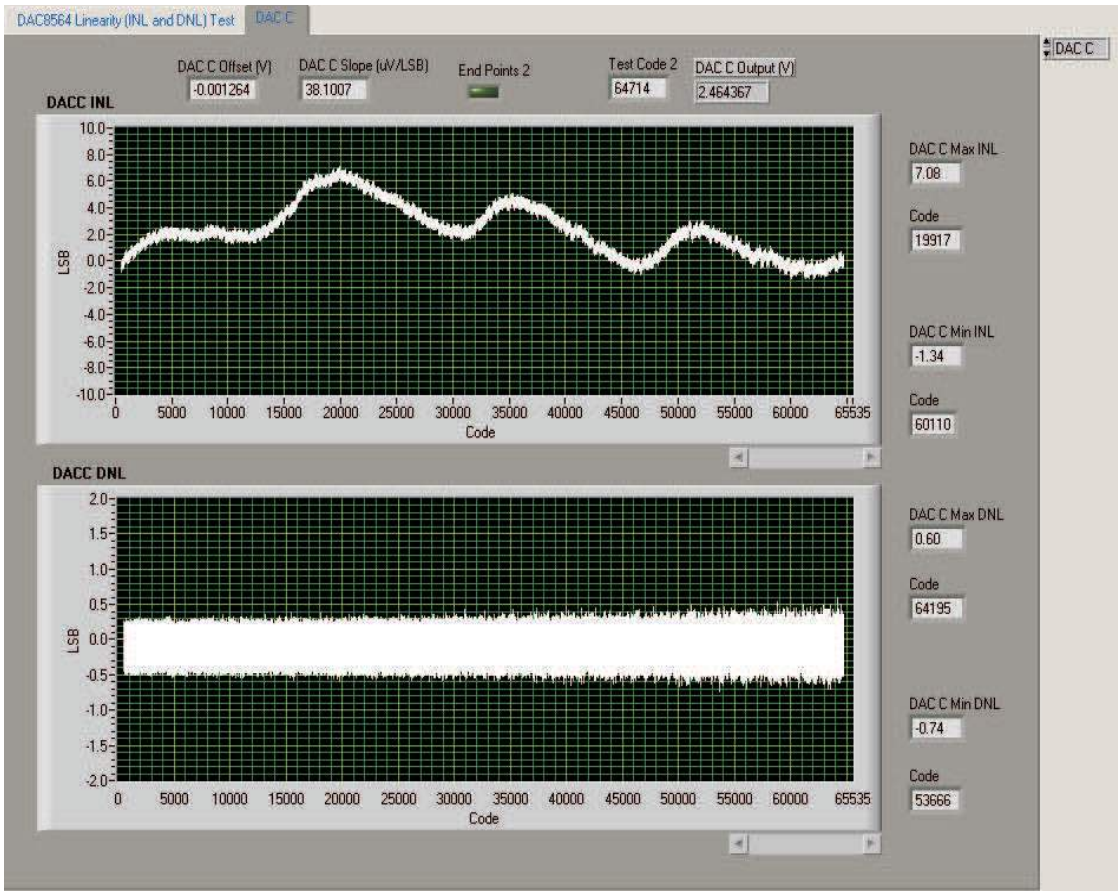


Figure 11. DAC8564 Channel C INL and DNL Characteristic Plot

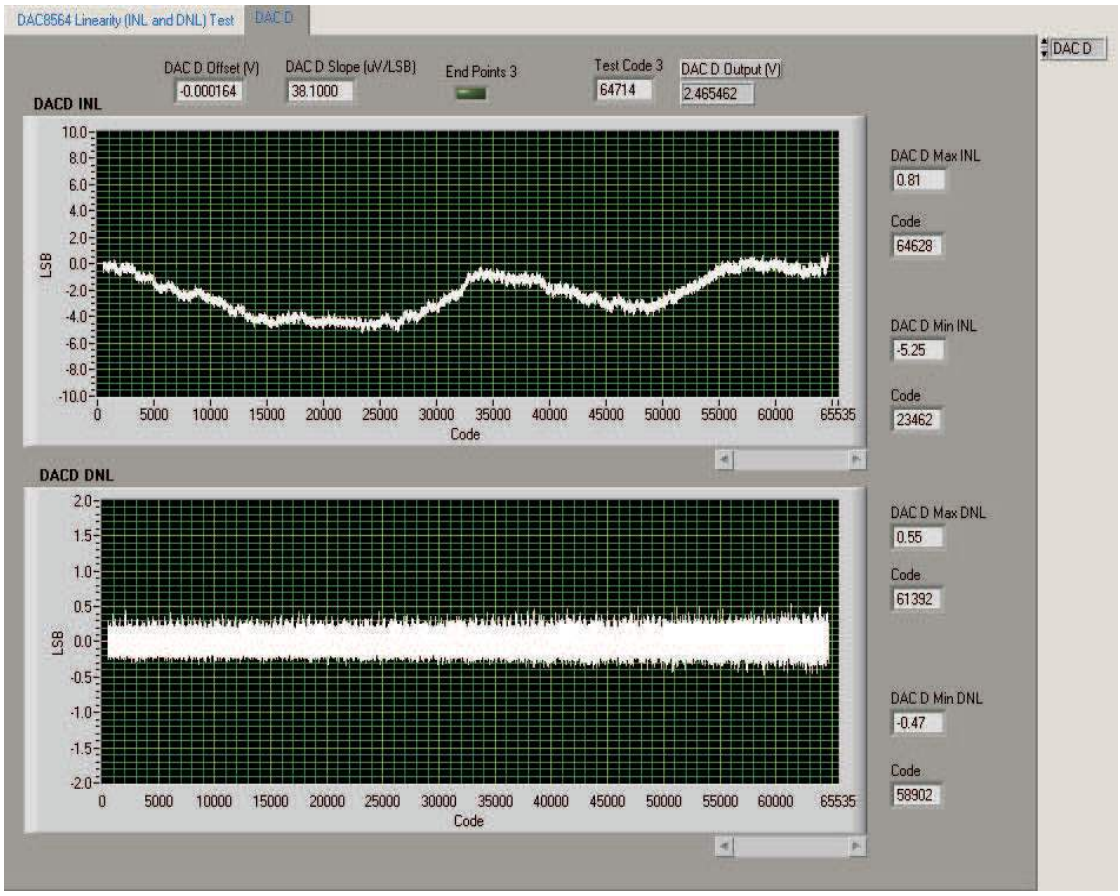


Figure 12. DAC8564 Channel D INL and DNL Characteristic Plot

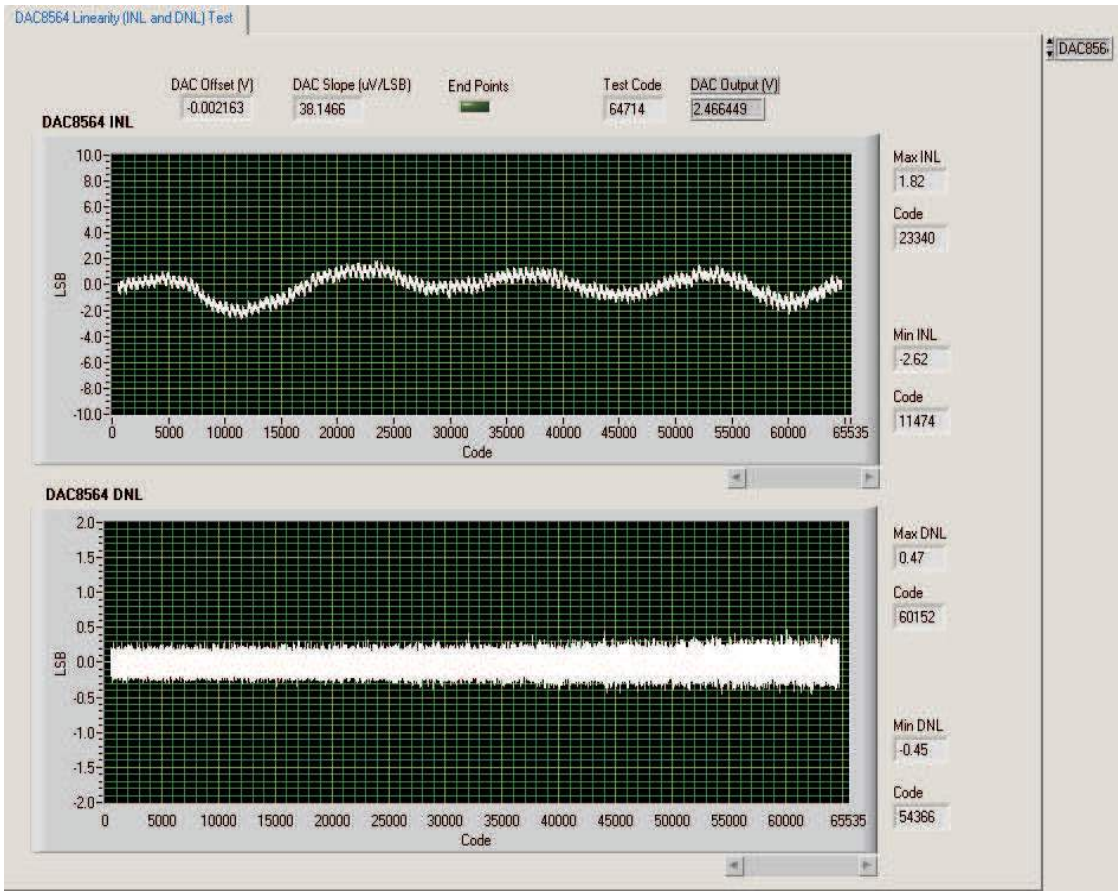


Figure 13. DAC8565 Channel A INL and DNL Characteristic Plot

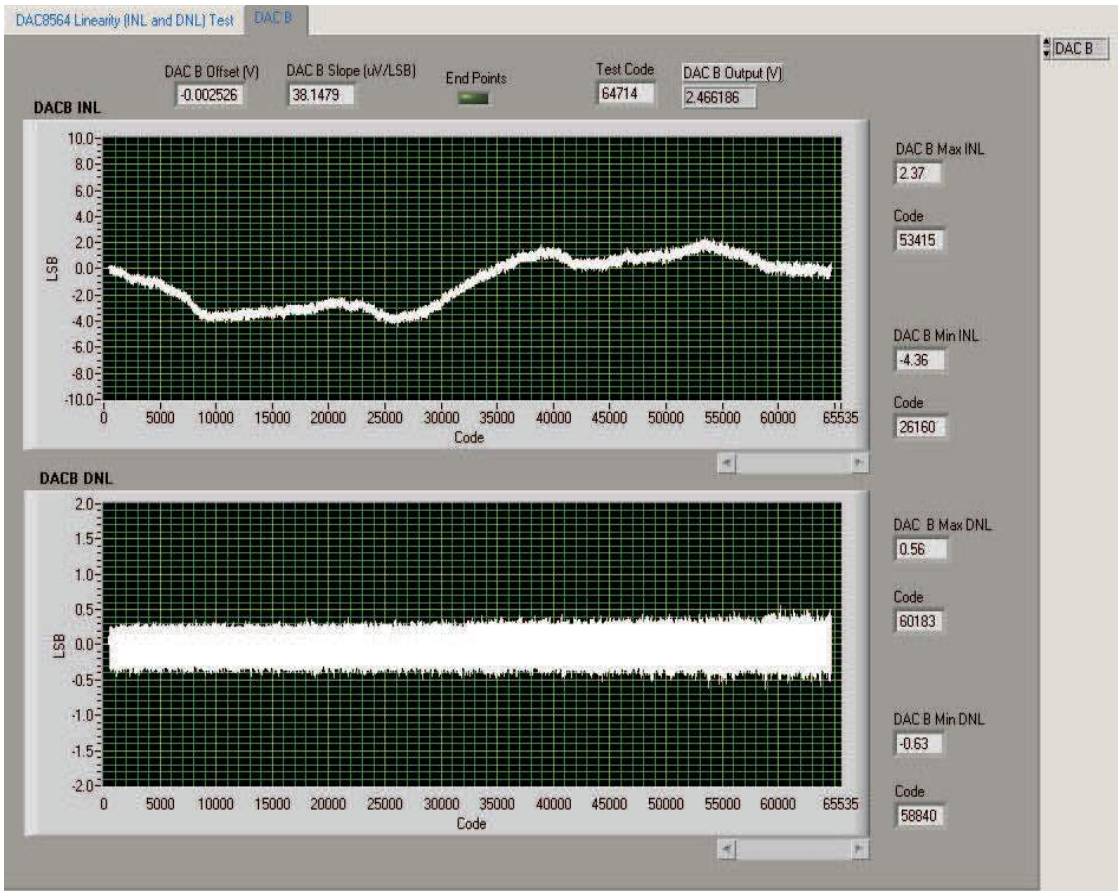


Figure 14. DAC8565 Channel B INL and DNL Characteristic Plot

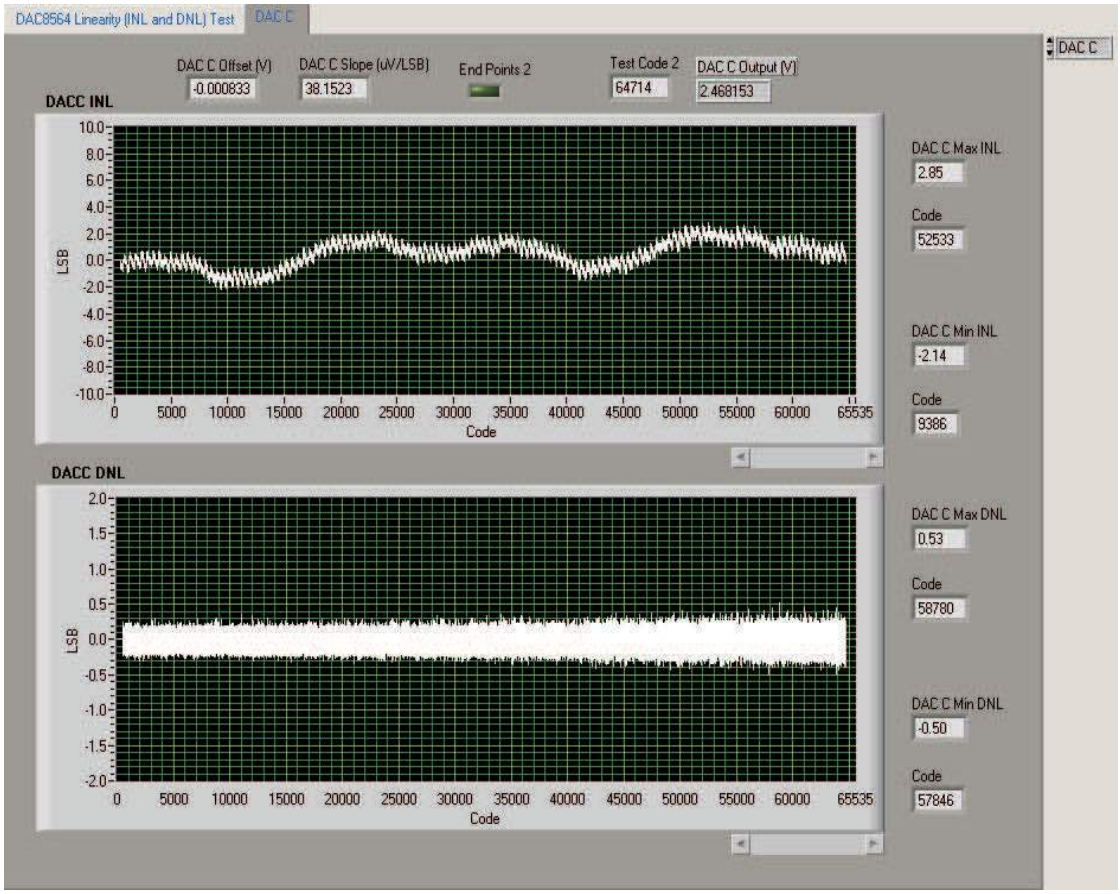


Figure 15. DAC8565 Channel C INL and DNL Characteristic Plot

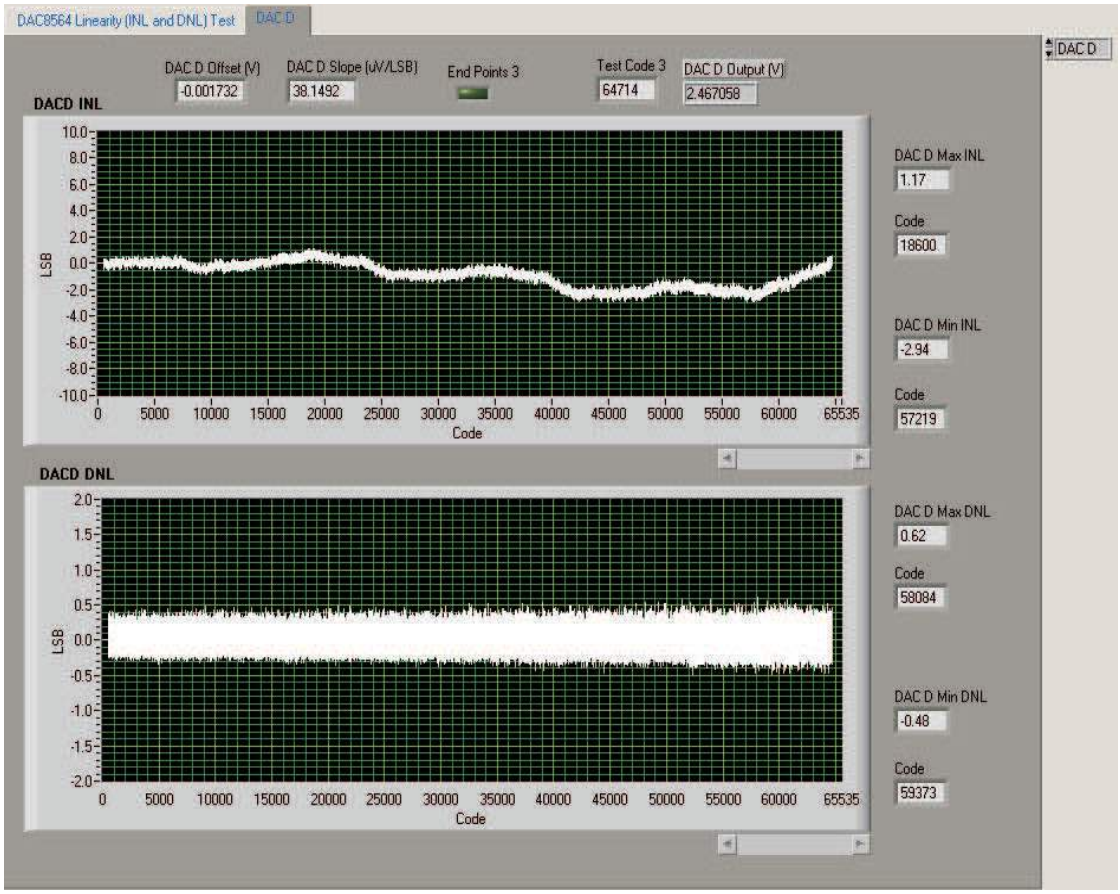


Figure 16. DAC8565 Channel D INL and DNL Characteristic Plot

2.3 Bill of Materials

Table 1. Parts List

Item	Qty.	Value	Designators	Description	Vendor	Vendor Part No.
1	7	10kΩ	R1–R4, R–R9	1/10W 0603 Thick Film Chip Resistor, ±1% Tol	Panasonic	ERJ-3EKF1002V
2	1	20kΩ Trim Pot	R10	5T Potentiometer, 4mm SMD, Cermet	Bourns	3214W-1-203E
3	4	0Ω	R11–R14	1/16W 0603 Thick Film Chip Resistor, ±1% Tol	Panasonic	ERJ-3EKF0R00V
4	1	100kΩ Trim Pot	R15	Potentiometer, 4mm SMD, Cermet	Bourns	3214W-1-104E
5	1	20KΩ	R16	1/10W 0603 Thick Film Chip Resistor, ±1% Tol	Panasonic	ERJ-3EKF2002V
6	1	100 Ω	R24	W 1206 Thick Film Chip Resistor, ±5% Tol	Panasonic	ERJ-8GEYJ101V
7	3	10F	C1–C3	Multilayer Ceramic Chip Capacitor, 1206 SMD, 16V, ±15% TC, ±20% Tol	TDK	C3216X7R1C106M
8	4	0.1µF	C4–C7	Multilayer Ceramic Chip Capacitor, 0603 SMD, 25V, ±15% TC, ±10% Tol	TDK	C1608X7R1E104K
9	2	1µF	C10, C11	Multilayer Ceramic Chip Capacitor, 0805 SMD, 25V, ±15% TC, ±10% Tol	TDK	C2012X7R1E105K
10	1	1nF	C12	Multilayer Ceramic Chip Capacitor, 0603 SMD, 50V, ±15% TC, ±5% Tol	TDK	C1608COG1H102J
11	1	100pF	C13	Multilayer Ceramic Chip Capacitor, 0603 SMD, 50V, 30ppm/°C, ±5% Tol	TDK	C1608COG1H101J
12	11	16-Bit String DAC	U1	TSSOP-16(PW), 4-CH, SPI, Low Glitch, Voltage Output DAC with Internal reference	Texas Instruments	DAC8564IDPW
						DAC8565IDPW
13	1	Difet Operational Amplifier	U2	8-SOP(D) Precision High-Speed, Difet Operational Amplifier	Texas Instruments	OPA627AU

Table 1. Parts List (continued)

Item	Qty.	Value	Designators	Description	Vendor	Vendor Part No.
14	1	5V Reference	U3	15ppm/°C, ±0.2% Tol Output, SOIC-8, Voltage Reference	Texas Instruments	REF02AU
15	1	FET Input Operational Amplifier	U4	8-SOIC(D) High Speed Low Noise Operational Amplifier	Texas Instruments	OPA2132UA
16	2	10 × 2 × 0.1 SMT	J2A J4A	20-Pin Terminal Strip	Samtec	TSM-110-01-S-DV-M
17	1	5 × 2 × 0.1 SMT	J3A	10-Pin Terminal Strip	Samtec	TSM-105-01-T-DV
18	2	10 × 2 × 0.1 SMT	**J2B, J4B**	20-Pin Socket Strip(1)	Samtec	SSW-110-22-S-D-VS-P
19	1	5 × 2 × 0.1 SMT	**J3B**	10-Pin Socket Strip(1)	Samtec	SSW-105-22-F-D-VS-K
20	6	2 × 1 × 0.7874 TH	JMP1–JMP6	2-Pin Terminal Strip	Samtec	TSW-102-07-G-S
21	10	3 × 1 × 0.7874 TH	JMP7–JMP16	3-Pin Terminal Strip	Samtec	TSW-103-07-G-S
22	7	1 × 1 × 0.040D TH	TP1–TP3, **TP5**, **TP6**, TP7,TP8	Testpoint Mini-Loop(1)	Keystone Electronics	5000
23	2	1 × 1 × 0.061D TH	TP4, TP9	Turret Terminal Pin	Mill-Max	2348-2-00-01-00-00-07-0
24	1	N/A	N/A	Printed Wiring Board	Texas Instruments	6496405
25	13	Do Not Populate	**C8, C9, C14, R5, R6, R17–R23, R25**	Do not install these components(1)	TBD	TBD
26	10	0.100 Shorting Blocks	N/A	Shorting Blocks	Samtec	SNT-100-BK-G-H
27	0	N/A	N/A	Schematic Diagram	Texas Instruments	6496406
28	0	N/A	N/A	Printed-Circuit Assembly	Texas Instruments	6496407
29	0	N/A	N/A	Kit Assembly	Texas Instruments	6496408

(1) J2B, J3B and J4B parts are not shown in the schematic diagram. All the JxB designated parts are installed in the bottom side of the PCB opposite the JxA designated counterpart. Example, J2A is installed on the topside while J2B is installed in the bottom side opposite of J2A. **Do NOT install the following: C8 C9 C14 R5 R6 R17 R18 R19 R20 R21 R22 R23 R25.**

3 EVM Operation

This section covers in detail the operation of the EVM to provide guidance to the user in evaluating the onboard DAC and how to interface the EVM to a specific host processor.

See the DAC8564 or the DAC8565 data sheet, (SBAS254) or (SBAS411), respectively, for information about its serial interface and other related topics.

The EVM board is factory tested and configured to operate in the unipolar output mode.

3.1 Factory Default Setting

The EVM board is set to its default configuration from factory as described on the Table 2 to operate in unipolar +2.5-V mode of operation. Figure 17 shows the default jumper configuration for the DAC8564/65EVM.

Table 2. Factory Default Jumper Setting

Reference	Jumper	Function
JMP1	CLOSE	ENABLE pin of the DAC8564/65 is tied to ground. DAC is permanently enabled.
JMP2	CLOSE	LDAC pin of the DAC8564/65 is tied to ground. DAC update is controlled by software.
JMP3	CLOSE	Address, A1, of DAC8564 is grounded (i.e., A1 = 0).
	CLOSE	RSTSEL pin of DAC8565 is grounded. DAC outputs reset to minimum scale.
JMP4	CLOSE	Address A0 of DAC8564 is grounded (i.e., A0 = 0).
	OPEN	RST pin of DAC8565 is pulled up to IOV_{DD}.
JMP5	OPEN	$V_{REF}H$ is not routed to the inverting input of the operational amplifier for voltage offset (or for bipolar mode of operation).
JMP6	OPEN	Output operational amplifier, U2, is configured as voltage follower.
JMP7	1-2	Analog supply AV_{DD} for the DAC8564/65 is +5 VA.

Table 2. Factory Default Jumper Setting (continued)

Reference	Jumper	Function
JMP8	OPEN	Onboard external buffered reference U3 is not selected. Default is the +2.5-V internal reference of the DAC8564/65.
JMP9	1-2	$V_{REF}L$ is connected to analog ground.
JMP10	1-2	Negative supply rail of U2 operational amplifier is supplied with V_{SS}.
JMP11	1-2	DAC output ($V_{OUT}A$) is routed to J4A-2.
JMP12	1-2	DAC output ($V_{OUT}B$) is routed to J4A-4.
JMP13	1-2	DAC output ($V_{OUT}C$) is routed to J4A-6.
JMP14	1-2	DAC output ($V_{OUT}D$) is routed to J4A-8.
JMP15	1-2	DAC output ($V_{OUT}A$) is routed to the non-inverting input of U2 operational amplifier.
JMP16	1-2	U2 output is monitored from J4A-5.
JMP17	1-2	Digital supply IOV_{DD} for the DAC8564/65 is +5 VD.
JMP18	2-3	FSX signal from J2A-7 is used for frame synchronization, $\overline{SYNC}$, signal.
J4A	1-2	DAC output ($V_{OUT}A$) is connected to the non-inverting input of the output operational amplifier, U2.

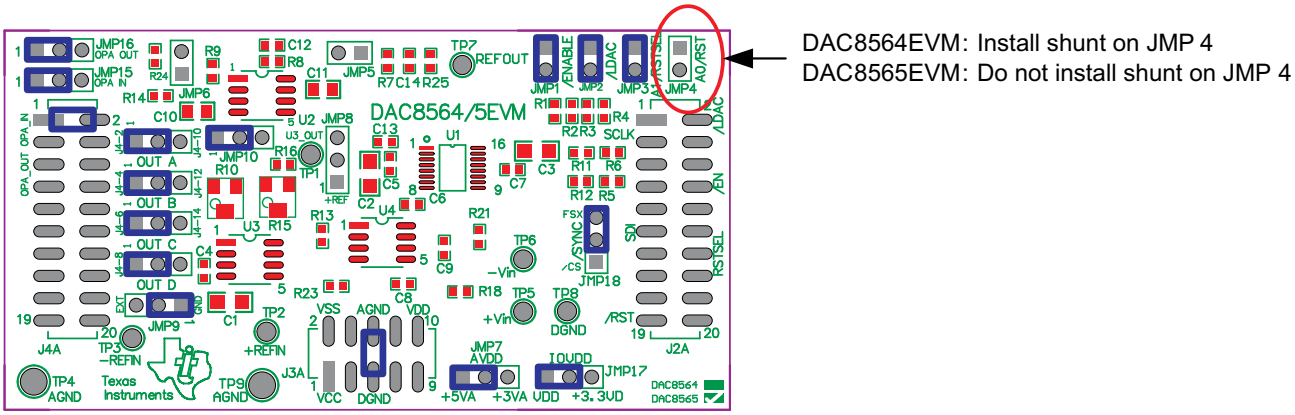


Figure 17. DAC8564/65 EVM Default Jumper Configuration

3.2 Host Processor Interface

The host processor basically drives the DAC, so the DACs proper operation depends on the successful configuration between the host processor and the EVM board. In addition, a properly written code is also required to operate the DAC.

A custom cable can be made specific to the host interface platform. The EVM allows interface to the host processor through J2A header connector for the serial control signals and the serial data input. The output can be monitored through the J4A header connector.

An interface adapter board is also available for specific TI DSP starter kit as well as an MSP430-based microprocessor as mentioned in section 1 of this manual. Using the interface card alleviates the tedious task of building customize cables and allows easy configuration of a simple evaluation system.

The DAC8564/65 interfaces with any host processor capable of handling SPI protocols or the popular TI DSP. For more information regarding the DAC8564 or the DAC8565 data interface, see the data sheet, (SBAS254 or SBAS411), respectively.

3.3 EVM Stacking

The stacking of EVM is possible if there is a need to evaluate two DAC8564/65 devices to yield a total of up to eight (DAC8564/65) channel outputs. A maximum of two EVMs are allowed since the output terminal, J4, dictates the number of DAC channels that can be connected without output bus contention. Table 3 shows how the DAC output channels are mapped into the output terminal, J4, with respect to the jumper position of JMP11, JMP12, JMP13 and JMP14.

Table 3. DAC Output Channel Mapping

Reference	Jumper Position	Function
JMP11	1-2	DAC output (V_{OUT}A) is routed to J4-2.
	2-3	DAC output (V_{OUT}A) is routed to J4-10.
JMP12	1-2	DAC output (V_{OUT}B) is routed to J4-4.
	2-3	DAC output (V_{OUT}B) is routed to J4-12.
JMP13	1-2	DAC output (V_{OUT}C) is routed to J4-6.
	2-3	DAC output (V_{OUT}C) is routed to J4-14.
JMP14	1-2	DAC output (V_{OUT}D) is routed to J4-8.
	2-3	DAC output (V_{OUT}D) is routed to J4-16.

In order to allow exclusive control of each EVM that are stacked together, the DAC8564/65 must have separate $\overline{\text{SYNC}}$ signal. This is accomplished in hardware by routing the $\overline{\text{SYNC}}$ signal of the first EVM through CS (J2A/J2B pin 1) by shorting pins 1-2 of jumper JMP18. The second EVM should use the FSX signal (J2A/J2B pin 7) to drive the $\overline{\text{SYNC}}$ signal by shorting pins 2-3 of the jumper JMP18. The outputs can be mapped as described in Table 3 for each of the EVM stacked.

3.4 The Output Operational Amplifier

The EVM includes an optional signal conditioning circuit for the DAC output through an external operational amplifier, U2. During stacking of EVM, only two DAC output channels can be monitored at any given time for evaluation because of the way the odd numbered pins of J4 header (J4A-1 to J4A-7) are configured. See the schematic included in this manual and Section 3.3.

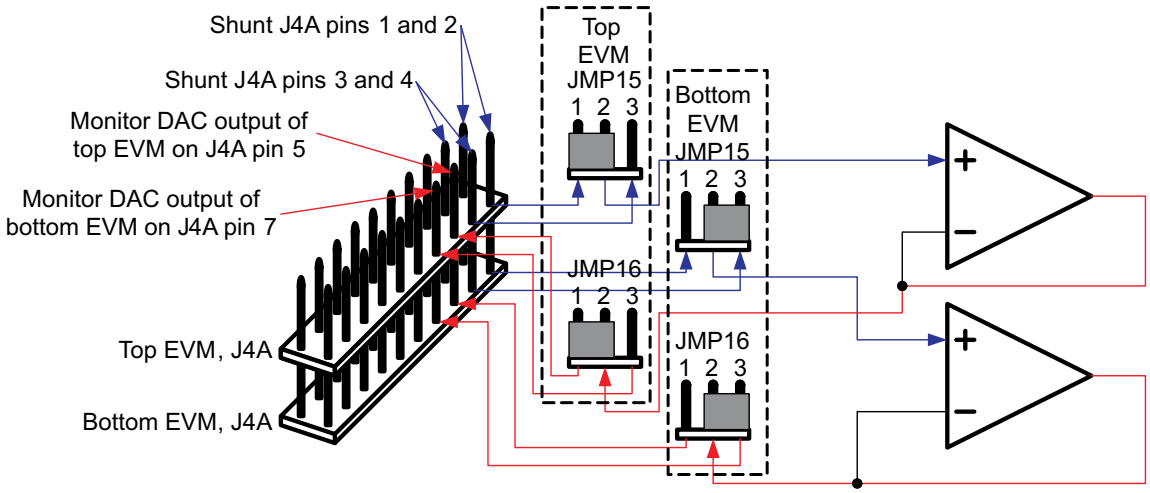


Figure 18. DAC8564/65 EVM Output Operational Amplifier Jumper Configuration for Stacking

The output operational amplifier is set to unity gain configuration by default but can be modified by simple jumper settings. Nevertheless, the raw output of the DAC can be probed through the specified pins of J4 output terminal, which also provides mechanical stability when stacking or plugging into any interface board. In addition, it provides easy access for monitoring up to two (DAC8564/65) DAC channels when stacking two EVMs together (see Section 3.3).

The following sections describe the different configurations of the output amplifier, U2.

3.4.1 Unity Gain Output

The buffered output configuration can be used to prevent loading the DAC8564/65 though it may present some slight distortion because of the feedback resistor and capacitor. The user can tailor the feedback circuit to closely match their desired wave shape by simply desoldering R8 and C12 and replacing it with the desired values. You can also simply get rid of R8 and C12 altogether and just solder a zero ohm resistor in replacement of R8, if desired and leave C12 unpopulated.

Table 4 shows the jumper setting for the unity gain configuration of the DAC external output buffer in unipolar mode.

Table 4. Unity Gain Output Jumper Settings

Reference	Jumper Setting	Function
JMP15	1-2	Connects DAC output (V_{OUT}A) to the non-inverting input of the output operational amplifier, U2.
	2-3	Connects DAC output (V_{OUT}B) to the non-inverting input of the output operational amplifier, U2.
JMP5	OPEN	Disconnect V_{REF}H from the inverting input of the operational amplifier, U2
JMP10	1-2	Connects the negative rail of the operational amplifier, U2, to AGND.
JMP6	OPEN	Disconnect negative input of the operational amplifier from the gain resistor, R9.
JMP16	1-2	Connects the output terminal of the operational amplifier, U2, to J4A-5 for monitoring the voltage output.

3.4.2 Output Gain of Two Operation

The configuration as described on Table 5 yields a gain of two output for a wider mode of voltage output operation.

Table 5. Gain of Two Output Jumper Settings

Reference	Jumper Setting	Function
JMP15	1-2	Connects DAC output (V_{OUT}A) to the non-inverting input of the output operational amplifier, U2.
	2-3	Connects DAC output (V_{OUT}B) to the non-inverting input of the output operational amplifier, U2.
JMP5	OPEN	Disconnect V_{REF}H from the inverting input of the operational amplifier, U2.
JMP10	1-2	Supplies power, V_{SS}, to the negative rail of operational amplifier, U2, for wider range of operation.
JMP6	CLOSE	Connect the negative input of the operational amplifier, U2, to the gain resistor, R9.
JMP16	1-2	Connects the output terminal of the operational amplifier, U2, to J4A-5 for monitoring the voltage output.

3.4.3 Bipolar Output Operation

Using the external V_{REF}H to offset the DAC output and extend the range of operation to achieve a bipolar mode of operation is possible by configuring the output operational amplifier, U2, properly. This configuration is described in Table 6.

Table 6. Bipolar Output Operation Jumper Settings

Reference	Jumper Setting	Function
JMP15	1-2	Connects DAC output (V_{OUT}A) to the non-inverting input of the output operational amplifier, U2.
	2-3	Connects DAC output (V_{OUT}B) to the non-inverting input of the output operational amplifier, U2.
JMP5	CLOSE	Connect V_{REF}H to the inverting input of the operational amplifier, U2.
JMP10	1-2	Supplies power, V_{SS}, to the negative rail of operational amplifier, U2, for wider range of operation.

Table 6. Bipolar Output Operation Jumper Settings (continued)

Reference	Jumper Setting	Function
JMP6	OPEN	Disconnect negative input of the operational amplifier from the gain resistor, R9.
JMP16	1-2	Connects the output terminal of the operational amplifier, U2, to J4A-5 for monitoring the voltage output.

3.4.4 Capacitive Load Drive

Another output configuration option is to drive a wide range of capacitive load requirement. However, all operational amplifiers under certain conditions may become unstable depending on the operational amplifier configuration, gain, and load value. These are just few factors that can affect operational amplifiers stability performance and should be considered when implementing.

In unity gain, the OPA627 operational amplifier, U2, performs well with large capacitive loads. Increasing the gain enhances the amplifier's ability to drive even more capacitance, and by adding a load resistor, even improves the capacitive load drive capability.

Table 7 shows the jumper setting configuration for a capacitive load drive.

Table 7. Capacitive Load Drive Output Jumper Settings

Reference	Jumper Setting	Function
JMP15	1-2	Connects DAC output ($V_{OUT}A$) to the non-inverting input of the output operational amplifier, U2.
	2-3	Connects DAC output ($V_{OUT}B$) to the non-inverting input of the output operational amplifier, U2.
JMP5	OPEN	Connect $V_{REF}H$ to the inverting input of the operational amplifier, U2.
JMP10	1-2	Supplies power, V_{SS}, to the negative rail of operational amplifier, U2, for wider range of operation.
JMP6	CLOSE	Connect the negative input of the operational amplifier, U2, to the gain resistor, R9.
JMP16	1-2	Connects the output terminal of the operational amplifier, U2, to J4A-5 for monitoring the voltage output.

3.5 Jumper Setting

Table 8 shows the function of each specific jumper setting of the EVM.

Table 8. Jumper Setting Function

Reference	Jumper Setting	Function
JMP1		Connects ENABLE to IOVDD and allows the host controller to enable the DUT via J2A-8
		Connects ENABLE to DGND and enables the DUT permanently.
JMP2		Connects LDAC to IOV_{DD} and allows the host controller to update the DAC output using hardware LDAC pin via J2A-2.
		Connects LDAC to DGND and allows the DAC output to be updated by software LDAC.
JMP3		Connects A1 (for DAC8564EVM) to IOV_{DD} and sets the address pin, A1 of the DAC8564EVM to high (A1 = 1). Also allows the host controller to control A1 pin via J2A-14.
		Connects RSTSEL (for DAC8565EVM) to IOV_{DD} and sets the DAC8565 to reset to mid-scale. Also allows the host controller to control the RSTSEL pin of the DUT via J2A-14.
		Connects A1 (for DAC8564EVM) to DGND and sets the address pin, A1 of the DAC8564EVM to low (A1 = 0).
		Connects RSTSEL (for DAC8565EVM) to DGND and sets the DAC8565 to reset to minimum scale.

Table 8. Jumper Setting Function (continued)

Reference	Jumper Setting	Function
JMP4		Connects A0 (for DAC8564EVM) to IOV_{DD} and sets the address pin, A0 of the DAC8564EVM to high (A0 = 1). Also allows the host controller to control A0 pin via J2A-19.
		Connects RST (for DAC8565EVM) to IOV_{DD} and puts the DAC8565 to reset mode. Also allows the host controller to control the RST pin of the DUT via J2A-19.
		Connects A0 (for DAC8564EVM) to DGND and sets the address pin, A0 of the DAC8564EVM to low (A0 = 0).
		Connects RST (for DAC8565EVM) to DGND and puts the DAC8565 to reset mode.
JMP5		Disconnects the inverting input of the output operational amplifier, U2, from the gain resistor, R7 and sets the output of the DAC for unipolar mode of operation.
		Connects the inverting input of the output operational amplifier, U2, to the gain resistor, R7, for bipolar mode of operation.
JMP6		Disconnects the inverting input of the output operational amplifier, U2, from the gain resistor, R9 and configures the operational amplifier for unity gain.
		Connects the inverting input of the output operational amplifier, U2, to the gain resistor, R9, and configures the operational amplifier for 2x gain output.
JMP7		+5-V analog supply is selected for AV_{DD}.
		+3.3-V analog supply is selected for AV_{DD}.
JMP8		This jumper position selects the adjustable +5V reference to route to the $V_{REF}H$ input of the DAC8564/65.
		This is the default jumper position for DAC8564/65 EVM because the +2.5V internal reference is enabled by default.
		This jumper position selects the TP2 input terminal for reference to route to the $V_{REF}H$ input of the DAC8564/65.
JMP9		This jumper position selects the AGND to route to the $V_{REF}L$ input of the DAC8564/65.
		This jumper position selects the TP3 input terminal for reference to route to the $V_{REF}L$ input of the DAC8564/65.
JMP10		Negative supply rail of the output operational amplifier, U2, is powered by V_{SS} for bipolar operation.
		Negative supply rail of the output operational amplifier, U2, is tied to AGND for unipolar operation.
JMP11		Routes V_{OUT} to J4A-2.
		Routes V_{OUT} to J4A-10.
JMP12		Routes V_{OUT} to J4-4.
		Routes V_{OUT} to J4-12.

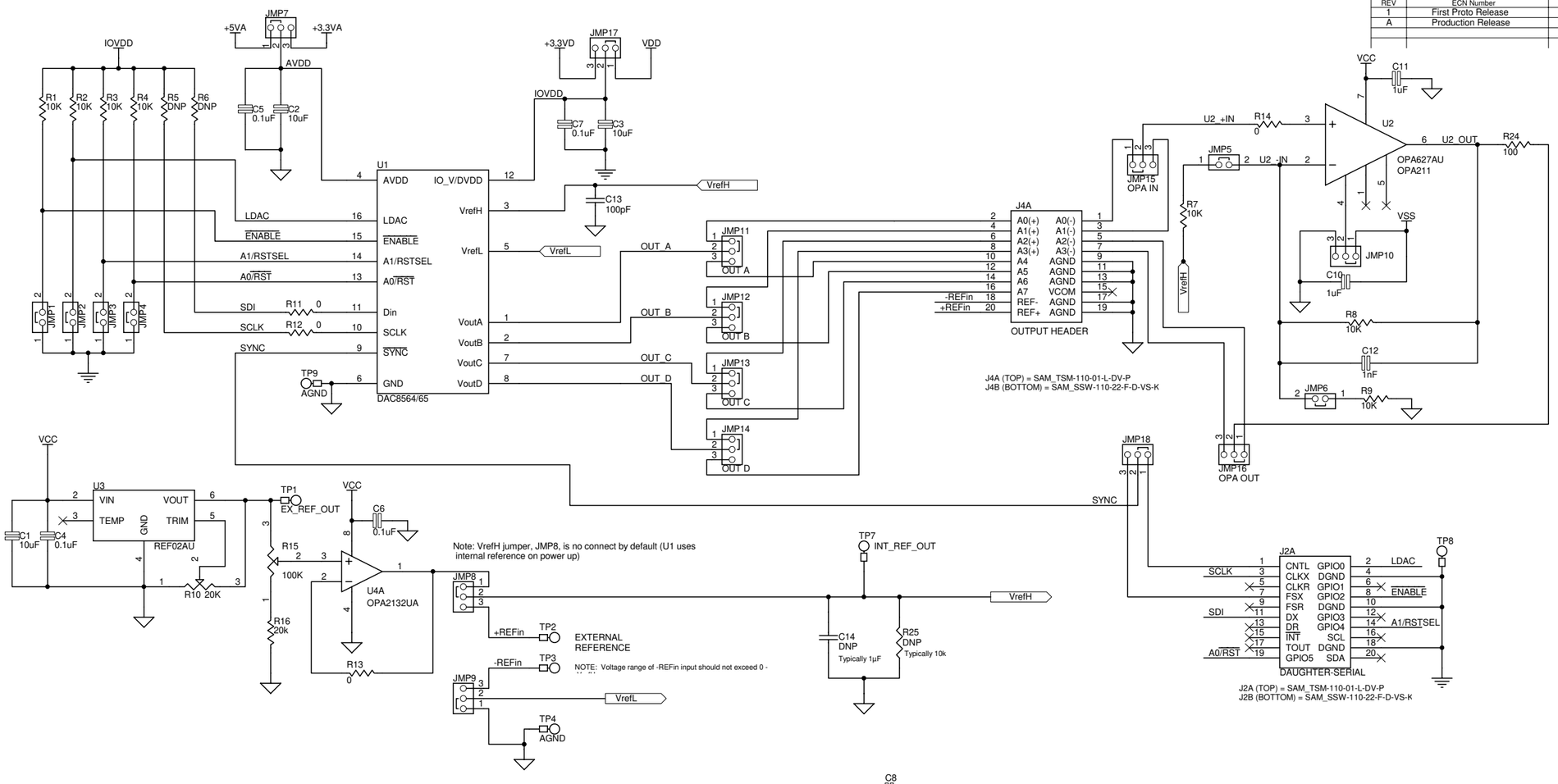
Table 8. Jumper Setting Function (continued)

Reference	Jumper Setting	Function
JMP13		Routes V_{OUT} to J4-6.
		Routes V_{OUT} to J4-14.
JMP14		Routes V_{OUT} to J4-8.
		Routes V_{OUT} to J4-16.
JMP15		This jumper position selects the J4A-1 pin of the output terminal, J4A, to route to the non-inverting input of the operational amplifier, U2.
		Disconnects the non-inverting input of the operational amplifier, U2, from the output terminal, J4A.
		This jumper position selects the J4A-3 pin of the output terminal, J4A, to route to the non-inverting input of the operational amplifier, U2.
JMP16		This jumper position selects the operational amplifier, U2, output pin to route to the J4A-5 output terminal.
		Disconnects the operational amplifier's, U2, output pin from the output terminal of J4A.
		This jumper position selects the operational amplifier, U2, output pin to route to the J4A-7 output terminal.
JMP17		+5-VD (VDD) digital supply is selected for IOVDD.
		+3.3-VD digital supply is selected for IOVDD.
JMP18		CS signal from J2A-1 is routed to drive the SYNC signal of the DAC8564/65.
		FSX signal from J2A-7 is routed to drive the SYNC signal of the DAC8564/65.
Legend:  indicates the corresponding pins that are shorted or closed		

3.6 Schematic

The DAC8564/65 evaluation module schematic appears on the following page.

Revision History		
REV	ECN Number	Approved
1	First Proto Release	JLP
A	Production Release	JLP



EDGE Numbers:

DAC8564EVM BOM = 6496403
DAC8565EVM BOM = 6496404
DAC8564/65EVM PWB = 6496405
DAC8564/65EVM DDB (BLOCK) = 6496406
DAC8564/65EVM PCA = 6496407
DAC8564EVM KIT (BLOCK) = 6496408
DAC8565EVM KIT (BLOCK) = 6496409
DAC8564EVM SFT = 6496410
DAC8565EVM SFT = 6496411

VCC = +15V Analog
VSS = 0V to -15V Analog
AVDD = +2.7V to +5.5V Analog
VDD = +2.7V to +5.5V Digital

TEXAS INSTRUMENTS
12500 TI Boulevard. Dallas, Texas 75243

Title:	DAC8564/65 EVM
Engineer: J. PARGUIAN	
Drawn By: J. PARGUIAN	
FILE: DAC8564 Rev A.Sch	
DOCUMENTCONTROL # 6496406	REV: A
DATE: 10-Feb-2008	SIZE: SHEET: 1 OF: 1

4 Information

4.1 Related Documentation from Texas Instruments

To obtain a copy of any of the following TI documents, call the Texas Instruments Literature Response Center at (800) 477–8924 or the Product Information Center (PIC) at (972) 644–5580. When ordering, identify this manual by its title and literature number. Updated documents also can be obtained through the TI Web site at www.ti.com.

Data Sheets	Literature Number:
DAC8564	SBAS254
DAC8565	SBAS411
REF02	SBVS003
OPA211	SB0S377
OPA627	SBOS165
OPA2132	SBOS054

4.2 Questions About This or Other Data Converter EVMs?

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