ISL59450

Multiformat Video Crosspoint with Integrated Sync Separator

FN7510
Rev 0.00
Feb 14, 2008

The ISL59450 is a video crosspoint switch supporting multiple video input formats (CVBS, S-Video, YPbPr, and RGB signals). Embedded anti-aliasing filters with programmable corner frequencies eliminate glitch noise from video DACs. The large number of inputs, wide range of The ISL59450 is a video crosspoint switch supporting multiple video input formats (CVBS, S-Video, YPbPr, and RGB signals). Embedded anti-aliasing filters with programmable corner frequencies eliminate glitch noise from video DACs. The large number of inputs, wide range of formats, integrated anti-aliasing filters, and dual sync-separators make the ISL59450 an ideal choice for video switching in nearly all display systems.

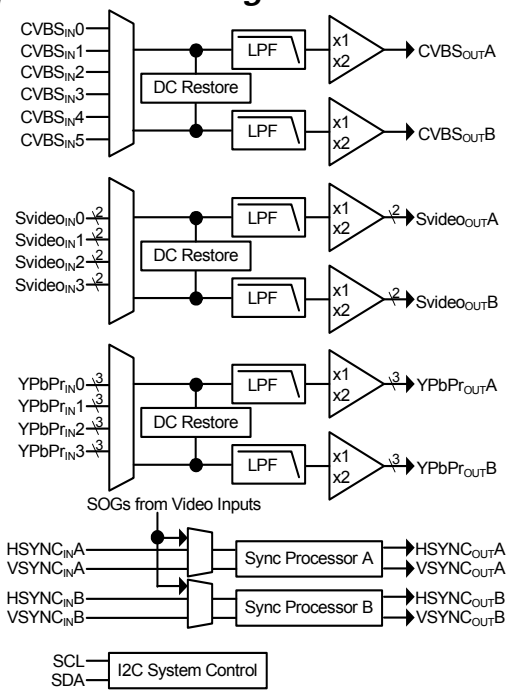
The ISL59450 is available in a 128 Ld MQFP package and is specified for operation over the full -40°C to +85°C temperature range.

Ordering Information

PART NUMBER (Note)	PART MARKING	PACKAGE (Pb-free)	PKG. DWG. #
ISL59450IQZ	ISL59450IQZ	128 Ld MQFP	MDP0055

NOTE: These Intersil Pb-free plastic packaged products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate PLUS ANNEAL - e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Simplified Block Diagram



Features

- 6 Composite, 4 S-Video and 4 Component Video Sources
- 2 Component Inputs can be Configured for VGA with Separate H and V Sync Inputs
- Multi-format Video Filtering
- Compatible with Macrovision® Encoded Signals
- Programmable Gain of x1 or x2
- Outputs have High Impedance Disable Mode
- Two Universal Sync Separators support SD, HD, and Computer Signals
- Pb-free (RoHS compliant)

Applications

- AV Receivers
- LCD-TVs
- AV Switch Boxes
- Projectors
- HDTV Systems
- Multiple Video Input Systems

Absolute Maximum Ratings

Voltage on V_A
(referenced to GND = GND_A = GND_D) 6.0V
Voltage on V_D
(referenced to GND = GND_A = GND_D) 4.0V
Voltage on any Analog Input Pin . . . . . -0.3V to V_A + 0.3V
Voltage on any Digital Input Pin . . . . . -0.3V to V_D + 0.3V
Current into any Output Pin . . . . . ±20mA
ESD Classification
Human Body Model 3000V
Machine Model 125V

Thermal Information

Thermal Resistance	θ_{JA} (°C/W)
MQFP Package	27.84

Maximum Biased Junction Temperature . . . . . +150°C
Storage Temperature . . . . . -65°C to +150°C
Pb-free Reflow Profile . . . . . see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

Recommended Operating Conditions

Temperature (Commercial) . . . . . -40°C to +85°C
Supply Voltage . . . . . V_A = 5.0V, V_D = 3.3V

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

IMPORTANT NOTE: All parameters having Min/Max specifications are guaranteed. Typical values are for information purposes only. Unless otherwise noted, all tests are at the specified temperature and are pulsed tests, therefore: $T_J = T_C = T_A$

AC Electrical Specifications

V_A = 5.0V, V_D = 3.3V, V_{IN} = 0.7V_{P-P}, T_A = +25°C, R_L = 150Ω, $V_{TIP}INx$ = 0.5V, $VSLICE_{INx}$ = 0.6V, $V_{LUMA}x1_{INx}$ = $V_{LUMA}x2_{INx}$ = 0.8; $V_{CHROMA}x1_{INx}$ = $V_{CHROMA}x2_{INx}$ = 1.15V, all frequency response measurements relative to f = 100kHz, unless otherwise specified.

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
YPbPr/RGB (Component) Video Inputs						
YPbPr-10MHz	Passband Flatness, 10MHz Filter	f = 6MHz, GAIN 1	-1.6	-1.1	-0.4	dB
		f = 6MHz, GAIN 2	-1.6	-1.1	-0.4	dB
	Cutoff Flatness, 10MHz Filter	f = 10MHz, GAIN 1	-4.2	-2.7	-1.5	dB
		f = 10MHz, GAIN 2	-4.2	-2.7	-1.5	dB
	Stopband Rejection, 10MHz Filter	f = 27MHz, GAIN 1	-30	-19	-11	dB
		f = 27MHz, GAIN 2	-30	-19	-11	dB
		f = 54MHz, GAIN 1		-51		dB
		f = 54MHZ, GAIN 2		-51		dB
YPbPr-20MHz	Passband Flatness, 20MHz Filter	f =12MHz, GAIN 1	-1.5	-0.9	-0.4	dB
		f =12MHz, GAIN 2	-1.5	-0.9	-0.4	dB
	Cutoff Bandwidth, 20MHz Filter	f = 20MHz, GAIN 1	-3.6	-2.3	-1.3	dB
		f = 20MHz, GAIN 2	-3.6	-2.3	-1.3	dB
	Stopband Rejection, 20MHz Filter	f = 54MHz, GAIN 1	-30	-15	-9	dB
		f = 54MHz, GAIN 2	-30	-15	-9	dB
YPbPr-36MHz	Passband Flatness, 36MHz Filter	f = 20MHz, GAIN 1	-1.6	-1	-0.4	dB
		f = 20MHz, GAIN 2	-1.6	-1	-0.4	dB
	Cutoff Bandwidth, 36MHz Filter	f = 36MHz, GAIN 1	-4.7	-2.7	-1.5	dB
		f = 36MHz, GAIN 2	-4.7	-2.7	-1.5	dB
	Stopband Rejection, 36MHz Filter	f = 108MHz, GAIN 1		-22		dB
		f = 108MHz, GAIN 2		-22		dB

AC Electrical Specifications V_A = 5.0V, V_D = 3.3V, V_{IN} = 0.7V_{P-P}, T_A = +25°C, R_L = 150Ω, $V_{TIP}INx$ = 0.5V, $VSLICE_{INx}$ = 0.6V, $V_{LUMA}x1_{INx}$ = $V_{LUMA}x2_{INx}$ = 0.8; $V_{CHROMA}x1_{INx}$ = $V_{CHROMA}x2_{INx}$ = 1.15V, all frequency response measurements relative to f = 100kHz, unless otherwise specified. **(Continued)**

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
YPbPr-Bypass	Passband Flatness, Filter Bypassed	f = 220MHz, GAIN 1		±1		dB
		f = 220MHz, GAIN 2		±1		dB
	Cutoff Bandwidth, Filter Bypassed	GAIN 1		275		MHz
		GAIN 2		275		MHz
	Positive Slew Rate, Filter Bypassed	V_{OUT} = 2V_{P-P}, GAIN 1	350	450		V/µs
		V_{OUT} = 2V_{P-P}, GAIN 2	450	590		V/µs
	Negative Slew Rate, Filter Bypassed	V_{OUT} = 2V_{P-P}, GAIN 1	350	440		V/µs
		V_{OUT} = 2V_{P-P}, GAIN 2	720	950		V/µs
S-Video VIDEO INPUTS						
SV-10MHz	Passband Flatness, 10MHz Filter	f =7MHz, GAIN 1	-2.3	-1.5	-0.8	dB
		f =7MHz, GAIN 2	-2.3	-1.5	-0.8	dB
	Cutoff Rejection, 10MHz Filter	f = 11MHz, GAIN 1	-5.5	-3.4	-2	dB
		f = 11MHz, GAIN 2	-5.5	-3.4	-2	dB
	Stopband Rejection, 10MHz	f = 27MHz, GAIN 1	-32	-21	-11	dB
		f = 27MHz, GAIN 2	-32	-21	-11	dB
SV-Bypass	Passband Flatness, Filter Bypassed	f = 27MHz, GAIN 2	-2.3	-1	-0.8	dB
	Cutoff Rejection, Filter Bypassed	f = 54MHz, GAIN 2	-12	-3.6	-2.5	dB
CVBS (Composite) VIDEO INPUTS						
CVBS-7MHz	Passband Flatness, 7MHz Filter	f = 5MHz, GAIN 1	-2.7	-1.7	-1	dB
		f = 5MHz, GAIN 2	-2.7	-1.7	-1	dB
	Cutoff Rejection, 7MHz Filter	f = 7MHz, GAIN 1	-5	-3.2	-1.8	dB
		f = 7MHz, GAIN 2	-5	-3.2	-1.8	dB
	Stopband Rejection, 7MHz Filter	f = 27MHz, GAIN 1	-50	-39	-26	dB
		f = 27MHz, GAIN 2	-50	-39	-26	dB
CVBS-Bypass	Passband Flatness, Filter Bypassed	f = 27MHz, GAIN 2	-1.9	-1.1	-0.7	dB
	Cutoff Rejection, Filter Bypassed	f = 54MHz, GAIN 2	-7.2	-3.8	-2.7	dB
dG	Differential Gain	f = 3.58MHz, GAIN 1		0.5		%
		f = 3.58MHz, GAIN 2		0.3		%
dP	Differential Phase	f = 3.58MHz, GAIN 1		0.45		°
		f = 3.58MHz, GAIN 2		0.65		°
ALL VIDEO INPUTS						
$INTER\text{-}X_{TALK}$	Inter-Channel Crosstalk	Any input of Channel A to any output Channel B and vice-versa, GAIN 1 and 2, f = 10MHz		85		dB

DC Electrical Specifications

V_A = 5.0V, V_D = 3.3V, T_A = +25°C, R_L = 150Ω, $V_{TIP}INx$ = 0.5V, $VSLICE_{INx}$ = 0.6V, $V_{LUMA}x1_{INx}$ = $V_{LUMA}x2_{INx}$ = 0.8; $V_{CHROMA}x1_{INx}$ = $V_{CHROMA}x2_{INx}$ = 1.15V, unless otherwise specified.

PARAMETER	DESCRIPTION	CONDITIONS	MIN	TYP	MAX	UNIT
V_A	Analog Supply Range		4.5		5.5	V
V_D	Digital Supply Range		2.7		3.6	V
I_A	Analog Supply Current	All output groups enabled		290	350	mA
		1 Composite output enabled		25		mA
		1 S-video output group enabled		48		mA
		1 Component output group enabled		75		mA
I_D	Digital Supply Current	Both sync separators enabled		3.5	6	mA
$I_{DISABLED}$	Standby Supply Current	Disabled Analog Current, I_A		0.7	3	mA
		Disabled Digital Current, I_D		0.7	2.5	mA
PSRR	Power Supply Rejection	GAIN 1 or 2, any output		50		dB
$PSRR_{CLAMP\_ON}$	Rejection with Clamp Enabled	GAIN 1 or 2		45		dB
Gain	Low Frequency Gain	GAIN 1	0.95	1	1.05	V/V
		GAIN 2	1.9	2.0	2.1	V/V
$V_{OS-CLAMP}$	Clamp Offset (Delta between external reference voltage and output during clamp)	V_{REF} = any reference input, GAIN 1	V_{REF} - 30mV		V_{REF} + 30mV	mV
		V_{REF} = any reference input, GAIN 2	V_{REF} - 30mV		V_{REF} + 30mV	mV
V_{OS}	V_{IN} - V_{OUT} (Useful if DC-Coupling)	Clamp disabled, A_V = 1		0.45		V
$I_{PULLDOWN}$	Input Pulldown Current	V_{IN} = 2V, clamp enabled (sinking)		1		µA
I_{CLAMP}	Clamp Pullup Current	CV and S-Video, normal offset mode, clamp enabled (sourcing)	100	130	170	µA
		Component/RGB, normal offset mode, clamp enabled (sourcing)	220	270	320	µA
		CV and S-Video, low offset mode, clamp enabled (sourcing)	220	270	320	µA
		Component/RGB, low offset mode, clamp enabled (sourcing)	400	500	650	µA
I_{SC}	Short Circuit Current	VIN = 3V, AV2 = 2.0V, Sourcing, R_L = 10Ω to GND	60	102	140	mA
		VIN = 0V, Sinking, R_L = 10Ω to +3V	20	30	40	mA
$V_{OUT-LIN}$	Output Linear Voltage Range		0.5		2.5	V
LOGIC INPUTS (SDA, SCL, Address, Reset, PowerDown, $HSYNC_{INx}$, $VSYNC_{INx}$, SDETx)						
V_{IH}	Input High Voltage (HIGH)	All logic pins, except $\overline{Reset}$	2			V
		$\overline{Reset}$ (Pin must be >3.5V to ensure part is not resetting)	3.5			V
V_{IL}	Input Low Voltage (LOW)				0.8	V
I_{IH}	Input High Current (V_{IN} = 5V, Logic Inputs, Sinking)	No pull-up or pull-down	-1	0	1	µA
		Pins with 300kΩ internal pull-downs: Address, $\overline{Reset}$, Power-down	8	17	34	µA
I_{IL}	Input Low Current (V_{IN} = 0V, Logic Inputs, Sourcing)	No pull-up or pull-down	-1	0	1	µA
		Pins with 300kΩ internal pull-up: SDETx	10	15	25	µA

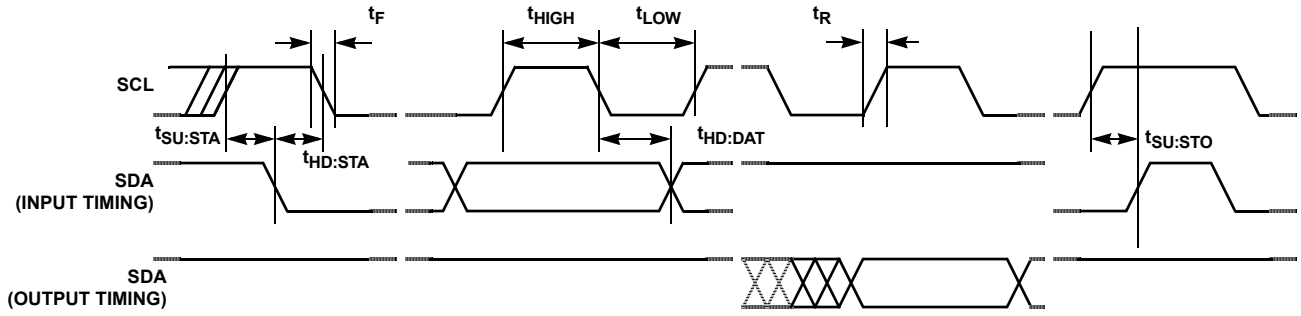
Serial Interface (I^2C) Specifications

SYMBOL	PARAMETER	CONDITIONS	MIN (Note 1)	TYP	MAX (Note 1)	UNIT
V_{OL}	SDA Output Buffer LOW Voltage	I_{OL} = 4mA	0		0.4	V
I_{LI}	Input Leakage Current on SCL	V_{IN} = 5.5V		0.1	1	µA
I_{LO}	I/O Leakage Current on SDA	V_{IN} = 5.5V		0.1	1	µA
TIMING CHARACTERISTICS						
f_{SCL}	SCL Frequency				400	kHz
t_{LOW}	Clock LOW Time	Measured at the 30% of V_D crossing.	1.3			µs
t_{HIGH}	Clock HIGH Time	Measured at the 70% of V_D crossing.	0		0.9	µs
$t_{SU:STA}$	START Condition Set-up Time	SCL rising edge to SDA falling edge. Both crossing 70% of V_D.	0.6			µs
$t_{HD:STA}$	START Condition Hold Time	From SDA falling edge crossing 30% of V_D to SCL falling edge crossing 70% of V_D.	0.6			µs
$t_{HD:DAT}$	Input Data Hold Time	From SCL falling edge crossing 70% of V_D to SDA entering the 30% to 70% of V_D window.	0		0.9	µs
$t_{SU:STO}$	STOP Condition Set-up Time	From SCL rising edge crossing 70% of V_D, to SDA rising edge crossing 30% of V_D	0.6			µs
t_R	SDA and SCL Rise Time	From 30% to 70% of V_D	20 + 0.1 x Cb			ns
t_F	SDA and SCL Fall Time	From 70% to 30% of V_D	20 + 0.1 x Cb			ns
Cb	Capacitive Loading of SDA or SCL	Total on-chip and off-chip			400	pF
Cpin	SDA and SCL Pin Capacitance				10	pF

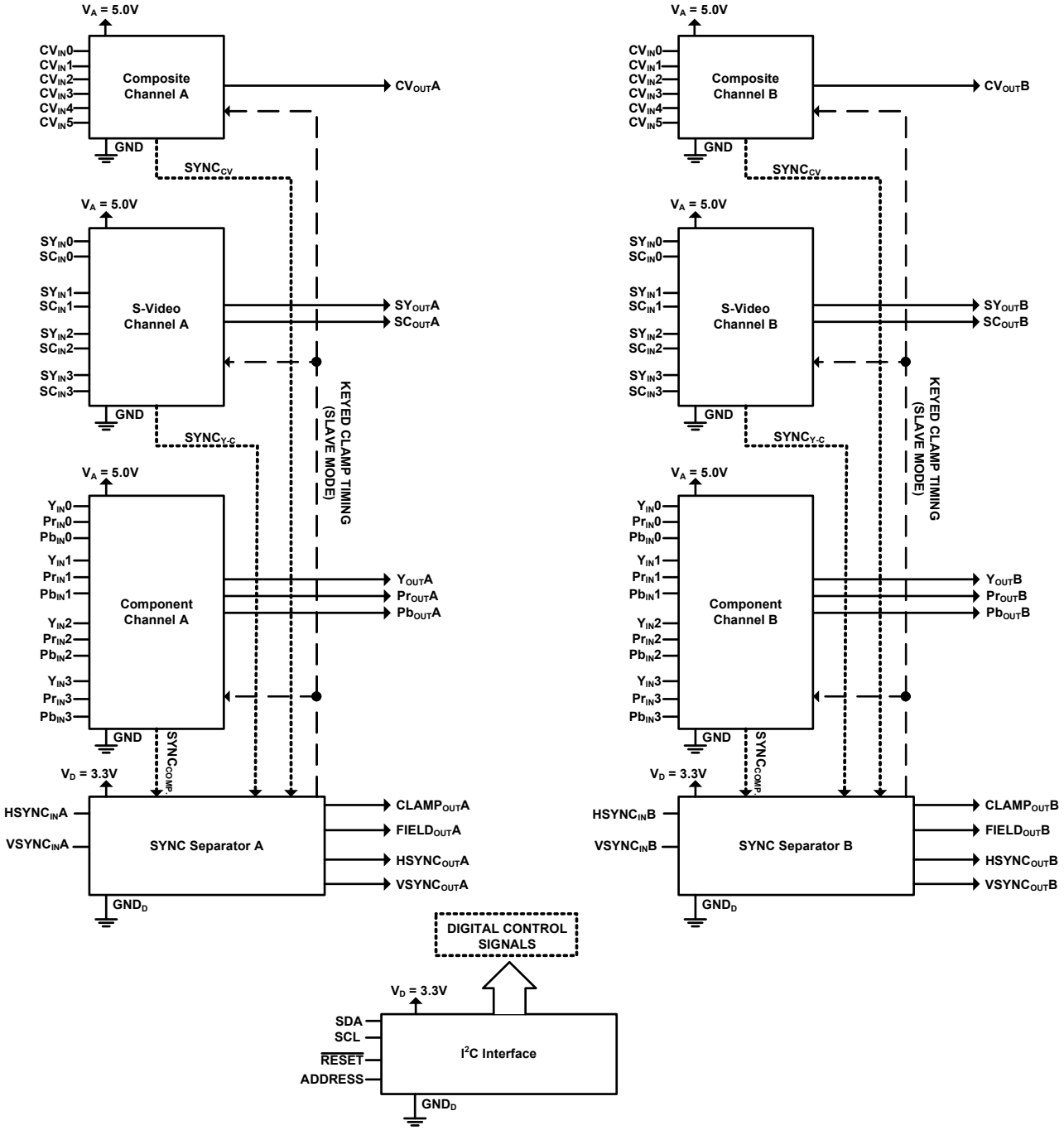
NOTE:

1. Parts are 100% tested at +25°C. Temperature limits established by characterization and are not production tested.

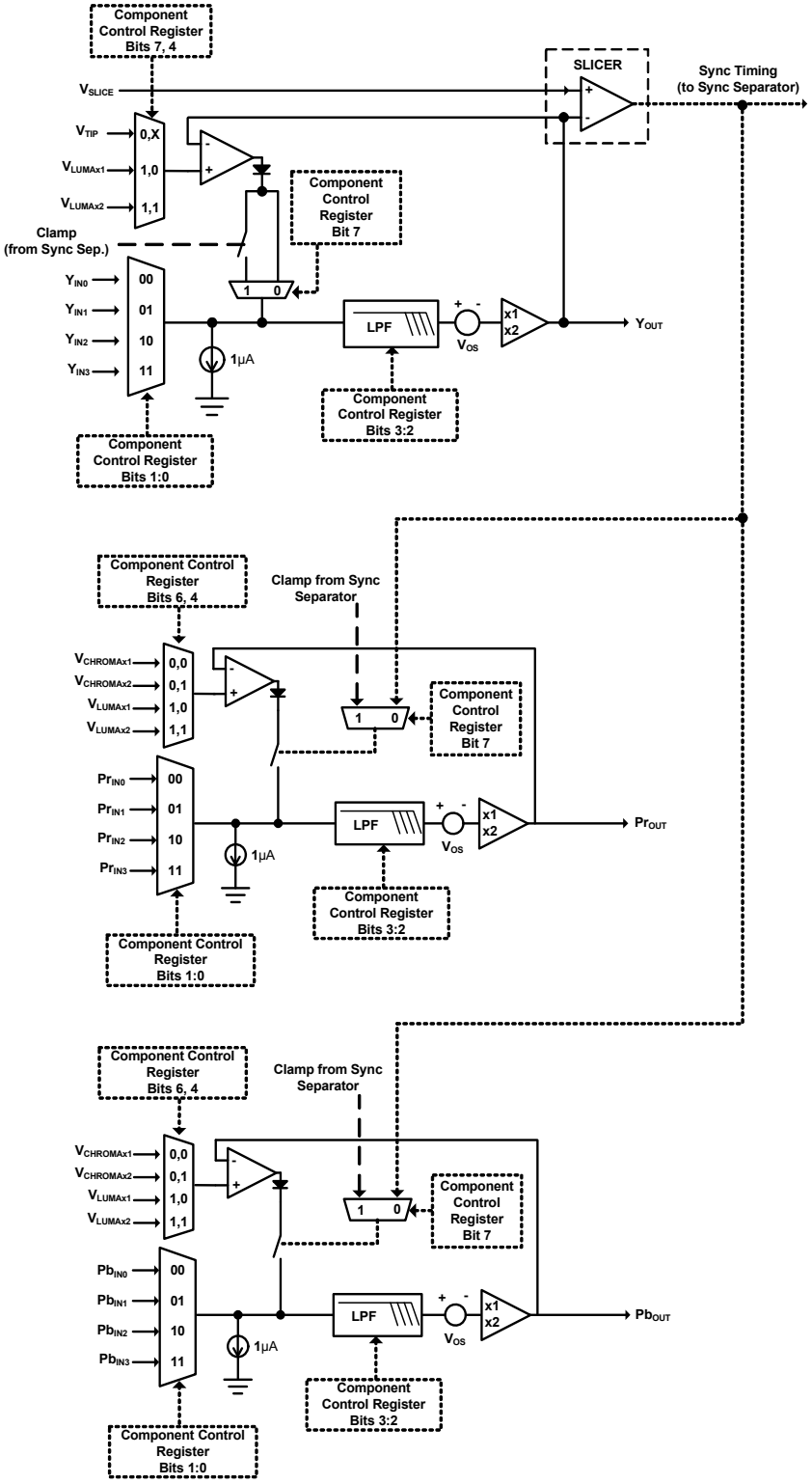
I^2C *Timing Diagram*



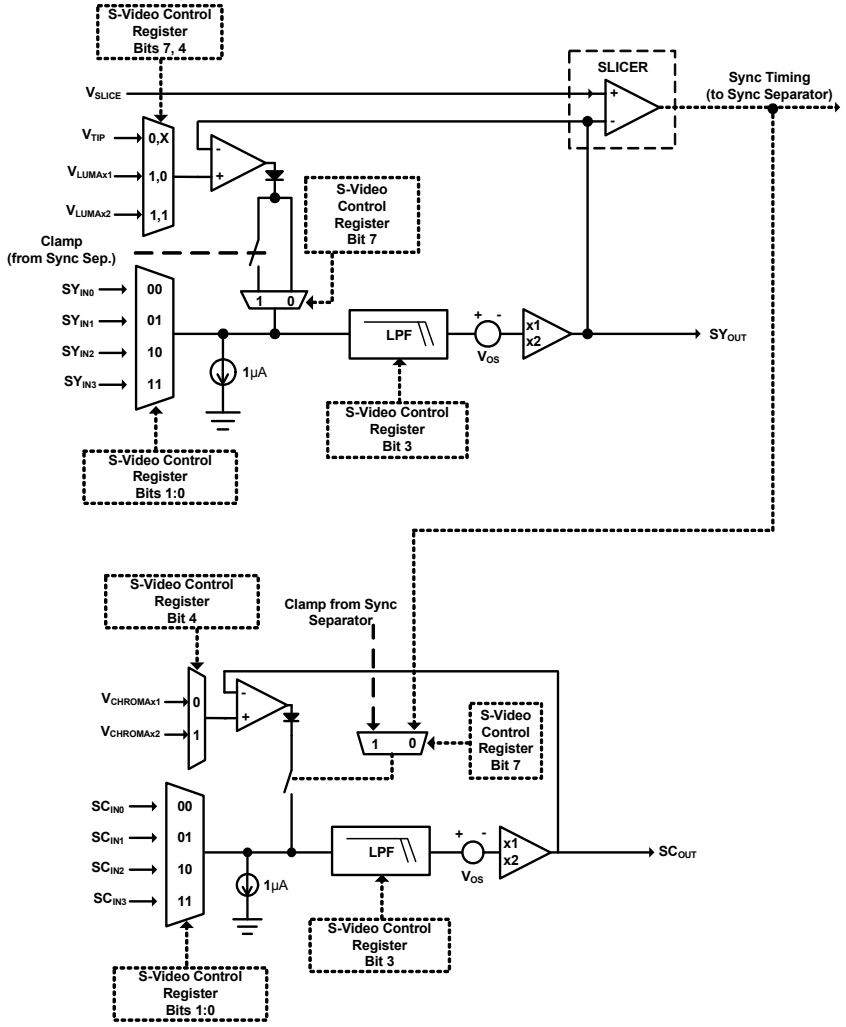
Functional Diagram



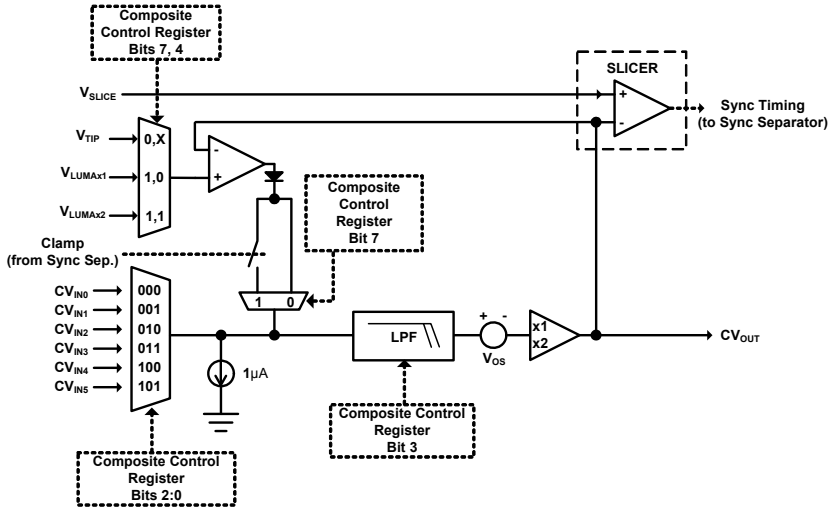
Component Block Diagram



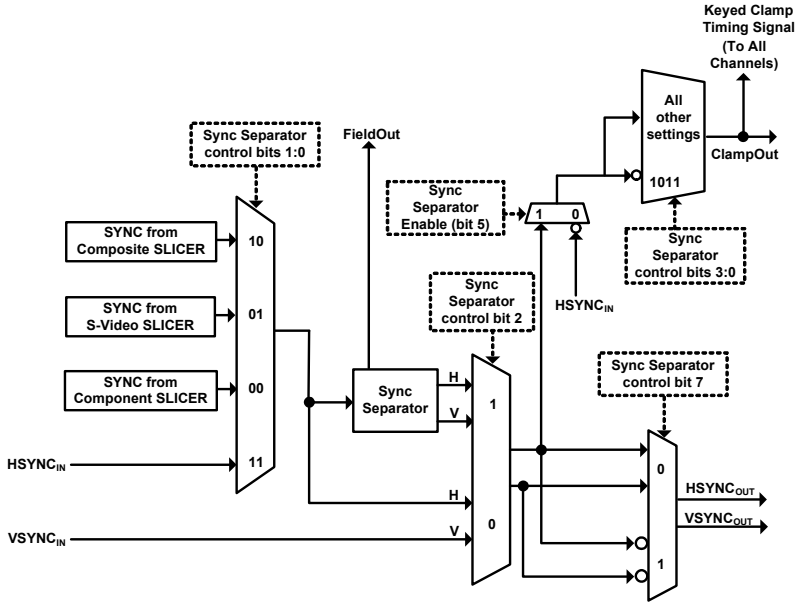
S-Video Block Diagram



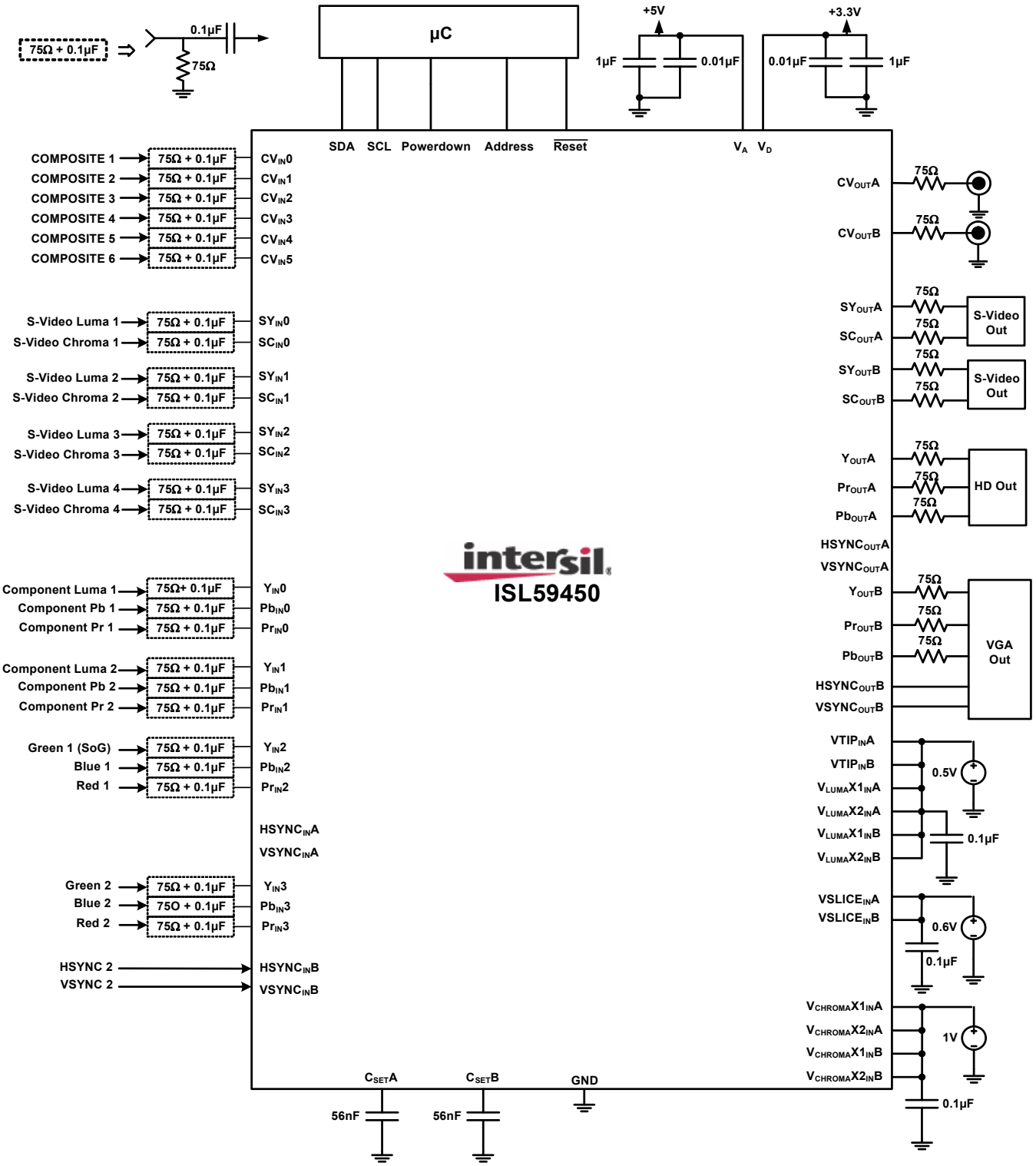
Composite Block Diagram



Sync Separator Block Diagram

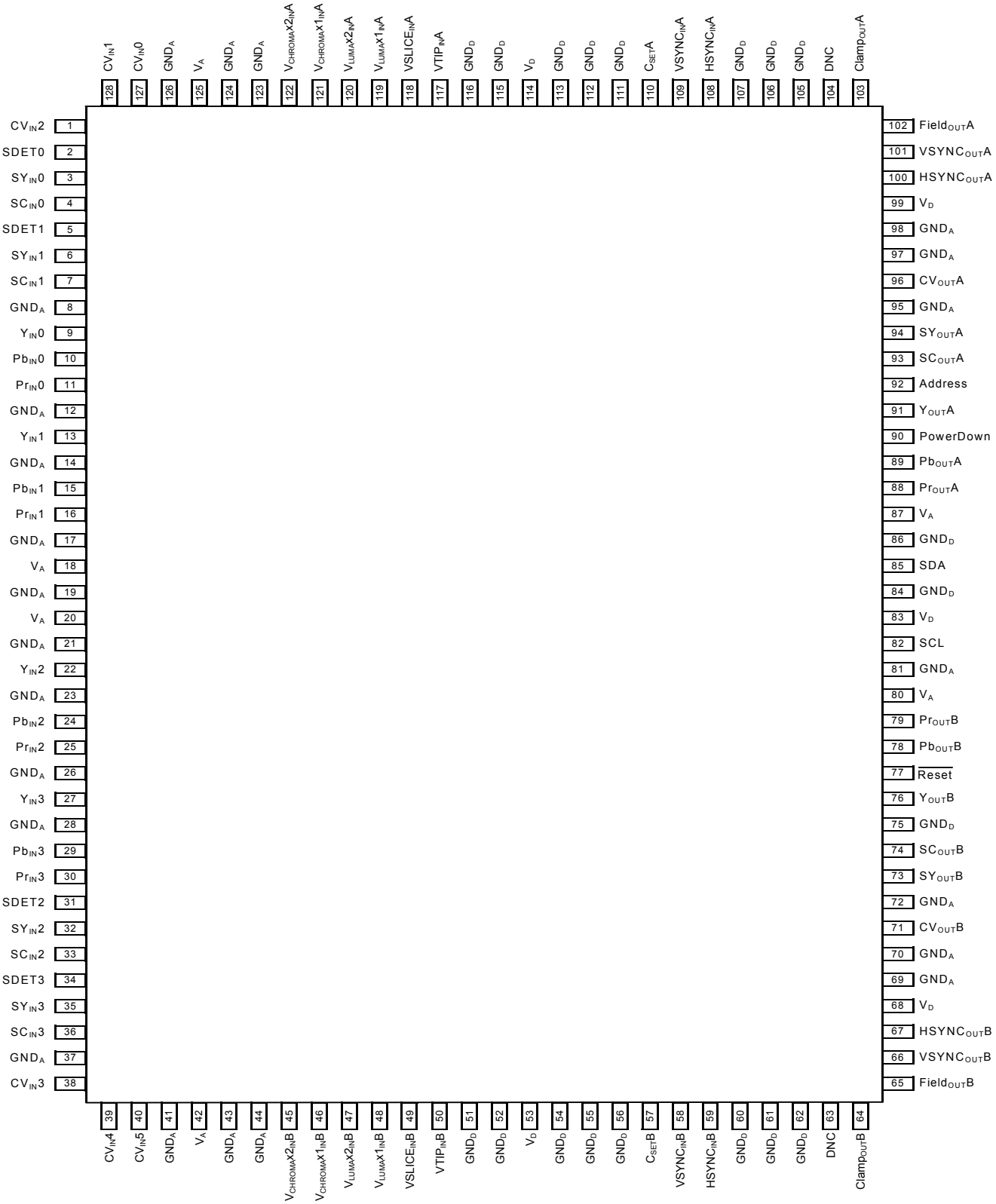


Typical Application Circuit



Pinout

ISL59450
(128 LD MQFP)
TOP VIEW



Pin Descriptions

PIN NUMBER	PIN NAME	DESCRIPTION
COMPOSITE (CV) VIDEO INPUTS (6x1)		
127	$CV_{IN}0$	Composite Video Input 0
128	$CV_{IN}1$	Composite Video Input 1
1	$CV_{IN}2$	Composite Video Input 2
38	$CV_{IN}3$	Composite Video Input 3
39	$CV_{IN}4$	Composite Video Input 4
40	$CV_{IN}5$	Composite Video Input 5
COMPOSITE (CV) VIDEO OUTPUTS		
96	$CV_{OUT}A$	Composite Video Output A with High-Z disable mode
71	$CV_{OUT}B$	Composite Video Output B with High-Z disable mode
S-VIDEO (SV) INPUTS (4x2)		
3	$SY_{IN}0$	S-Video Luma Input 0
4	$SC_{IN}0$	S-Video Chroma Input 0
6	$SY_{IN}1$	S-Video Luma Input 1
7	$SC_{IN}1$	S-Video Chroma Input 1
32	$SY_{IN}2$	S-Video Luma Input 2
33	$SC_{IN}2$	S-Video Chroma Input 2
35	$SY_{IN}3$	S-Video Luma Input 3
36	$SC_{IN}3$	S-Video Chroma Input 3
S-VIDEO (SV) OUTPUTS		
94	$SY_{OUT}A$	S-Video Luma Output A with High-Z disable mode
93	$SC_{OUT}A$	S-Video Chroma Output A with High-Z disable mode
73	$SY_{OUT}B$	S-Video Luma Output B with High-Z disable mode
74	$SC_{OUT}B$	S-Video Chroma Output B with High-Z disable mode
S-VIDEO CONNECTION DETECTION PINS		
2	SDET0	Digital Input with internal pull-up to V_A. Detects S-Video connector 0. Tie to NC switch on S-Video connector, with other end of switch tied to ground. 0V = no cable attached, V_A = S-Video cable attached. 300k pull-up to analog supply.
5	SDET1	Digital Input with internal pull-up to V_A. Detects S-Video connector 1. Tie to NC switch on S-Video connector, with other end of switch tied to ground. 0V = no cable attached, V_A = S-Video cable attached. 300k pull-up to analog supply.
31	SDET2	Digital Input with internal pull-up to V_A. Detects S-Video connector 2. Tie to NC switch on S-Video connector, with other end of switch tied to ground. 0V = no cable attached, V_A = S-Video cable attached. 300k pull-up to analog supply.
34	SDET3	Digital Input with internal pull-up to V_A. Detects S-Video connector 3. Tie to NC switch on S-Video connector, with other end of switch tied to ground. 0V = no cable attached, V_A = S-Video cable attached. 300k pull-up to analog supply.
COMPONENT (YPbPr) VIDEO INPUTS (4x3)		
9	$Y_{IN}0$	Luma component (or Green RGB) video input 0
10	$Pb_{IN}0$	Chroma Pb component (or Blue RGB) video input 0
11	$Pr_{IN}0$	Chroma Pr component (or Red RGB) video input 0
13	$Y_{IN}1$	Luma component (or Green RGB) video input 1
15	$Pb_{IN}1$	Chroma Pb component (or Blue RGB) video input 1

Pin Descriptions (Continued)

PIN NUMBER	PIN NAME	DESCRIPTION
16	$Pr_{IN}1$	Chroma Pr component (or Red RGB) video input 1
22	$Y_{IN}2$	Luma component (or Green RGB) video input 2
24	$Pb_{IN}2$	Chroma Pb component (or Blue RGB) video input 2
25	$Pr_{IN}2$	Chroma Pr component (or Red RGB) video input 2
27	$Y_{IN}3$	Luma component (or Green RGB) video input 3
29	$Pb_{IN}3$	Chroma Pb component (or Blue RGB) video input 3
30	$Pr_{IN}3$	Chroma Pr component (or Red RGB) video input 3
COMPONENT VIDEO OUTPUTS		
91	$Y_{OUT}A$	Component Video Luma Output A with High-Z disable mode
89	$Pb_{OUT}A$	Chroma Pb component (or Blue Component) Video Output A with High-Z disable
88	$Pr_{OUT}A$	Chroma Pr component (or Red Component) Video Output A with High-Z disable
76	$Y_{OUT}B$	Component Video Luma Output B with High-Z disable mode
78	$Pb_{OUT}B$	Chroma Pb component (or Blue Component) Video Output B with High-Z disable
79	$Pr_{OUT}B$	Chroma Pr component (or Red Component) Video Output B with High-Z disable
A SYNC SEPARATOR INPUTS AND OUTPUTS		
108	$HSYNC_{IN}A$	Horizontal External Sync Source for Sync Separator A. This signal may be pure HSYNC or CSYNC.
109	$VSYNC_{IN}A$	Vertical External Sync Source for Sync Separator A
110	$C_{SET}A$	Sync Separator filter capacitor. Connect a 0.056µF capacitor between this pin and analog ground.
100	$HSYNC_{OUT}A$	Horizontal Sync Output for Sync Separator A
101	$VSYNC_{OUT}A$	Vertical Sync Output for Sync Separator A
102	$Field_{OUT}A$	Field Flag for Sync Separator A. Low = odd field, high = even field.
103	$Clamp_{OUT}A$	External Clamp Timing Pulse for Sync Separator A (for timed back porch clamping)
B SYNC SEPARATOR INPUTS AND OUTPUTS		
59	$HSYNC_{IN}B$	Horizontal External Sync Source for Sync Separator B. This signal may be pure HSYNC or CSYNC.
58	$VSYNC_{IN}B$	Vertical External Sync Source for Sync Separator B
57	$C_{SET}B$	Sync Separator filter capacitor. Connect a 0.056µF capacitor between this pin and analog ground.
67	$HSYNC_{OUT}B$	Horizontal Sync Output from Sync Separator B
66	$VSYNC_{OUT}B$	Vertical Sync Output from Sync Separator B
65	$Field_{OUT}B$	Field Flag for Sync Separator B. Low = odd field, high = even field.
64	$Clamp_{OUT}B$	External Clamp Timing Pulse for Sync Separator B (for timed back porch clamping)
EXTERNAL DC REFERENCE LEVELS		
122	$V_{CHROMA}x2_{IN}A$	Analog Input. Chroma Reference Level for DC-Restore when A_V = 2, for Channel A. This DC voltage sets the midpoint voltage of the C signal (S-Video) and the Pb, Pr signals (Component video) for Channel A when the gain is set to x2. **When using the YPbPr inputs in YPbPr mode**, this DC voltage sets the clamp voltage of the Pr/R and Pb/B signals for Channel A. This input is typically tied together with $V_{CHROMA}x2_{IN}B$ and driven with the same voltage.
121	$V_{CHROMA}x1_{IN}A$	Analog Input. Chroma Reference Level for DC-Restore when A_V = 1, for Channel A. This voltage sets the midpoint voltage of the C signal (S-Video) and the Pb, Pr signals (Component video) for Channel A when the gain is set to x1. **When using the YPbPr inputs in YPbPr mode**, this DC voltage sets the clamp voltage of the Pr/R and Pb/B signals for Channel A. This input is typically tied together with $V_{CHROMA}x1_{IN}B$ and driven with the same voltage.

Pin Descriptions (Continued)

PIN NUMBER	PIN NAME	DESCRIPTION
120	$V_{LUMA}x2_{IN}A$	Analog Input. Luma Reference Level for DC-Restore when A_V = 2, for Channel A. **When using the YPbPr inputs in RGB mode**, this DC voltage sets the clamp voltage of the Pr/R and Pb/B signals for Channel A when the gain is set to x2. **When using the YPbPr inputs in YPbPr mode**, this DC voltage sets the clamp voltage of the Pr/R and Pb/B signals for Channel A.This input is typically tied together with $V_{LUMA}x2_{IN}B$ and driven with the same voltage. The Y/G signal is clamped to the $VTIP_{IN}A$ voltage in master mode and $V_{LUMA}x2_{IN}A$ in slave mode.
119	$V_{LUMA}x1_{IN}A$	Analog Input. Luma Reference Level for DC-Restore when A_V = 1, for Channel A. **When using the YPbPr inputs in RGB mode**, this DC voltage sets the clamp voltage of the R and B signals for Channel A when the gain is set to x1. This input is typically tied together with $V_{LUMA}x1_{IN}B$ and driven with the same voltage. The Y/G signal is clamped to the $VTIP_{IN}A$ voltage in master mode and $V_{LUMA}x1_{IN}A$ in slave mode.
118	$VSLICE_{IN}A$	Analog Input. Slicer comparator threshold for extracting composite sync from video, for Channel A. This DC voltage is typically set to 0.07V above $VTIP_{IN}A$, creating a sync tip slicing level of 70mV. This input is typically tied together with $VSLICE_{IN}B$ and driven with the same voltage.
117	$VTIP_{IN}A$	Analog Input. Sync Tip Reference Level for DC-Restore, for Channel A. This DC voltage sets the level of the sync tip of Channel A's output signal. This input is typically tied together with $VTIP_{IN}B$ and driven with the same voltage. In RGB mode (with no Sync-on-Green), this sets the black level of the G channel.
45	$V_{CHROMA}x2_{IN}B$	Analog Input. Chroma Reference Level for DC-Restore when A_V = 2, for Channel A. This DC voltage sets the midpoint voltage of the C signal (S-Video) and the Pb, Pr signals (Component video) for Channel A when the gain is set to x2. **When using the YPbPr inputs in YPbPr mode**, this DC voltage sets the clamp voltage of the Pr/R and Pb/B signals for Channel B. This input is typically tied together with $V_{CHROMA}x2_{IN}A$ and driven with the same voltage.
46	$V_{CHROMA}x1_{IN}B$	Analog Input. Chroma Reference Level for DC-Restore when A_V = 1, for Channel A. This voltage sets the midpoint voltage of the C signal (S-Video) and the Pb, Pr signals (Component video) for Channel A when the gain is set to x1. **When using the YPbPr inputs in YPbPr mode**, this DC voltage sets the clamp voltage of the Pr/R and Pb/B signals for Channel B. This input is typically tied together with $V_{CHROMA}x1_{IN}A$ and driven with the same voltage.
47	$V_{LUMA}x2_{IN}B$	Analog Input. Luma Reference Level for DC-Restore when A_V = 2, for Channel B. **When using the YPbPr inputs in RGB mode**, this DC voltage sets the clamp voltage of the R and B signals for Channel B when the gain is set to x2. This input is typically tied together with $V_{LUMA}x2_{IN}A$ and driven with the same voltage. The Y/G signal is clamped to the $VTIP_{IN}B$ voltage in master mode and $V_{LUMA}x2_{IN}B$ in slave mode.
48	$V_{LUMA}x1_{IN}B$	Analog Input. Luma Reference Level for DC-Restore when A_V = 1, for Channel B. **When using the YPbPr inputs in RGB mode**, this DC voltage sets the clamp voltage of the R and B signals for Channel B when the gain is set to x1. This input is typically tied together with $V_{LUMA}x1_{IN}A$ and driven with the same voltage. The Y/G signal is clamped to the $VTIP_{IN}B$ voltage in master mode and $V_{LUMA}x1_{IN}B$ in slave mode.
49	$VSLICE_{IN}B$	Analog Input. Slicer comparator threshold for extracting composite sync from video, for Channel B. This DC voltage is typically set to 0.07V above $VTIP_{IN}B$, creating a sync tip slicing level of 70mV. This input is typically tied together with $VSLICE_{IN}A$ and driven with the same voltage.
50	$VTIP_{IN}B$	Analog Input. Sync Tip Reference Level for DC-Restore, for Channel B. This DC voltage sets the level of the sync tip of Channel B's output signal. This input is typically tied together with $VTIP_{IN}A$ and driven with the same voltage. In RGB mode (with no Sync-on-Green), this sets the black level of the G channel.
I^2C CONTROL AND I/O		
85	SDA	I^2C Bus Data I/O
82	SCL	I^2C Bus Clock
92	Address	Digital Input with internal pull-down. Sets I^2C address: 0x84 if tied low, 0x8C if tied high. (300k pull-down)
IC RESET, ENABLE AND MISC.		
77	$\overline{\text{Reset}}$	5V Digital Input, with 3.5V logic threshold and a 300k pull-down. Tie to +5V for normal operation. Taking Reset to 0V and back to 5V initializes all data registers to 0x00.
90	PowerDown	Digital Input with 300k pull-down. When this pin is taken high, all analog circuitry is disabled to minimize power consumption. In PowerDown mode, the outputs are tri-stated while the I^2C interface remains active and all register data is retained.
POWER SUPPLIES		
18, 20, 42, 125	V_A	+5V Analog supply

Pin Descriptions (Continued)

PIN NUMBER	PIN NAME	DESCRIPTION
80, 87	V_A	+5V Analog supply for output drivers
POWER SUPPLIES DIGITAL (3V)		
83	V_D	Digital Plus Supply for I^2C
53, 68, 99, 114	V_D	Digital Supply for Sync Separators
POWER SUPPLIES ANALOG GROUND (0V)		
8, 12, 14, 17, 19, 21, 23, 26, 28, 37, 41, 43, 44, 69, 70, 72, 81, 95, 97, 98, 123, 124, 126	GND_A	Analog Ground
POWER SUPPLIES DIGITAL GROUND (0V)		
51, 52, 54, 55, 56, 60, 61, 62, 75, 84, 86, 105, 106, 107, 111, 112, 113, 115, 116	GND_D	Digital Ground
UNUSED PINS		
63, 104	DNC	Not Implemented. Do Not Connect these pins to anything (leave floating).

Typical Performance Curves V_A = +5V, V_D = +3.3V, R_L = 150Ω to GND, T_A = +25°C, unless otherwise specified.

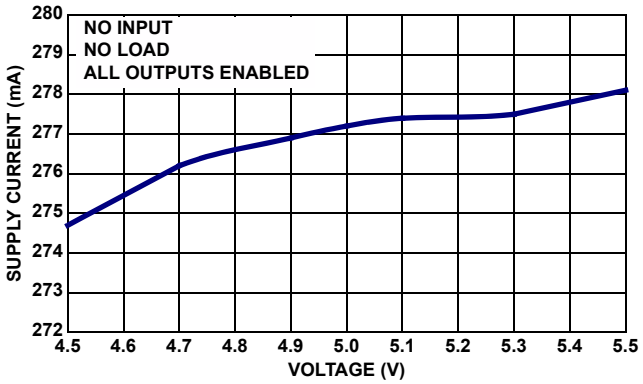


FIGURE 1. ANALOG SUPPLY CURRENT vs SUPPLY VOLTAGE

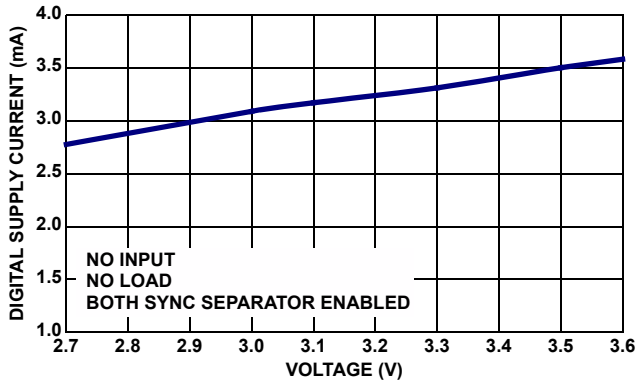


FIGURE 2. DIGITAL SUPPLY CURRENT vs SUPPLY VOLTAGES

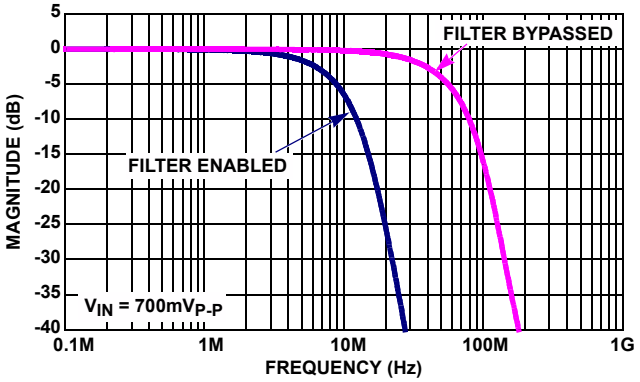


FIGURE 3. COMPOSITE FREQUENCY RESPONSE (GAIN 1)

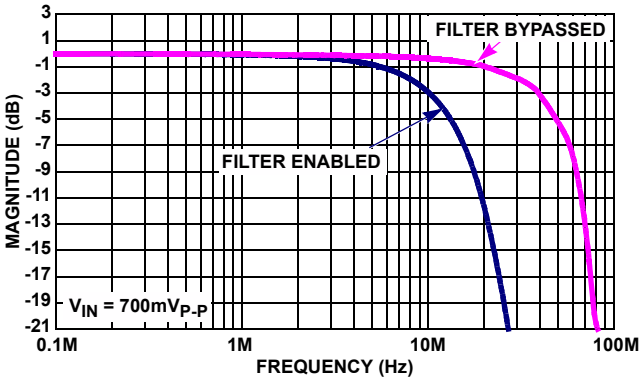


FIGURE 4. COMPOSITE FREQUENCY RESPONSE (GAIN 2)

Typical Performance Curves V_A = +5V, V_D = +3.3V, R_L = 150Ω to GND, T_A = +25°C, unless otherwise specified. **(Continued)**

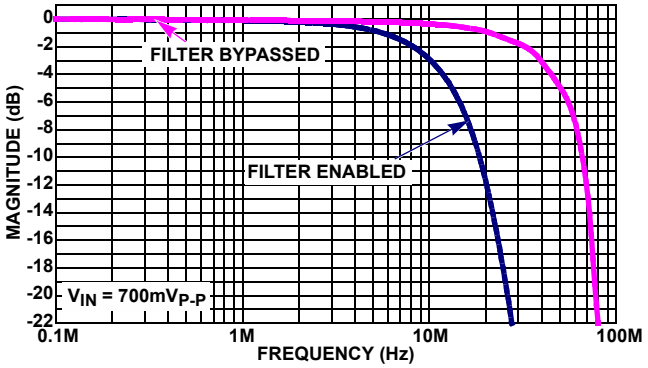


FIGURE 5. S-VIDEO FREQUENCY RESPONSE (GAIN 1)

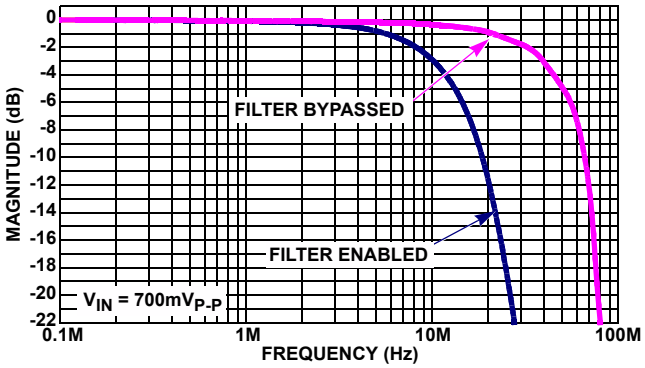


FIGURE 6. S-VIDEO FREQUENCY RESPONSE (GAIN 2)

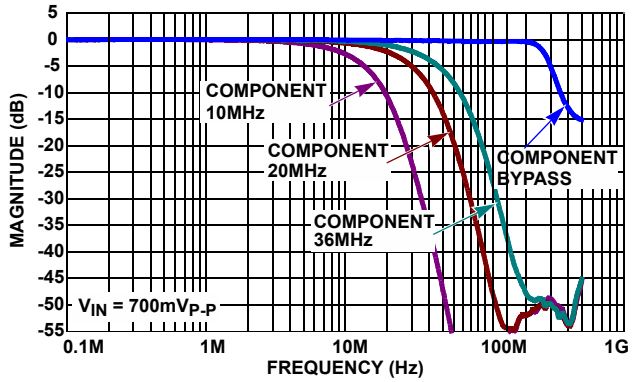


FIGURE 7. COMPONENT BANDWIDTH vs FREQUENCY RESPONSE (GAIN = 1)

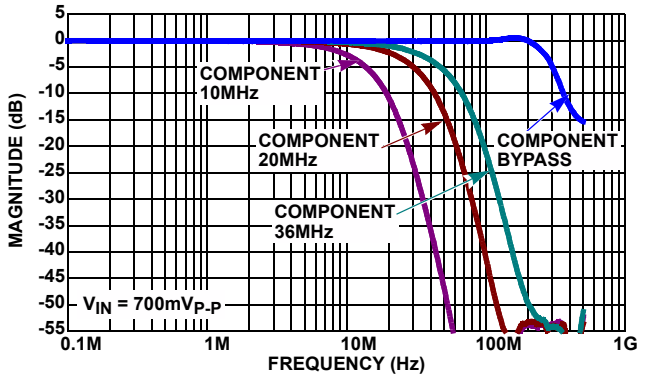


FIGURE 8. COMPONENT BANDWIDTH vs FREQUENCY RESPONSE (GAIN = 2)

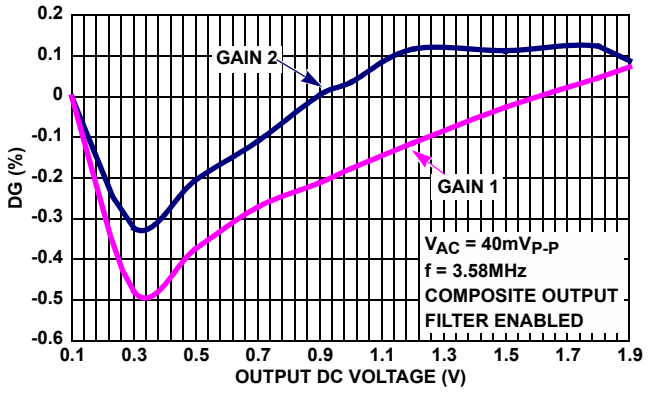


FIGURE 9. DIFFERENTIAL GAIN

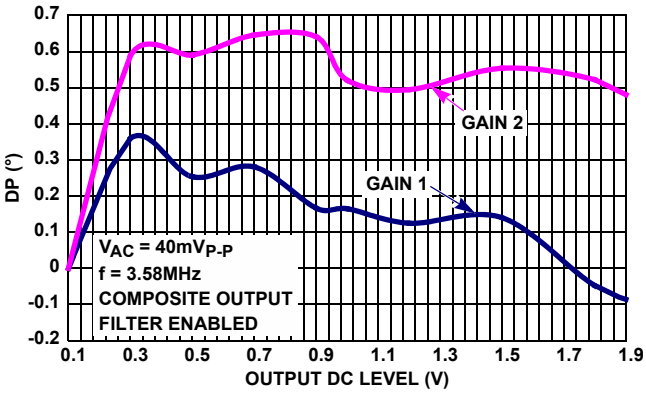


FIGURE 10. DIFFERENTIAL PHASE

Typical Performance Curves V_A = +5V, V_D = +3.3V, R_L = 150Ω to GND, T_A = +25°C, unless otherwise specified. **(Continued)**

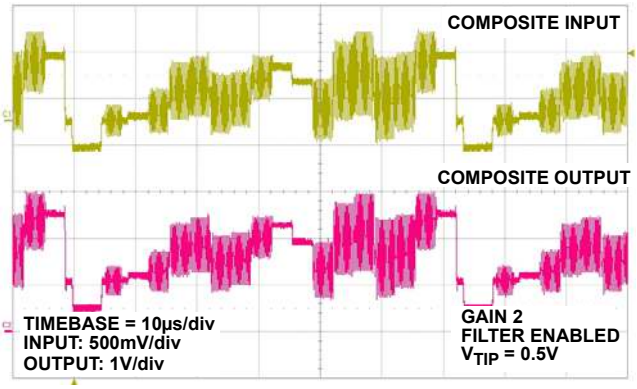


FIGURE 11. COLORBAR RESPONSE

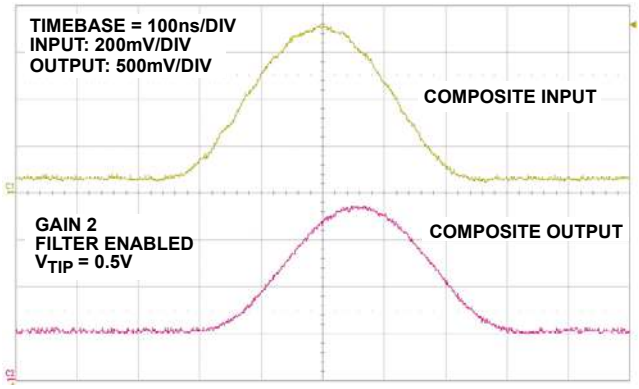


FIGURE 12. 2T RESPONSE

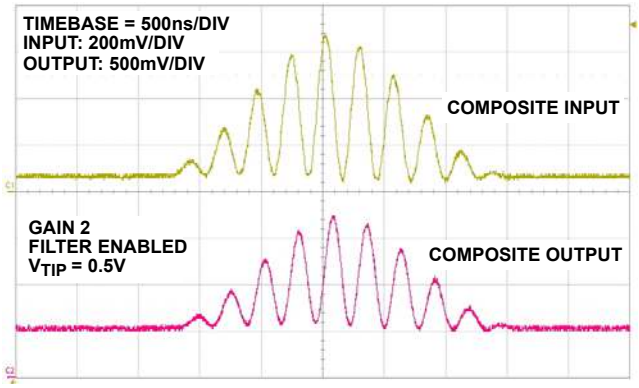


FIGURE 13. 12.5T RESPONSE

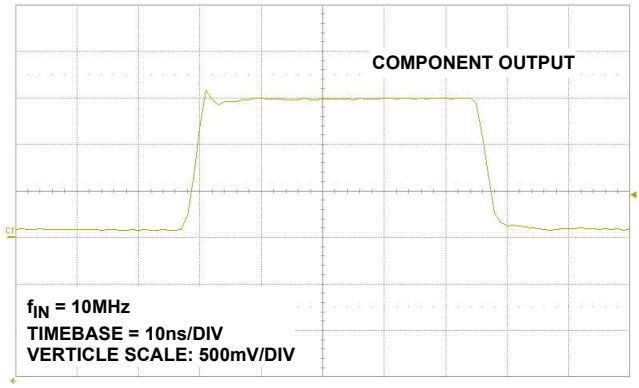


FIGURE 14. COMPONENT LARGE SIGNAL PULSE RESPONSE GAIN 1

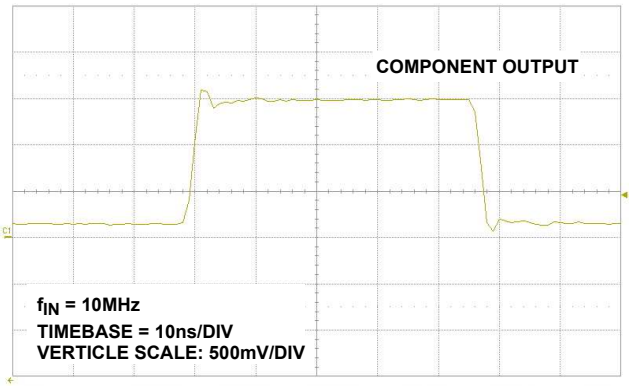


FIGURE 15. COMPONENT LARGE SIGNAL PULSE RESPONSE GAIN 2

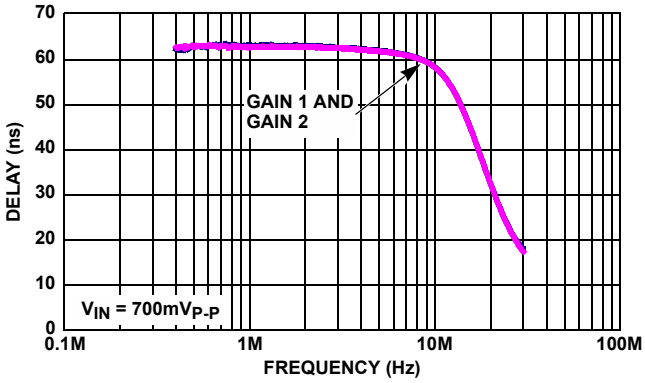


FIGURE 16. COMPOSITE GROUP DELAY

Typical Performance Curves V_A = +5V, V_D = +3.3V, R_L = 150Ω to GND, T_A = +25°C, unless otherwise specified. **(Continued)**

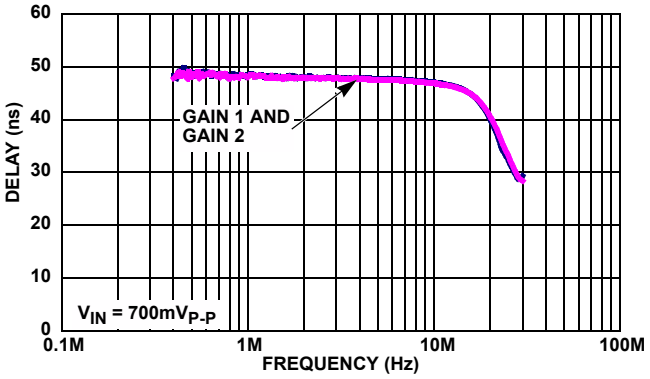


FIGURE 17. S-VIDEO GROUP DELAY

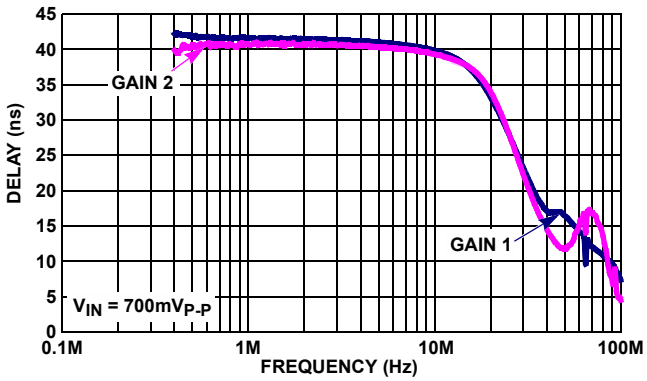


FIGURE 18. COMPONENT 10MHz FILTER GROUP DELAY

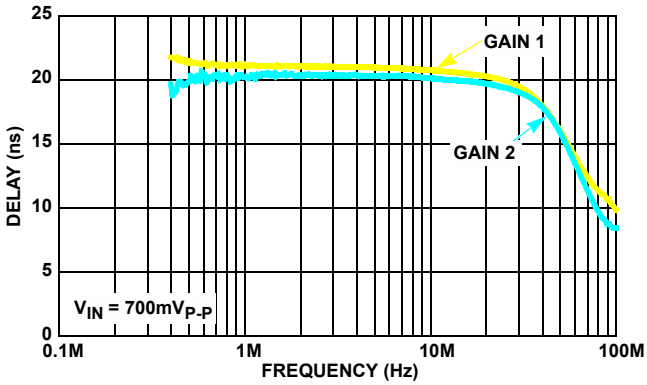


FIGURE 19. COMPONENT 20MHz FILTER GROUP DELAY

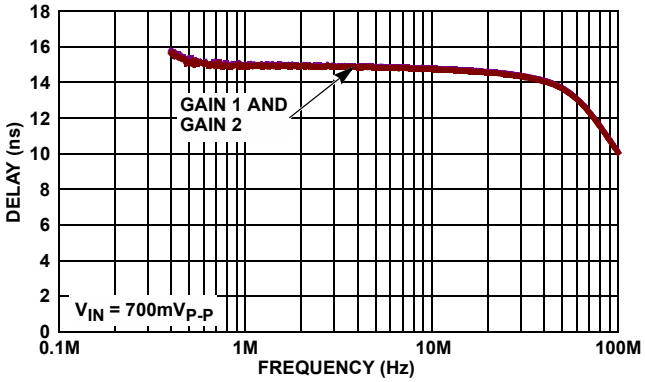


FIGURE 20. COMPONENT 36MHz FILTER GROUP DELAY

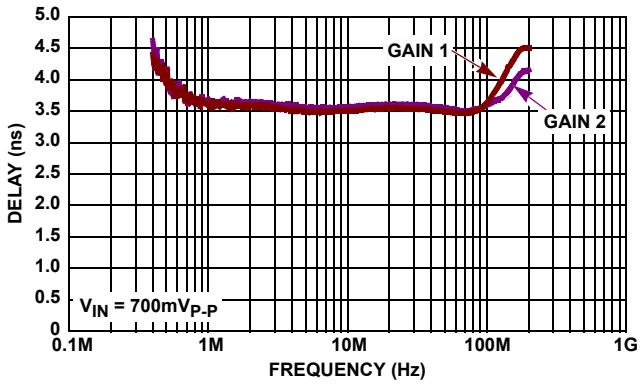


FIGURE 21. COMPONENT BYPASS GROUP DELAY

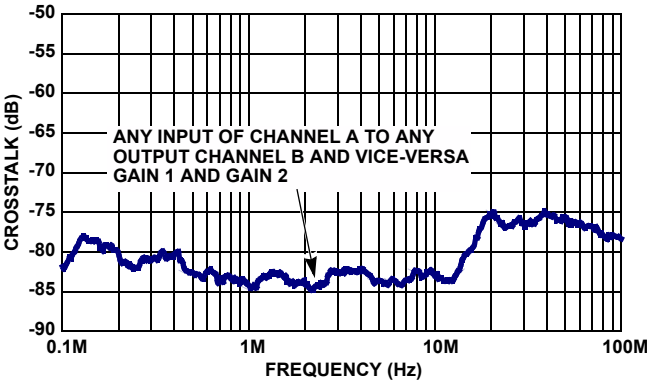


FIGURE 22. INTER-CHANNEL CROSSTALK

Typical Performance Curves V_A = +5V, V_D = +3.3V, R_L = 150Ω to GND, T_A = +25°C, unless otherwise specified. **(Continued)**

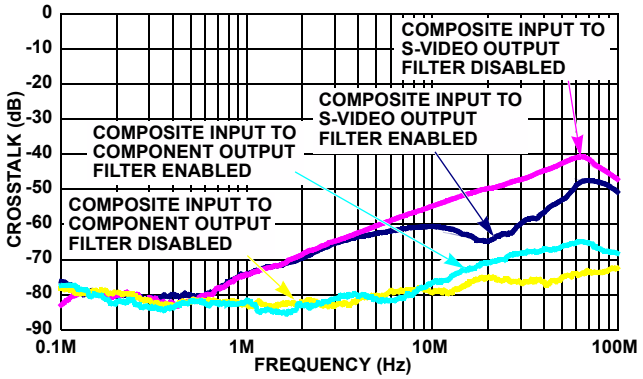


FIGURE 23. INTRA-CHANNEL CROSSTALK: COMPOSITE TO COMPONENT/S-VIDEO

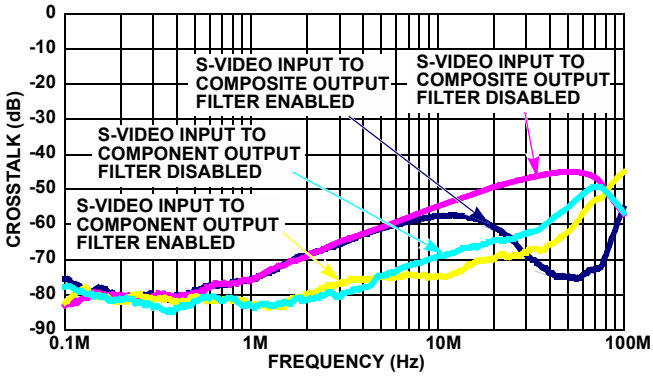


FIGURE 24. INTRA-CHANNEL CROSSTALK: S-VIDEO TO COMPONENT/COMPOSITE

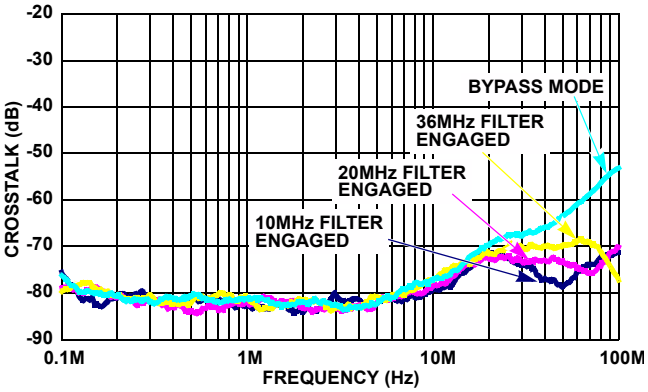


FIGURE 25. INTRA-CHANNEL CROSSTALK: COMPONENT INPUT TO COMPOSITE OUTPUT

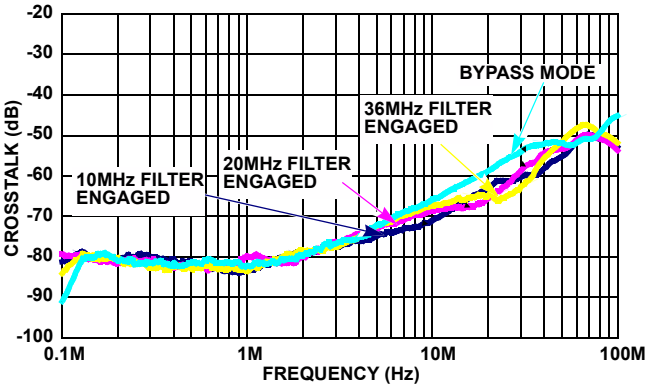


FIGURE 26. INTRA-CHANNEL CROSSTALK: COMPONENT INPUT TO S-VIDEO OUTPUT

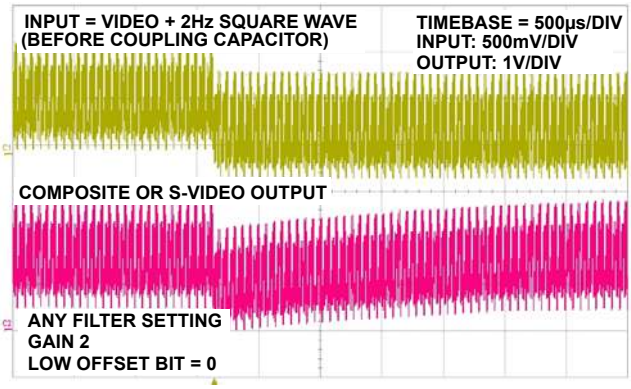


FIGURE 27. COMPOSITE/S-VIDEO: CLAMP RESPONSE TO +250mV STEP ON INPUT (HIGH OFFSET MODE)

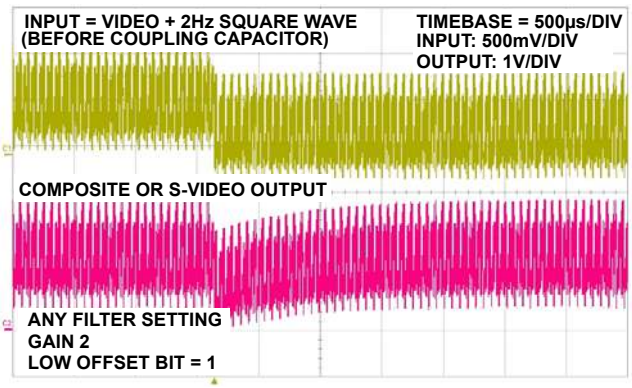


FIGURE 28. COMPOSITE/S-VIDEO: CLAMP RESPONSE TO +250mV STEP ON INPUT (LOW OFFSET MODE)

Typical Performance Curves V_A = +5V, V_D = +3.3V, R_L = 150Ω to GND, T_A = +25°C, unless otherwise specified. **(Continued)**

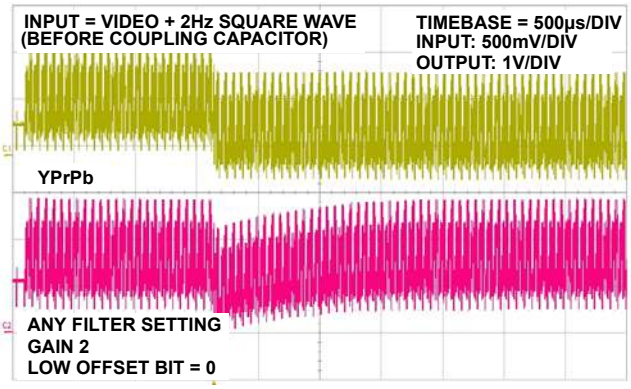


FIGURE 29. COMPONENT: CLAMP RESPONSE TO +250mV STEP ON INPUT (HIGH OFFSET MODE)

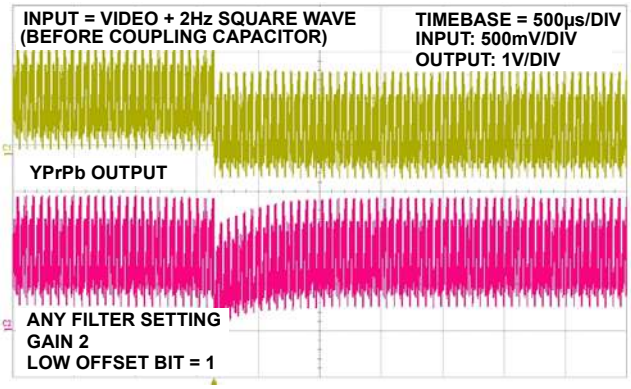


FIGURE 30. COMPONENT: CLAMP RESPONSE TO +250mV STEP ON INPUT (LOW OFFSET MODE)

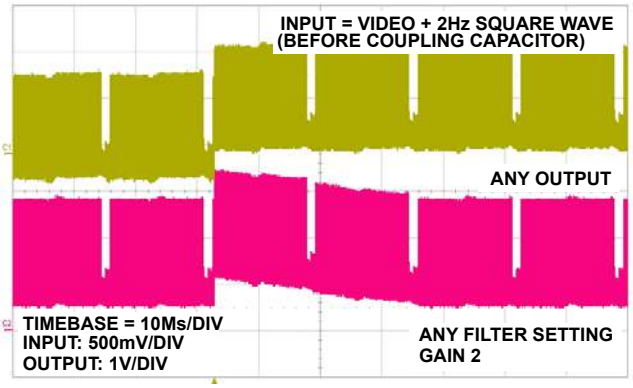


FIGURE 31. PULL-DOWN CURRENT RESPONSE

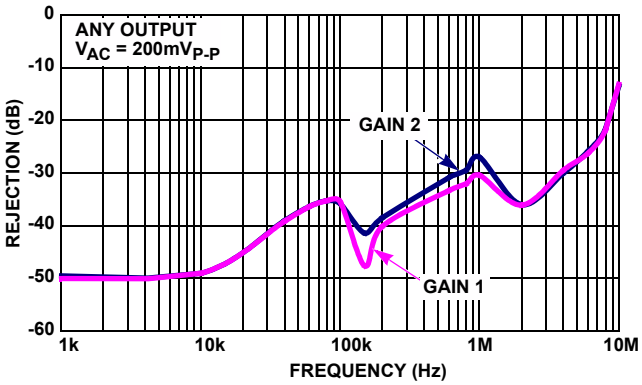


FIGURE 32. PSRR vs FREQUENCY

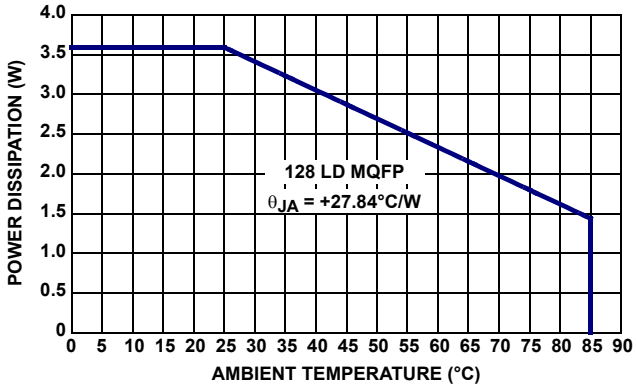


FIGURE 33. PACKAGE POWER DISSIPATION

Functional Description

Signal Muxes

The ISL59450 accepts 6 composite, 4 S-video and 4 component video sources. Each signal type is routed into a crosspoint mux with two outputs. The 6 composite signals are routed into a 6:2 mux, the S-video inputs are routed into a double 4:2 mux and the component video signals are routed into a triple 4:2 mux. Each mux is controlled through the I^2C interface.

Each signal type has two dedicated outputs, A and B. Signal types cannot be routed to different signal type outputs. For example, an S-video signal (Y, C) cannot be routed to the composite outputs.

For the luma (Y and CVBS) channels, the DC-restore function is either a standard sync-tip clamp (Master Mode) or slaved to a clamp signal generated from the sync separator (Slave Mode).

For the chroma (C and Pr/Pb) channels, the DC-restore function is a keyed clamp timed to the luma channel (Master Mode) or timed to a clamp signal generated from the sync separator (Slave Mode).

The clamping circuit restores the AC-coupled video signal to a fixed DC level (V_{TIP}, or V_{LUMA}). The clamping circuit provides line-by-line restoration of the video sync level to a the selected DC reference voltage during the sync tip.

Clamp Modes

The ISL59450 has two clamp modes: master and slave. Each output group can operate in either mode. In master mode, sync timing is derived directly from the video signal and video levels are clamped using this internal sync signal. In slave mode, video sync is derived from the input groups corresponding sync separator (A or B) or an external source connected to the corresponding sync separator. In the slave mode, the sync timing can come from $HSYNC_{IN}$ and $VSYNC_{IN}$ or it can be derived from the sync timing on the active video on the composite, S-video, or component channels (see “Sync Separator Block Diagram” on page 9). In the slave mode, clamping occurs during the sync tip of the selected video signal or the HSYNC signal (external HSYNC input).

Filters

The ISL59450 has integrated anti-aliasing/smoothing filters for SD and HD video signals. For the Composite Video signals, the user can use a 7MHz low pass filter or bypass it (40MHz bandwidth). S-video signals have an 10MHz filter with bypass (43MHz). Component Video signals have a user-selectable 36MHz, 20MHz, or 10MHz filter, or bypass (275MHz). All filters selections are made via the I^2C host interface.

Clamps

The clamps for all the luma and composite channels can be sync tip clamps (master mode) or timed keyed clamps (slave mode) driven off the sync separator. The clamps for the chroma channels (C/Pr/Pb) are keyed clamps timed to either the luma (master mode) or the sync separator (slave mode).

Clamp Disable

The clamp can be disabled for each channel by setting the appropriate bit high in the Miscellaneous 2 register (0x16).

For the S-video and component channels, additional action needs to be taken in order to completely disable the clamps.

For S-video, setting the bit in the Miscellaneous 2 register disables the pull-down 1µA pull-down current for both the luma and chroma channel along with the clamp pull-up current for the luma channel. However, it does not disable the clamp pull-up current for the chroma channel unless the sync separator for that channel is set to 0x25.

For component, setting the bit in the Miscellaneous 2 register disables the pull-down 1µA pull-down current for all three channels, along with the clamp pull-up current for the luma channel. However, it does not disable the clamp pull-up current for the Pr and Pb channels unless the sync separator for that channel is set to 0x24.

Low Offset Mode

Setting bit 6 in the Composite and S-Video Channel registers increases the maximum amount of pull-up clamp current available from 130µA to 270µA, which slightly reduces the offset between the reference and the output when the clamp is enabled.

For the component channels, this setting can be enabled by setting Bit 7 in the Miscellaneous 2 register for Channel A and Bit 3 for Channel B. This mode increases the maximum amount of pull-up clamp current available from 270µA to 500µA.

References

Table 1 shows the references used for clamping depending on the mode and video input being used. V_{SLICE} should usually be set to 70mV to 100mV above the selected reference level for luma.

TABLE 1. CHANNEL REFERENCE LEVELS

VIDEO OUTPUT	MASTER MODE		SLAVE MODE	
	GAIN 1	GAIN 2	GAIN 1	GAIN 2
Composite	V_{TIP}	V_{TIP}	$V_{LUMA}x1$	$V_{LUMA}x2$
S-Video **Luma**	V_{TIP}	V_{TIP}	$V_{LUMA}x1$	$V_{LUMA}x2$
S-Video **Chroma**	$V_{CHROMA}x1$	$V_{CHROMA}x2$	$V_{CHROMA}x1$	$V_{CHROMA}x2$
Component: **Luma/Green** *(YPrPb Mode)*	V_{TIP}	V_{TIP}	$V_{LUMA}x1$	$V_{LUMA}x2$
Component: **Luma/Green** *(RGB Mode)*	V_{TIP}	V_{TIP}	$V_{LUMA}x1$	$V_{LUMA}x2$

TABLE 1. CHANNEL REFERENCE LEVELS (Continued)

VIDEO OUTPUT	MASTER MODE		SLAVE MODE	
	GAIN 1	GAIN 2	GAIN 1	GAIN 2
Component: **Pr/Pb** *(YPrPb Mode)*	$V_{CHROMA}x1$	$V_{CHROMA}x2$	$V_{CHROMA}x1$	$V_{CHROMA}x2$
Component: **Pr/Pb** *(RGB Mode)*	$V_{LUMA}x1$	$V_{LUMA}x2$	$V_{LUMA}x1$	$V_{LUMA}x2$

Bypass each reference voltage with a 0.01µF capacitor to ground to reduce noise injection.

TABLE 2. SUGGESTED REFERENCE LEVELS

REFERENCE	VOLTAGE (V)
$VTIP_{IN}A$	0.5
$VTIP_{IN}B$	0.5
$V_{LUMA}x1_{IN}A$	0.5
$V_{LUMA}x2_{IN}A$	0.5
$V_{LUMA}x1_{IN}B$	0.5
$V_{LUMA}x2_{IN}B$	0.5
$V_{CHROMA}x1_{IN}A$	1
$V_{CHROMA}x2_{IN}A$	1
$V_{CHROMA}x1_{IN}B$	1
$V_{CHROMA}x2_{IN}B$	1
$VSLICE_{IN}A$	0.6
$VSLICE_{IN}B$	0.6

Outputs/Levels

Each signal output has a selectable gain of 0dB (GAIN 1) or 6dB (GAIN 2).

The input to the sync separators can be any of the video inputs, as shown in the “Sync Separator Block Diagram” on page 9. The HSYNC and VSYNC inputs are dedicated to their respective sync separator (i.e. Sync Separator A can connect to $HSYNC_{IN}A$ and $VSYNC_{IN}A$, but not $HSYNC_{IN}B$ and $VSYNC_{IN}B$).

Sync Separators

The ISL59450 contains two high performance video sync separators that automatically lock to any SD and HD video signal. They will also extract sync timing information from non-standard video inputs and in the presence of Macrovision pulses. Composite sync, vertical sync and horizontal sync outputs are provided from each sync separator. Timing is adjusted automatically for various video standards. The composite sync output follows video in sync pulses and a vertical sync pulse is output on the rising edge of the first vertical serration following the vertical pre-equalizing string. For non-standard vertical inputs, a default vertical pulse is output when the vertical signal stays low for longer than the vertical sync default delay time. The horizontal output gives horizontal timing with pre/post equalizing pulses.

The use of two sync separators allows the user to send independent sync information for two signals to downstream devices. An example would be two video decoders or two ADCs that are used in a picture-in-picture application. Each sync separator is dedicated to its respective channel, Sync Separator A for Channel A and Sync Separator B for Channel B. It is important to note that the syncs for each channel cannot be MUXed onto the other channel. For example, $HSYNC_{IN}A$ and $VSYNC_{IN}A$ **cannot** be MUXed to $HSYNC_{OUT}B$ and $VSYNC_{OUT}B$.

See the “Sync Separator Timing Diagrams” beginning on page 32 for typical horizontal and vertical sync output timing.

VERTICAL SYNC

A low-going Vertical Sync pulse is output during the start of the vertical cycle of the incoming video signal. The vertical cycle starts with a pre-equalizing phase of pulses with a duty cycle of about 93%, followed by a vertical serration phase that has a duty cycle of about 15%. Vertical Sync is clocked out of the ISL59450 on the first rising edge during the vertical serration phase. In the absence of vertical serration pulses, a vertical sync pulse will be forced out after the vertical sync default delay time, approximately 60µs after the last falling edge of the vertical equalizing phase.

HORIZONTAL SYNC

The horizontal circuit senses the composite sync edges and produces the true horizontal pulses of nominal width 5µs for standard definition NTSC signals. The pulse width of the HSYNC output changes as the line frequency of the input signal changes. For example, an NTSC input generates an $HSYNC_{OUT}$ with a pulse width of 5µs; while a 720p HD video input generates an $HSYNC_{OUT}$ with a pulse width of 1.9µs. The leading edge is triggered from the leading edge of the input HSYNC with the same propagation delay as composite sync. The half line pulses present in the input signal during vertical blanking are removed with an internal 2H line eliminator circuit. This is a circuit that inhibits horizontal output pulses until 75% of the line time is reached, then the horizontal output operation is enabled again. Any signals present on the I/P signal after the true H sync will be ignored, thus the horizontal output will not be effected by MacroVision copy protection. When there is a loss of sync, the Horizontal Sync output is held high.

C_{SET}

Connect external capacitors from $C_{SET}A$ and $C_{SET}B$ to ground. The C_{SET} capacitor should be a X7R grade or better as the Y5U general use capacitors may be too leaky and cause faulty operation. The C_{SET} capacitor should be very close to the $C_{SET}A$ and $C_{SET}B$ pins to reduce possible board leakage. 56nF is recommended. The C_{SET} capacitor rectifies a 5µs pulse current and creates a voltage on C_{SET}.

The C_{SET} voltage is converted to bias current for H_{SYNC} and V_{SYNC} timing.

Internal Control Registers

The ISL59450 is initialized and controlled by a set of internal registers that define the operating parameters of the entire device. Communication is established between the external controller and the ISL59450 through a standard I^2C host port interface, as described earlier. The Register Listing table on page 24 describes all of these registers. Detailed I^2C programming information for each register is described in "ISL59450 Serial Communications" on page 33.

Note: Do not write to reserved registers. Reserved bits in any register should be written with 0s, unless otherwise noted.

INITIALIZATION

It is recommended that the registers are initialized to 0x00 by toggling the $\overline{\text{Reset}}$ pin low after powering the device. Once the registers are initialized, set bit 0 of Miscellaneous Register 1 to **one** to engage the global enable and allow the various channels to be powered up.

Logic Control Signals

$\overline{\text{Reset}}$ is a 5V digital Input, with 3.5V logic threshold and a 300k pull-down. Tie to +5V for normal operation. Taking Reset to 0V and back to 5V initializes all data registers to 0x00.

Power-down is a digital input with 300k pull-down. When this pin is taken high, all analog circuitry is disabled to minimize power consumption. In Power-down mode, the outputs are tri-stated while the I^2C interface remains active and all register data is retained.

Crosstalk Issues

Do not set any one input to both A and B channels if the references and modes for A and B are different. For example, do not send $CV_{IN}0$ to both $CV_{OUT}A$ and $CV_{OUT}B$ if the references for Channel A and Channel B are different or if one channel is in slave mode while the other is in master mode. This could cause clamping conflicts and compromise performance.

Use the lowest bandwidth setting suitable for each application to minimize noise, aliasing, and crosstalk. See "Typical Application Curves" on page 19 and page 19.

Layout Issues

- Match channel-to-channel analog I/O trace lengths and layout symmetry. This will minimize propagation delay mismatches for S-video and component traces.
- All signal I/O lines should be routed over continuous ground planes (i.e. no split planes or PCB gaps under these lines).
- Put the proper termination resistors as close to the device as possible.
- When testing, use high quality connectors and cables, matching cable types and keep cable lengths to a minimum.
- Decouple well using a minimum of 2 power supply decoupling capacitors (1000pF, 0.01µF), placed as close to the devices as possible. Vias between the capacitor and the device add unwanted inductance. Larger capacitors can be farther away.

Power Dissipation

With the high output drive capability of the ISL59450, it is possible to exceed the +125°C absolute maximum junction temperature under certain load current conditions. Therefore, it is important to calculate the maximum junction temperature for an application to determine if load conditions or package types need to be modified to assure operation of the amplifier in a safe operating area.

The maximum power dissipation allowed in a package is determined according to Equation 1:

$$PD_{MAX} = \frac{T_{JMAX} - T_{AMAX}}{\theta_{JA}} \quad \text{(EQ. 1)}$$

Where:

T_{JMAX} = Maximum junction temperature

T_{AMAX} = Maximum ambient temperature

θ_{JA} = Thermal resistance of the package

The maximum power dissipation actually produced by an IC is the total quiescent supply current times the total power supply voltage, plus the power in the IC due to the load, or:

for sourcing use Equation 2:

$$PD_{MAX} = V_S \times I_{SMAX} + (V_S - V_{OUT}) \times \frac{V_{OUT}}{R_L} \quad \text{(EQ. 2)}$$

for sinking use Equation 3:

$$PD_{MAX} = V_S \times I_{SMAX} + (V_{OUT} - V_S) \times I_{LOAD} \quad \text{(EQ. 3)}$$

Where:

V_S = Supply voltage

I_{SMAX} = Maximum quiescent supply current

V_{OUT} = Maximum output voltage of the application

R_{LOAD} = Load resistance tied to ground

I_{LOAD} = Load current

Register Listings

ISL59450 I²C CONTROL MAP		DATA GREY = READ ONLY, WHITE = READ/WRITE							
I²C ADDR.	FUNCTION	BIT 7	BIT 6	BIT 5	BIT 4	BIT 3	BIT 2	BIT 1	BIT 0
0x00	**Sync Separator A**	Sync Output Polarity	Reserved Set to 0	Enable	Reserved Set to 0	Sync Input Polarity	Sync Type	Input Select b1	Input Select b0
0x01	**Sync Separator B**	Sync Output Polarity	Reserved Set to 0	Enable	Reserved Set to 0	Sync Input Polarity	Sync Type	Input Select b1	Input Select b0
0x02	**Composite Output A**	Slave Mode A	Low Offset Mode	Enable	Output Amplifier Gain	Filter Disable	Input Select b2	Input Select b1	Input Select b0
0x03	**Composite Output B**	Slave Mode B	Low Offset Mode	Enable	Output Amplifier Gain	Filter Disable	Input Select b2	Input Select b1	Input Select b0
0x04	**S-Video Output Group A**	Slave Mode A	Low Offset Mode	Enable	Output Amplifier Gain	Filter Disable	Reserved Set to 0	Input Select b1	Input Select b0
0x05	**S-Video Output Group B**	Slave Mode B	Low Offset Mode	Enable	Output Amplifier Gain	Filter Disable	Reserved Set to 0	Input Select b1	Input Select b0
0x06	**Component Video Output Group A**	Slave Mode A	RGB Mode	Enable	Output Amplifier Gain	Filter b1	Filter b0	Input Select b1	Input Select b0
0x07	**Component Video Output Group B**	Slave Mode B	RGB Mode	Enable	Output Amplifier Gain	Filter b1	Filter b0	Input Select b1	Input Select b0
0x08 - 0x13	**Reserved** Ignore the contents of and do not write to these registers.	0	0	0	0	0	0	0	0
0x14	**Miscellaneous 1** S-Video Connected. Field Invert Enable allows Field output signal to be inverted when "Sync Output Polarity" bit is set. Global Enable: 0: Low power standby mode with outputs in high-impedance state, 1: Powers up all internal reference	S-Video 3 Connected	S-Video 2 Connected	S-Video 1 Connected	S-Video 0 Connected	Reserved Set to 0	Reserved Set to 0	Field Invert Enable	Global Enable
0x15	**Reserved** Ignore the contents of and do not write to these registers.	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved
0x16	**Miscellaneous 2**	Component A Low Offset Mode	Disable Component A Clamp	Disable S-Video A Clamp	Disable Composite A Clamp	Component B Low Offset Mode	Disable Component B Clamp	Disable S-Video B Clamp	Disable Composite B Clamp

Register Descriptions

ADDRESS	REGISTER	BIT(S)	FUNCTION NAME	DESCRIPTION
0x00	Sync Separator A	1:0	Input Select A	Chooses the sync source for Sync Separator A to process. Use these bits in conjunction with the Sync Type bit directly below. 00: Component SOG (Channel A) 01: S-Video SOG (Channel A) 10: Composite SOG (Channel A) 11: External H and V or CSYNC on H (Channel A)
		2	Sync Type A	This bit must be set to the type of incoming sync. For all SOG or CSYNC signals, this bit should be set. 0: HSYNC is on HSYNCA, VSYNC is on VSYNCA 1: SOG or CSYNC on HSYNCA
		3	Sync Input Polarity A	This bit must be set depending on the polarity of the incoming sync. 0: SOG and active low external HSYNC/CSYNC. 1: Active high external, HSYNC/CSYNC signal. This forces the internal polarity of the HSYNC signal to be correct for clamping. Please note setting this bit also inverts the polarity of HsyncA and VsyncA outputs. See “Typical Register Settings” on page 31 for correct values.
		4	Reserved	Set this bit to 0.
		5	Enable A	0: Sync Separator A is disabled 1: Sync Separator A is enabled
		6	Reserved	Set this bit to 0.
		7	Sync Output Polarity A	Polarity of HsyncA and VsyncA outputs 0: Active Low 1: Active High Note: If the Field Invert Enable bit (register 0x14b1) is set, FieldA’s output will also be inverted when this bit is set.

Register Descriptions (Continued)

ADDRESS	REGISTER	BIT(S)	FUNCTION NAME	DESCRIPTION
0x01	Sync Separator B	1:0	Input Select B	Chooses the sync source for Sync Separator B to process. Use these bits in conjunction with the Sync Type bit directly below. 00: Component SOG (Channel B) 01: S-Video SOG (Channel B) 10: Composite SOG (Channel B) 11: External H and V or CSYNC on H (Channel B)
		2	Sync Type B	This bit must be set to the type of incoming sync. For all SOG or CSYNC signals, this bit should be set. 0: HSYNC is on HSYNCB, VSYNC is on VSYNCB 1: SOG or CSYNC on HSYNCB
		3	Sync Input Polarity B	This bit must be set depending on the polarity of the incoming sync. 0: SOG and active low external HSYNC/CSYNC. 1: Active high external, HSYNC/CSYNC signal. This forces the internal polarity of the HSYNC signal to be correct for clamping. Please note setting this bit also inverts the polarity of HsyncB and VsyncB outputs. See “Typical Register Settings” on page 31 for correct values.
		4	Reserved	Set this bit to 0.
		5	Enable B	0: Sync Separator B is disabled 1: Sync Separator B is enabled
		6	Reserved	Set this bit to 0.
		7	Sync Output Polarity B	Polarity of HsyncB and VsyncB outputs 0: Active Low 1: Active High Note: If the Field Invert Enable bit (register 0x14b1) is set, FieldB’s output will also be inverted when this bit is set.
0x02	Composite Channel A	2:0	Input Select A	0: $CVBS_{IN}0$ 1: $CVBS_{IN}1$ 2: $CVBS_{IN}2$ 3: $CVBS_{IN}3$ 4: $CVBS_{IN}4$ 5: $CVBS_{IN}5$
		3	Filter Disable A	0: 7MHz Smoothing Filter 1: Smoothing Filter bypassed (40MHz bandwidth)
		4	Output Amplifier Gain A	0: x1 1: x2
		5	Enable A	0: Disables (High-Z) Composite A output 1: Enables Composite output A
		6	Low Offset Mode A	0: Normal Mode 1: Low Offset Mode Slightly lowers the DC offset from input to output by increasing the maximum amount of clamp restore current from 130µA to 270µA.
		7	Slave Mode A	0: Sync tip DC-restore on selected channel (master mode) 1: DC-restore clamp timing slaved to Sync Separator A (slave mode)

Register Descriptions (Continued)

ADDRESS	REGISTER	BIT(S)	FUNCTION NAME	DESCRIPTION
0x03	Composite Channel B	2:0	Input Select B	0: $CVBS_{IN}0$ 1: $CVBS_{IN}1$ 2: $CVBS_{IN}2$ 3: $CVBS_{IN}3$ 4: $CVBS_{IN}4$ 5: $CVBS_{IN}5$
		3	Filter Disable B	0: 7MHz Smoothing Filter 1: Smoothing Filter bypassed (40MHz bandwidth)
		4	Output Amplifier Gain B	0: x1 1: x2
		5	Enable B	0: Disables (High-Z) Composite B output 1: Enables Composite output B
		6	Low Offset Mode B	0: Normal Mode 1: Low Offset Mode Slightly lowers the DC offset from input to output by increasing the maximum amount of clamp restore current from 130µA to 270µA.
		7	Slave Mode B	0: Sync tip DC-restore on selected channel (master mode) 1: DC-restore clamp timing slaved to Sync Separator B (slave mode)
0x04	S-Video Channel A	1:0	Input Select A	0: $Svideo_{IN}0$ 1: $Svideo_{IN}1$ 2: $Svideo_{IN}2$ 3: $Svideo_{IN}3$
		2	Reserved	Set this bit to 0
		3	Filter Disable A	0: 10MHz Smoothing Filter 1: Smoothing Filter bypassed (40MHz bandwidth)
		4	Output Amplifier Gain A	0: x1 1: x2
		5	Enable A	0: Disables (High-Z) S-Video A outputs 1: Enables S-Video A outputs
		6	Low Offset Mode A	0: Normal Mode 1: Low Offset Mode Slightly lowers the DC offset of the output by increasing the maximum amount of clamp restore current from 130µA to 270µA.
		7	Slave Mode A	0: Sync tip DC-restore on selected channel (master mode) 1: DC-restore clamp timing slaved to Sync Separator A (slave mode)

Register Descriptions (Continued)

ADDRESS	REGISTER	BIT(S)	FUNCTION NAME	DESCRIPTION
0x05	S-Video Channel B	1:0	Input Select B	0: $Svideo_{IN}0$ 1: $Svideo_{IN}1$ 2: $Svideo_{IN}2$ 3: $Svideo_{IN}3$
		2	Reserved	Set this bit to 0
		3	Filter Disable B	0: 10MHz Smoothing Filter 1: Smoothing Filter bypassed (40MHz bandwidth)
		4	Output Amplifier Gain B	0: x1 1: x2
		5	Enable B	0: Disables (High-Z) S-Video B outputs 1: Enables S-Video B outputs
		6	Low Offset Mode B	0: Normal Mode 1: Low Offset Mode Slightly lowers the DC offset of the output by increasing the maximum amount of clamp restore current from 130µA to 270µA.
		7	Slave Mode B	0: Sync tip DC-restore on selected channel (master mode) 1: DC-restore clamp timing slaved to Sync Separator B (slave mode)
0x06	Component Channel A	1:0	Input Select A	0: $YPbPr_{IN}0$ 1: $YPbPr_{IN}1$ 2: $YPbPr_{IN}2$ 3: $YPbPr_{IN}3$
		3:2	Filter Select A	0: 10MHz Smoothing FIlter 1: 20MHz Smoothing FIlter 2: 36MHz Smoothing Filter 3: Smoothing Filter Bypassed (250MHz bandwidth)
		4	Output Amplifier Gain A	0: x1 1: x2
		5	Enable A	0: Disables (High-Z) Component A outputs 1: Enables Component A outputs
		6	RGB Mode A	0: YPbPr Mode Y clamps to $VTIP_{IN}A$ (master mode) Y clamps to $V_{LUMA}x1/2_{IN}A$ (slave mode) Pb/Pr clamps to $V_{CHROMA}x1/2_{IN}A$ 1: RGB Mode Y clamps to $VTIP_{IN}A$ (master mode) Y clamps to $V_{LUMA}x1/2_{IN}A$ (slave mode) Pb/Pr clamps to $V_{LUMA}x1/2_{IN}A$
		7	Slave Mode A	0: Sync tip DC-restore on selected channel (master mode) 1: DC-restore clamp timing slaved to Sync Separator A (slave mode)

Register Descriptions (Continued)

ADDRESS	REGISTER	BIT(S)	FUNCTION NAME	DESCRIPTION
0x07	Component Channel B	1:0	Input Select B	0: $YPbPr_{IN}0$ 1: $YPbPr_{IN}1$ 2: $YPbPr_{IN}2$ 3: $YPbPr_{IN}3$
		3:2	Filter Select B	0: 10MHz Smoothing Filter 1: 20MHz Smoothing Filter 2: 36MHz Smoothing Filter 3: Smoothing Filter Bypassed (250MHz bandwidth)
		4	Output Amplifier Gain B	0: x1 1: x2
		5	Enable B	0: Disables (High-Z) Component B outputs 1: Enables Component B outputs
		6	RGB Mode B	0: YPbPr Mode Y clamps to $VTIP_{IN}B$ (master mode) Y clamps to $V_{LUMA}x1/2_{IN}B$ (slave mode) Pb/Pr clamps to $V_{CHROMA}x1/2_{IN}B$ 1: RGB Mode Y clamps to $VTIP_{IN}B$ (master mode) Y clamps to $V_{LUMA}x1/2_{IN}B$ (slave mode) Pb/Pr clamps to $V_{LUMA}x1/2_{IN}B$
		7	Slave Mode B	0: Sync tip DC-restore on selected channel (master mode) 1: DC-restore clamp timing slaved to Sync Separator B (slave mode)
0x08-0x0B	Reserved (Read only)	7:0	Reserved	Reserved
0x0C-0x0D	Reserved	7:0	Reserved	Write 0x00 to these registers
0x0E-0x11	Reserved (Read only)	7:0	Reserved	Reserved
0x12-0x13	Reserved	7:0	Reserved	Write 0x00 to these registers
0x14	Miscellaneous 1 (Bits 4 thru 7 are read-only)	0	Global Enable	0: All outputs disabled 1: Outputs enabled per their individual Enable settings
		1	Field Invert Enable	0: The Sync Output Polarity bit (Sync Separator) does not affect Field polarity. 1: The Sync Output Polarity bit (Sync Separator) inverts the Field output.
		2	Reserved	Set this bit to 0
		3	Reserved	Set this bit to 0
		4	S-Video 0 Connected	0: Cable plugged in to S-Video Channel 0 1: Nothing plugged in to S-Video Channel 0
		5	S-Video 1 Connected	0: Cable plugged in to S-Video Channel 1 1: Nothing plugged in to S-Video Channel 1
		6	S-Video 2 Connected	0: Cable plugged in to S-Video Channel 2 1: Nothing plugged in to S-Video Channel 2
		7	S-Video 3 Connected	0: Cable plugged in to S-Video Channel 3 1: Nothing plugged in to S-Video Channel 3
0x15	Reserved	7:0	Reserved	Reserved

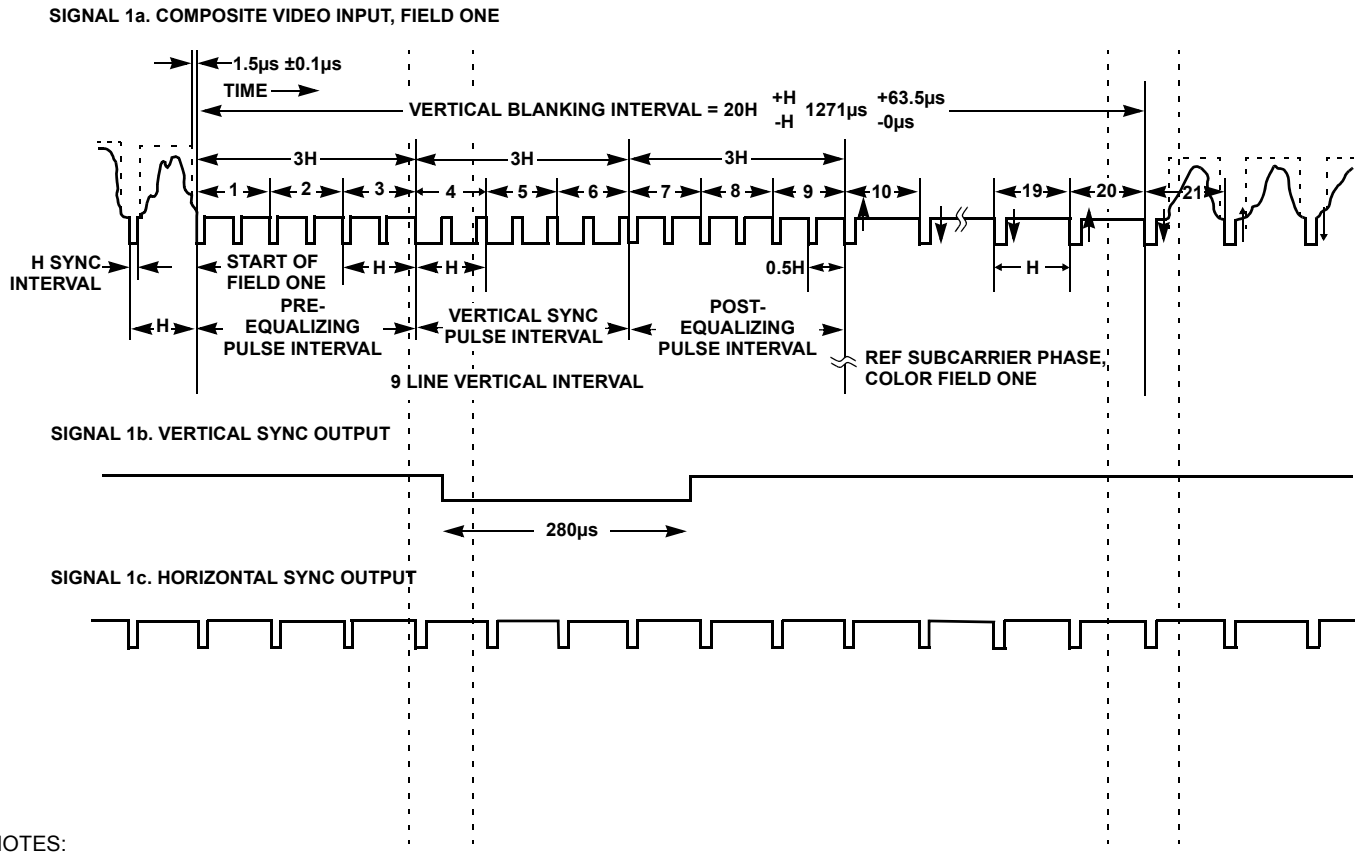
Register Descriptions (Continued)

ADDRESS	REGISTER	BIT(S)	FUNCTION NAME	DESCRIPTION
0x16	Miscellaneous 2	0	Disable Composite B Clamp	This bit disables the DC-restore clamp for composite Channel B. 0: Composite A clamp enabled 1: Composite A clamp disabled
		1	Disable S-Video B Clamp	This bit disables the DC-restore clamp for the luma (Y) of S-Video Channel B. Disables the 1µA pull-down currents for **both** Y and C. Does **not** disable the clamp for chroma channel unless in Slave mode **and** Sync Separator. B = 0x25. 0: S-Video A clamp enabled 1: S-Video A clamp disabled
		2	Disable Component B Clamp	This bit disables the DC-restore clamp for Y/G of component Channel B. Disables the 1µA pull-down currents for **ALL** three channels. Does **not** disable the pull-up clamp for Pr/R and Pb/B unless in Slave mode **AND** Sync Separator. B = 0x24. 0: Y Component A clamp enabled 1: Y Component A clamp disabled
		3	Component B Low Offset Mode	0: Normal operation 1: DC-restore clamp has a lower offset. Slightly lowers the DC offset of the component outputs by increasing the maximum amount of clamp restore current from 250µA to 500µA.
		4	Disable Composite A Clamp	This bit disables the DC-restore clamp for composite Channel A 0: Composite A clamp enabled 1: Composite A clamp disabled
		5	Disable S-Video A Clamp	This bit disables the DC-restore clamp for the luma (Y) of S-Video Channel A. Disables the 1µA pull-down currents for **both** Y and C. Does **not** disable the clamp for chroma channel unless in Slave mode **and** Sync Separator. A = 0x25. 0: S-Video A clamp enabled 1: S-Video A clamp disabled
		6	Disable Component A Clamp	This bit disables the DC-restore clamp for Y/G of component Channel A. Disables the 1µA pull-down currents for **ALL** three channels. Does **not** disable the clamps for Pr/R and Pb/B unless in Slave mode **AND** Sync Separator. A = 0x24. 0: Y Component A clamp enabled 1: Y Component A clamp disabled
		7	Component A Low Offset Mode	0: Normal operation 1: DC-restore clamp has a lower offset. Slightly lowers the DC offset of the component outputs by increasing the maximum amount of clamp restore current from 250µA to 500µA.

Typical Register Settings

REGISTER SETTINGS	VIDEO TYPE	CHANNEL A REGISTER ADDRESS	CHANNEL B REGISTER ADDRESS	CHANNEL REGISTER VALUE	SYNC SEPARATOR REGISTER VALUE
For all settings, Miscellaneous 1 Register (0x14) = 0xX1 and Miscellaneous 2 (0x16) = 0x00.					
Composite 0	Composite	0x02	0x03	0x30	0x00
Composite 1	Composite	0x02	0x03	0x31	0x00
Composite 2	Composite	0x02	0x03	0x32	0x00
Composite 3	Composite	0x02	0x03	0x33	0x00
Composite 4	Composite	0x02	0x03	0x34	0x00
Composite 5	Composite	0x02	0x03	0x35	0x00
S-Video 1	S-Video	0x04	0x05	0x30	0x00
S-Video 2	S-Video	0x04	0x05	0x31	0x00
S-Video 3	S-Video	0x04	0x05	0x32	0x00
S-Video 4	S-Video	0x04	0x05	0x33	0x00
Component 0	Component	0x06	0x07	0x3C	0x00
	RGB + HV	0x06	0x07	0xFC	0x23 (active low sync in) 0xAB (active high sync in)
Component 1	Component	0x06	0x07	0x3D	0x00
	RGB + HV	0x06	0x07	0xFD	0x23 (active low sync in) 0xAB (active high sync in)
Component 2	Component	0x06	0x07	0x3E	0x00
	RGB + HV	0x06	0x07	0xFE	0x23 (active low sync in) 0xAB (active high sync in)
Component 3	Component	0x06	0x07	0x3F	0x00
	RGB+HV	0x06	0x07	0xFF	0x23 (active low sync in) 0xAB (active high sync in)

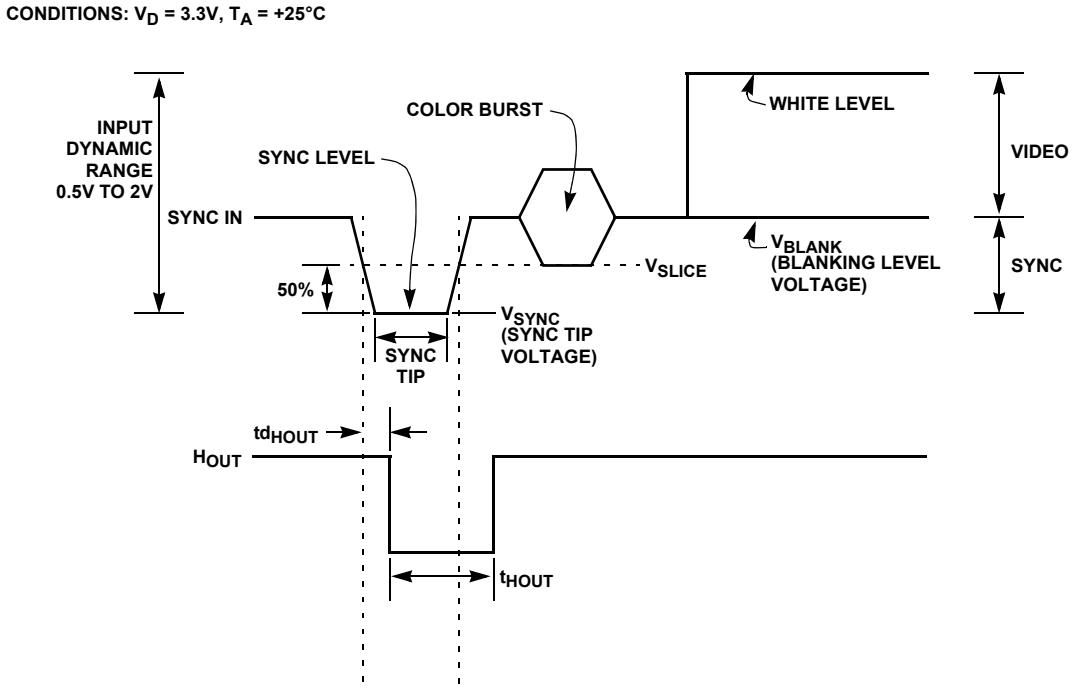
Sync Separator NTSC Vertical Timing



NOTES:

2. The composite sync output reproduces all the video input sync pulses, with a propagation delay.
3. Vertical sync leading edge is coincident with the first vertical serration pulse leading edge with a propagation delay.
4. Horizontal sync output produces the true “H” pulses of nominal width of 5µs. It has the same delay as the composite sync.

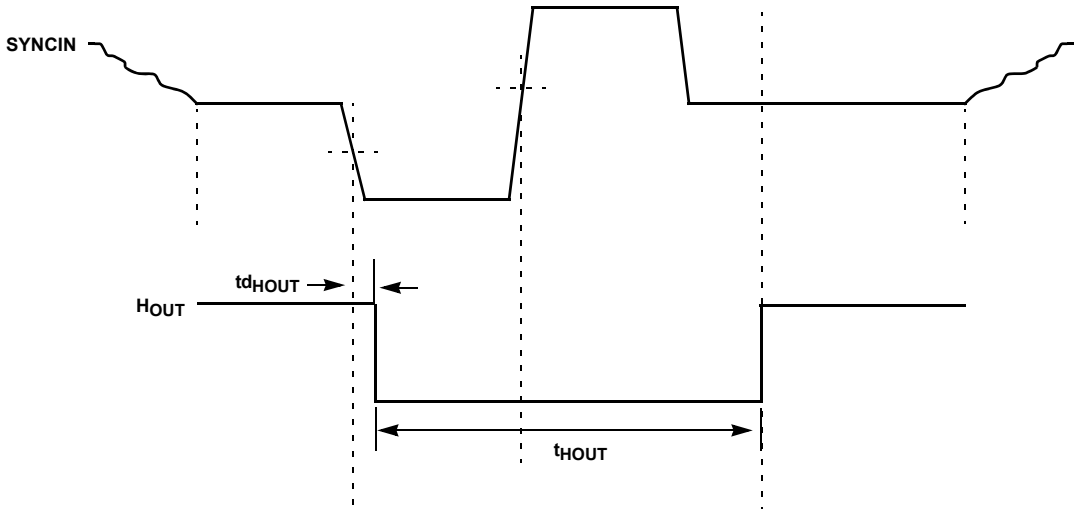
Sync Separator NTSC Horizontal Timing



PARAMETER	DESCRIPTION	CONDITIONS	TYP	UNIT
td_{HOUT}	HOUT Timing Relative to Input		200	ns
t_{HOUT}	Horizontal Output Width		5	µs

Sync Separator HSYNC Timing for 720p

CONDITIONS: V_D = 3.3V T_A = +25°C



PARAMETER	DESCRIPTION	CONDITIONS	TYP @ 3.3V	UNIT
td_{HOUT}	HOUT Timing Relative to Input		90	ns
t_{HOUT}	Horizontal Output Width		1.90	µs

ISL59450 Serial Communications

I^2C Overview

The ISL59450 uses a 2-wire I^2C serial bus for communication with its host. SCL is the Serial Clock line, driven by the host, and SDA is the Serial Data line, which can be driven by all devices on the bus. SDA is open drain to allow multiple devices to share the same bus simultaneously.

Communication is accomplished in three steps:

1. The Host selects the ISL59450 with which it wishes to communicate.
2. The Host writes the initial ISL59450 Configuration Register address it wishes to write to or read from.
3. The Host writes to or reads from the ISL59450's Configuration Register. The ISL59450's internal address pointer auto increments, so to read registers 0x00 through 0x16, for example, one would write 0x00 in step two, then repeat step four 28 times, with each read returning the next register value.

The ISL59450 has a 7-bit address on the serial bus. The upper 6-bits are permanently set to 100010x, with the x determined by the state of the Address pin (Table 3). This allows two ISL59450s to be independently controlled while sharing the same bus. The Address pin has an internal pull-down resistor to pull the terminal low to set a zero.

TABLE 3. I^2C ADDRESS OPTIONS

B7	B6	B5	B4	B3	B2	B1	B0	HEX
A6 (MSB)	A5	A4	A3	A2	A1	A0 (Address)	R/W	
1	0	0	0	0	1	0	1/0	0x85/0x84
1	0	0	0	0	1	1	1/0	0x87/0x86

The bus is nominally inactive, with SDA and SCL high. Communication begins when the host issues a START command by taking SDA low while SCL is high (Figure 34). The ISL59450 continuously monitors the SDA and SCL lines for the start condition and will not respond to any command until this condition has been met. The host then transmits the 7-bit serial address plus a R/$\overline{W}$ bit, indicating if the next transaction will be a Read (R/$\overline{W}$ = 1) or a Write (R/$\overline{W}$ = 0). If the address transmitted matches that of any device on the bus, that device must respond with an ACKNOWLEDGE (Figure 35).

Once the serial address has been transmitted and acknowledged, one or more bytes of information can be written to or read from the slave. Communication with the selected device in the selected direction (read or write) is ended by a STOP command, where SDA rises while SCL is high (Figure 34), or a second START command, which is commonly used to reverse data direction without relinquishing the bus.

Data on the serial bus must be valid for the entire time SCL is high (Figure 36). To achieve this, data being written to the ISL59450 is latched on a delayed version of the rising edge of SCL. SCL is delayed and de-glitched inside the ISL59450 for three crystal clock periods (120ns for a 25MHz crystal) to eliminate spurious clock pulses that could disrupt serial communication.

When the contents of the ISL59450 are being read, the SDA line is updated after the falling edge of SCL, delayed and de-glitched in the same manner.

Configuration Register Write

Figure 37 shows two views of the steps necessary to write one or more words to the Configuration Register.

Configuration Register Read

Figure 38 shows two views of the steps necessary to read one or more words from the Configuration Register.

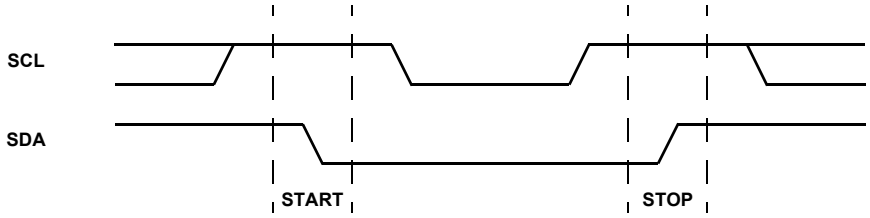


FIGURE 34. VALID START AND STOP CONDITIONS

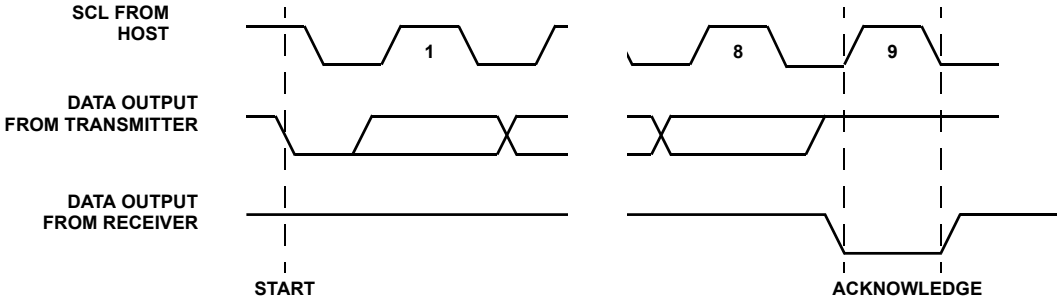


FIGURE 35. ACKNOWLEDGE RESPONSE FROM RECEIVER

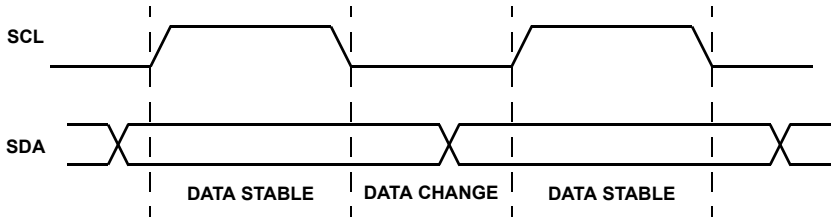
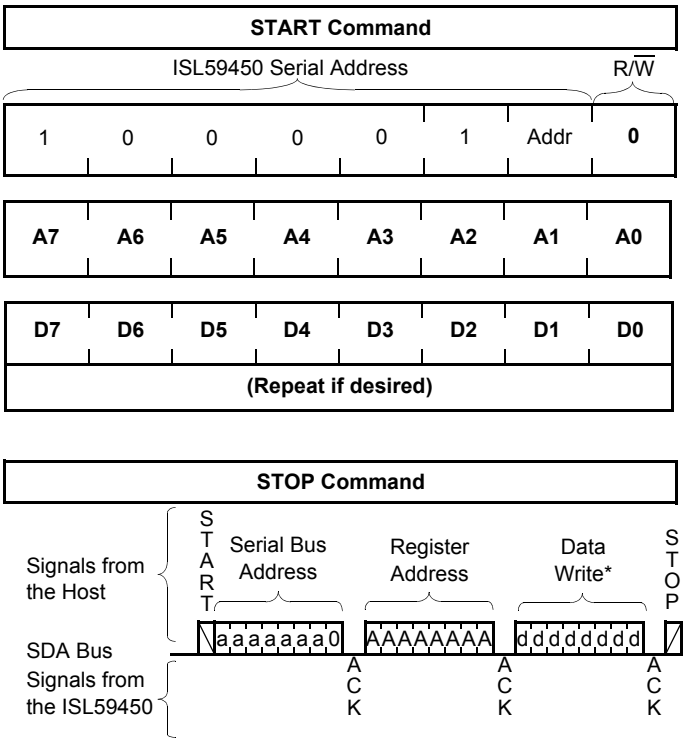


FIGURE 36. VALID DATA CHANGES ON THE SDA BUS



START Command — **Signals the beginning of serial I/O**

ISL59450 Device Select Address Write

The first 7 bits of the first byte select the ISL59450 on the 2-wire bus at the address set by the Address pin. R/$\overline{W}$ = 0, indicating the next transaction will be a write.

ISL59450 Register Address Write

This is the address of the ISL59450's configuration register that the following byte will be written to.

ISL59450 Register Data Write(s)

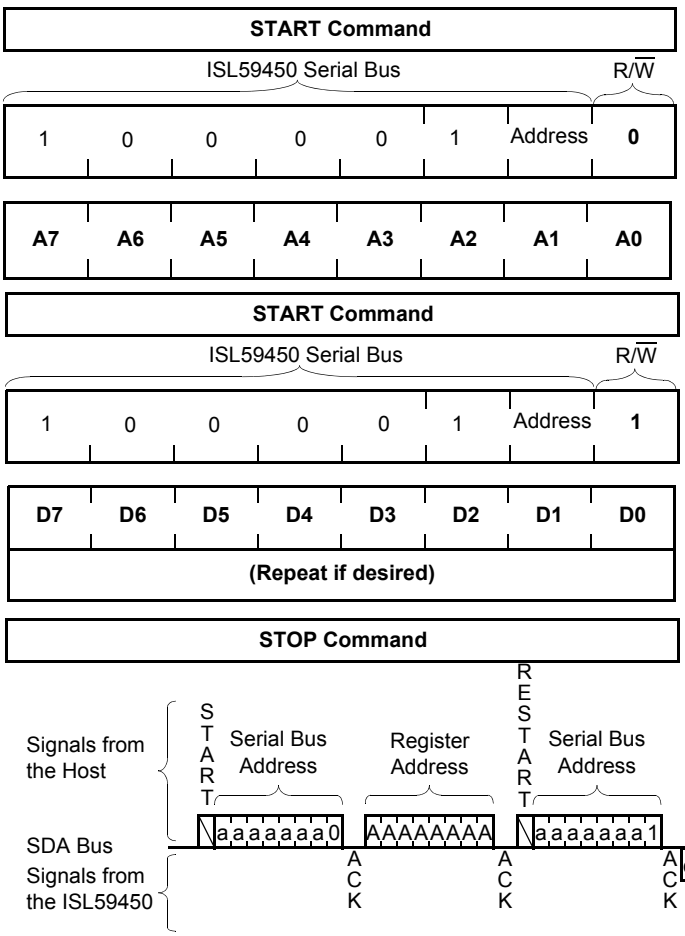
This is the data to be written to the ISL59450's configuration register.

Note: The ISL59450's Configuration Register's address pointer auto increments after each data write. Repeat this step to write multiple sequential bytes of data to the Configuration Register.

STOP Command — **Signals the ending of serial I/O**

* The data write step may be repeated to write to the ISL59450's Configuration Register sequentially, beginning at the Register Address written in the previous step.

FIGURE 37. CONFIGURATION REGISTER WRITE



Signals the beginning of serial I/O

ISL59450 Device Select Address Write

The first 7 bits of the first byte select the ISL59450 on the 2-wire bus at the address set by the Address pin. R/$\overline{W}$ = 0, indicating the next transaction will be a write.

ISL59450 Register Address Write

This sets the initial address of the ISL59450's configuration register for subsequent reading.

Ends the previous transaction and starts a new one

ISL59450 Serial Bus Address Read

This is the 7-bit address of the ISL59450 on the 2-wire bus. The address is 0x85 if pin 92 is low, 0x87 if pin 92 is high. R/$\overline{W}$ = 1, indicating next transaction(s) will be a read.

ISL59450 Register Data Read(s)

This is the data read from the ISL59450's configuration register.

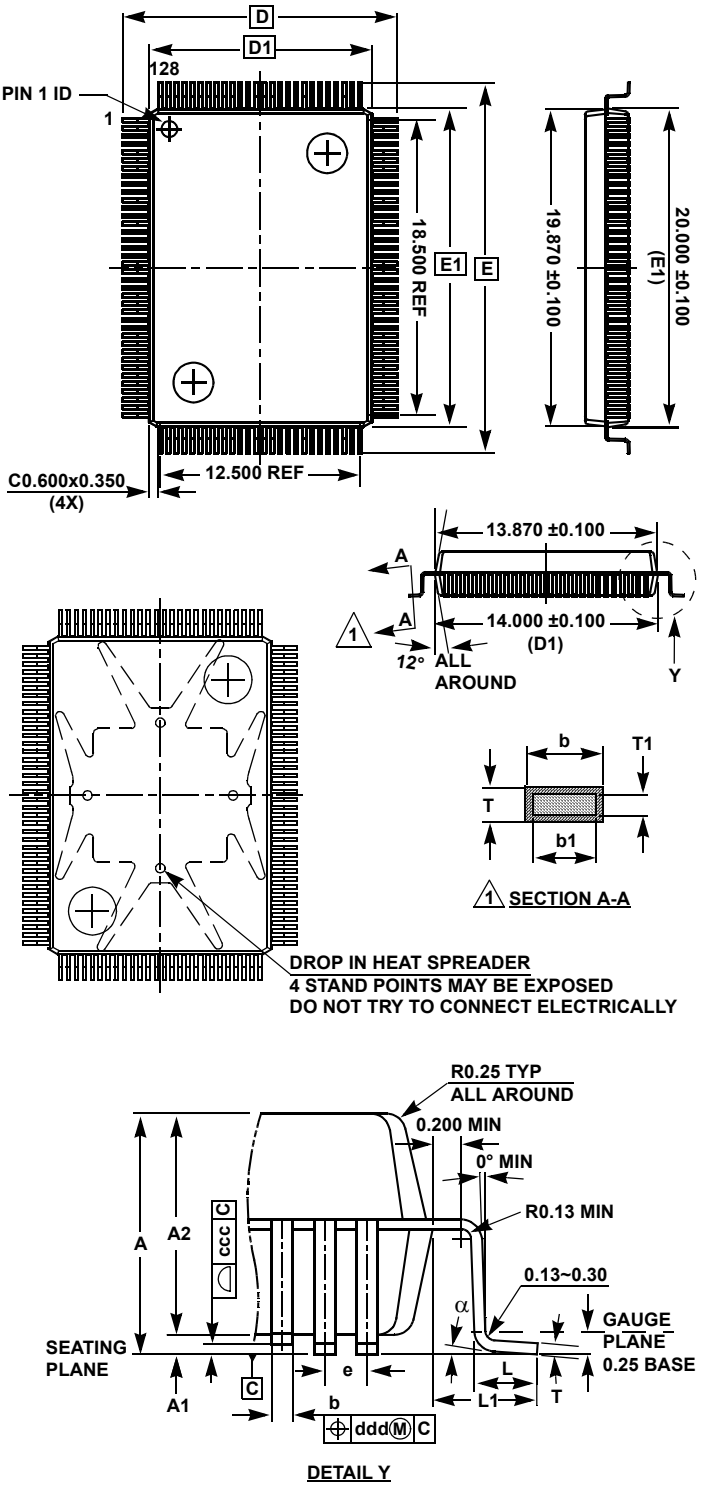
Note: The ISL59450's Configuration Register's address pointer auto increments after each data read. Repeat this step to read multiple sequential bytes of data from the Configuration Register.

Signals the ending of serial I/O

* The data read step may be repeated to read from the ISL59450's Configuration Register sequentially, beginning at the Register Address written in the two previous steps.

FIGURE 38. CONFIGURATION REGISTER READ

Metric Plastic Quad Flatpack Packages (MQFP)



MDP0055

14x20mm 128 LEAD MQFP (WITH AND WITHOUT HEAT SPREADER) 3.2mm FOOTPRINT

SYMBOL	DIMENSIONS (MILLIMETERS)	REMARKS
A	Max 3.40	Overall height
A1	0.250~0.500	Standoff
A2	2.750 ±0.250	Package thickness
α	0°~7°	Foot angle
b	0.220 ±0.050	Lead width (1)
b1	0.200 ±0.030	Lead base metal width (1)
D	17.200 ±0.250	Lead tip to tip
D1	14.000 ±0.100	Package length
E	23.200 ±0.250	Lead tip to tip
E1	20.000 ±0.100	Package width
e	0.500 Base	Lead pitch
L	0.880 ±0.150	Foot length
L1	1.600 Ref.	Lead length
T	0.170 ±0.060	Frame thickness (1)
T1	0.152 ±0.040	Frame base metal thickness (1)
ccc	0.100	Foot coplanarity
ddd	0.100	Foot position

Rev. 2 2/07

NOTES:

1. General tolerance: Distance ±0.100, Angle +2.5°.
2. (1) Matte finish on package body surface except ejection and pin 1 marking (Ra 0.8~2.0um).
3. All molded body sharp corner RADII unless otherwise specified (Max RO.200).
4. Package/Leadframe misalignment (X, Y): Max. 0.127
5. Top/Bottom misalignment (X, Y): Max. 0.127
6. Drawing does not include plastic or metal protrusion or cutting burr.
7. (2) Compliant to JEDEC MS-022.