Description

The 8V41N012A is a PLL-based clock generator specifically designed for Cavium Networks Octeon II processors. This high-performance device is optimized to generate the processor core reference clock, the PCI-Express, sRIO, XAUI, SerDes reference clocks, and the clocks for both the Gigabit Ethernet MAC and PHY. The output frequencies are generated from a 25MHz external input source or an external 25MHz parallel resonant crystal.

The industrial temperature range of the 8V41N012A supports telecommunication, networking, and storage requirements.

Features

- Ten selectable 100MHz, 125MHz, 156.25MHz and 312.5MHz clocks for PCI Express, sRIO, and GbE, HCSL interface levels
- One single-ended QG LVCMOS/LVTTL clock output at 125MHz
- One single-ended QF LVCMOS/LVTTL clock output at 50MHz
- Two single-ended QREFx LVCMOS/LVTTL outputs at 25MHz
- Selectable external crystal or differential (single-ended) input source
- Crystal oscillator interface designed for 25MHz, parallel resonant crystal
- Differential CLK, nCLK input pair that can accept: LVPECL, LVDS, LVHSTL, and HCSL input levels
- Internal resistor bias on nCLK pin allows the user to drive CLK input with external single-ended (LVCMOS/ LVTTL) input levels
- Supply Modes, (125MHz QG output and 25MHz QREFx outputs):
  - Core / Output
  - 3.3V / 3.3V
  - 3.3V / 2.5V
- Supply Modes, (HCSL outputs, and 50MHz QF output):
  - Core / Output
  - 3.3V / 3.3V
- -40°C to 85°C ambient operating temperature
- 10 x 10 mm 72-VFQFPN, lead-free (RoHS 6) packaging

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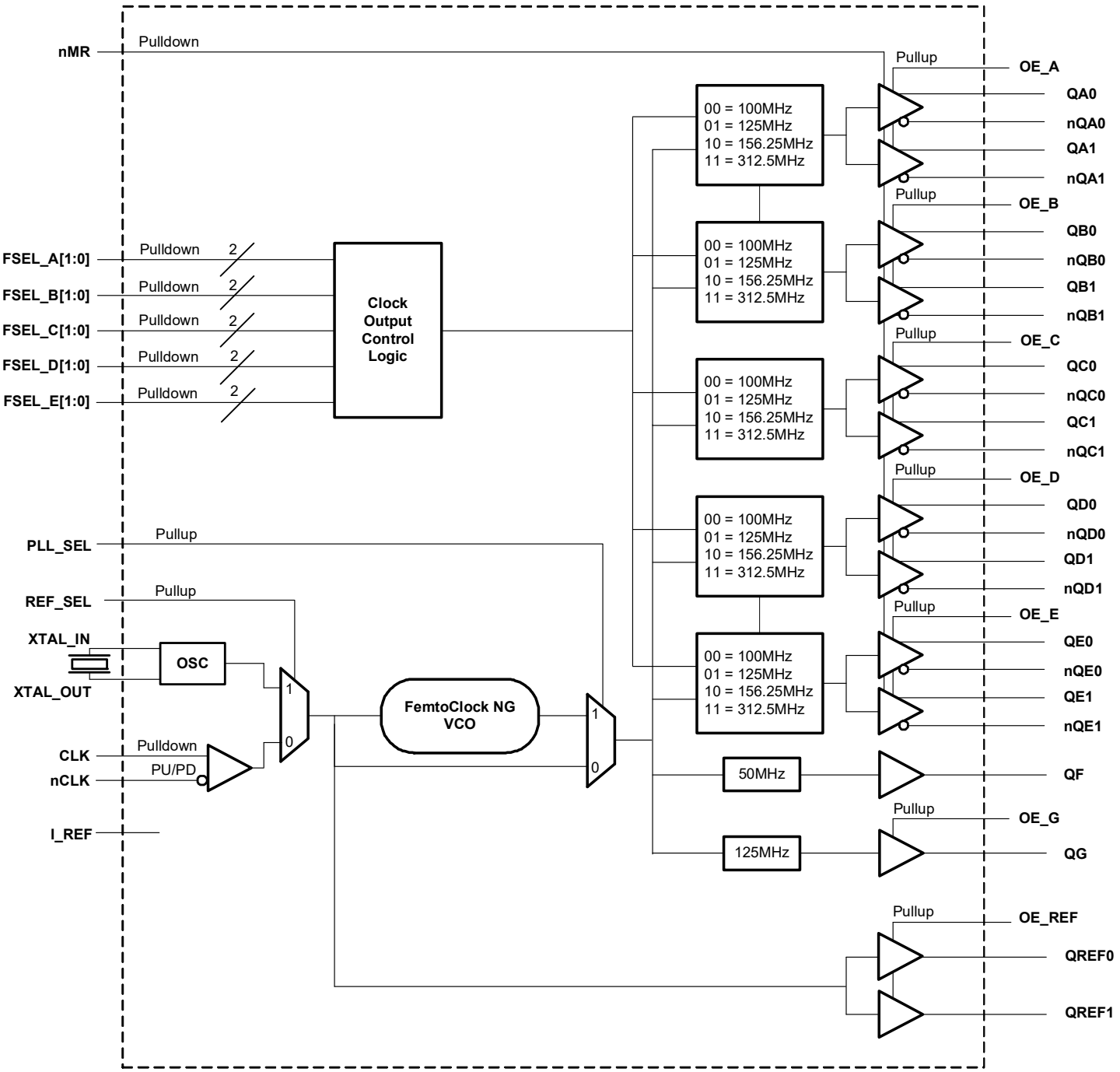
Block Diagram



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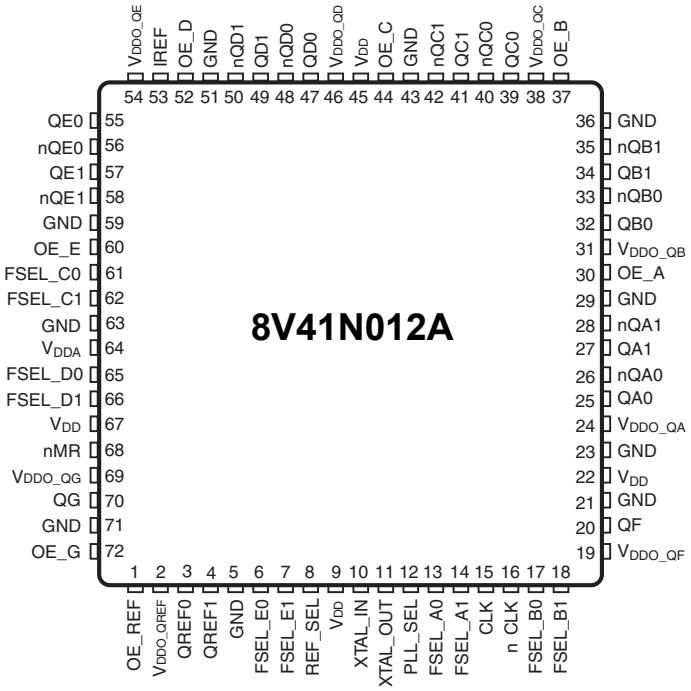
Pin Assignments



10 x 10 mm 72-VFQFPN

Note: Exposed pad must always be connected to GND.
Note: Pin 1 is located at bottom left corner as shown.

Pin Descriptions

Table 1. Pin Descriptions

Number	Name	Type		Description
1	OE_REF	Input	Pullup	Active HIGH output enable for QREF0 and QREF1 outputs. LVCMOS/LVTTL interface levels. 0 = QREF0, QREF1 outputs disabled/high impedance 1 = QREF0, QREF1 outputs enabled (default)
2	V_{DDO_QREF}	Power		QREF0, QREF1 output supply pin (LVCMOS/LVTTL). 3.3V or 2.5V supply.
3, 4	QREF0, QREF1	Output		Single-ended REF outputs. 3.3V or 2.5V LVCMOS/LVTTL interface levels.
5, 21, 23, 29, 36, 43, 51, 59, 63, 71	GND	Power		Power supply ground.
6, 7	FSEL_E0 FSEL_E1	Input	Pulldown	Selects the QEx, nQEx output frequency. LVCMOS/LVTTL interface levels. 00 = 100MHz (default) 01 = 125MHz 10 = 156.25MHz 11 = 312.5MHz

Table 1. Pin Descriptions (Continued)

Number	Name	Type		Description
8	REF_SEL	Input	Pullup	Input source control pin. LVCMOS/LVTTL interface levels. 0 = CLK, nCLK 1 = XTAL (default)
9, 22, 45, 67	V_{DD}	Power		Core supply pins.
10, 11	XTAL_IN XTAL_OUT	Input		Parallel resonant crystal interface. XTAL_OUT is the output, XTAL_IN is the input.
12	PLL_SEL	Input	Pullup	PLL bypass control pin. LVCMOS/LVTTL interface levels. 0 = Bypass mode 1 = PLL mode (default)
13, 14	FSEL_A0 FSEL_A1	Input	Pulldown	Selects the QAx, nQAx output frequency. LVCMOS/LVTTL interface levels. 00 = 100MHz (default) 01 = 125MHz 10 = 156.25MHz 11 = 312.5MHz
15	CLK	Input	Pulldown	Non-inverting differential clock input.
16	nCLK	Input	Pullup/ Pulldown	Inverting differential clock input. Internal resistor bias to $V_{DD}/2$.
17, 18	FSEL_B0 FSEL_B1	Input	Pulldown	Selects the QBx, nQBx output frequency. LVCMOS/LVTTL interface levels. 00 = 100MHz (default) 01 = 125MHz 10 = 156.25MHz 11 = 312.5MHz
19	V_{DDO_QF}	Power		QF output supply pin (LVCMOS/LVTTL). 3.3V supply.
20	QF	Output		Single-ended output. 3.3V LVCMOS/LVTTL interface levels.
24	V_{DDO_QA}	Power		Bank A (HCSL) output supply pin. 3.3 V supply.
25, 26	QA0, nQA0	Output		Bank A differential output pair. HCSL interface levels.
27, 28	QA1, nQA1	Output		Bank A differential output pair. HCSL interface levels.
30	OE_A	Input	Pullup	Active HIGH output enable for Bank A outputs. LVCMOS/LVTTL interface levels. 0 = Bank A outputs disabled/high impedance 1 = Bank A outputs enabled (default)
31	V_{DDO_QB}	Power		Bank B (HCSL) output supply pin. 3.3V supply.
Continued on next page				
32, 33	QB0, nQB0	Output		Bank B differential output pair. HCSL interface levels.
34, 35	QB1, nQB1	Output		Bank B differential output pair. HCSL interface levels.
37	OE_B	Input	Pullup	Active HIGH output enable for Bank B outputs. LVCMOS/LVTTL interface levels. 0 = Bank B outputs disabled/high impedance 1 = Bank B outputs enabled (default)
38	V_{DDO_QC}	Power		Bank C (HCSL) output supply pin. 3.3V supply.

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Table 1. Pin Descriptions (Continued)

Number	Name	Type		Description
39, 40	QC0, nQC0	Output		Bank C differential output pair. HCSL interface levels.
41, 42	QC1, nQC1	Output		Bank C differential output pair. HCSL interface levels.
44	OE_C	Input	Pullup	Active HIGH output enable for Bank C outputs. LVCMOS/LVTTL interface levels. 0 = Bank C outputs disabled/high impedance 1 = Bank C outputs enabled (default)
46	V_{DDO_QD}	Power		Bank D (HCSL) output supply pin. 3.3V supply.
47, 48	QD0, nQD0	Output		Bank D differential output pair. HCSL interface levels.
49, 50	QD1, nQD1	Output		Bank D differential output pair. HCSL interface levels.
52	OE_D	Input	Pullup	Active HIGH output enable for Bank D outputs. LVCMOS/LVTTL interface levels. 0 = Bank D outputs disabled/high impedance 1 = Bank D outputs active (default)
53	I_{REF}	Input		External fixed precision resistor (475Ω) from this pin to ground provides a reference current used for differential current-mode.
54	V_{DDO_QE}	Power		Bank E (HCSL) output supply pin. 3.3V supply.
55, 56	QE0, nQE0	Output		Bank E differential output pair. HCSL interface levels.
57, 58	QE1, nQE1	Output		Bank E differential output pair. HCSL interface levels.
60	OE_E	Input	Pullup	Active HIGH output enable for Bank E outputs. LVCMOS/LVTTL interface levels. 0 = Bank E outputs disabled/high impedance 1 = Bank E outputs enabled (default)
61, 62	FSEL_C0 FSEL_C1	Input	Pulldown	Selects the QCx, nQCx output frequency. LVCMOS/LVTTL interface levels. 00 = 100MHz (default) 01 = 125MHz 10 = 156.25MHz 11 = 312.5MHz
64	V_{DDA}	Power		Analog supply pin.
65, 66	FSEL_D0 FSEL_D1	Input	Pulldown	Selects the QDx, nQDx output frequency. LVCMOS/LVTTL interface levels. 00 = 100MHz (default) 01 = 125MHz 10 = 156.25MHz 11 = 312.5MHz
68	nMR	Input	Pulldown	Active LOW Master Reset. LVCMOS/LVTTL interface levels. 0 = Reset. The internal dividers are reset causing the true outputs Qx to go low and the inverted outputs nQx to go high. (default) 1 = Active. The internal dividers and the outputs are active.
69	V_{DDO_QG}	Power		QG output supply pins (LVCMOS/LVTTL). 3.3V or 2.5V supply.

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Table 1. Pin Descriptions (Continued)

Number	Name	Type		Description
70	QG	Output		Bank G single-ended output. 3.3V or 2.5V LVCMOS/LVTTL interface levels.
72	OE_G	Input	Pullup	Active HIGH output enable for Bank G output. LVCMOS/LVTTL interface levels. 0 = Bank G outputs disabled/high impedance 1 = Bank G outputs enabled (default)
	EPAD			Connect to GND.

Pin Characteristics

Table 2. Pin Characteristics[a]

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
C_{IN}	Input Capacitance	CLK, nCLK			2.5		pF
		Control Pins			6		pF
R_{PULLUP}	Input Pullup Resistor				50		kΩ
$R_{PULLDOWN}$	Input Pulldown Resistor				50		kΩ
R_{OUT}	Output Impedance	QF, QG, QREF[1:0]	$V_{DDO\_QF} = V_{DDO\_QG} = V_{DDO\_QREF} = 3.465V$		15		W
		QG, QREF[1:0]	V_{DDO_QREF}, $V_{DDO\_QG} = 2.625V$		19		W

[a] *Pullup* and *Pulldown* refer to internal input resistors. For typical values, see Table 2.

Function Tables

Table 3. FSEL_X Control Input Function Table[a][b]

Input	Output Frequency
FSEL_X[1:0]	**Q[Ax:Ex], nQ[Ax:Ex]**
00 (default)	100MHz
01	125MHz
10	156.25MHz
11	312.50MHz

[a] FSEL_X denotes FSEL_A, _B, _C, _D, _E.

[b] Any two outputs operated at the same frequency will be synchronous.

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Table 4. PLL_SEL Control Input Function Table

Input	
PLL_SEL	Operation
0	PLL Bypass
1 (default)	PLL Mode

Table 5. REF_SEL Control Input Function Table

Input	
REF_SEL	Clock Source
0	CLK, nCLK
1 (default)	XTAL_IN, XTAL_OUT

Table 6. OE_[A:E] Control Input Function Table

Input	Outputs
OE_[A:E]	Q[Ax:Ex], nQ[Ax:Ex]
0	High-Impedance
1 (default)	Enabled

Table 7. OE_G Control Input Function Table

Input	Outputs
OE_G	QG
0	High-Impedance
1 (default)	Enabled

Table 8. OE_REF Control Input Function Table

Input	Output
OE_REF	QREF[1:0]
0	High-Impedance
1 (default)	Enabled

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Absolute Maximum Ratings

Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only. Functional operation of product at these conditions or any conditions beyond those listed in the *DC Characteristics or AC Characteristics* is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Table 9. Absolute Maximum Ratings

Item	Rating
Supply Voltage, V_{DD}	3.6V
Inputs, V_I XTAL_IN Other Inputs	 0V to 2V -0.5V to V_{DD} + 0.5V
Outputs, V_O	-0.5V to V_{DDO_QX} + 0.5V
Package Thermal Impedance, θ_{JA}	26.6°C/W (0 mps)
Storage Temperature, T_{STG}	-65°C to 150°C

DC Electrical Characteristics

Table 10. Power Supply DC Characteristics (V_{DD} = 3.3V ±5%, $V_{DDO\_Q[A:E]}$ = $V_{DDO\_Q[F:G]}$ = V_{DDO_QREF} = 3.3V ±5%, T_A = -40°C to 85°C)[a] [b]

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		3.135	3.3	3.465	V
V_{DDA}	Analog Supply Voltage		VDD - 0.81	3.3	V_{DD}	V
V_{DDO_QX}	Output Supply Voltage		3.135	3.3	3.465	V
I_{DD}	Power Supply Current			193	235	mA
I_{DDA}	Analog Supply Current			36	45	mA
I_{DDO_QX}	Output Supply Current	No Load		24	30	mA

[a] V_{DDO_QX} denotes $V_{DDO\_Q[A:E]}$, $V_{DDO\_Q[F:G]}$, V_{DDO_QREF}.

[b] I_{DDO_QX} denotes $I_{DDO\_Q[A:E]}$ + $I_{DDO\_Q[F:G]}$ + I_{DDO_QREF}.

Table 11. Power Supply DC Characteristics (V_{DD} = VDDO_Q[A:E] = VDDO_QF = 3.3V ±5%, V_{DDO_QG} = V_{DDO_QREF} = 2.5V ± 5%, T_A = -40°C to 85°C)

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	Units
V_{DD}	Core Supply Voltage		3.135	3.3	3.465	V
V_{DDA}	Analog Supply Voltage		2.6	3.3	V_{DD}	V
V_{DDO_QG}/ V_{DDO_QREF}	Output Supply Voltage		2.375	2.5	2.625	V
I_{DD}	Power Supply Current			193	235	mA
I_{DDA}	Analog Supply Current			36	45	mA
I_{DDO_QG} + IDDO_QREF	Output Supply Current	No Load		8	15	mA

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Table 12. LVCMOS/LVTTL DC Characteristics (V_{DD} = $V_{DDO\_Q[A:E]}$ = V_{DDO_QF} = 3.3V ± 5%; V_{DDO_QG} = V_{DDO_QREF} = 3.3V ± 5% or 2.5V ± 5%, T_A = -40°C to 85°C)

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
V_{IH}	Input High Voltage			2.2		V_{DD} + 0.3	V
V_{IL}	Input Low Voltage			-0.3		0.8	V
I_{IH}	Input High Current	nMR, FSEL_A[1:0], FSEL_B[1:0], FSEL_C[1:0], FSEL_D[1:0], FSEL_E[1:0]	V_{DD} = V_{IN} = 3.465V			150	µA
		REF_SEL, PLL_SEL, OE_REF, OE_A, OE_B, OE_C, OE_D, OE_E, OE_G	V_{DD} = V_{IN} = 3.465V			10	uA
I_{IL}	Input Low Current	nMR, FSEL_A[1:0], FSEL_B[1:0], FSEL_C[1:0], FSEL_D[1:0], FSEL_E[1:0]	V_{DD} = 3.465V, V_{IN} = 0V	-10			µA
		REF_SEL, PLL_SEL, OE_REF, OE_A, OE_B, OE_C, OE_D, OE_E, OE_G	V_{DD} = 3.465V, V_{IN} = 0V	-150			uA
V_{OH}	Output High Voltage		V_{DDO_QF} = V_{DDO_QG}, V_{DDO_QREF} = 3.465V	2.6			V
			V_{DDO_QG}, V_{DDO_QREF} = 2.625V	1.8			V
V_{OL}	Output Low Voltage		V_{DDO_QF} = V_{DDO_QG}, V_{DDO_QREF} = 3.465V or V_{DDO_QG}, V_{DDO_QREF} = 2.625V			0.6	V

Table 13. Differential DC Characteristics, V_{DD} = 3.3V ± 5%, T_A = -40°C to 85°C[a][b]

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
I_{IH}	Input High Current	CLK, nCLK	V_{DD} = V_{IN} = 3.465V			150	µA
I_{IL}	Input Low Current	CLK	V_{DD} = 3.465V, V_{IN} = 0V	-5			µA
		nCLK	V_{DD} = 3.465V, V_{IN} = 0V	-150			µA
V_{PP}	Peak-to-Peak Input Voltage; NOTE 1			0.15		1.3	V
V_{CMR}	Common Mode Input Voltage; NOTE 1, 2			0.5		V_{DD} – 0.85	V

[a] V_{IL} should not be less than -0.3V.

[b] Common mode voltage is defined as V_{IH}.

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Table 14. Crystal Characteristics

Parameter	Test Conditions	Minimum	Typical	Maximum	Units
Mode of Oscillation			Fundamental		
Frequency			25		MHz
Equivalent Series Resistance (ESR)				50	W
Load Capacitance (CL)			12		pF
Shunt Capacitance				7	pF

Table 15. Input Frequency Characteristics (V_{DD} = $V_{DDO\_Q[A:E]}$ = V_{DDO_QF} = 3.3V ± 5%; V_{DDO_QG} = V_{DDO_QREF} = 3.3V ± 5% or 2.5V ± 5%, T_A = -40°C to 85°C)

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
F_{IN}	Input Frequency	CLK, nCLK			25		MHz
		XTAL_IN, XTAL_OUT			25		MHz

AC Electrical Characteristics

Table 16. PCI Express Jitter Specifications (V_{DD} = $V_{DDO\_Q[A:E]}$ = 3.3V ± 5%, T_A = -40°C to 85°C)

Symbol	Parameter	Test Conditions	Minimum	Typical	Maximum	PCIe Industry Spec.	Units
t_j (PCIe Gen 1)	Phase Jitter Peak-to-Peak; NOTE 1, 4	*f* = 100MHz, 25MHz Crystal Input Evaluation Band: 0Hz - Nyquist (clock frequency/2)		8.07	13.7	86	ps
$t_{REFCLK\_HF\_RMS}$ (PCIe Gen 2)	Phase Jitter RMS; NOTE 2, 4	*f* = 100MHz, 25MHz Crystal Input High Band: 1.5MHz - Nyquist (clock frequency/2)		0.95	2.17	3.10	ps
$t_{REFCLK\_LF\_RMS}$ (PCIe Gen 2)	Phase Jitter RMS; NOTE 2, 4	*f* = 100MHz, 25MHz Crystal Input Low Band: 10kHz - 1.5MHz		0.05	0.10	3.0	ps
t_{REFCLK_RMS} (PCIe Gen 3)	Phase Jitter RMS; NOTE 3, 4	*f* = 100MHz, 25MHz Crystal Input Evaluation Band: 0Hz - Nyquist (clock frequency/2)		0.24	0.57	0.8	ps

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions. For additional information, refer to the *PCI Express Application Note section* in the datasheet.
NOTE 1: Peak-to-Peak jitter after applying system transfer function for the Common Clock Architecture. Maximum limit for PCI Express Gen 1 is 86ps peak-to-peak for a sample size of 10^6 clock periods.
NOTE 2: RMS jitter after applying the two evaluation bands to the two transfer functions defined in the Common Clock Architecture and reporting the worst case results for each evaluation band. Maximum limit for PCI Express Generation 2 is 3.1ps RMS for $t_{REFCLK\_HF\_RMS}$ (High Band) and 3.0ps RMS for $t_{REFCLK\_LF\_RMS}$ (Low Band).
NOTE 3: RMS jitter after applying system transfer function for the common clock architecture. This specification is based on the PCI Express Base Specification *Revision 0.7, October 2009* and is subject to change pending the final release version of the specification.
NOTE 4: This parameter is guaranteed by characterization. Not tested in production.

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Table 17. HCSL AC Characteristics (V_{DD} = $V_{DDO\_Q[A:E]}$ = V_{DDO_QF} = 3.3V ± 5%; V_{DDO_QG} = V_{DDO_QREF} = 3.3V ± 5% or 2.5V ± 5%, T_A = -40°C to 85°C)

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency	Q[A:E], nQ[A:E]	FSEL_x[1:0] = 00		100		MHz
			FSEL_x[1:0] = 01		125		MHz
			FSEL_x[1:0] = 10		156.25		MHz
			FSEL_x[1:0] = 11		312.5		MHz
V_{RB}	Ring-Back Voltage Margin; NOTE 1, 2	Q[A:E], nQ[A:E]		-100		100	mV
t_{STABLE}	Time before V_{RB} is allowed; NOTE 1, 2	Q[A:E], nQ[A:E]		500			ps
V_{MAX}	Absolute Max Output Voltage; NOTE 3, 4	Q[A:E], nQ[A:E]				1150	mV
V_{MIN}	Absolute Min Output Voltage; NOTE 3, 5	Q[A:E], nQ[A:E]		-300			mV
V_{CROSS}	Absolute Crossing Voltage; NOTE 3, 6, 7	Q[A:E], nQ[A:E]		175		550	mV
ΔV_{CROSS}	Total Variation of V_{CROSS} over All Edges; NOTE 3, 6, 8	Q[A:E], nQ[A:E]				140	mV
t_{SLEW+}	Rising Edge Rate; NOTE 1, 9	Q[A:E], nQ[A:E]		0.6		4.0	V/ns
t_{SLEW-}	Falling Edge Rate; NOTE 1, 9	Q[A:E], nQ[A:E]		0.6		4.0	V/ns
odc	Output Duty Cycle	Q[A:E], nQ[A:E]		45	50	55	%
tjit(Ø)	RMS Phase Jitter, (Random); NOTE 10	Q[A:E], nQ[A:E]	100MHz, Integration Range: (12kHz to 20MHz)		0.32	0.45	ps
			125MHz, Integration Range: (12kHz to 20MHz)		0.31	0.45	ps
			156.25MHz, Integration Range: (12kHz to 20MHz)		0.30	0.45	ps
			312.5MHz, Integration Range: (12kHz to 20MHz)		0.29	0.45	ps

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
NOTE: All parameters measured at f_{OUT} and in PLL mode unless noted otherwise.
NOTE 1: Measurement taken from differential waveform.
NOTE 2: t_{STABLE} is the time the differential clock must maintain a minimum ±150mV differential voltage after rising/falling edges before it is allowed to drop back into the V_{RB} ±100mV range. See Parameter Measurement Information Section.
NOTE 3: Measurement taken from single-ended waveform.
NOTE 4: Defined as the maximum instantaneous voltage including overshoot. See Parameter Measurement Information Section.

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NOTE 5: Defined as the minimum instantaneous voltage including undershoot. See Parameter Measurement Information Section.
NOTE 6: Measured at the crossing point where the instantaneous voltage value of the rising edge of Q[Ax:Ex] equals the falling edge of nQ[Ax:Ex].
NOTE 7: Refers to the total variation from the lowest crossing point to the highest, regardless of which edge is crossing. Refers to all crossing points for this measurement.
NOTE 8: Defined as the total variation of all crossing voltages of rising Q[Ax:Ex] and falling nQ[Ax:Ex]. This is the maximum allowed variance in Vcross for any particular system.
NOTE 9: Measured from -150mV to +150mV on the differential waveform (derived from Q[Ax:Ex] minus nQ[Ax:Ex]). The signal must be monotonic through the measurement region for rise and fall time. The 300mV measurement window is centered on the differential zero crossing.
NOTE 10: Measurements taken with 25MHz XTAL as input source and spur off.

Table 18. LVCMOS AC Characteristics (V_{DD} = $V_{DDO\_Q[A:E]}$ = V_{DDO_QF} = 3.3V ± 5%; V_{DDO_QG} = V_{DDO_QREF} = 3.3V ± 5% or 2.5V ± 5%, T_A = -40°C to 85°C)

Symbol	Parameter		Test Conditions	Minimum	Typical	Maximum	Units
f_{OUT}	Output Frequency	QF			50		MHz
		QG			125		MHz
		QREF[1:0]			25		MHz
tr / tf	Output Rise/Fall Time	QF, QG, QREF[1:0]	20% to 80%	180		760	ps
odc	Output Duty Cycle	QF, QG, QREF[1:0]		46	50	54	%
tjit(Ø)	RMS Phase Jitter, (Random); NOTE 1	QF	50MHz, Integration Range: (12kHz to 20MHz)		0.36	0.48	ps
		QG	125MHz, Integration Range: (12kHz to 20MHz)		0.32	0.43	ps
		QREF[1:0]	25MHz, Integration Range: (12kHz to 5MHz)		0.32	0.40	ps

NOTE: Electrical parameters are guaranteed over the specified ambient operating temperature range, which is established when the device is mounted in a test socket with maintained transverse airflow greater than 500 lfpm. The device will meet specifications after thermal equilibrium has been reached under these conditions.
NOTE: All parameters measured at f_{OUT} and in PLL mode unless noted otherwise.
NOTE 1: Measurements taken with 25MHz XTAL as input source and spur off.

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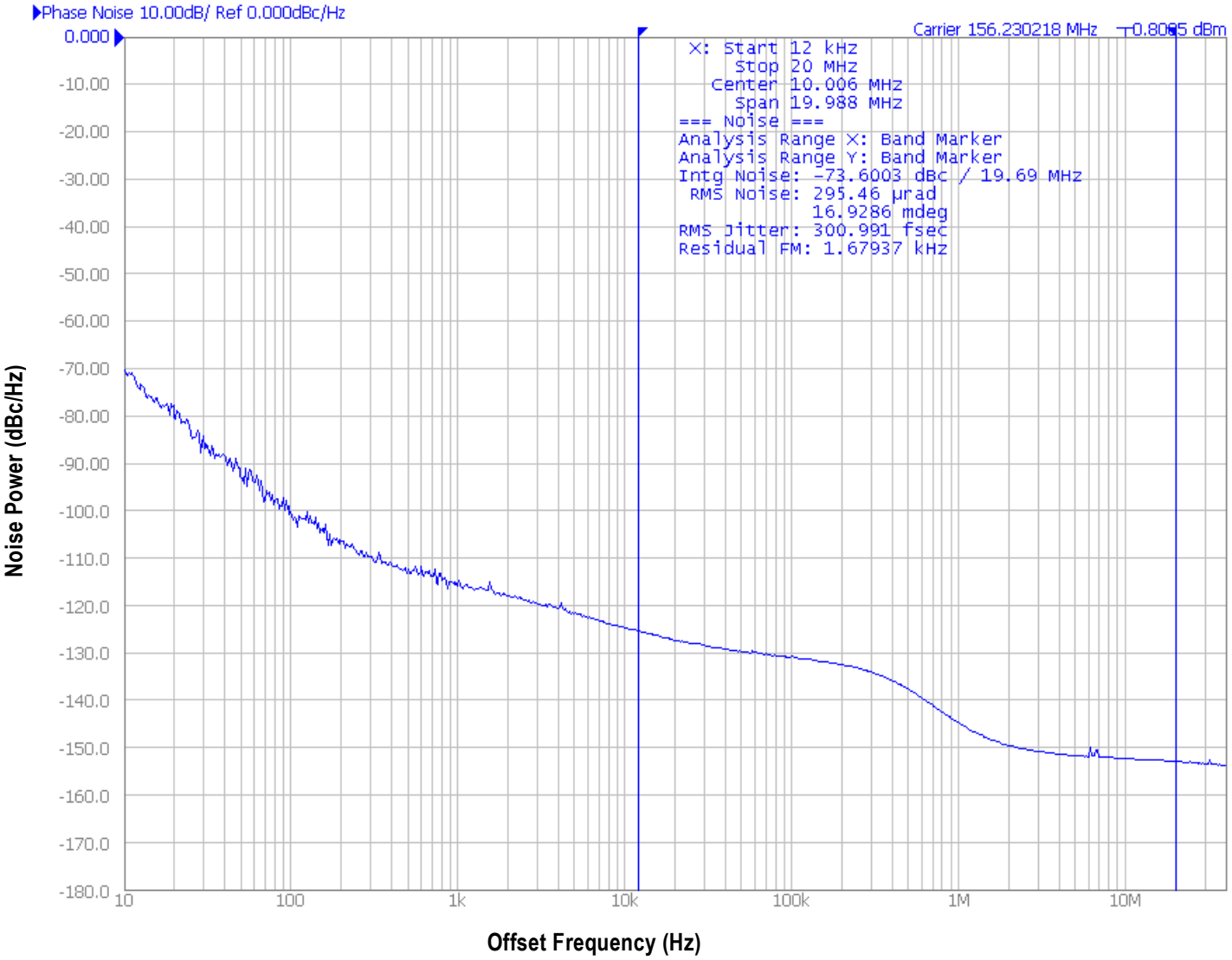
Typical Phase Noise at 156.25MHz



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Parameter Measurement Information

Figure 1. 3.3V Core/3.3V LVCMOS Output Load Test Circuit

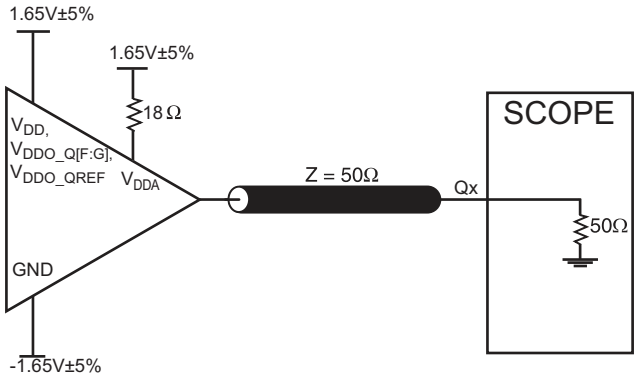
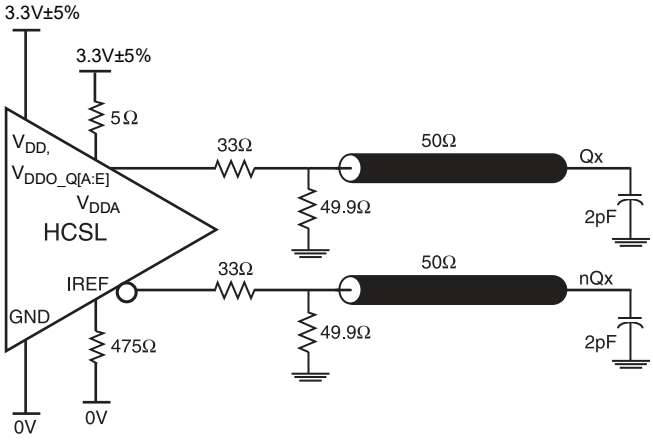


Figure 2. 3.3V Core/3.3V HCSL Output Load Test Circuit 1



This load condition is used for V_{MAX}, V_{MIN}, V_{RB}, t_{STABLE}, V_{CROSS}, ΔV_{CROSS} and $t_{SLEW\pm}$ measurements.

Figure 3. Differential Input Level

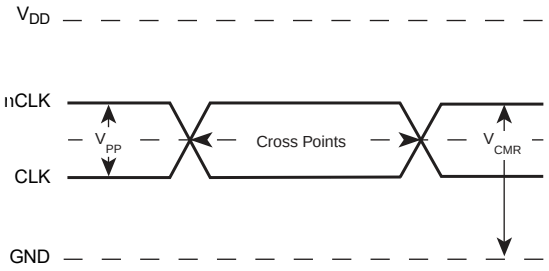


Figure 4. 3.3V Core/2.5V LVCMOS Output Load Test Circuit

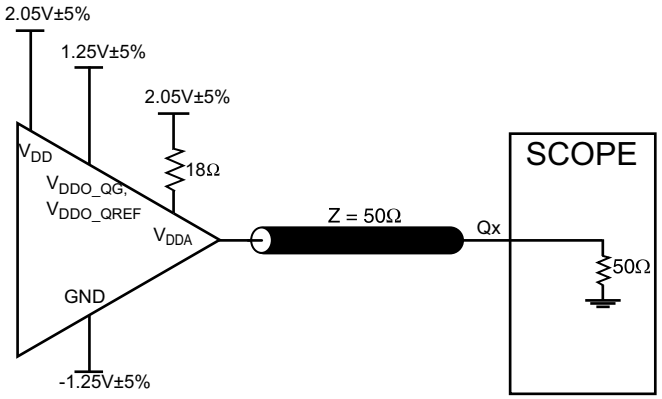
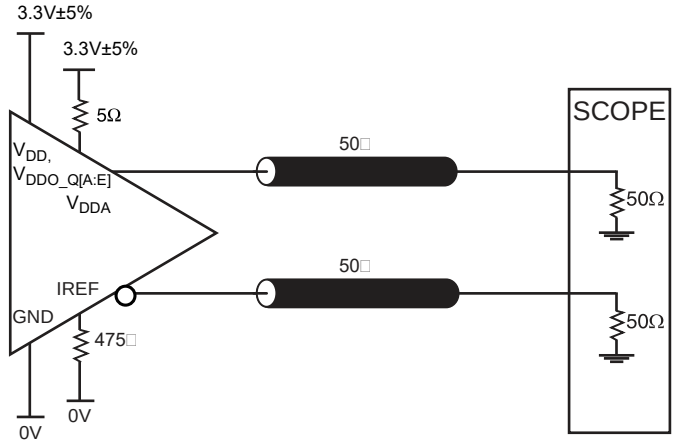
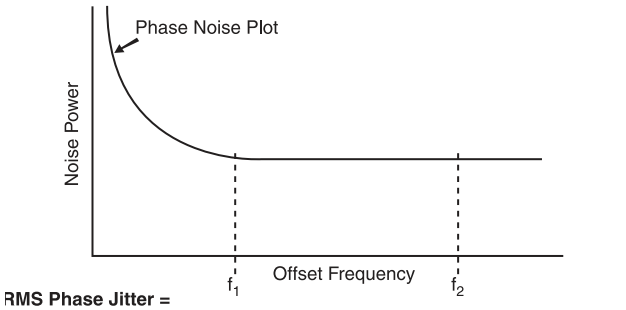


Figure 5. 3.3V Core/3.3V HCSL Output Load Test Circuit 2



This load condition is used for tjit and odc measurements.

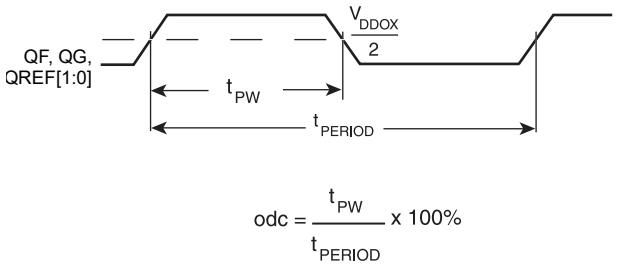
Figure 6. RMS Phase Jitter



RMS Phase Jitter =

$$\frac{1}{\sqrt{2} * \pi * f} * \sqrt{\text{Area Under Curve Defined by the Offset Frequency Markers}}$$

Figure 7. LVCMOS Output Duty Cycle/Pulse Width



$$odc = \frac{t_{PW}}{t_{PERIOD}} \times 100\%$$

Figure 8. Differential Measurement Points for Rise/Fall Time Edge Rate

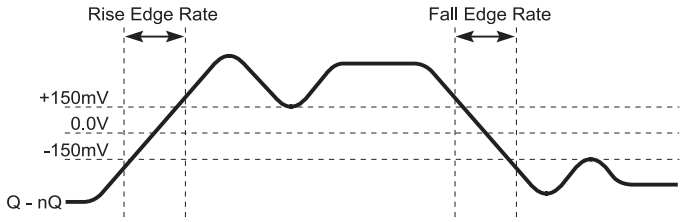


Figure 9. Single-ended Measurement Points for Delta Cross Point

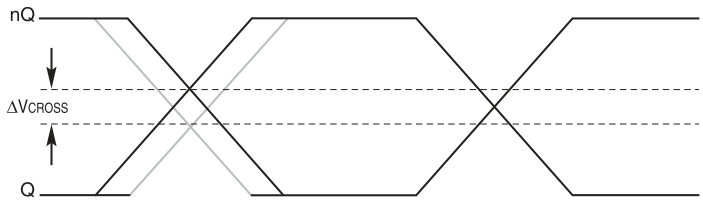


Figure 10. LVCMOS Output Rise/Fall Time

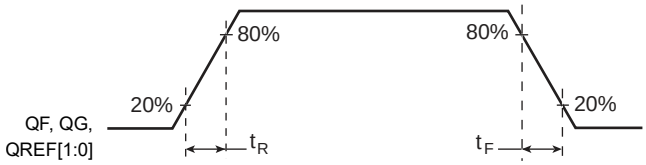


Figure 11. Single-ended Measurement Points for Absolute Cross Point/Swing

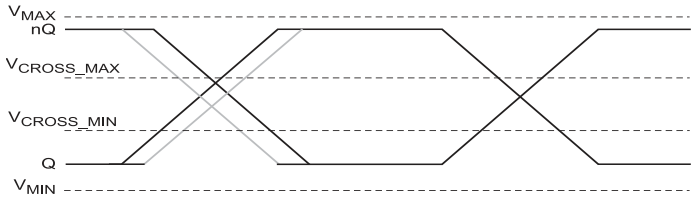


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Figure 12. Differential Measurement Points for Ringback

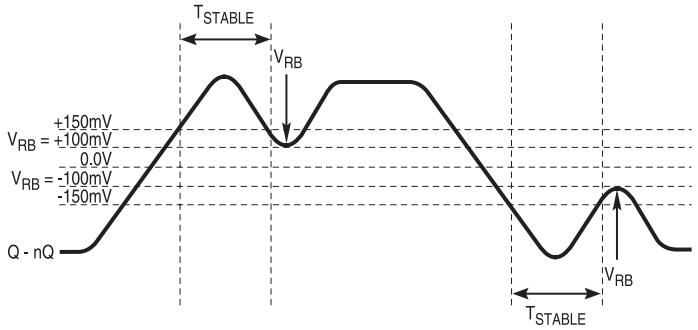
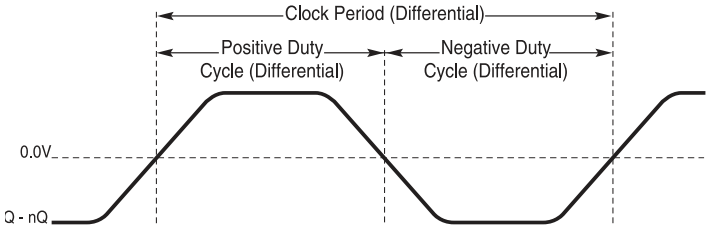


Figure 13. Differential Measurement Points for Duty Cycle/Period

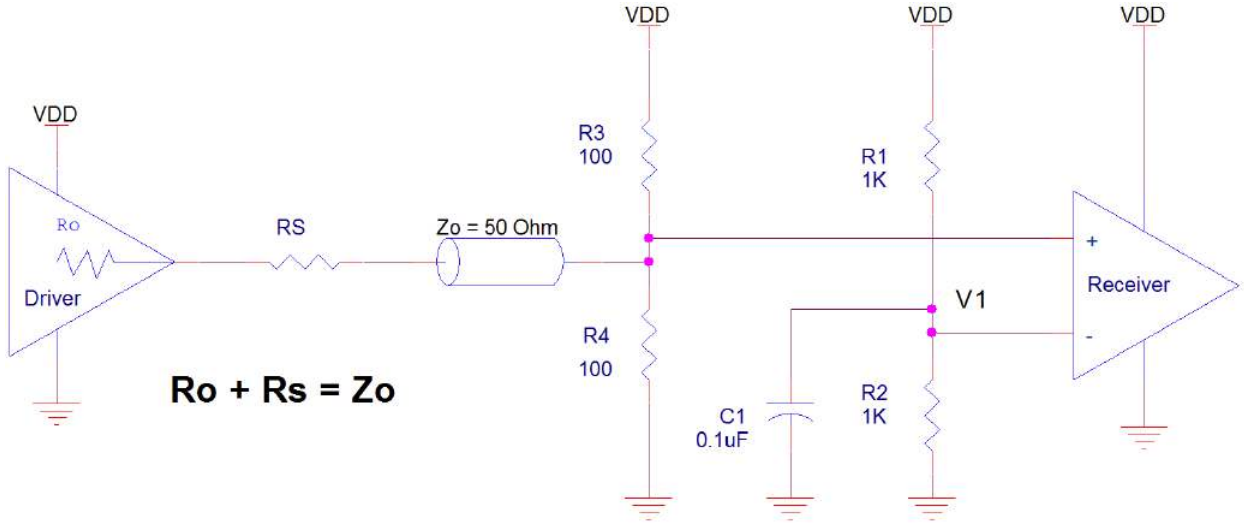


Application Information

Wiring the Differential Input to Accept Single-Ended Levels

Figure 1 shows how a differential input can be wired to accept single ended levels. The reference voltage $V_1 = V_{DD}/2$ is generated by the bias resistors R1 and R2. The bypass capacitor (C1) is used to help filter noise on the DC bias. This bias circuit should be located as close to the input pin as possible. The ratio of R1 and R2 might need to be adjusted to position the V_1 in the center of the input voltage swing. For example, if the input clock is driven from a single-ended 2.5V LVCMOS driver and the DC offset (or swing center) of this signal is 1.25V, the R1 and R2 values should be adjusted to set the V1 at 1.25V. The values below are for when both the single ended swing and V_{DD} are at the same voltage.

Figure 14. Recommended Schematic for Wiring a Differential Input to Accept Single-ended Levels



This configuration requires that the sum of the output impedance of the driver (Ro) and the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the input will attenuate the signal in half. This can be done in one of two ways. First, R3 and R4 in parallel should equal the transmission line impedance. For most 50Ω applications, R3 and R4 can be 100Ω. The values of the resistors can be increased to reduce the loading for slower and weaker LVCMOS driver. When using single-ended signaling, the noise rejection benefits of differential signaling are reduced. Even though the differential input can handle full rail LVCMOS signaling, it is recommended that the amplitude be reduced while maintaining an edge rate faster than 1V/ns. The datasheet specifies a lower differential amplitude, however this only applies to differential signals. For single-ended applications, the swing can be larger, however V_{IL} cannot be less than -0.3V and V_{IH} cannot be more than V_{DD} + 0.3V. Though some of the recommended components might not be used, the pads should be placed in the layout. They can be utilized for debugging purposes. The datasheet specifications are characterized and guaranteed by using a differential signal.

Differential Clock Input Interface

The CLK /nCLK accepts LVDS, LVPECL, LVHSTL, HCSL and other differential signals. Both V_{SWING} and V_{OH} must meet the V_{PP} and V_{CMR} input requirements. Figure 15 to Figure 19 show interface examples for the CLK/nCLK input driven by the most common driver types. The input interfaces suggested here are examples only. Please consult with the vendor of the driver component to confirm the driver termination requirements. For example, in Figure 15, the input termination applies for IDT open emitter LVHSTL drivers. If you are using an LVHSTL driver from another vendor, use their termination recommendation.

Figure 15. CLK/nCLK Input Driven by an IDT Open Emitter LVHSTL Driver

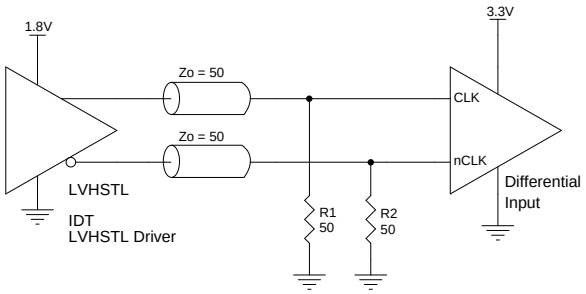


Figure 16. CLK/nCLK Input Driven by a 3.3V LVPECL Driver

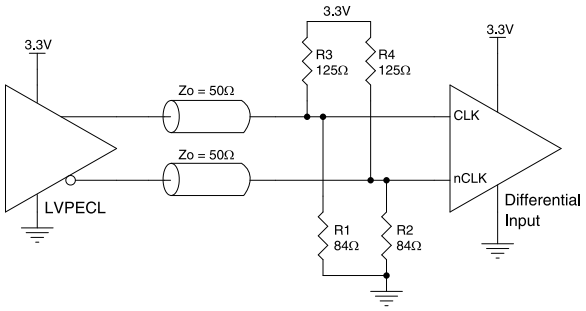


Figure 17. CLK/nCLK Input Driven by a 3.3V LVDS Driver

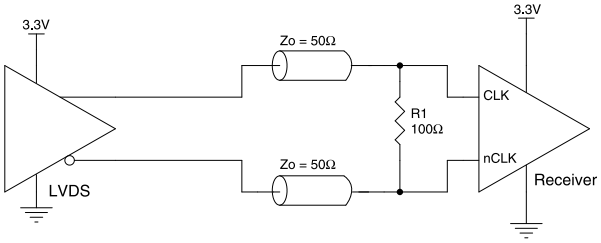


Figure 18. CLK/nCLK Input Driven by a 3.3V LVPECL Driver

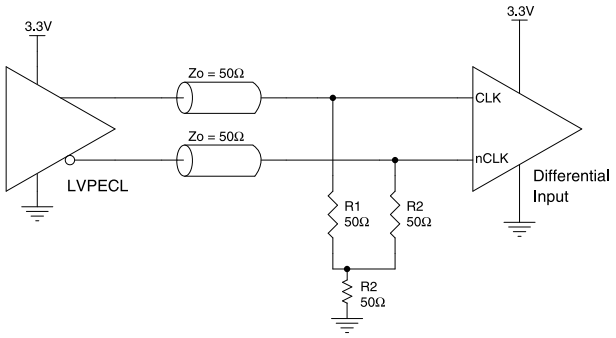
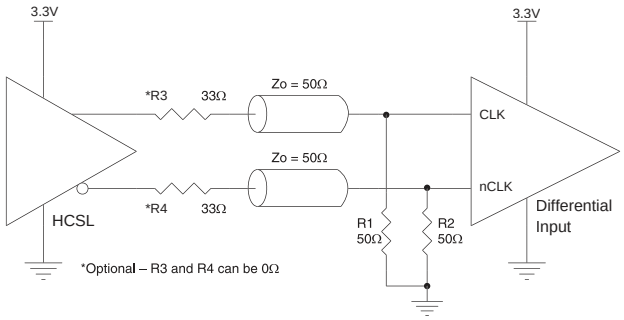


Figure 19. CLK/nCLK Input Driven by a 3.3V HCSL Driver



Overdriving the XTAL Interface

The XTAL_IN input can be overdriven by an LVCMOS driver or by one side of a differential driver through an AC coupling capacitor. The XTAL_OUT pin can be left floating. The amplitude of the input signal should be between 500mV and 1.8V and the slew rate should not be less than 0.2V/nS. For 3.3V LVCMOS inputs, the amplitude must be reduced from full swing to at least half the swing in order to prevent signal interference with the power rail and to reduce internal noise. Figure 20 shows an example of the interface diagram for a high speed 3.3V LVCMOS driver. This configuration requires that the sum of the output impedance of the driver (Ro) and the series resistance (Rs) equals the transmission line impedance. In addition, matched termination at the crystal input will attenuate the signal in half. This can be done in one of two ways.

First, R1 and R2 in parallel should equal the transmission line impedance. For most 50Ω applications, R1 and R2 can be 100Ω. This can also be accomplished by removing R1 and changing R2 to 50Ω. The values of the resistors can be increased to reduce the loading for a slower and weaker LVCMOS driver. Figure 21 shows an example of the interface diagram for an LVPECL driver. This is a standard LVPECL termination with one side of the driver feeding the XTAL_IN input. It is recommended that all components in the schematics be placed in the layout. Though some components might not be used, they can be utilized for debugging purposes. The datasheet specifications are characterized and guaranteed by using a quartz crystal as the input.

Figure 20. General Diagram for LVCMOS Driver to XTAL Input Interface

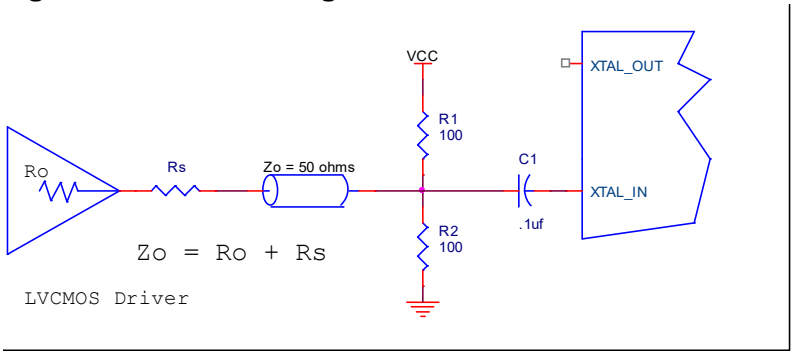
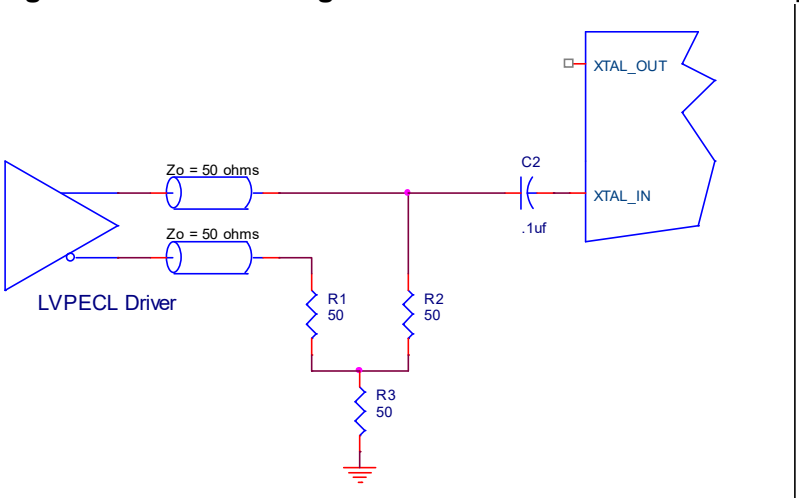


Figure 21. General Diagram for LVPECL Driver to XTAL Input Interface



Recommended Termination

Figure 22 is the recommended source termination for applications where the driver and receiver will be on a separate PCBs. This termination is the standard for PCI Express™ and HCSL output types. All traces should be 50Ω impedance single-ended or 100Ω differential.

Figure 22. Recommended Source Termination (where the driver and receiver will be on separate PCBs)

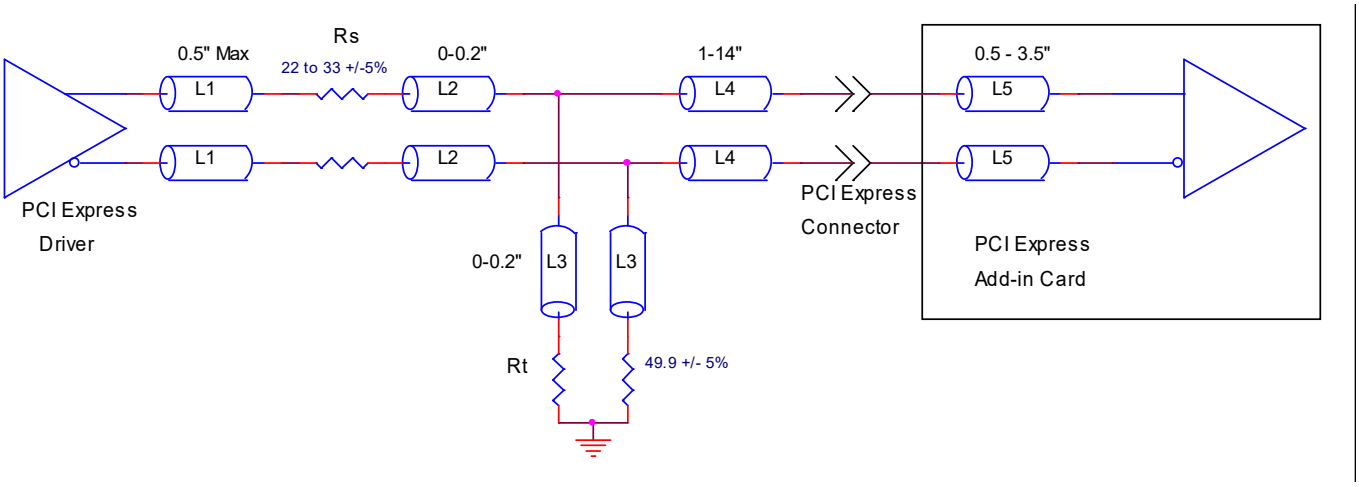
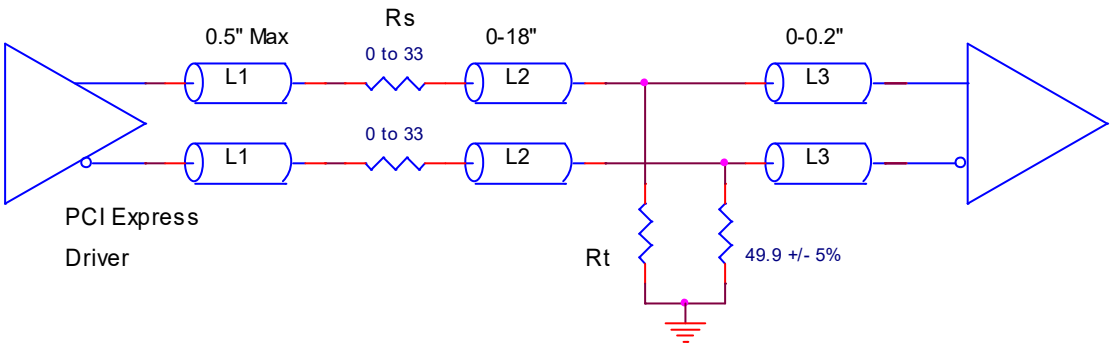


Figure 23 is the recommended termination for applications where a point-to-point connection can be used. A point-to-point connection contains both the driver and the receiver on the same PCB. With a matched termination at the receiver, transmission-line reflections will be minimized. In addition, a series resistor (Rs) at the driver offers flexibility and can help dampen unwanted reflections. The optional resistor can range from 0Ω to 33Ω. All traces should be 50Ω impedance single-ended or 100Ω differential.

Figure 23. Recommended Termination (where a point-to-point connection can be used)

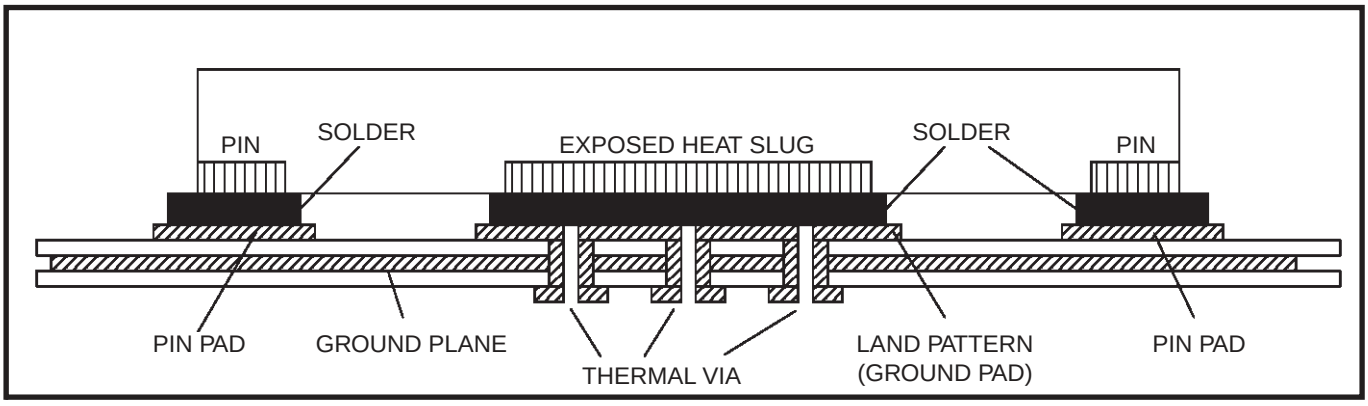


VFQFPN EPAD Thermal Release Path

In order to maximize both the removal of heat from the package and the electrical performance, a land pattern must be incorporated on the Printed Circuit Board (PCB) within the footprint of the package corresponding to the exposed metal pad or exposed heat slug on the package, as shown in Figure 24. The solderable area on the PCB, as defined by the solder mask, should be at least the same size/shape as the exposed pad/slug area on the package to maximize the thermal/electrical performance. Sufficient clearance should be designed on the PCB between the outer edges of the land pattern and the inner edges of pad pattern for the leads to avoid any shorts.

While the land pattern on the PCB provides a means of heat transfer and electrical grounding from the package to the board through a solder joint, thermal vias are necessary to effectively conduct from the surface of the PCB to the ground plane(s). The land pattern must be connected to ground through these vias. The vias act as “heat pipes”. The number of vias (i.e. “heat pipes”) are application specific and dependent upon the package power dissipation as well as electrical conductivity requirements. Thus, thermal and electrical analysis and/or testing are recommended to determine the minimum number needed. Maximum thermal and electrical performance is achieved when an array of vias is incorporated in the land pattern. It is recommended to use as many vias connected to ground as possible. It is also recommended that the via diameter should be 12 to 13mils (0.30 to 0.33mm) with 1oz copper via barrel plating. This is desirable to avoid any solder wicking inside the via during the soldering process which may result in voids in solder between the exposed pad/slug and the thermal land. Precautions should be taken to eliminate any solder voids between the exposed heat slug and the land pattern. Note: These recommendations are to be used as a guideline only. For further information, please refer to the Application Note on the Surface Mount Assembly of Amkor’s Thermally/ Electrically Enhance Leadframe Base Package, Amkor Technology.

Figure 24. P.C. Assembly for Exposed Pad Thermal Release Path – Side View (drawing not to scale)



Recommendations for Unused Input and Output Pins

Inputs

LVCMOS Control Pins

All control pins have internal pullups or pulldowns; additional resistance is not required but can be added for additional protection. A 1kΩ resistor can be used.

Crystal Inputs

For applications not requiring the use of the crystal oscillator input, both XTAL_IN and XTAL_OUT can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from XTAL_IN to ground.

CLK/nCLK Inputs

For applications not requiring the use of the differential input, both CLK and nCLK can be left floating. Though not required, but for additional protection, a 1kΩ resistor can be tied from CLK to ground.

Outputs

LVCMOS Outputs

All unused LVCMOS outputs can be left floating. There should be no trace attached.

Differential Outputs

All unused differential outputs can be left floating. We recommend that there is no trace attached. Both sides of the differential output pair should either be left floating or terminated.

PCI Express Application Information

PCI Express jitter analysis methodology models the system response to reference clock jitter. The block diagram below shows the most frequently used *Common Clock Architecture* in which a copy of the reference clock is provided to both ends of the PCI Express Link.

In the jitter analysis, the transmit (Tx) and receive (Rx) serdes PLLs are modeled as well as the phase interpolator in the receiver. These transfer functions are called H1, H2, and H3 respectively. The overall system transfer function at the receiver is:

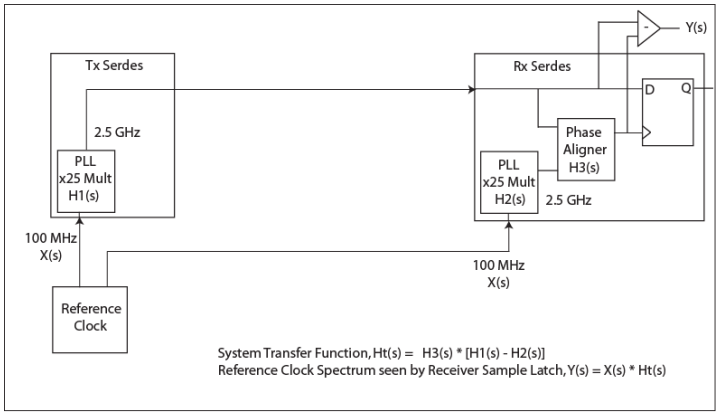
$$Ht(s) = H3(s) \times [H1(s) - H2(s)]$$

The jitter spectrum seen by the receiver is the result of applying this system transfer function to the clock spectrum X(s) and is:

$$Y(s) = X(s) \times H3(s) \times [H1(s) - H2(s)]$$

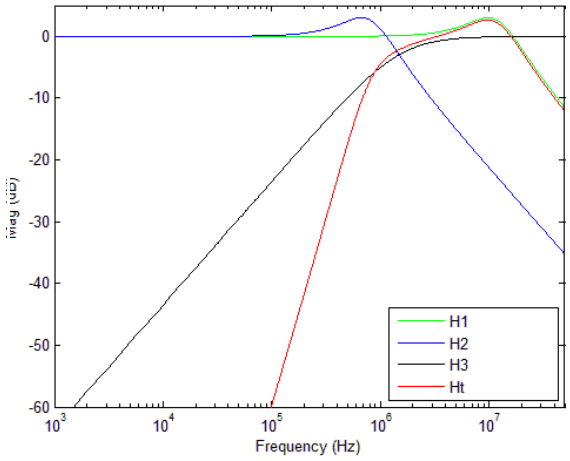
In order to generate time domain jitter numbers, an inverse Fourier Transform is performed on X(s)*H3(s) * [H1(s) - H2(s)].

Figure 25. PCI Express Common Clock Architecture



For **PCI Express Gen 1**, one transfer function is defined and the evaluation is performed over the entire spectrum: DC to Nyquist (e.g for a 100MHz reference clock: 0Hz – 50MHz) and the jitter result is reported in peak-peak.

Figure 26. PCIe Gen 1 Magnitude of Transfer Function



For **PCI Express Gen 2**, two transfer functions are defined with 2 evaluation ranges and the final jitter number is reported in RMS. The two evaluation ranges for PCI Express Gen 2 are 10kHz – 1.5MHz (Low Band) and 1.5MHz – Nyquist (High Band). The plots show the individual transfer functions as well as the overall transfer function Ht.

Figure 27. PCIe Gen 2A Magnitude of Transfer Function

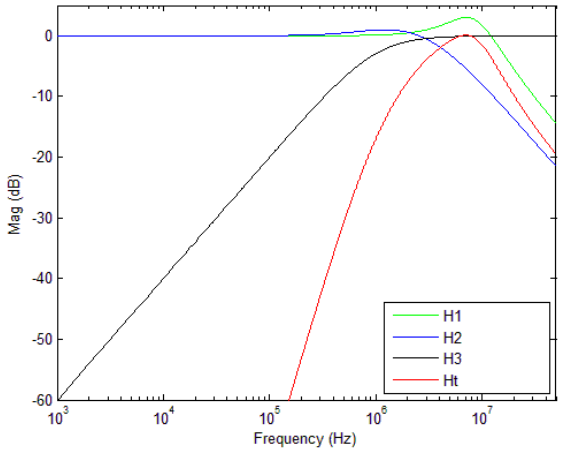
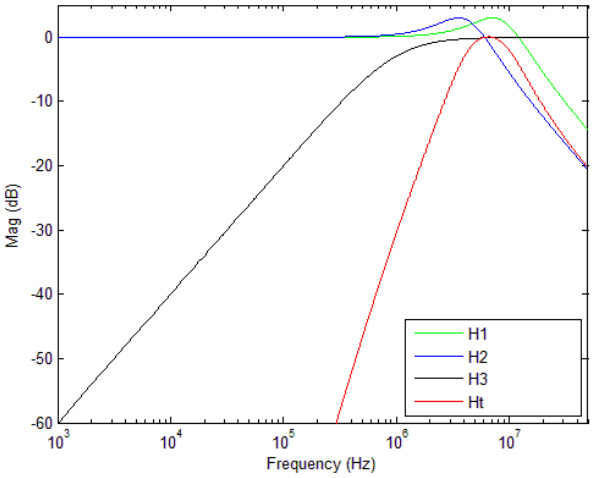
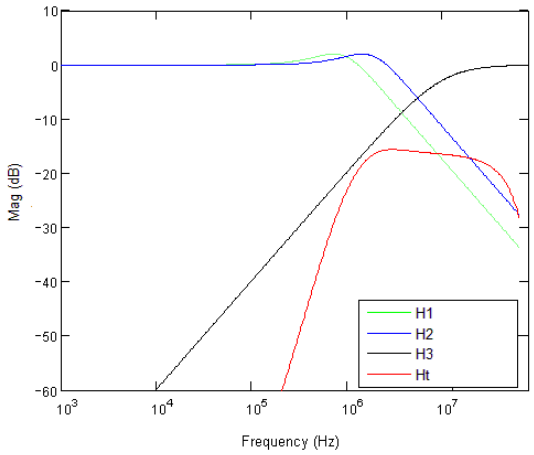


Figure 28. PCIe Gen 2B Magnitude of Transfer Function



For **PCI Express Gen 3**, one transfer function is defined and the evaluation is performed over the entire spectrum. The transfer function parameters are different from Gen 1 and the jitter result is reported in RMS.

Figure 29. PCIe Gen 3 Magnitude of Transfer Function



For a more thorough overview of PCI Express jitter analysis methodology, please refer to IDT Application Note *PCI Express Reference Clock Requirements.*

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Schematic Example

Figure 30 shows an example of 8V41N012A application schematic. In this example, the device is operated at V_{DD} = V_{DDA} = V_{DDO_Qx} = 3.3V. The schematic example focuses on functional connections and is not configuration specific. Refer to the pin description and functional tables in the datasheet to ensure that the logic control inputs are properly set.

A 12pF parallel resonant 25MHz crystal is used. For this device, the crystal load capacitors are required for proper operation. The load capacitance, C1 = C2 = 2pF, are recommended for frequency accuracy. Depending on the variation of the parasitic stray capacity of the printed circuit board traces between the crystal and the Xtal_In and Xtal_Out pins, the values of C1 and C2 might require a slight adjustment to optimize the frequency accuracy. Crystals with other load capacitance specifications can be used, but this will require adjusting C1 and C2. When designing the circuit board, return the capacitors to ground though a single point contact close to the package. Two Fox crystal options are shown in the schematic for design flexibility.

The ePAD provides a low thermal impedance connection between the internal device and the PCB. It also provides an electrical connection to the die and must be connected to ground.

As with any high speed analog circuitry, the power supply pins are vulnerable to random noise. To achieve optimum jitter performance, power supply isolation is required. The 8V41N012A provides separate power supplies to isolate any high switching noise from coupling into the internal PLL.

In order to achieve the best possible filtering, it is recommended that the placement of the filter components be on the device side of the PCB as close to the power pins as possible. If space is limited, the 0.1µF capacitor in each power pin filter should be placed on the device side. The other components can be on the opposite side of the PCB.

Power supply filter recommendations are a general guideline to be used for reducing external noise from coupling into the devices. The filter performance is designed for a wide range of noise frequencies. This low-pass filter starts to attenuate noise at approximately 10kHz. If a specific frequency noise component is known, such as switching power supplies frequencies, it is recommended that component values be adjusted and if required, additional filtering be added. Additionally, good general design practices for power plane voltage stability suggests adding bulk capacitance in the local area of all devices.

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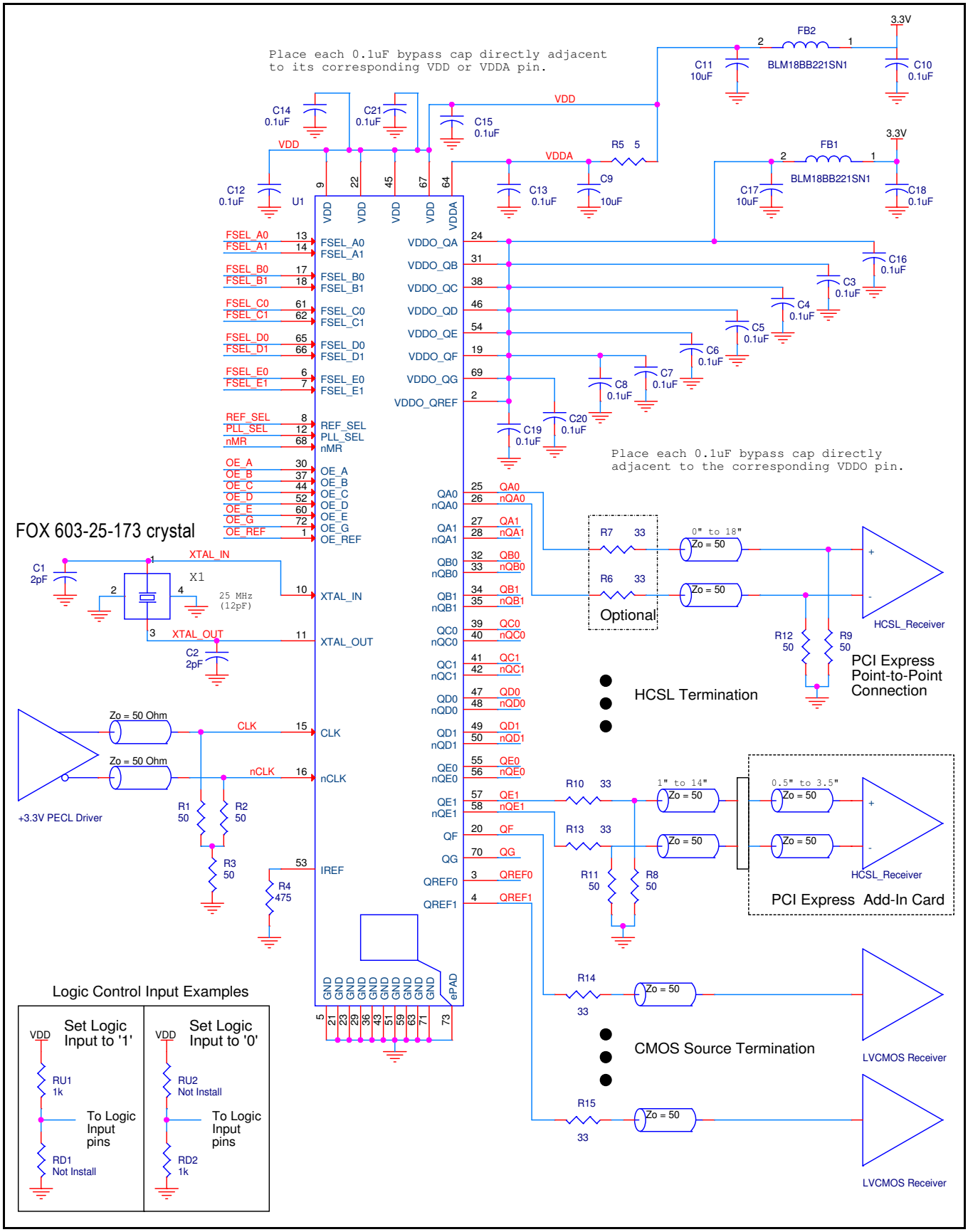
Figure 30. 8V41N012A Schematic Example



Power Considerations

This section provides information on power dissipation and junction temperature for the 8V41N012A. Equations and example calculations are also provided.

1. Power Dissipation.

The total power dissipation for the 8V41N012A is the sum of the core power plus the analog power plus the power dissipated due to loading.
The following is the power dissipation for V_{DD} = 3.3V + 5% = 3.465V, which gives worst case results.

NOTE: Please refer to Section 3 for details on calculating power dissipated due to loading.

- Power $(core)_{MAX}$ = V_{DD_MAX} * (I_{DD} + I_{DDA})= 3.465V * (235mA + 45mA) = **970.2mW**
- Power $(HCSL)_{MAX}$ = (3.465V – 17mA * 50) 17mA = **44.5mW** per output
- Total Power $(HCSL)_{MAX}$ = 44.5mW * 10 = **445mW**

LVCMOS Driver Power Dissipation

- Output Impedance R_{OUT} Power Dissipation due to Loading 50Ω to V_{DDO_Qx} / 2
  Output Current I_{OUT} = V_{DD_MAX} / [2 * (50Ω + R_{OUT})] = 3.465V / [2 * (50Ω + 15Ω)] = **26.65mA**
- Power Dissipation on the R_{OUT} per LVCMOS output
  Power (LVCMOS) = R_{OUT} * $(I_{OUT})^2$ = 15Ω * $(26.65mA)^2$ = **10.65mW per output**
- Total Power Dissipation on the R_{OUT}
  Total Power (R_{OUT}) = 10.65mW * 4 = **42.6mW**

- Total Power Dissipation
- **Total Powe**r
  = Power (core) + Total Power (HCSL) + Total Power (R_{OUT})
  = 970.2mW + 445mW + 42.6mW
  = 1457.8mW

2. Junction Temperature.

Junction temperature, Tj, is the temperature at the junction of the bond wire and bond pad directly affects the reliability of the device. The maximum recommended junction temperature is 125°C. Limiting the internal transistor junction temperature, Tj, to 125°C ensures that the bond wire and bond pad temperature remains below 125°C.

The equation for Tj is as follows: Tj = θ_{JA} * Pd_total + T_A

Tj = Junction Temperature

θ_{JA} = Junction-to-Ambient Thermal Resistance

Pd_total = Total Device Power Dissipation (example calculation is in section 1 above)

T_A = Ambient Temperature

In order to calculate junction temperature, the appropriate junction-to-ambient thermal resistance θ_{JA} must be used. Assuming no air flow and a multi-layer board, the appropriate value is 26.6°C/W per Table 19.

Therefore, Tj for an ambient temperature of 85°C with all outputs switching is:

85°C + 1.458W * 26.6°C/W = 123.8°C. This is below the limit of 125°C.

This calculation is only an example. Tj will obviously vary depending on the number of loaded outputs, supply voltage, air flow and the type of board (multi-layer).

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Table 19. Thermal Resistance θ_{JA} for 72 Lead VFQFPN, Forced Convection

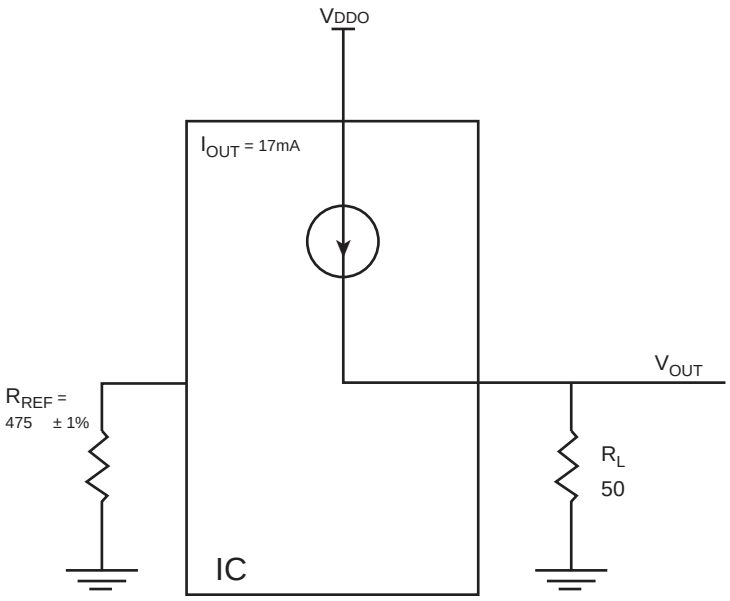
θ_{JA} vs. Air Flow			
Meters per Second	**0**	**1**	**2**
Multi-Layer PCB, JEDEC Standard Test Boards	26.6°C/W	20°C/W	17.9°C/W

3. Calculations and Equations.

The purpose of this section is to calculate power dissipation on the IC per HCSL output pair.

HCSL output driver circuit and termination are shown in Figure 31.

Figure 31. HCSL Driver Circuit and Termination



HCSL is a current steering output which sources a maximum of 17mA of current per output. To calculate worst case on-chip power dissipation, use the following equations which assume a 50Ω load to ground.

The highest power dissipation occurs when V_{DD_MAX}.

Power= $(V_{DD\_MAX} - V_{OUT}) * I_{OUT}$
since $V_{OUT} = I_{OUT} * R_L$

Power= $(V_{DD\_MAX} - I_{OUT} * R_L) * I_{OUT}$

= (3.465V – 17mA * 50Ω) * 17mA

Total Power Dissipation per output pair = **44.5mW**

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Reliability Information

Table 20. θ_{JA} vs. Air Flow Table for a 72 Lead VFQFPN

θ_{JA} vs. Air Flow			
Meters per Second	0	1	2
Multi-Layer PCB, JEDEC Standard Test Boards	26.6°C/W	20°C/W	17.9°C/W

Transistor Count

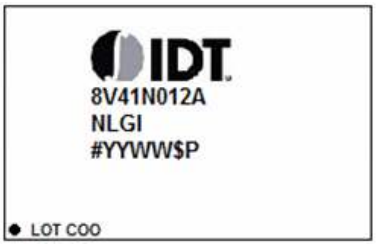
The transistor count for 8V41N012A is: 176,555.

Package Outline Drawings

The package outline drawings are appended at the end of this document and are accessible from the link below. The package information is the most current data available.

www.idt.com/document/psc/72-vfqfpn-package-outline-drawing-100-x-100-x-090-mm-body-epad-590-x-590-mm-punch-050mm-pitch

Marking Diagram



- Line 1 is the part number.
- Line 2 indicates the package type.
- Line 3 indicates the following:
  - "#" denotes stepping.
  - "YY" is the last two digits of the year and "WW" is a work week number that the part was assembled.
  - "$" denotes the mark code.

Ordering Information

Orderable Part Number	Marking	Package	Shipping Packaging	Temperature
8V41N012ANLGI	8V41N012ANLGI	10 x 10 mm 72-VFQFPN, Lead-Free	Tray	-40°C to 85°C
8V41N012ANLGI8	8V41N012ANLGI	10 x 10 mm 72-VFQFPN, Lead-Free	Tape and Reel	-40°C to 85°C

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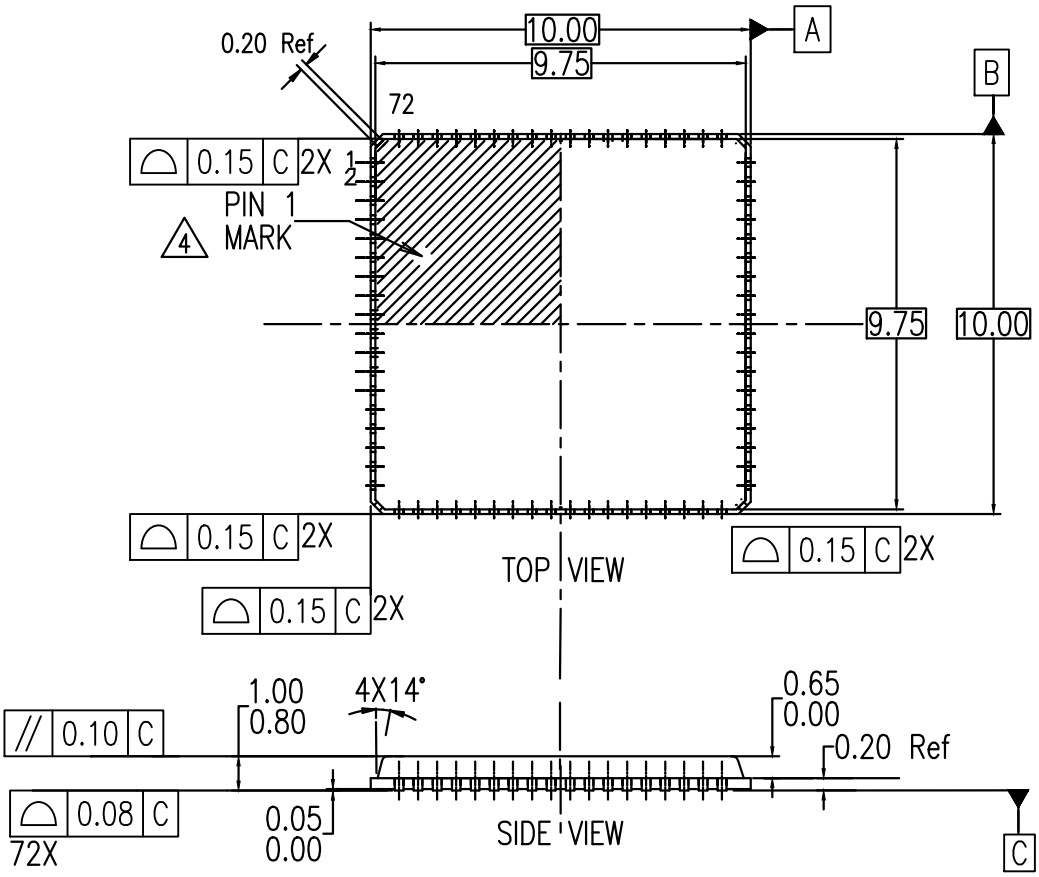
Revision History

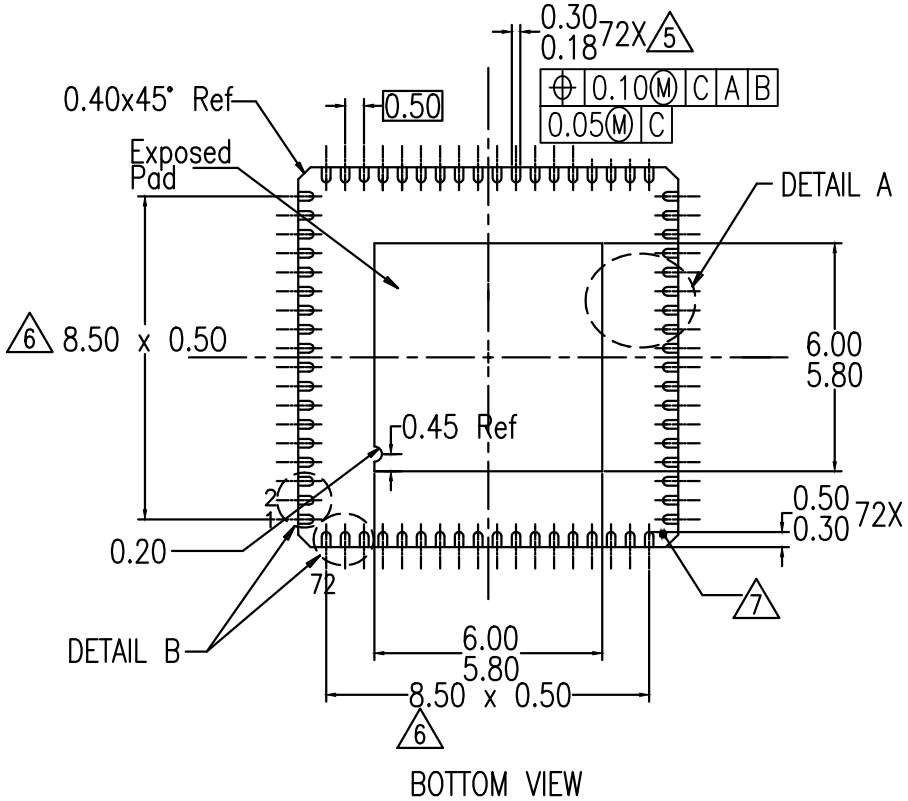
Revision Date	Description of Change
October 11, 2019	▪ Updated the package diagrams; however, no technical changes ▪ Changed the document status to production
October 12, 2018	Initial release.

72-VFQFPN, Package Outline Drawing

10.0 x 10.0 x 0.90 mm Body, Epad 5.90 x 5.90 mm Punch 0.50mm Pitch

NLG72D1, PSC-4208-05, Rev 01, Page 1





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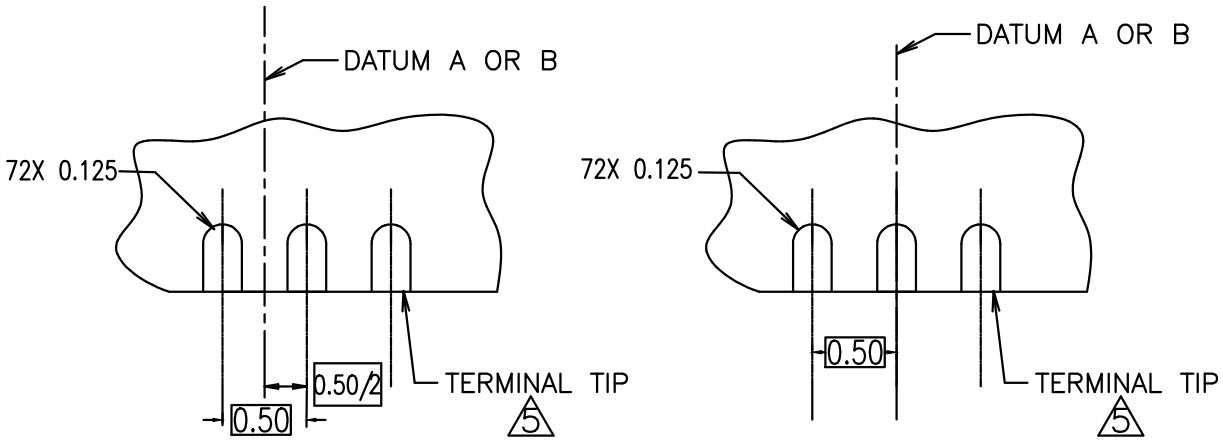

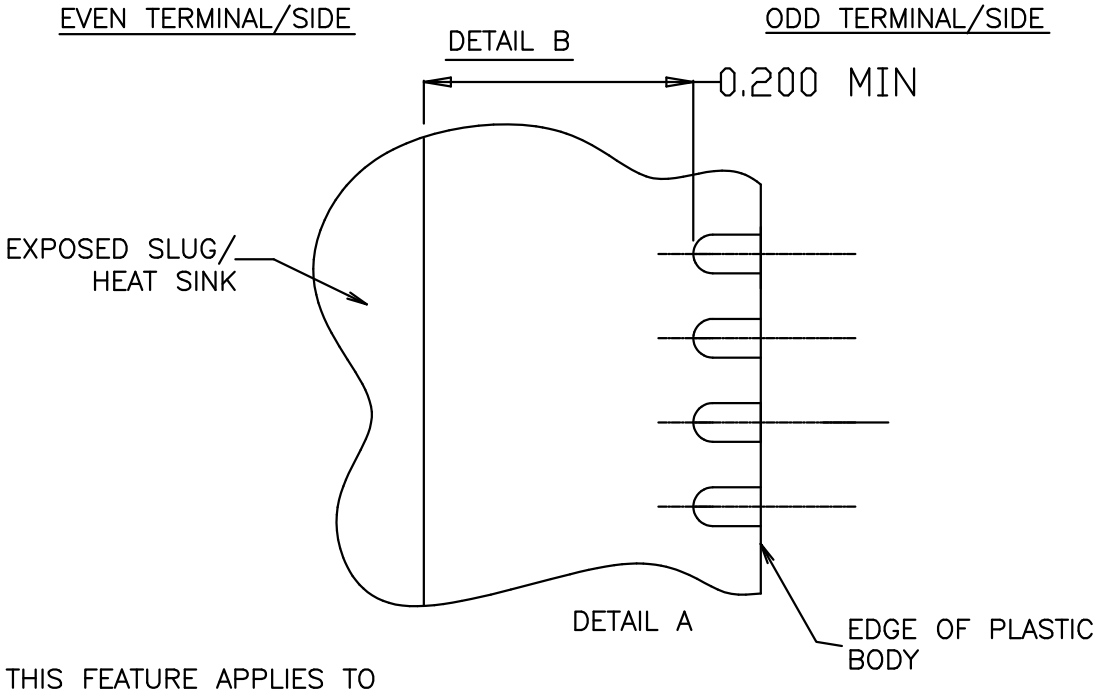

THIS FEATURE APPLIES TO
ALL ENDS OF THE PKG.

NOTES:

1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M–1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
   Nd IS THE NUMBER OF TERMINALS IN X–DIRECTION &
   Ne IS THE NUMBER OF TERMINALS IN Y–DIRECTION.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JEDEC PUB. 95 SEC. 4.3 SPP–002. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25mm AND 0.30mm FROM TERMINAL TIP.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.

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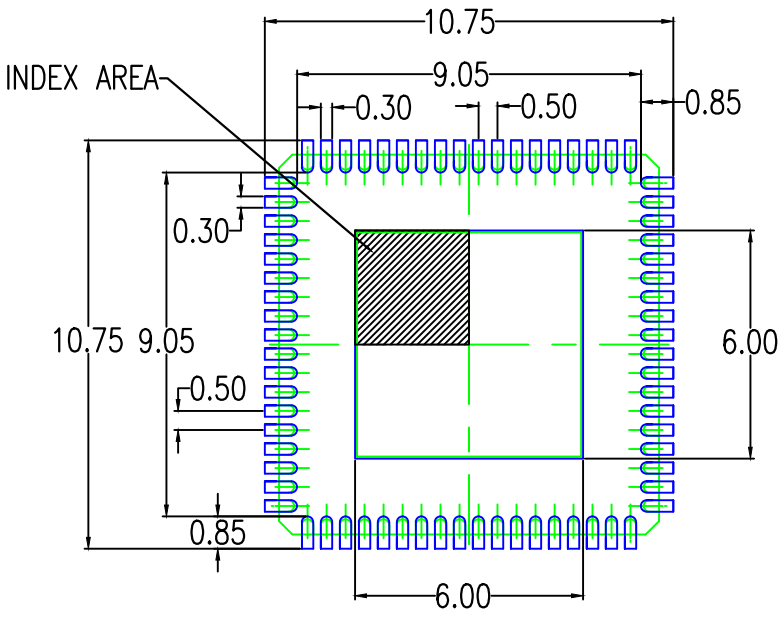

RECOMMENDED LAND PATTERN DIMENSION

NOTES:

1. ALL DIMENSIONS ARE IN MM. ANGLES IN DEGREES.
2. TOP DOWN VIEW. AS VIEWED ON PCB.
3. COMPONENT OUTLINE SHOWS FOR REFERENCE IN GREEN.
4. LAND PATTERN IN BLUE. NSMD PATTERN ASSUMED.
5. LAND PATTERN RECOMMENDATION PER IPC-7351B GENERIC REQUIREMENT FOR SURFACE MOUNT DESIGN AND LAND PATTERN.

Package Revision History		
Date Created	Rev No.	Description
Sept 5, 2019	Rev 01	Update to New Format
Feb 2, 2016	Rev 00	Initial Release

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(Disclaimer Rev.1.0 Mar 2020)

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